BEC - Assignment - 2 :-

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Q1) Design a Schmitt trigger to generate a square waveform with a sine wave of 1V rms and 1KHz frequency. Plot the waveforms.

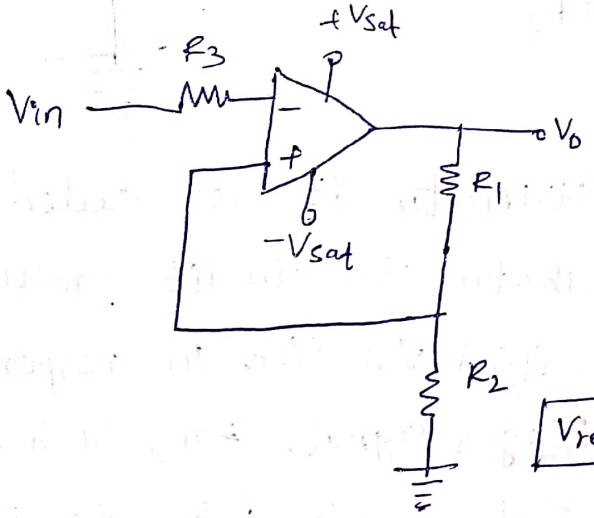
Sol :- $V_{rms} = 1V$ & $F = 1kHz = 10^3 Hz$.

$$V_{rms} = \frac{V_{in}}{\sqrt{2}}$$

$$\boxed{V_o' = \sqrt{2}V}$$

$$V_{in} = V_o' \sin(\omega t)$$
$$= \sqrt{2}\sin(2\pi \times 10^3 \times t)$$
$$V_{in} = \sqrt{2}\sin(2000\pi t)$$

Schmitt trigger :-

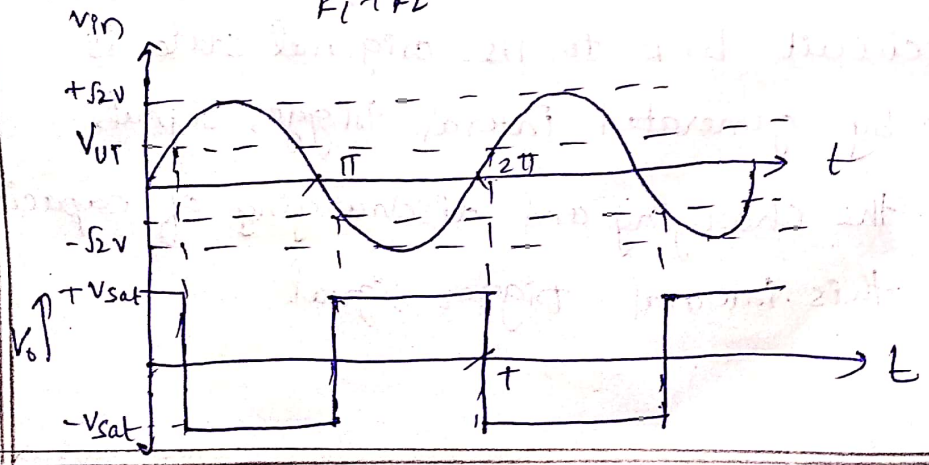


$$\boxed{V_{ref} = 0}$$

as $V_{ref} = 0$, It is a symmetric square wave.

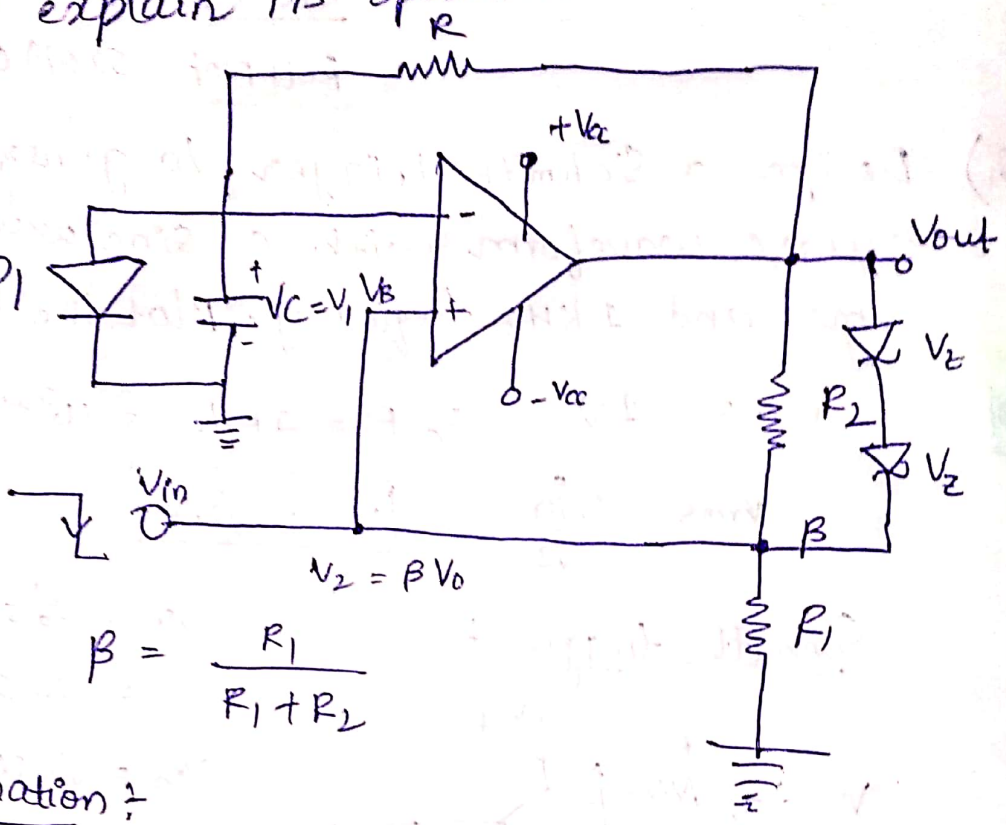
$$V_{UT} = \frac{R_2}{R_1 + R_2} V_{sat}$$

$$V_{LT} = \frac{-R_2}{R_1 + R_2} V_{sat}$$



Q2) Draw monostable multivibrator using op-amp and explain its operation.

Sol:-



Explaination :-

The monostable multivibrator is also called as one-shot multivibrator. The circuit produces a signal pulse of specified vibration in response to each external trigger signal. For, such a circuit only one stable state exists. When the external trigger is applied, the output changes its state. The new state is called as: quasi-stable-state. The circuit back to its original state is driven by generated interal trigger signal. Usually, the charging and discharging of capacitor provides this internal trigger signal

* The diode D_1 connected to capacitor is called clamping diode. It clamps the capacitor voltage to 0.7V, when the output is $+V_{sat}$.

* Operation of the circuit:

1) Let us assume the Output V_o is at $+V_{sat}$ (Stable).
2) The diode D_1 conducts and the voltage across the capacitor $C \Rightarrow V_c$ gets clamped to 0.7 V.
3) The voltage at the non-inverting terminal is constructed by voltage divider circuit.
4) Voltage at non-inverting terminal $(V_2) = +\beta V_o$. $\because \beta = \frac{R_2}{R_1 + R_2}$
5) If, a negative trigger of V_T is applied to the non-inverting terminal, so that effective voltage at this terminal is less than 0.7, then Output changes from $+V_{sat}$ to $-V_{sat}$.
6) The diode is now reverse biased and the capacitor starts charging exponentially to $-V_{sat}$ through resistance R.
7) The voltage at non-inverting terminal is now $-\beta V_{sat}$. When capacitor becomes just slightly more than negative $-\beta V_{sat}$, the output gets back to $+V_{sat}$ state.
8) The capacitor now starts charging towards $+V_{sat}$ through R until it reaches 0.7 V as capacitor gets clamped to the voltage.