INDIAN INSTITUTE OF INFORMATION TECHNOLOGY SRI CITY

MID SEMESTER EXAMINATION – FEB, 2021

(ONLINE MODE)

HIGH PERFORMANCE COMPUTING

DATE: 18-02-2021

SET 3

1a.	A memory access to main memory on a cache "miss" takes 30 ns and a memory access to the cache on a cache "hit" takes 3 ns. If 80% of the processor's memory requests result in a cache "hit", what is the average memory access time? **(2 marks)**
1b.	Given an algorithm where the fraction that the program is serial (f) is 0.25, what is the overall speedup for the entire algorithm for local speed up (s) of 2 and 4 times? **(1 mark)**
2a	Explain the Coarse grain parallel, Medium grain parallel and Fine grain parallel **with an example.** **(4 marks)**
2b	Discuss the NUMA and UMA Shared-Address-Space Platforms. **(3 marks)**
3a	Write a **OpenMP** program to find the sum of elements of an array A with n elements **(2 marks)**
3b	Write a program using **PThreads** to parallelize odd-even transposition sort. **(5 marks)**
4	Which of the following statements w.r.t. threads are true? a) All threads have access to the same global / shared memory. b) Threads have their own private data. c) Programmers are responsible for synchronizing access to global memory d) none of the above **(1 mark)**
5	True or false? By having the cache act as a bridge between main memory and the CPU, the time it takes to retrieve a block of data from main memory is longer than it would be if the cache did not exist **(1 mark)**
6	Multi-core processors are used across many application domains. List any four applications. **(1 mark)**