Anirudh Jakhotia Roll:- S20190010007

Indian Institute of Information Technology, Sri City.

: HPC (High Performance Computing)

Assignment - 1

Question - 1)

Suppose for a RISC ISA implementation, there are four instruction types LOAD, STORE, ALU and BRANCH with relative frequencies of 45%, 13%, 20% and 25% respectively, and CPI values are 5, 2.5, 1 and 2, respectively.

Find overall CPI of RISC ISA?

Ans) CPI is average no. of cycles per instruction.

Given,

LOAD with frequency : 45%
STORE with frequency 13%
ALU with frequency 20%
BRANCH with frequency. 25%

We know that

If for each instruction type, we know its frequency and no. of cycles need to execute it, we can compute the overall CPI as follows:

$$\text{Overall CPI} = \sum \text{CPI} \times F$$

Operation	F	CPI	CPI × F
LOAD	45%	5	2.25
STORE	13%	2.5	0.325
ALU	20%	1	0.20
BRANCH	25%	2.2	0.55

Overall CPI = 2.25 + 0.325 + 0.20 + 0.55

= 3.325

∴ Overall CPI of RISC ISA = 3.325

20) If 90% of the computation can be parallelized, what is the max. speedup achievable using 8 processors?

Soln We use Amdahl's Law to solve this problem

→ Amdahl's Law states that, let f be fraction of operations in a computation that must be performed sequentially, where $0 \leq f \leq 1$.

→ the maximum speedup $\psi(n, p)$ achieved by parallel computer with p processors performing computations is

$$\psi(n, p) \leq \frac{1}{f + \frac{(1-f)}{p}}$$

Upper limit : as $p \to \infty$, $\psi(n, p) \leq \frac{1}{f + \frac{1-f}{p}} \leq \frac{1}{f}$

→ It assumes problem size is fixed and provides an upperbound on the speedup achievable by applying certain no. of processors

From question, $f = 10\%$; $n = 8$

Substituting, $\psi(n, p) \leq \frac{1}{0.1 + \frac{(1-0.1)}{8}}$

$$\leq \frac{1}{\frac{0.1 \times 8 + 0.9}{8}} \leq \frac{8}{0.8 + 0.9}$$

$$\leq \frac{8}{1.7} \leq 4.70 \text{ times}$$

∴ Maximum speedup achievable is 4.7 times

Question 3)

Ans) Given that,

→ memory system with a level 1 cache of 32KB and DRAM of 512 MB with the processor operating at 1GHz

→ Latency to L1 cache is one cycle and latency to DRAM is 100 cycles.

→ In each memory cycle, the processor fetches four words.

To find :

Peak achievable performance of dot product of two vectors.

→ Let us consider two arbitrary vectors a and b.

The dot product of vectors is given by (5)

```
for(i=0; i<dim; i++)
{
    dot_prod+= a[i] * b[i];
}
```

→ We can consider this problem as memory bound & consider only cache & memory access.

We know that,

→ the first iteration creates a cache miss.

→ the next iterations (3) has access to a[i], and b[i] which refers to in cache data.

→ As given, for every 4 iterations, there are 2 cache misses for a[i] & b[i]

→ Thus, 4 iterations cost 2*100 cycles (memory latency).

In four iterations, we perform 4*2 ops (* & +=)

So, 8 operations every 200ns.

Aniruddh Jakhotia Roll: 2019001007

$$= \frac{8}{2\times10^{-9}\times10^{2}} = 40\times10^{6} \text{ ops/sec}$$

$$= 40\times10^{6} \text{ Flops} = \underline{40 \text{ MFlops}}$$

∴ Peak achievable performance = 40MFlops

Question 4)

a) Which processor has highest performance expressed in instructions per second?

Ans) we know that

$$\text{CPU time} = \frac{\text{Instructions} \times \text{CPI}}{\text{clock rate}}$$

$$\text{now, } \frac{\text{Instructions}}{\text{CPU time}} = \frac{\text{clock rate}}{\text{CPI}}$$

↓

$$\boxed{\text{Instruction per second} = \frac{\text{clock rate}}{\text{CPI}}}$$

$$1 \text{ GHz} = 10^{9} \text{ Hz}$$

$$IPS_1 = \frac{3 \text{ GHz}}{1.5} = 2\times10^{9}$$

$$IPS_2 = \frac{2.5 \text{ GHz}}{1} = 2.5\times10^{9}$$

$IPS_3 = \frac{4\ GHz}{2.2} = 1.82 \times 10^9$

We can see that processor 2 has highest performance in instructions per second

b) If processors each execute a program in 10 seconds, find no. of cycles & no. of instructions

Ans) We know that

Instructions = IPS x CPU time

$Instructions_1 = 2 \times 10^9 \times 10 = 2 \times 10^{10}$

$Instructions_2 = 2.5 \times 10^9 \times 10 = 2.5 \times 10^{10}$

$Instructions_3 = 1.89 \times 10^9 \times 10 = 1.89 \times 10^{10}$

Clock cycles = CPU time x clock rate

$Clock\ cycles_1 = 10 \times 3\ GHz = 3 \times 10^{10}$

$Clock\ cycles_2 = 10 \times 2.5\ GHz = 2.5 \times 10^{10}$

$Clock\ cycles_3 = 10 \times 4\ GHz = 4 \times 10^{10}$

∴

Processor	Instructions	Clock cycles
1	2×10^{10}	3×10^{10}
2	2.5×10^{10}	2.5×10^{10}
3	1.82×10^{10}	4×10^{10}

c) Execution time is reduced by 30% but leads to increase in 20% in CPI. What clock rate should we have to get this ~~info~~ time reduction?

Soln

$$\text{Execution time}_{new} = 0.7 \times \text{Execution time}_{old}$$

$$CPI_{new} = 1.2\ CPI_{old}$$

$$\text{Instructions}_{old} = \text{Instructions}_{new}$$

$$\text{Execution time} = \frac{\text{Instructions} \times CPI}{\text{Clock rate}}$$

Equating the Instructions old & Instructions new we get,

$$\frac{\text{Execution time}_{old} \times \text{Clock rate}_{old}}{CPI_{old}} = \frac{\text{Execution}_{new} \times \text{Clock rate}_{new}}{CPI_{new}}$$

$$= \frac{\text{Execution}_{old} \times \text{Clock rate}_{old}}{CPI_{old}} = \frac{0.7 \times \text{Execution}_{old} \times \text{Clock rate}_{new}}{1.2 \times CPI_{old}}$$

$$\Rightarrow \text{Clock rate}_{old} = \frac{0.7}{1.2} \times \text{Clock rate}_{new}$$

Aniruddh Jakhotia Roll: 520190010007

(9)

$$\text{Clock rate}_{new} = \frac{1.2}{0.7} \times \text{clock rate}_{old}.$$

$$= 1.71 \times \text{clock rate}_{old}$$

$$= 71\% \text{ approximately}$$

→ The new clock rate must be increased by 71% approximately to get the required time reduction.