Indian Institute of Information Technology, Sri City,
Chittoor Dist., Andhra Pradesh

(An Institute of National Importance under an Act of Parliament)

S20190010007

# High Performance Computing

## Mid-Sem Exam-UG3

**Date: 23/03/2022** **Duration: 90 Minutes** **Marks: 20**

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**Answer all the Questions**

1. What is cache coherence in a multiprocessor system and how to overcome it? Explain with diagram. [3]

2. Assume 1% of the runtime of a program is not parallelizable. This program is run on 61 cores of an Intel Xeon Phi. Under the assumption that the program runs at the same speed on all of those cores, and there are no additional overheads, what is the parallel speedup? [2]

3. A program's runtime is determined by the product of instructions per program, cycles per instruction, and clock frequency. Assume the following instruction mix for a MIPS-like RISC instruction set: 15% stores, 25% loads, 15% branches, and 30% integer arithmetic, 5% integer shift, and 5% integer multiply. Given that stores require one cycle, load instructions require two cycles, branches require four cycles, integer ALU instructions require one cycle, and integer multiplies require ten cycles, compute the overall (step by step procedure) [2]

4. Explain in detail the performance metrics of parallel systems. [4]

5. Describe the building granularity of parallel systems with an example. [3]

6. What are threads? Explain in detail how to create and terminate pthreads [3]

7. Explain mutual exclusion in threads [3]

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