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CONVERTER CIRCUIT

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LIST OF ABBREVIATIONS

MC	Matrix Converter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
4QSW	4 Quadrant Switch
PIC	Peripheral Interface Controller
FOSC	Frequency Of Oscillation
ZCD	Zero Crossing Detector
V_o	Output Voltage
V_s	Source Voltage
f_o	Output Frequency
f_s	Supply Frequency
V_m	Peak Phase Voltage
d_a	Duty cycle of voltage sector ‘n’
d_β	Duty cycle of voltage sector ‘n+1’
d_γ	Duty cycle of current sector ‘n’
d_δ	Duty cycle of current sector ‘n+1’

CHAPTER 1

INTRODUCTION

1.1. Wind Energy Conversion

Interest in renewable energy sources has been on the rise over the past years. A reduction in the availability of fossil fuels and improved interest in non-polluting sources as led to a lot of investment being made on renewable energy sources such as wind, solar, tidal, geothermal, etc. Of these wind and solar are the preferred sources especially due to their global availability and relative non-dependence on the location to a certain extent. In countries such as India and Denmark wind energy conversion systems have found huge popularity especially due to the high availability of the resource in many regions.

A wind turbine is deployed to capture the incoming wind energy and obtain useful work from it. The wind turbine, connected to the rotor of an electric generator via a gear system, acts as the prime mover. The electrical machine used is usually of Induction type and doubly fed induction generators are preferred nowadays. Due to the versatile nature of wind, a converter is required at the output of the generator before it may be fed to the 230V, 50Hz grid i.e. a variable voltage variable frequency ac-ac three-phase converter is required. The conversion scheme is shown in Fig 1.1.

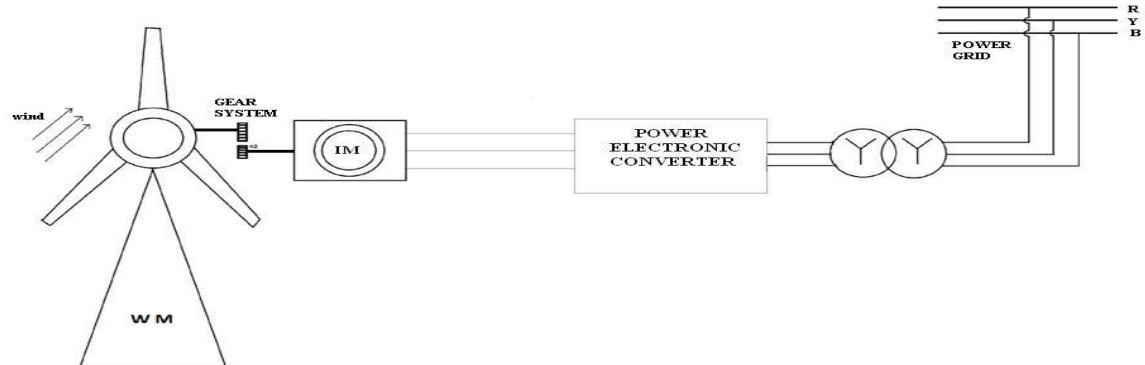


Fig. 1.1 Wind Energy Conversion Scheme

1.2 Need for Matrix Converters

Matrix converters have enjoyed increasing interest in recent years. This interest is reflected in the number of articles and papers written about matrix converters in the last ten years. This interest is due mainly to the promise of an all-silicon converter which can inherently provide amplitude and frequency conversion, bidirectional power flow and input displacement factor control. Matrix converters are one-stage converters capable of providing simultaneous voltage and frequency transformation. They can be applied to any multi-phase system, but the most significant case is the 3-phase to 3-phase converter. This consists of nine 4-quadrant or bidirectional switches distributed in a 3x3 matrix form. These switches connect each input phase with the three output lines. There are no energy storage elements such as large capacitors and inductors. The inductive load and the input filter capacitors filter the high frequency current components produced by the high frequency switch commutations. Despite all of its eye-catching features, matrix converters are not commonly seen in commercial applications. There are several reasons for this rejection.

Firstly, the matrix converter is a new technology. Although the principles of matrix converters have been known since the 1970's, it has only been in recent years that some of the more critical areas of matrix converter operation, like multi-step commutation techniques, have been developed.

Secondly, the number of the semiconductor switches in a matrix converter is greater than the number used in a dc-link converter. Therefore, the cost of implementation of a matrix converter is larger than a conventional dc-link converter of the same ratings.

Finally, the amplitude of the output voltages generated by a matrix converter is limited to 86.7% of the input voltage amplitude for the most popular modulation methods. Consequently, electrical motors or any other standard

device connected as load to a matrix converter do not operate at their nominal rated voltage. The three-phase matrix converter topology is shown in Fig. 1.2.

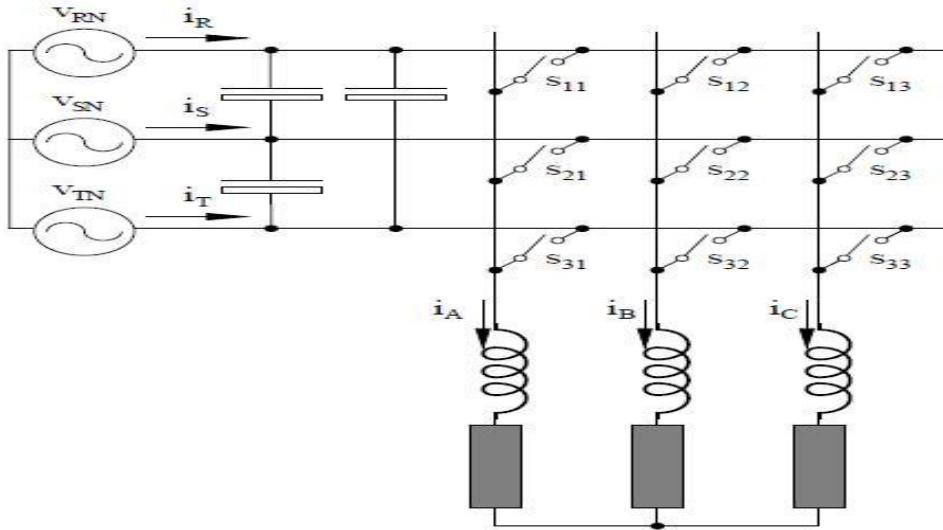


Fig. 1.2 Three-phase Matrix Converter Topology

1.3. Need for an economical implementation

Despite the drawbacks mentioned in the previous section, there are several reasons why matrix converters remain very attractive for some applications.

Firstly, there are applications where energy storage elements like capacitors and inductors are to be avoided. For example, the large electrolytic capacitors of a dc-link converter are some of the elements that decrease the reliability of the converter.

Secondly, the cost of power semiconductors continues to fall and there is no evidence to suggest that this trend will change for the foreseeable future. On the other hand, the real cost of energy storage elements is not falling. For this reason, matrix converters will become increasingly more cost competitive.

Thirdly, a matrix converter is a very attractive solution when regeneration is required. The bidirectional flow capability and displacement factor control of matrix converters make them an ideal solution for application.

The matrix converter will also benefit from the current trend in electrical drive technology to integrate the frequency converter, the electrical motor and even the gear or pump into a single unit in order to reduce costs and increase overall efficiency and equipment reliability. By redesigning the motor to operate at lower nominal voltages, the disadvantage of the low output input voltage ratio is overcome.

Finally, there are applications where the converter size, weight and performance is of major concern. The lack of bulky energy storage elements and the integration of semiconductors in power modules specifically designed for matrix converters mean that large power density factors are achievable employing matrix converters.

Thus it can be seen that if an economical implementation of matrix converters can be achieved it may be widely used in many applications. Wind energy conversion systems might find themselves much more accessible to consumers if the cost of these matrix converters can be reduced. Conventional matrix converters are realized using FPGAs or DSPs for their digital implementation. A low cost implementation using multiple PIC micro-controllers has been proposed. Such an implementation may reduce the cost of the converters by upto ten times. Further employing modern power switches such as IGBTs in the place of thyristors reduces the need for extra commutation circuits thereby reducing the cost.

1.4. Modulation Technique

The control technique chosen for matrix converters are extremely important in their efficient implementation. The Venturini method and Indirect Space Vector Modulation are the most commonly applied modulation techniques.

Control of the matrix converter must comply with the following basic two rules. Firstly, any two input terminals should never be connected to the same output line to prevent short-circuit, because the MC is fed by a voltage source.

The other, an output phase must never be open-circuited, owing to the absence of a path for the inductive load current which leads to the over-voltages. When these restrictions are applied only 27 states out of a total of $2^9=512$ are possible. These 27 states are applied appropriately for the Venturini method.

In Indirect method of modulation, the 3×3 matrix converter is considered to be made of a fictitious three-phase rectifier and three-phase inverter. Space Vector Modulation is applied on this rectifier and inverter individually to obtain a 2×3 matrix for each. Then the rectifier switching state matrix is transposed and multiplied with that of the inverter to obtain a 3×3 switching state matrix which is then applied on the matrix converter.

1.5. Four –Quadrant Switch Realization

Bi-directional power transfer in ac regulators necessitates the use of switches capable of blocking voltages of either polarity and controlled conduction of current in both forward and reverse directions. The four-quadrant switches (4QSWs) possess this capability; however, since no four-quadrant switch is commercially available. These are realized by embedding a transistor inside a diode bridge or by inverse parallel connections of transistor as shown in Fig.1.3.

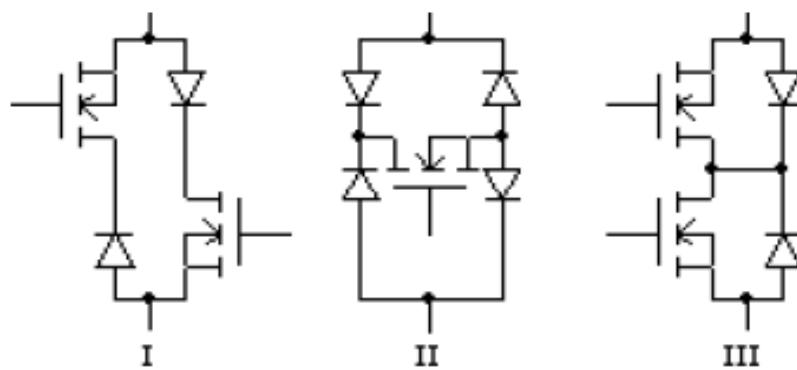


Fig. 1.3 Four-Quadrant Switch (4QSW) realizations

1.6. Literature Review:

The study of matrix converters and space vector modulation were done from various journals and technical papers.

The first analysis of all-silicon converter structures was carried out by L. Gyugyi and B. R. Pelly in 1976.

- [1] Gyugyi, Laszlo, and Brian Raymond Pelly. “*Static power frequency changers: theory, performance, and application*”. New York: Wiley, 1976.

The Venturini method matrix converters are studied from the following papers.

- [2] Alesina, Alberto, and Marco GB Venturini. "Analysis and design of optimum-amplitude nine-switch direct AC-AC converters." *Power Electronics, IEEE Transactions on* 4.1 (1989): 101-112.

- [3] Karaca, Hulusi, and Ramazan Akkay. "Control of Venturini method based matrix converter in input voltage variations." *Proceedings of the International Multi Conference of Engineers and Computer Scientists IMECS, Hong Kon.* Vol. 2. 2009.

- [4] Gyugyi, Laszlo, and Brian Raymond Pelly. *Static power frequency changers: theory, performance, and application*. New York: Wiley, 1976.

An analysis of different modulation techniques for three-phase to three-phase matrix converters is dealt with in the above-mentioned paper.

- [5] Jussila, Matti, and Heikki Tuusa. "Comparison of simple control strategies of space-vector modulated indirect matrix converter under distorted supply voltage." *Power Electronics, IEEE Transactions on* 22.1 (2007): 139-148.

The different control strategies are discussed and an experimental verification is carried out in the above paper.

- [6] Kwong Loong, Kelvin Lye, and Nik ramzi bin Idris. "Microcontroller Based Space Vector Modulation (SVM) Signal Generator." (2008).

The above mentioned paper discusses the methodology of using microcontrollers for Space vector modulation.

[7] Parekh, Rakesh. "VF control of 3-phase induction motor using space vector modulation." *Microchip Technology Inc., AN955, USA* (2005).

This application note includes the description of SVM theory and its digital implementation.

[8] Rashid, Muhammad H., ed. *Power electronics handbook*. Academic Pr, 2001.

The book gives the operating principal of matrix converter

[9] Microchip Technology Inc. "PIC18F2331/2431/4331/4431 Data Sheet." (2010).

[10] Microchip Technology Inc. "PIC18F2455/2550/4455/4550 Data Sheet." (2009).

The above two datasheets are about the two microcontroller's that are used in this project.

[11] Jidin, Auzani, And Tole Sutikno. "MATLAB/SIMULINK Based Analysis Of Voltage Source Inverter With Space Vector Modulation,"." *Jurnal TELKOMNIKA, Teknik Elektro, Universitas Ahmad Dahlan* 7.1 (2009).

The above mentioned paper deals with simulation of inverter using space vector modulation method.

CHAPTER 2

SPACE VECTOR MODULATED INVERTER

2.1. Three-phase Voltage Source Inverters

Single-phase VSIs cover low-range power applications and three-phase VSIs cover the medium to high-power applications. The main purpose is to provide a three-phase voltage source, where the amplitude, phase and frequency of the voltages should always be controllable. Although most of the applications require sinusoidal voltage waveforms (e.g.,ASDs, UPSs, FACTS), arbitrary voltages are also required in some emerging applications (e.g.,active filters, voltage compensators).

The standard three-phase VSI topology is shown in Fig. 2.1 and the eight valid switch states are given in Table 3. As in single-phase VSIs, the switches of any leg of the inverter (S_1 and S_2 , S_3 and S_6 , or S_5 and S_2) cannot be switched on simultaneously because this would result in a short circuit across the dc link voltage supply. Similarly, in order to avoid undefined states in the VSI, and thus undefined ac output line voltages, the switches of any leg of the inverter cannot be switched off simultaneously as this will result in voltages that will depend upon the respective line current polarity. Of the eight valid states, two of them (7 and 8 in Table 3) produce zero ac line voltages. The remaining states produce non-zero ac output voltages. In order to generate a given voltage waveform, the inverter moves from one state to another. Thus the resulting ac output line voltages consist of discrete values of voltages that are V_{dc} , 0 and $-V_{dc}$ for the topology shown in Fig. 2.1.

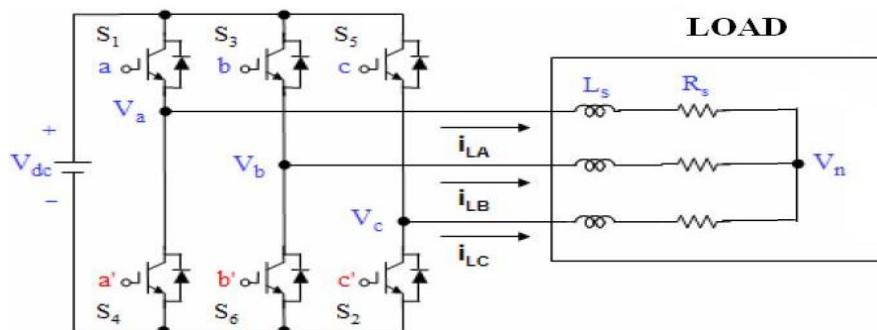


Fig.2.1. Three-phase Inverter Topology

2.2. Space Vector Modulation

2.2.1 Pulse Width Modulation

Fig. 2.2 shows circuit model of a single-phase inverter with a center-tapped grounded DC bus, and Fig. 2.3 illustrates principle of pulse width modulation.

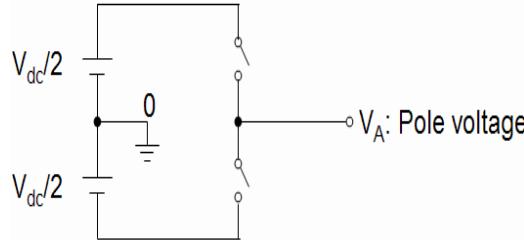


Fig.2.2. Circuit model of a single-phase inverter

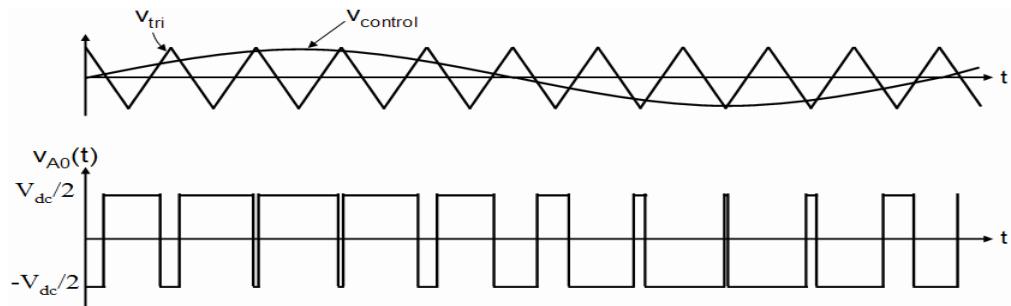


Fig.2.3. Pulse Width Modulation

As depicted in Fig. 2.3, the inverter output voltage is determined in the following:

When $V_{\text{control}} > V_{\text{tri}}$, $V_{AO} = V_{dc}/2$

Also, the inverter output voltage has the following features:

- PWM frequency is the same as the frequency of V_{tri}
- Amplitude is controlled by the peak value of V_{control}
- Fundamental frequency is controlled by the frequency of V_{control}

Modulation index (m) is defined as:

$$m = \frac{V_{\text{control}}}{V_{\text{tri}}} = \text{peak of } (V_{AO})_1 / (V_{dc}/2)$$

where, $(V_{AO})_1$ is the fundamental frequency component of V_{AO} .

2.2.2 Principle of Space Vector PWM

From Fig.2.1, S_1 to S_6 are the six power switches that shape the output, which are controlled by the switching variables a, a', b, b', c and c' . When an upper transistor is switched on, i.e., when a, b or c is 1, the corresponding lower transistor is switched off, i.e., the corresponding a', b' or c' is 0. Therefore, the on and off states of the upper transistors S_1, S_3 and S_5 can be used to determine the output voltage. The relationship between the switching variable vector $[a, b, c]^t$ and the line-to-line voltage vector $[V_{ab} V_{bc} V_{ca}]^t$ is given by the following:

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (2.1)$$

Also, the relationship between the switching variable vector $[a, b, c]^t$ and the phase voltage vector $[V_a V_b V_c]^t$ can be expressed as below.

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \quad (2.2)$$

As illustrated in Fig. 2.1, there are eight possible combinations of on and off patterns for the three upper power switches. The on and off states of the lower power devices are opposite to the upper one and so are easily determined once the states of the upper power transistors are determined. The output line to neutral voltage (phase voltage), and output line-to-line voltages in terms of DC-link V_{dc} , are given in Table. 2.1 and Fig. 2.4 shows the eight inverter voltage vectors (V_0 to V_7).

Voltage Vectors	Switching Vectors			Line to neutral voltage			Line to line voltage		
	a	b	c	V_{an}	V_{bn}	V_{cn}	V_{ab}	V_{bc}	V_{ca}
V_0	0	0	0	0	0	0	0	0	0
V_1	1	0	0	2/3	-1/3	-1/3	1	0	-1
V_2	1	1	0	1/3	1/3	-2/3	0	1	-1
V_3	0	1	0	-1/3	2/3	-1/3	-1	1	0
V_4	0	1	1	-2/3	1/3	1/3	-1	0	1
V_5	0	0	1	-1/3	-1/3	2/3	0	-1	1
V_6	1	0	1	1/3	-2/3	1/3	1	-1	0
V_7	1	1	1	0	0	0	0	0	0

(Note that the respective voltage should be multiplied by V_{dc})

Table 1.1 Switching vectors, phase voltages and output line to line voltages

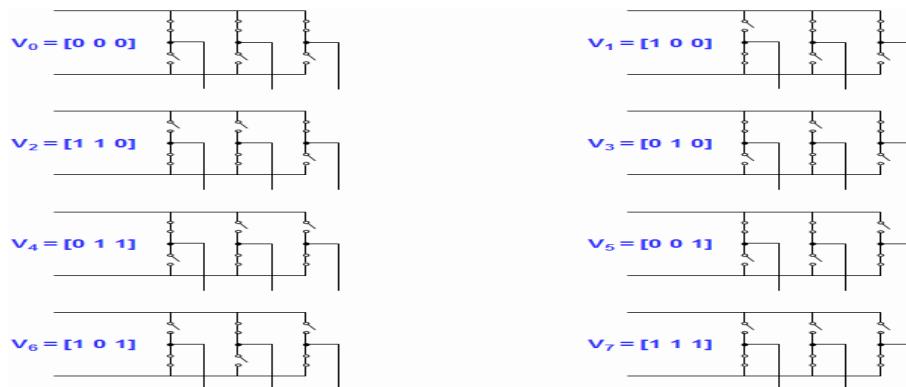


Fig. 2.4 The eight inverter voltage vectors (V_0 to V_7)

Space Vector PWM (SVPWM) refers to a special switching sequence of the upper three power transistors of a three-phase power inverter. It has been shown to generate less harmonic distortion in the output voltages and or currents applied to the phases of an AC motor and to provide more efficient use of supply voltage compared with sinusoidal modulation technique as shown in Fig. 2.5.

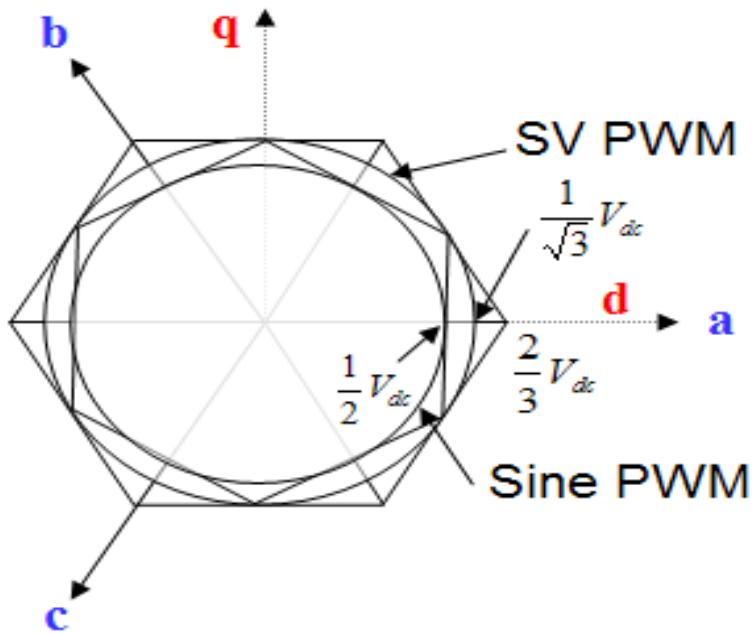


Fig. 2.5. Locus comparison of maximum linear control voltage in Sine PWM and SVPWM.

To implement the space vector PWM, the voltage equations in the *abc* reference frame can be transformed into the stationary *dq* reference frame that consists of the horizontal (*d*) and vertical (*q*) axes as depicted in Fig. 2.6.

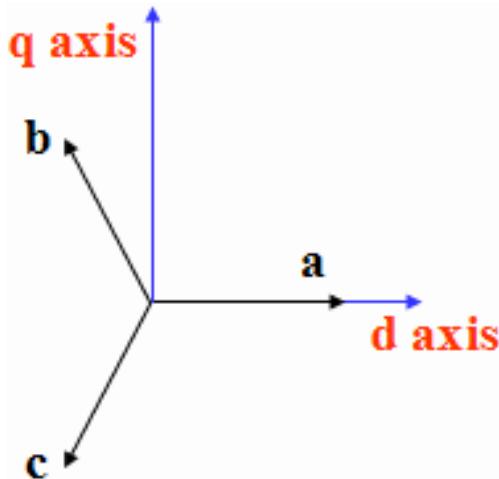


Fig. 2.6 The relationship of *abc* reference frame and stationary *dq* reference frame

As a result of the transformation, six non-zero vectors and two zero vectors are possible. Six nonzero vectors ($V_1 - V_6$) shape the axes of a hexagonal as

depicted in Fig. 2.7, and feed electric power to the load. The angle between any adjacent two non-zero vectors is 60 degrees. Meanwhile, two zero vectors (V_0 and V_7) are at the origin and apply zero voltage to the load. The eight vectors are called the basic space vectors and are denoted by V_0 , V_1 , V_2 , V_3 , V_4 , V_5 , V_6 , and V_7 . The same transformation can be applied to the desired output voltage to get the desired reference voltage vector V_{ref} in the d-q plane.

The objective of space vector PWM technique is to approximate the reference voltage vector V_{ref} using the eight switching patterns. One simple method of approximation is to generate the average output of the inverter in a small period, T to be the same as that of V_{ref} in the same period.

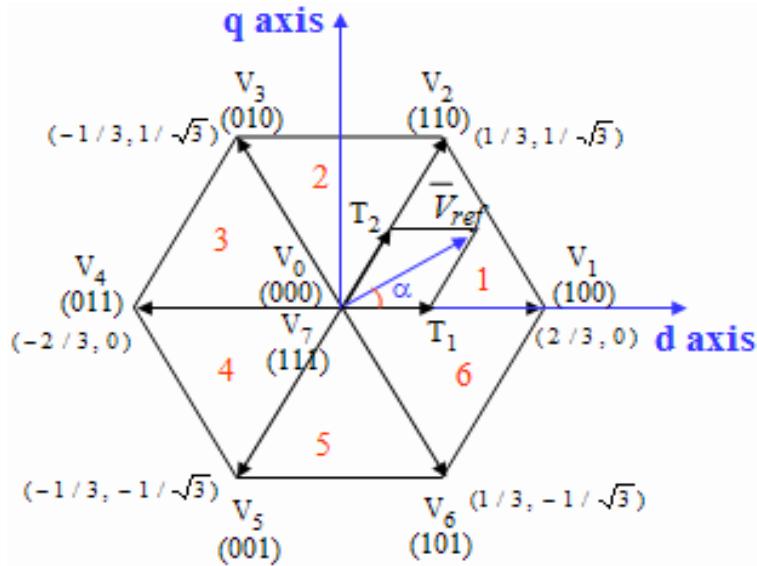


Fig. 2.7 Basic switching vectors and sectors.

2.2.3. Steps to Implement SVPWM

Therefore, space vector PWM can be implemented by the following steps:

- Step 1. Determine V_d , V_q , V_{ref} , and angle (α)
- Step 2. Determine time duration T_1 , T_2 , T_0
- Step 3. Determine the switching time of each transistor (S_1 to S_6)

Step 1: Determine V_d , V_q , V_{ref} , and angle (α)

From Fig. 2.8, the V_d , V_q , V_{ref} , and angle (α) can be determined as follows:

$$\begin{aligned} V_d &= V_{an} - V_{bn} \cdot \cos 60 - V_{cn} \cdot \cos 60 \\ &= V_{an} - \frac{1}{2} V_{bn} - \frac{1}{2} V_{cn} \end{aligned}$$

$$\begin{aligned} V_q &= 0 + V_{bn} \cdot \cos 30 - V_{cn} \cdot \cos 30 \\ &= V_{an} + \frac{\sqrt{3}}{2} V_{bn} - \frac{\sqrt{3}}{2} V_{cn} \end{aligned}$$

$$\therefore \begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix}$$

$$\therefore |\bar{V}_{ref}| = \sqrt{V_d^2 + V_q^2}$$

$$\therefore \alpha = \tan^{-1} \left(\frac{V_q}{V_d} \right) = \omega t = 2\pi f t, \quad (2.3)$$

Where f= fundamental frequency.

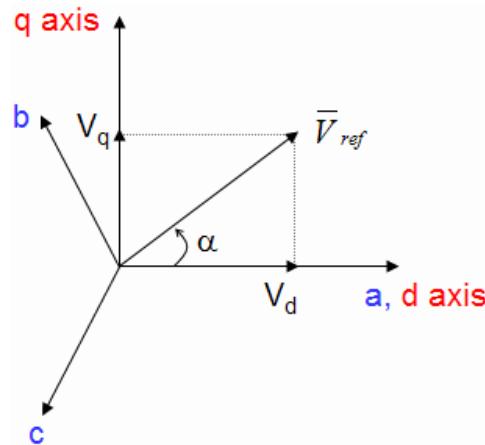


Fig 2.3 Voltage Space Vector and its components in (d, q).

Step 2: Determine time duration T_1, T_2, T_0

From Fig. 2.9, the switching time duration can be calculated as follows:

- Switching time duration at Sector 1

$$\int_0^{T_z} \bar{V}_{\text{ref}} = \int_0^{T_1} \bar{V}_1 dt + \int_{T_1}^{T_1+T_2} \bar{V}_2 dt + \int_{T_1+T_2}^{T_z} \bar{V}_0$$

$$\therefore T_z \cdot \bar{V}_{\text{ref}} = (T_1 \cdot \bar{V}_1 + T_2 \cdot \bar{V}_2)$$

$$\Rightarrow T_z \cdot |\bar{V}_{\text{ref}}| \cdot \begin{bmatrix} \cos(\alpha) \\ \sin(\alpha) \end{bmatrix} = T_1 \cdot \frac{2}{3} \cdot V_{dc} \cdot \begin{bmatrix} 1 \\ 0 \end{bmatrix} + T_2 \cdot \frac{2}{3} \cdot V_{dc} \cdot \begin{bmatrix} \cos(\pi/3) \\ \sin(\pi/3) \end{bmatrix}$$

(where, $0 \leq \alpha \leq 60^\circ$)

$$\therefore T_1 = T_z \cdot a \cdot \frac{\sin(\pi/3 - \alpha)}{\sin(\pi/3)}$$

$$\therefore T_2 = T_z \cdot a \cdot \frac{\sin(\alpha)}{\sin(\pi/3)}$$

$$\therefore T_0 = T_z - (T_1 + T_2), \quad \left(\text{where, } T_z = \frac{1}{f_z} \text{ and } a = \frac{|\bar{V}_{\text{ref}}|}{\frac{2}{3} V_{dc}} \right) \quad (2.4)$$

- Switching time duration at any Sector

$$\therefore T_1 = \frac{\sqrt{3} \cdot T_z \cdot |\bar{V}_{\text{ref}}|}{V_{dc}} \left(\sin \left(\frac{\pi}{3} - \alpha + \frac{n-1}{3} \pi \right) \right)$$

$$= \frac{\sqrt{3} \cdot T_z \cdot |\bar{V}_{\text{ref}}|}{V_{dc}} \left(\sin \frac{n}{3} \pi - \alpha \right)$$

$$= \frac{\sqrt{3} \cdot T_z \cdot |\bar{V}_{\text{ref}}|}{V_{dc}} \left(\sin \frac{n}{3} \pi \cos \alpha - \cos \frac{n}{3} \pi \sin \alpha \right)$$

$$\begin{aligned}
T_2 &= \frac{\sqrt{3} \cdot T_z \cdot |\bar{V}_{ref}|}{V_{dc}} \left(\sin \left(\alpha - \frac{n-1}{3} \pi \right) \right) \\
&= \frac{\sqrt{3} \cdot T_z |\bar{V}_{ref}|}{V_{dc}} \left(-\cos \alpha \cdot \sin \frac{n-1}{3} \pi + \sin \alpha \cdot \cos \frac{n-1}{3} \pi \right) \\
\therefore T_0 &= T_z - T_1 - T_2, \quad \left(\begin{array}{l} \text{where, } n = 1 \text{ through } 6 \text{ (that is, Sector 1 to 6)} \\ 0 \leq \alpha \leq 60^\circ \end{array} \right) \quad (2.5)
\end{aligned}$$

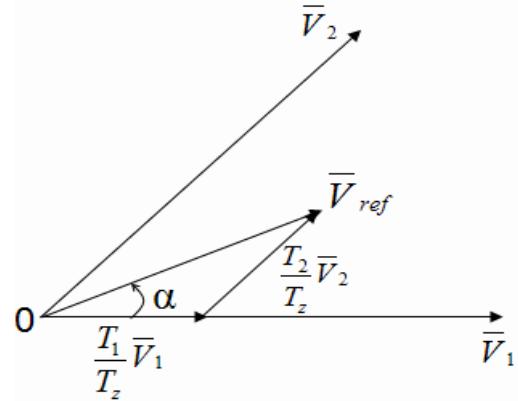
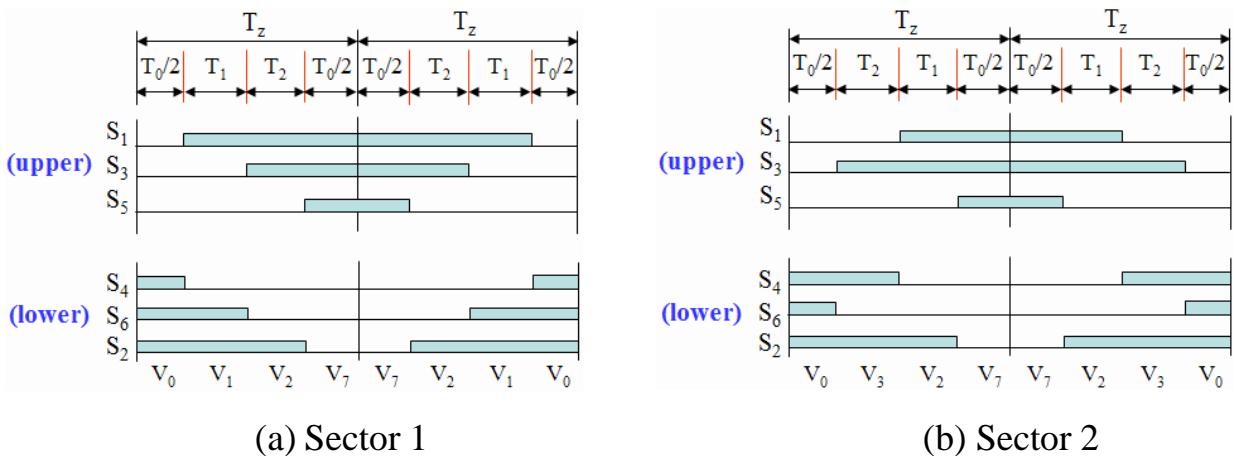


Fig. 2.9. Reference vector as a combination of adjacent vectors at sector 1.

Step 3: Determine the switching time of each transistor (S₁ to S₆)

Fig. 2.10 shows space vector PWM switching patterns at each sector.



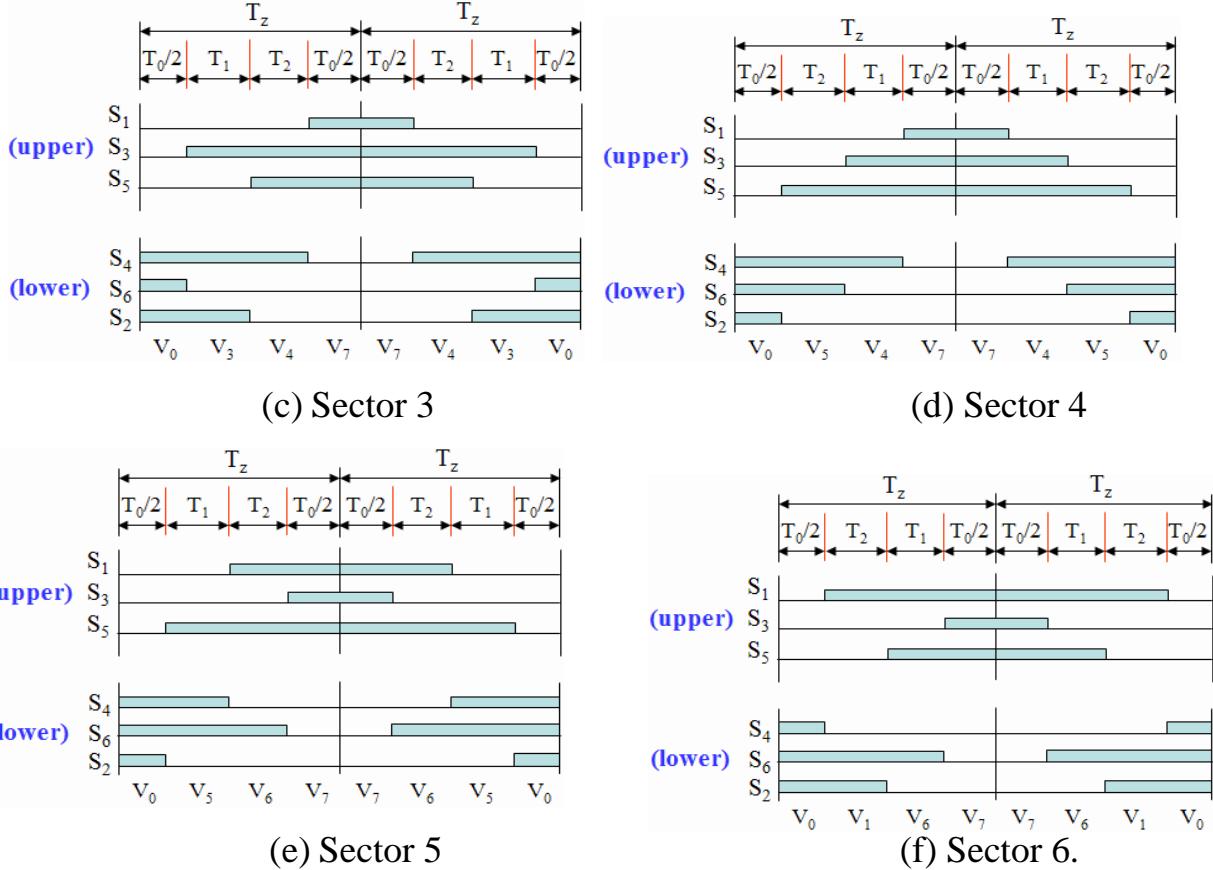


Fig.2.10. Space Vector PWM switching patterns at each sector.

Based on Fig.2.10, the switching time at each sector is summarized in Table 2.2.

Sector	Upper Switches (S_1, S_3, S_5)	Lower Switches (S_4, S_6, S_2)
1	$S_1 = T_1 + T_2 + T_0 / 2$ $S_3 = T_2 + T_0 / 2$ $S_5 = T_0 / 2$	$S_4 = T_0 / 2$ $S_6 = T_1 + T_0 / 2$ $S_2 = T_1 + T_2 + T_0 / 2$
2	$S_1 = T_1 + T_0 / 2$ $S_3 = T_1 + T_2 + T_0 / 2$ $S_5 = T_0 / 2$	$S_4 = T_2 + T_0 / 2$ $S_6 = T_0 / 2$ $S_2 = T_1 + T_2 + T_0 / 2$
3	$S_1 = T_0 / 2$ $S_3 = T_1 + T_2 + T_0 / 2$ $S_5 = T_2 + T_0 / 2$	$S_4 = T_1 + T_2 + T_0 / 2$ $S_6 = T_0 / 2$ $S_2 = T_1 + T_0 / 2$
4	$S_1 = T_0 / 2$ $S_3 = T_1 + T_0 / 2$ $S_5 = T_1 + T_2 + T_0 / 2$	$S_4 = T_1 + T_2 + T_0 / 2$ $S_6 = T_2 + T_0 / 2$ $S_2 = T_0 / 2$
5	$S_1 = T_2 + T_0 / 2$ $S_3 = T_0 / 2$ $S_5 = T_1 + T_2 + T_0 / 2$	$S_4 = T_1 + T_0 / 2$ $S_6 = T_1 + T_2 + T_0 / 2$ $S_2 = T_0 / 2$
6	$S_1 = T_1 + T_2 + T_0 / 2$ $S_3 = T_0 / 2$ $S_5 = T_1 + T_0 / 2$	$S_4 = T_0 / 2$ $S_6 = T_1 + T_2 + T_0 / 2$ $S_2 = T_2 + T_0 / 2$

Table 2.2. Switching Time Calculation at Each Sector

2.3. Digital Implementation:

8-bit PIC18F4331 microcontroller was chosen to obtain the gate pulses for the inverter. This Microcontroller is operated at 20MHz and has 33 input/output (I/O) pins, interrupts, counters, timers, I/O ports, RAM, and ROM/EPROM. The Peripheral Interface Controllers (PICs) are the integrated circuits based on CMOS technology. The main components of a PIC are RAM, EPROM, EEPROM, and Peripheral Interface Adaptor (PIA). The address bus, the data bus and the control bus connecting the components are placed in the PIC circuit by the manufacturer. Because of these advantages, PICs have been preferred devices in practical control applications. The PIC used here runs each instruction as fast as 200 ns. Flash Program Memory is up to 8Kb. Data memory is partitioned into four banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits. Each bank extends up to 7Fh (128 bytes). It contains 256 bytes of EEPROM, 768 bytes of SRAM, 15 special hardware registers, 36 general purpose registers and 64 byte EEPROM as a data memory. PICs have been preferred control devices because of their low cost, less energy consumption and small volume.

The primary reason PIC18F4331 was chosen over other PIC controllers is the availability of a Power Control PWM module which can provide upto four PWM generators, each of which has two channels, for motor control operation. Its features are:

- Up to 4 Channels with Complementary Outputs
- Edge or Center-Aligned Operation
- Flexible Dead-Band Generator
- Hardware Fault Protection Inputs
- Simultaneous Update of Duty Cycle and Period

- Flexible Special Event Trigger output

The Power Control PWM module simplifies the task of generating multiple, synchronized Pulse-Width Modulated (PWM) outputs for use in the control of motor controllers and power conversion applications. This module contains four duty cycle generators, numbered 0 through 3. The module has eight PWM output pins, numbered 0 through 7. The eight PWM outputs are grouped into output pairs of even and odd numbered outputs. In Complementary modes, the even PWM pins must always be the complement of the corresponding odd PWM pin. The dead-time generator inserts an OFF period called “dead time” between the going OFF of one pin to the going ON of the complementary pin of the paired pins. This is to prevent damage to the power switching devices that will be connected to the PWM output pins. This module operates in four different modes out of which the Continuous Up/Down mode gives Center-aligned operation. In Continuous Up/Down Count modes, the PWM time base counts upwards until the value in the PTPER register matches with the PTMR register. On the following input clock edge, the timer counts downwards. The PTDIR bit in the PTCON1 register is read-only and indicates the counting direction. The PTDIR bit is set when the timer counts downwards. The PWM period is calculated using the following formula:

$$TPWM = ((PTPER + 1) \times PTMRPS) / (FOSC/4)$$

Where TPWM is the PWM period given by 1/PWM frequency;

PTPER is the value to be loaded to the PTPER register;

PTMRPS is the PWM Timer PostScale, chosen to be 1 here and

FOSC is the crystal frequency.

Some sample PWM frequencies and resolutions are given in Table 2.3.

PWM Frequency = 1/T _{PWM}				
Fosc	MIPS	PTPER Value	PWM Resolution	PWM Frequency
40 MHz	10	0FFFh	14 bits	2.4 kHz
40 MHz	10	07FFh	13 bits	4.9 kHz
40 MHz	10	03FFh	12 bits	9.8 kHz
40 MHz	10	01FFh	11 bits	19.5 kHz
40 MHz	10	FFh	10 bits	39.0 kHz
40 MHz	10	7Fh	9 bits	78.1 kHz
40 MHz	10	3Fh	8 bits	156.2 kHz
40 MHz	10	1Fh	7 bits	312.5 kHz
40 MHz	10	0Fh	6 bits	625 kHz
25 MHz	6.25	0FFFh	14 bits	1.5 kHz
25 MHz	6.25	03FFh	12 bits	6.1 kHz
25 MHz	6.25	FFh	10 bits	24.4 kHz
10 MHz	2.5	0FFFh	14 bits	610 Hz
10 MHz	2.5	03FFh	12 bits	2.4 kHz
10 MHz	2.5	FFh	10 bits	9.8 kHz
5 MHz	1.25	0FFFh	14 bits	305 Hz
5 MHz	1.25	03FFh	12 bits	1.2 kHz
5 MHz	1.25	FFh	10 bits	4.9 kHz
4 MHz	1	0FFFh	14 bits	244 Hz
4 MHz	1	03FFh	12 bits	976 Hz
4 MHz	1	FFh	10 bits	3.9 kHz

Table 2.3. Example PWM Frequencies and Resolutions

The switching frequency, input dc voltage and desired output magnitude are chosen and the corresponding switching times for one cycle of the fundamental period are calculated for each sector and stored in an MS Excel Sheet. Then the duty cycles to be loaded to each of the PWM generators are calculated in the same sheet. The upper and lower limb switches of the first limb of the inverter are connected to PWM generator 1, those of second limb to PWM generator 2 and those of the last limb to PWM generator 2 in the PIC. These duty cycles are then

stored as ROM array variables in the program memory of the PIC. The PIC is programmed such that upon detecting the zero crossing of phase a, done using a Zero Crossing Detector, the gate pulses for the six switches are generated continuously. It may be noted that the PIC inherently allows gate signals of the same limb to be complementary and thus no extra programming is required to ensure that. Care is taken to generate sufficient dead-times, using the Dead Time Generation block provided in the PIC'S PCPWM module, so that no two switches in the same limb are simultaneously turned when switching from HIGH to LOW or LOW to HIGH is made. The programming is done using MPLAB IDE and C18 compiler.

CHAPTER 3

SPACE VECTOR MODULATED RECTIFIER

3.1. Three-phase Rectifiers

In Fig. 3.1, the basic rectifier topology is presented. This structure is derived from the bidirectional rectifier with the additional dc rail diode. A large number of topologies of unidirectional pulse width modulation (PWM) rectifiers are available with power factor correction. A generalized topology as presented in Fig.3.1 is assumed to be the fictitious rectifier feeding the inverter in indirect modulation strategy of a matrix converter.

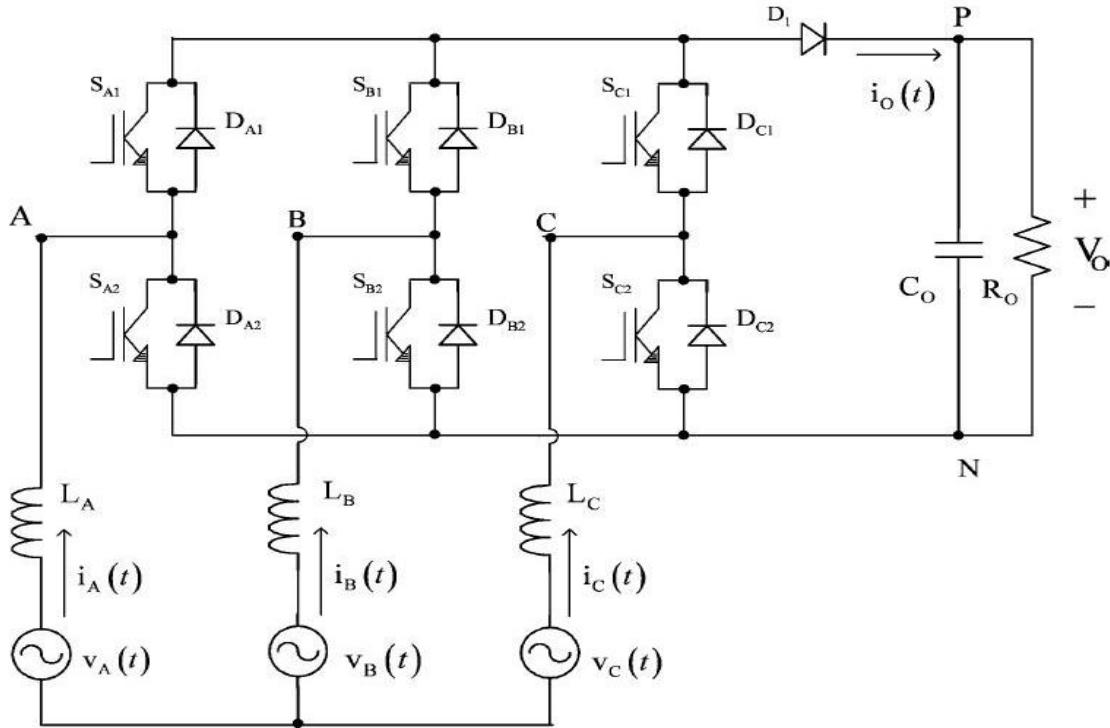


Fig.3.1. Three-phase Rectifier Topology

3.2. Space Vector Modulation

The Space Vector Modulation strategy followed in three-phase rectifiers is very similar to the one followed for three-phase inverters. But it must be seen that while the modulation is done on the output voltage vectors in an

inverter, the modulation is done on the input current vectors in a rectifier. Thus while an inverter provides output voltage modulation, a rectifier provides input current modulation.

The complex current space vector is represented by

$$i_0 = 2/3 [i_{AB}(t) + i_{BC}(t) e^{j2\pi/3} + i_{CA}(t) e^{j4\pi/3}] = i_{ol} e^{j\omega t} \quad (3.1)$$

Here 2/3 is the scaling factor and $e^{j\omega t}$ represents phase shift operator.

In the SVM method, the valid switching states of a rectifier are represented as current space vectors. Within a sufficiently small time interval a set of these vectors are chosen to approximate a reference current vector with the desired frequency and amplitude. At the next sample instant, when the reference current vector rotates to a new angular position, a new set of stationary current vectors are selected. Carrying this process onward by sequentially sampling the complete cycle of the desired current vector, the average current emulates closely the reference current. Meanwhile, the selected vectors should also give the desired phase shift between the input voltage and current. The available vectors are represented in Table 3.1.

Vector	Point A	Point B	Point C	\mathbf{V}_{AB}	\mathbf{V}_{BC}	\mathbf{V}_{CA}
$\vec{V}_0 (0 0 0)$		$A = B = C$		0	0	0
$\vec{V}_1 (1 0 0)$	P	N	N	$+V_o$	0	$-V_o$
$\vec{V}_2 (1 1 0)$	P	P	N	0	$+V_o$	$-V_o$
$\vec{V}_3 (0 1 0)$	N	P	N	$-V_o$	$+V_o$	0
$\vec{V}_4 (0 1 1)$	N	P	P	$-V_o$	0	$+V_o$
$\vec{V}_5 (0 0 1)$	N	N	P	0	$-V_o$	$+V_o$
$\vec{V}_6 (1 0 1)$	P	N	P	$+V_o$	$-V_o$	0

Table 3.1. Available current vectors

Here each sector is divided into a subsector based on the direction of the currents. The current space vector representation with definition of subsectors is shown in Fig.3.2.

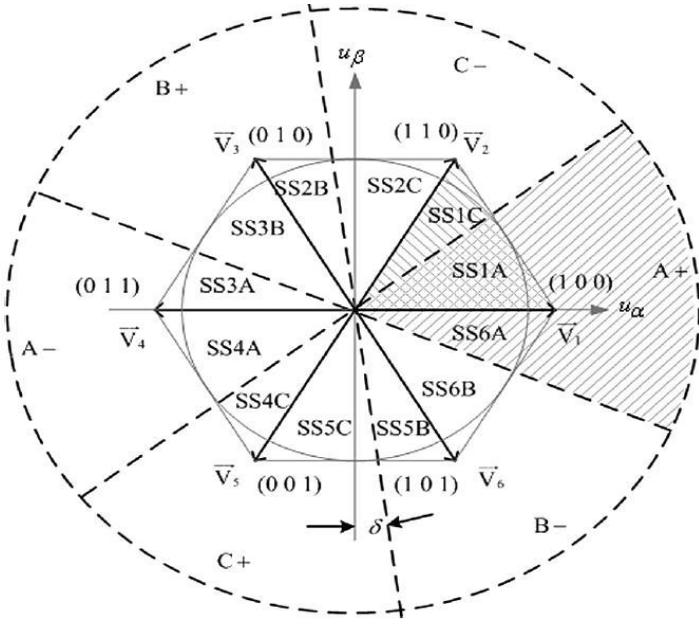


Fig. 3.2. Space vector representation with definition of subsectors.

The definition of subsectors is elaborated in Fig.3.3

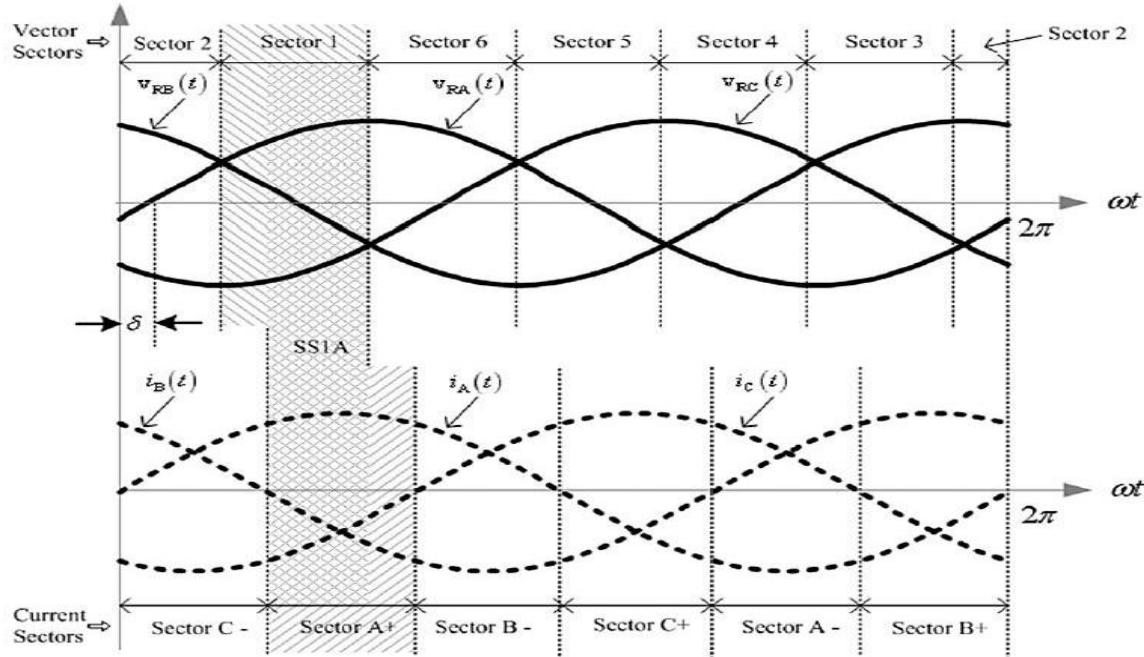


Fig. 3.3. Definition of subsectors

The same methodology used to apply the space vector modulation technique in inverters is extended to unidirectional PWM rectifiers. This methodology is summarized as:

- 1) identification of current sectors and vector sectors, and definition of subsectors;
 - 2) analysis of topological stages of the converter and verification of available vectors in each subsector;
 - 3) definition of most appropriate logic for the available command signals and vector sequence;
 - 4) determination of intervals for application of vectors and calculation of duty cycle functions in subsectors;
 - 5) implementation of command signals from the PWM.

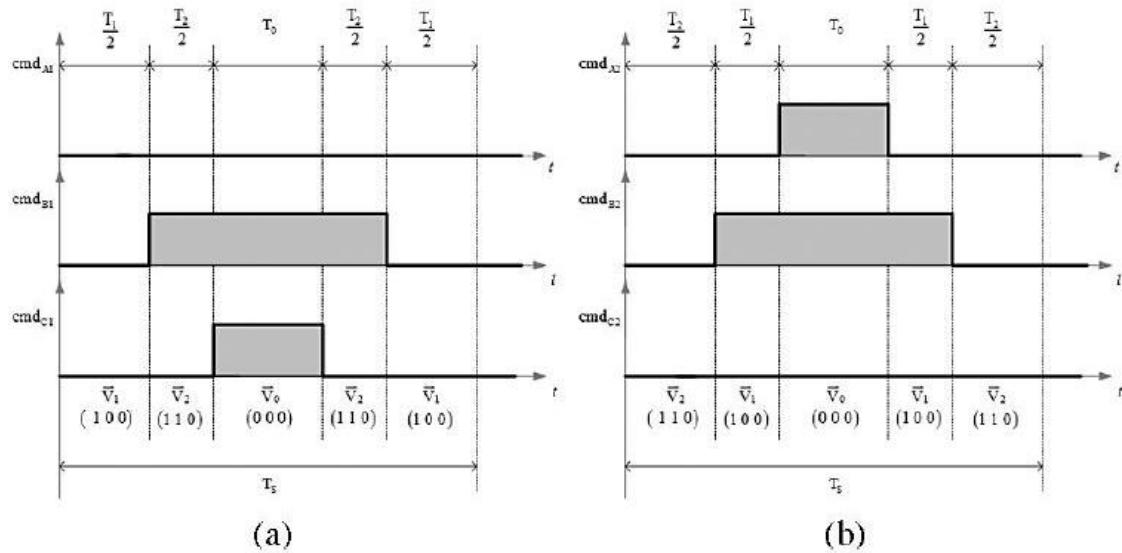


Fig. 3.4. Drive signals for rectifier. (a) Subsector SS1A. (b) Subsector SS1C.

Sample drive signals are represented in Fig.3.4. They represent drive signals in sector 1 when the switching sequence followed is as in Table 3.2.

Sub-Sector	Vector sequence	Signal of I
SS1A	$\vec{V_1} \vec{V_2} \vec{V_0} \vec{V_2} \vec{V_1}$	+
SS1C	$\vec{V_2} \vec{V_1} \vec{V_0} \vec{V_1} \vec{V_2}$	-
SS2C	$\vec{V_2} \vec{V_3} \vec{V_0} \vec{V_3} \vec{V_2}$	-
SS2B	$\vec{V_3} \vec{V_2} \vec{V_0} \vec{V_2} \vec{V_3}$	+

Table 3.2. Vector sequence

The switching times are calculated using a strategy similar to the one adopted for inverters.

3.3. Digital Implementation:

8-bit PIC18F4331 microcontroller was chosen to obtain the gate pulses for the inverter. This Microcontroller is operated at 20MHz and has 33 input/output (I/O) pins, interrupts, counters, timers, I/O ports, RAM, and ROM/EPROM. The Peripheral Interface Controllers (PICs) are the integrated circuits based on CMOS technology. The main components of a PIC are RAM, EPROM, EEPROM, and Peripheral Interface Adaptor (PIA). These components are inserted in the same integrated circuit to reduce the size, the cost of the system and make design of the system easier. The address bus, the data bus and the control bus connecting the components are placed in the PIC circuit by the manufacturer. Because of these advantages, PICs have been preferred devices in practical control applications. The PIC used here runs each instruction as fast as 200 ns. Flash Program Memory is up to 8Kb. Data memory is partitioned into four banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 and RP0 are the bank select bits. Each bank extends up to 7Fh (128 bytes). It contains 256 bytes of EEPROM, 768 bytes of SRAM, 15 special hardware registers, 36 general purpose registers and 64 byte EEPROM as a data memory. PICs have been preferred control devices because of their low cost, less energy consumption and small volume.

The principal difference between the implementation of SVM in rectifier from that of inverter is that PIC18F4331 is designed to drive gate signals for inverters. It provides complementary PWM channels on a single PWM generator which is not necessary for rectifiers. Although it is possible to configure the module to work in non-complementary mode, only a single duty cycle may be loaded to both channels in a single generator. Thus six PWM generators are

required to generate six individual gate pulses which mean the requirement of another PIC controller and a possible wastage of resources.

Further the gate pulses for the rectifier are staggered and although a fixed duty cycle may be generated for each sampling period, it is not possible to define these gate pulses using a fixed pattern as the ON period is neither center-aligned nor edge-aligned. Thus it is not possible to operate the Power Control PWM module in any of the specified modes.

In order to avoid complexity of programming, a simpler approach is chosen wherein the required time periods are calculated and specified explicitly as delay times for the micro-controller. This approach eliminates the need for the PCPWM module, though it has a drawback: the dead times have to be manually specified as automatic generation of dead times are possible only when the PCPWM module is used.

In order to program the microcontroller, similar to an inverter, the switching frequency, input voltage and desired output magnitude are chosen and the corresponding switching times for one cycle of the fundamental period are calculated for each sector and stored in an MS Excel Sheet. Then these times are stored as ROM variables in the program memory of the micro-controller and explicitly loaded during program execution in order to specify the time for which each state occurs. These times are specified using inbuilt delay functions. The MPLAB IDE and CCS C compiler are chosen for programming. Here the CCS C compiler is preferred over the C18 compiler due to ease of use and a more convenient range of delay functions available.

CHAPTER 4

SPACE VECTOR MODULATED MATRIX CONVERTER

4.1. Three-phase Matrix Converter topology

The matrix converter has several advantages over traditional rectifier-inverter type power frequency converter. The three-phase matrix converter has 9 bi-directional switches that allow any output phase to be connected to any input phase. The circuit scheme is shown in Fig.4.1.

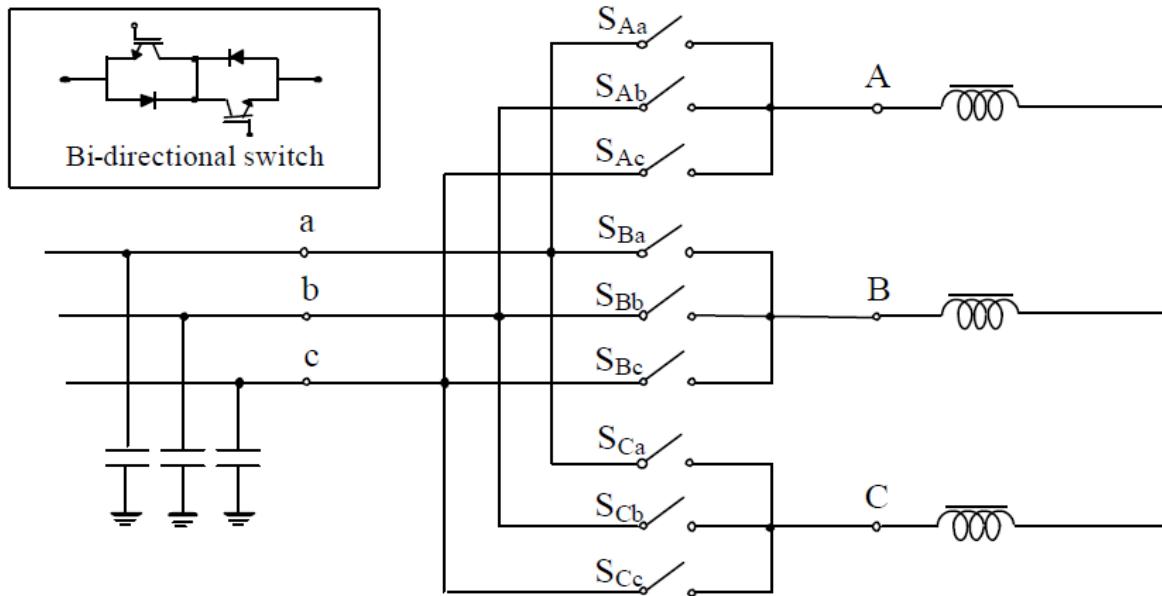


Fig.4.1. Three-phase Matrix Converter Topology.

The multiple conversion stages and energy storage components of conventional inverter and cycloconverter circuits can be replaced by one switching matrix. The number of input and output phases do not have to be equal so that rectification, inversion, and frequency conversion are all realizable. The phase angles between the voltages and currents at the input can be controlled to give unity displacement factor for any loads. Both sides of the matrix cannot be voltage sources simultaneously since this would involve the direct connection of

unequal voltages. If the input is a voltage source, then the output must be a current source, and vice versa. It is a basic requirement that the switching functions must not short circuit the voltage sources nor open circuit the current sources.

The basic circuit of a three-phase to three-phase matrix converter is shown in Fig.4.1 consists of three-phase groups. Each of the nine switches can either block or conduct current in both directions thus allowing any of the output phases to be connected to any of the input phases. The input side of the converter is a voltage source, and the output is a current source. Only one of the three switches connected to the same output phase can be on at any instant of time.

4.2. Switching States of Three-Phase Matrix Converter

With 9 bi-directional switches the matrix converter can have theoretically assume $512 (2^9)$ different switching states combinations. But not all of them can be usefully employed. Regardless to the control method used, the choice of matrix converter switching states combinations to be used must comply with two basic rules. Taking into account the converter is supplied by a voltage source and usually feeds an inductive load, the input phases should never be short-circuited and the output current should not be interrupted. From practical point of view these rules imply that one and only bi-directional switch of output phase must be switched on at any instant. By this constraint, in a three-phase to three-phase matrix converter 27 are permitted switching combinations.

4.3. Input filter

Although the matrix converter is sometimes presented as an all silicon solution, due to lack of bulky and expensive dc link capacitors of traditional indirect frequency converter, it also requires a minimum of reactive components. The input filter acts like an interface between the matrix converter and the ac mains. The basic input filter configuration are shown in Fig.4.2.

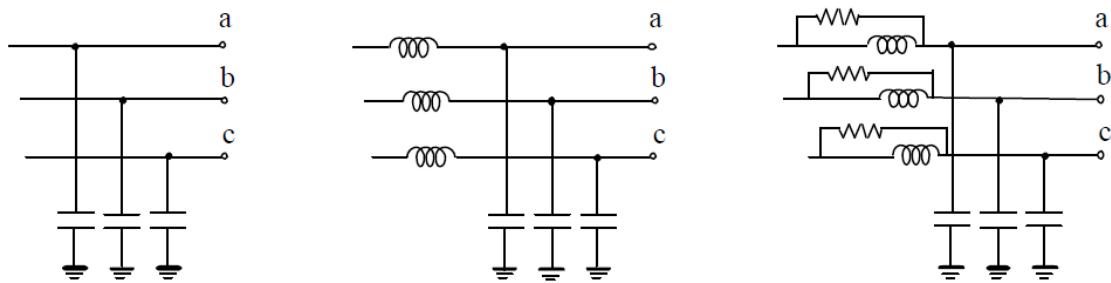


Fig.4.2. Basic input filter configuration used in matrix converter prototypes.

4.4 Venturini Control Method

A generalized high-frequency switching strategy for matrix converters was proposed by venturini in 1980. This method was further modified to increase the output-to-input voltage transfer ratio from 0.5 to 0.866. In addition, it can generate sinusoidal input currents at unity power factor irrespective of the load power factor.

4.5 Space Vector Modulation (SVM) Control Method

The space vector modulation (SVM) technique adopts a different approach to the Venturini method-it constructs the desired sinusoidal output three-phase voltage by selecting the valid switching states of a three-phase and calculating their corresponding on-time durations. In indirect method of modulation SVM is done on a fictitious rectifier and a fictitious inverter.

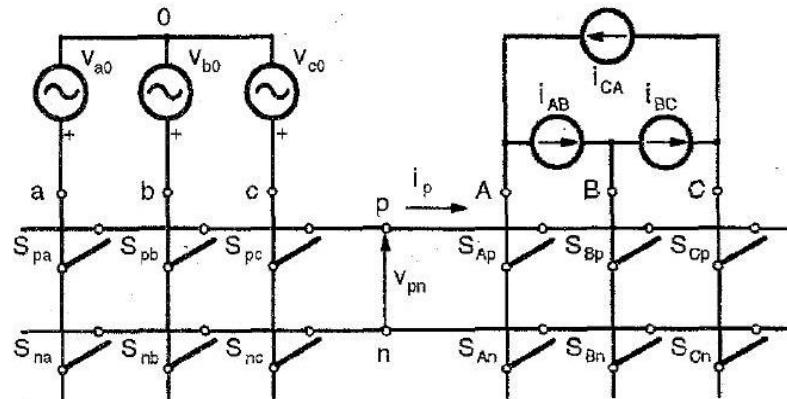


Fig 4.3 Emulation of VSR-VSI conversion

A simplified circuit of the Voltage Source Rectifier (VSR)- Voltage Source Inverter (VSI) conversion is shown in Fig.4.3.

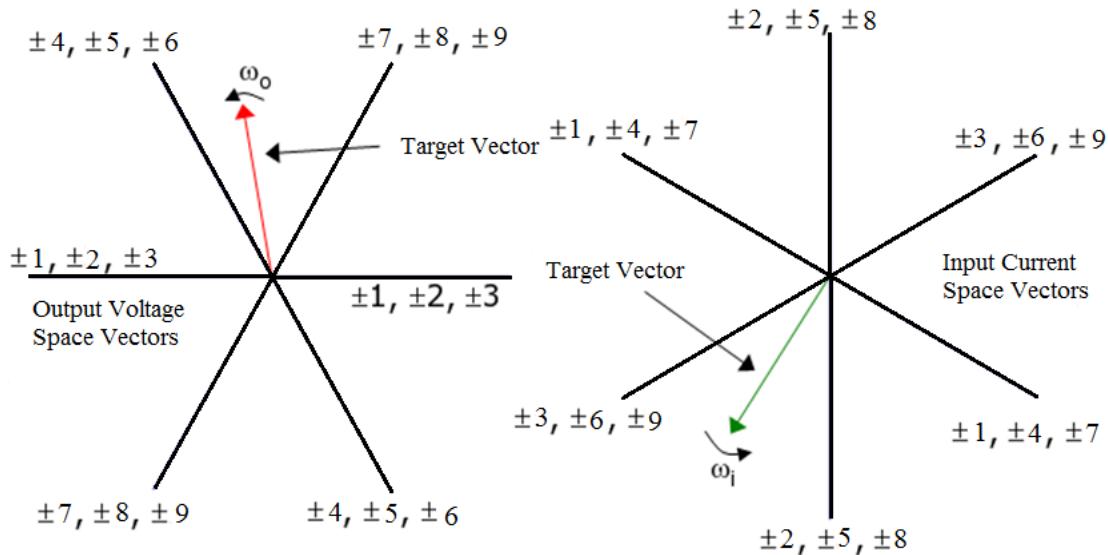


Fig 4.4 Output Voltage and Input Current Vectors

Fig 4.4 shows the output voltage vectors and the input current vectors. Thus Space Vector Modulation (SVM) is an indirect method used for the operation of three-phase matrix converter topologies.

SSV Pair	Switching Combination				Output Line Voltage			Input Phase Current			Switch States								
	p	n	A	B	C	v _{AB}	v _{BC}	v _{CA}	i _a	i _b	i _c	s _{Aa}	s _{Ab}	s _{Ac}	s _{Ba}	s _{Bb}	s _{Bc}	s _{Ca}	s _{Cb}
I ₆ -V ₆	a	b	a	b	a	v _{ab}	-v _{ab}	0	-i _B	i _B	0	1	0	0	0	1	0	1	0
I ₆ -V ₁	a	b	a	b	b	v _{ab}	0	-v _{ab}	i _A	-i _A	0	1	0	0	0	1	0	0	1
I ₁ -V ₆	a	c	a	c	c	v _{ac}	0	-v _{ac}	i _A	0	-i _A	1	0	0	0	0	1	0	0
I ₁ -V ₁	a	c	a	c	a	v _{ac}	-v _{ac}	0	-i _B	0	i _B	1	0	0	0	0	1	1	0
I ₀ -V ₀	a	a	a	a	a	0	0	0	0	0	0	1	0	0	1	0	0	1	0

Table 4.1 Matrix Switching Sequence example

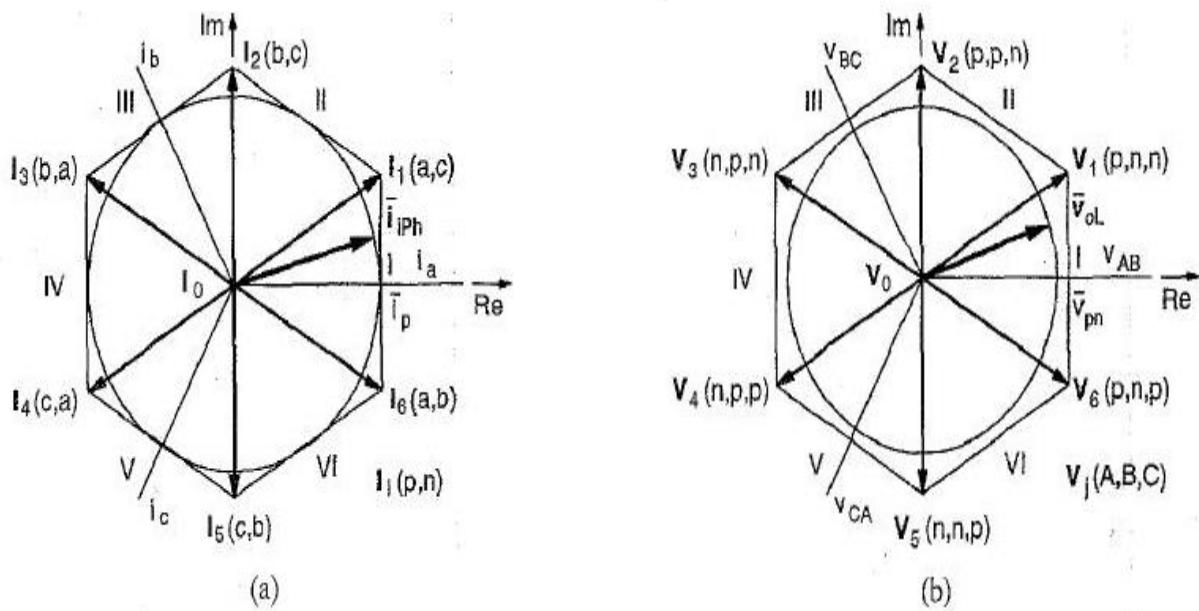


Fig 4.5 Voltage and Current Hexagons

An example of the matrix switching sequence is presented in Table 4.1 and the Voltage and Current Hexagons are shown in Fig.4.5.

Let the rectifier switching matrix be represented by

$$R = \begin{bmatrix} r1 & r3 & r5 \\ r2 & r4 & r6 \end{bmatrix} \quad (4.1)$$

The inverter switching matrix is represented by

$$I = \begin{bmatrix} i1 & i3 & i5 \\ i2 & i4 & i6 \end{bmatrix} \quad (4.2)$$

The matrix converter switching matrix is obtained by taking the transpose of the inverter matrix and multiplying it with that of the inverter.

$$M = R^T * I = \begin{bmatrix} r1 & r2 \\ r3 & r4 \\ r5 & r6 \end{bmatrix} \begin{bmatrix} i1 & i3 & i5 \\ i2 & i4 & i6 \end{bmatrix} = \begin{bmatrix} m11 & m12 & m13 \\ m21 & m22 & m23 \\ m31 & m32 & m33 \end{bmatrix} \quad (4.3)$$

4.6. Digital Implementation

8-bit PIC18F4550 microcontroller was chosen to obtain the gate pulses for the inverter. This Microcontroller is operated at 20MHz and has 33

input/output (I/O) pins, interrupts, counters, timers, I/O ports, RAM, and ROM/EPROM. The PIC Control circuit is shown in Fig.4.6.

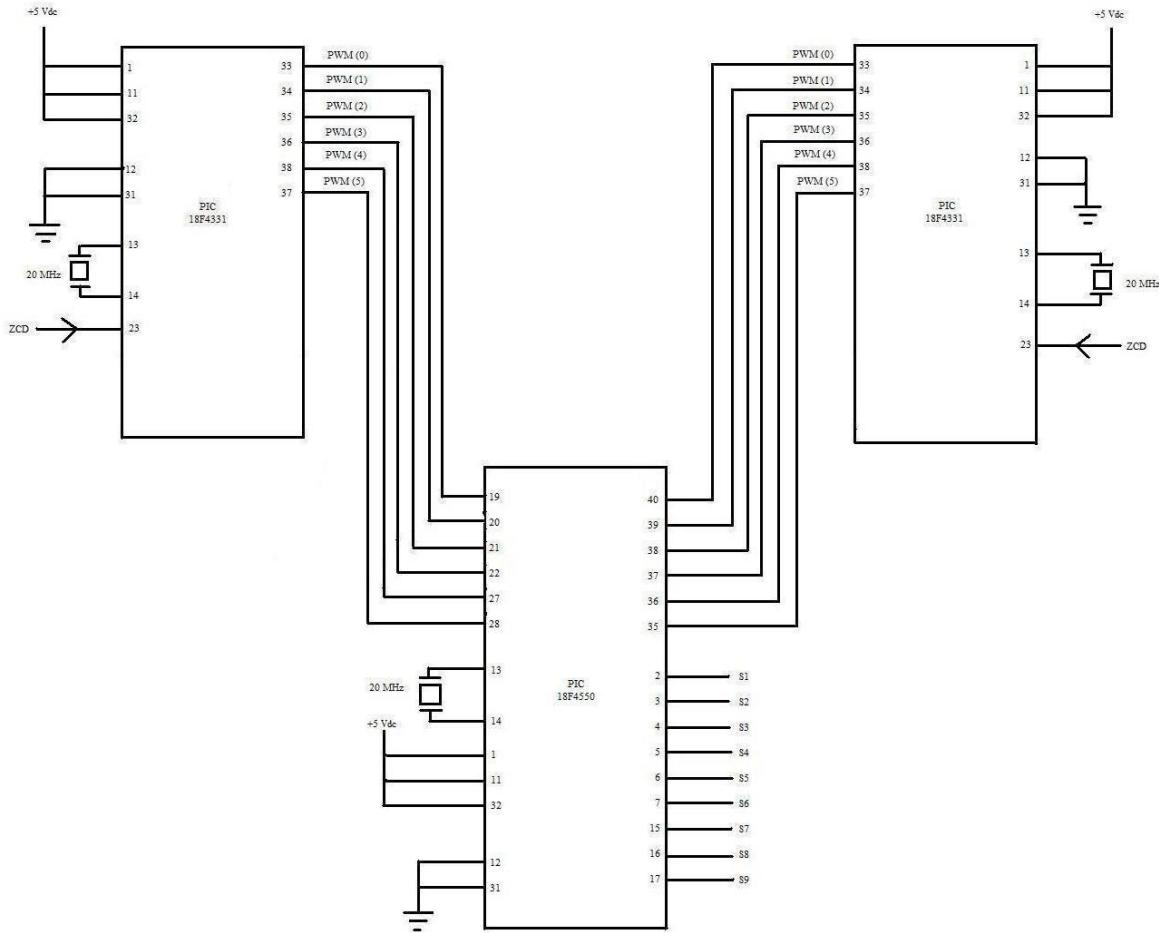


Fig 4.6 Control Circuit

The gate pulses for inverter and rectifier are generated using two PIC18F4331s. These two ICs are synchronised with a ZCD in order to detect the sector. The necessary mathematical operations of performed in PIC18F4550 and the nine signals are obtained from it. Since a Power Control PWM module is not necessary to realize this, PIC18F4550 is chosen. Further, since each 4QSW consists of two IGBTs, it is necessary to replicate these signals. Thus a total of 18 gate signals are obtained from the PIC18F4550. The programming is done using MPLAB IDE and C18 compiler.

4.7. Zero Crossing Detector

The need for the zero crossing detector (ZCD) arises as the supply frequency is not constant and varies between 47Hz and 52Hz. Hence the ZCD is used to sense the half cycle time through which the frequency of input voltage sinusoid is known. Fig. 4.7 shows the pin diagram of the ZCD used.

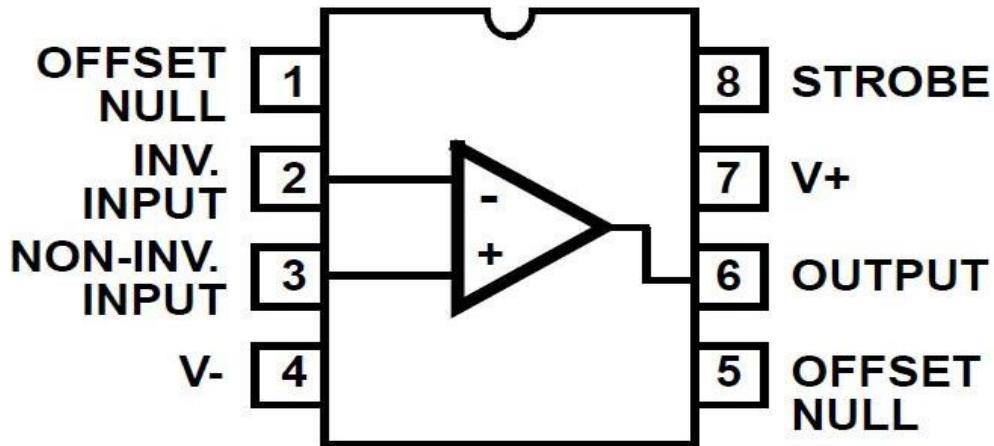


Fig 4.7 Pin diagram of ZCD IC- CA3130

CA3130 is a high-speed comparator with TTL compatible push-pull output. A 230/3V transformer is used to step down the supply voltage. The voltage is fed as positive input to the comparator. The negative input of the comparator is maintained at the reference voltage. The ZCD output will remain high throughout the positive half cycle and low through the negative half cycle. Only phase a of the supply voltage is fed to the input transformer. It is seen that when phase a crosses zero on a rising edge, the reference is at 0 degrees. This is detected in the microcontroller using external edge-triggered interrupts.

4.8. Isolation Circuit

In the power circuit the drain terminals of the power switches are not at the same potential. Isolation is required between the control and the power circuit. This is attained by using the optocoupler 4N26. The IR led is fed by the switching signal from the microcontroller. The collector-emitter bias of the

phototransistor is provided by separate 12V sources. Each 12V source is obtained by rectifying the output of a 230/12V transformer using RB156 bridge rectifier and regulated by a LM7812 voltage regulator.

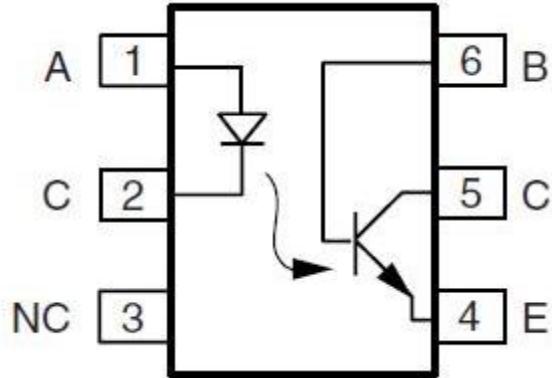


Fig 4.8 Pin diagram of optocoupler IC- 4N26

4.9. Driver Circuit

The output of the isolation circuit is fed to the driver circuit. The driver used here is IXDD614PI. The pin diagram is shown in Fig. 4.9.

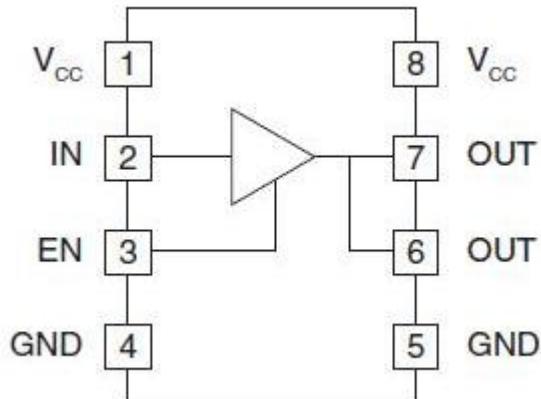


Fig 4.9 Pin diagram of driver IC- IXDD614PI

IXDD614PI is a high speed IGBT driver, characterized by peak current withstand capability of 14A. This has separate source and sink outputs to individually control the rise and fall times of the switching pulse. As fast switching is preferred, the source and sink output have been directly shorted and fed to the gate of the IGBT.

CHAPTER-5

SIMULATION AND HARDWARE RESULTS ANALYSIS

The simulations have been conducted assuming an ideal supply voltage of 50Hz. This implies that the source impedance and the distortion factor of the supply are considered to be zero. The source frequency is assumed to be constant. All simulations are conducted with $V_s = 230V$ (rms) i.e. 325.26V (peak). The static loads are assumed to have the following parameters: Resistive load, $R = 100 \Omega$. The simulation of space vector modulated three-phase matrix converter is done for fundamental supply frequency ($f_s = 50$ Hz and $f_0 = 50\text{Hz}$).The space vector modulation for inverter, rectifier and matrix converter is done seperately for a resistive load.

5.1 Three-Phase Space Vector Modulated Inverter with R Load

The simulation control circuit for generating the gate signals is shown in Fig. 5.1 and the power circuit for variable voltage and variable frequency output at fundamental frequency of a space vector modulated inverter is shown in Fig.5.2. The generated gate signals for triggering the six switches in an inverter circuit is shown in the Fig.5.3 The ouput line and phase voltages of the space vector modulated inverter is shown in the Fig. 5.4. The FFT analysis for the three-phase inverter is shown in Fig. 5.5.

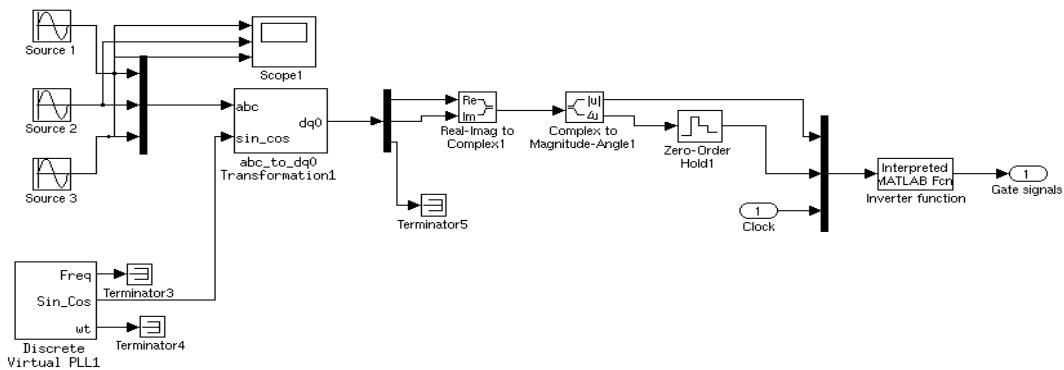


Fig 5.1 Simulation Control circuit for generation of gate signals in a three-phase inverter.

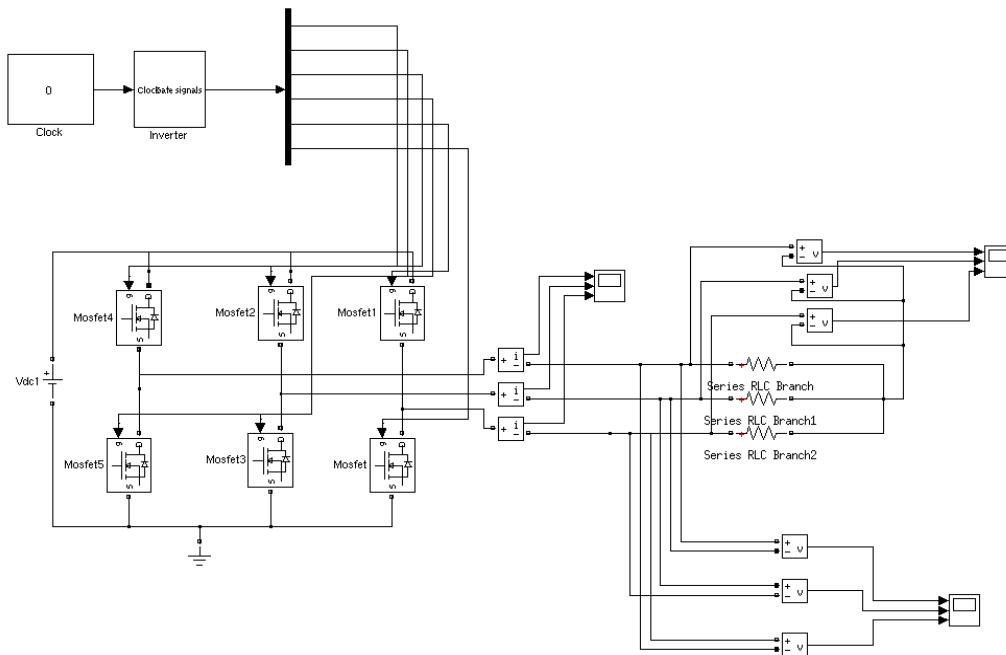


Fig 5.2 Simulation power circuit for space vector modulated three-phase inverter a load $R=100 \Omega$ and $L= 40 \text{ mH}$

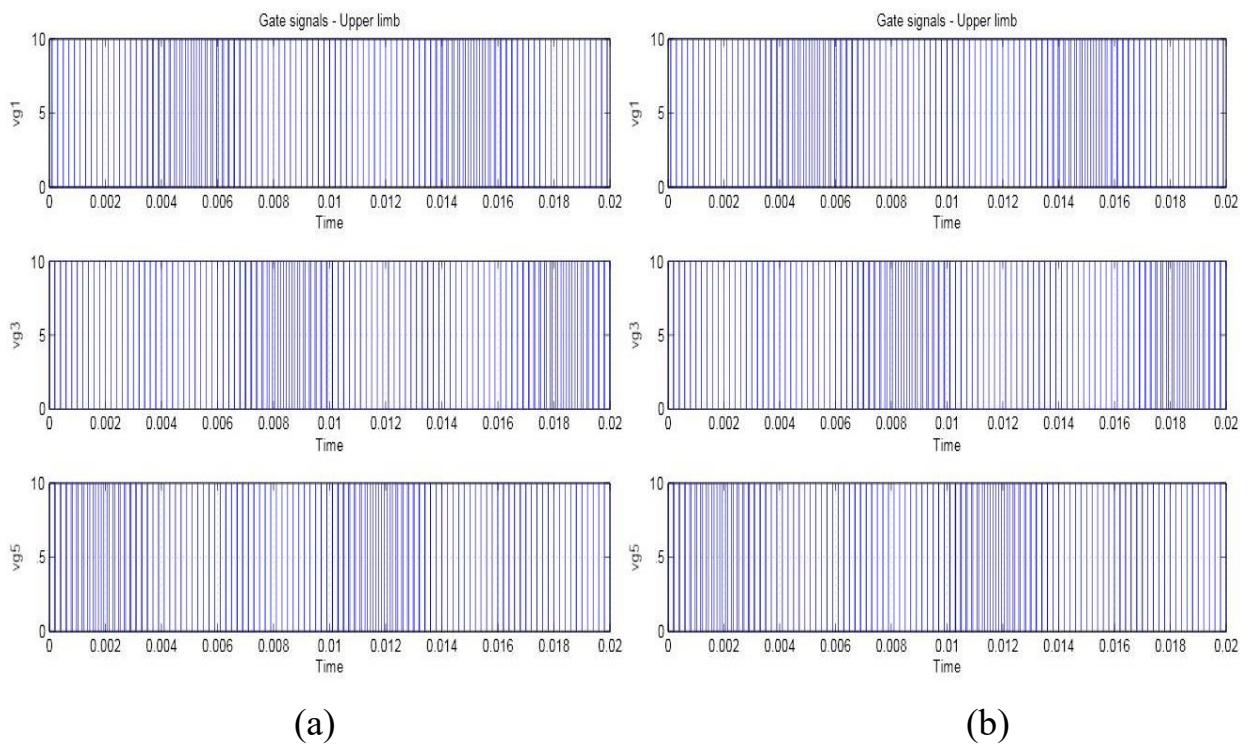
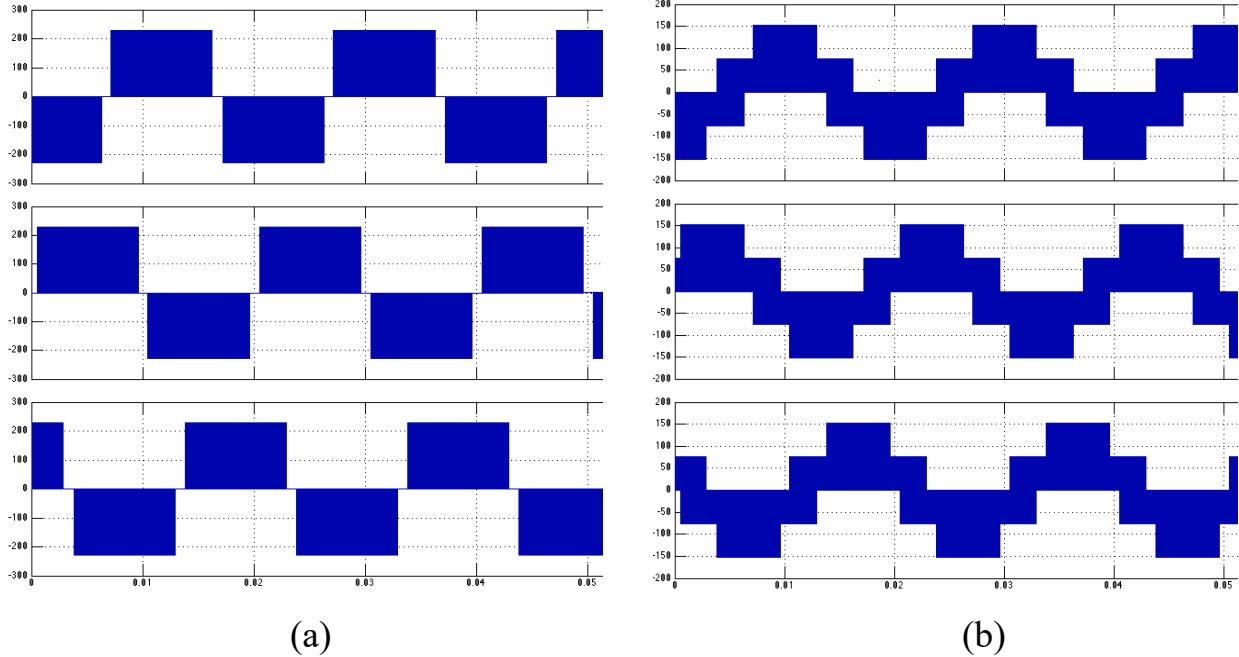


Fig. 5.3 Gate signals for triggering the (a) upper limb and (b) lower limb switches in the inverter circuit.



(a)

(b)

Fig. 5.4 Output (a) Line Voltages and (b) phase voltages for a three-phase space vector modulated inverter.

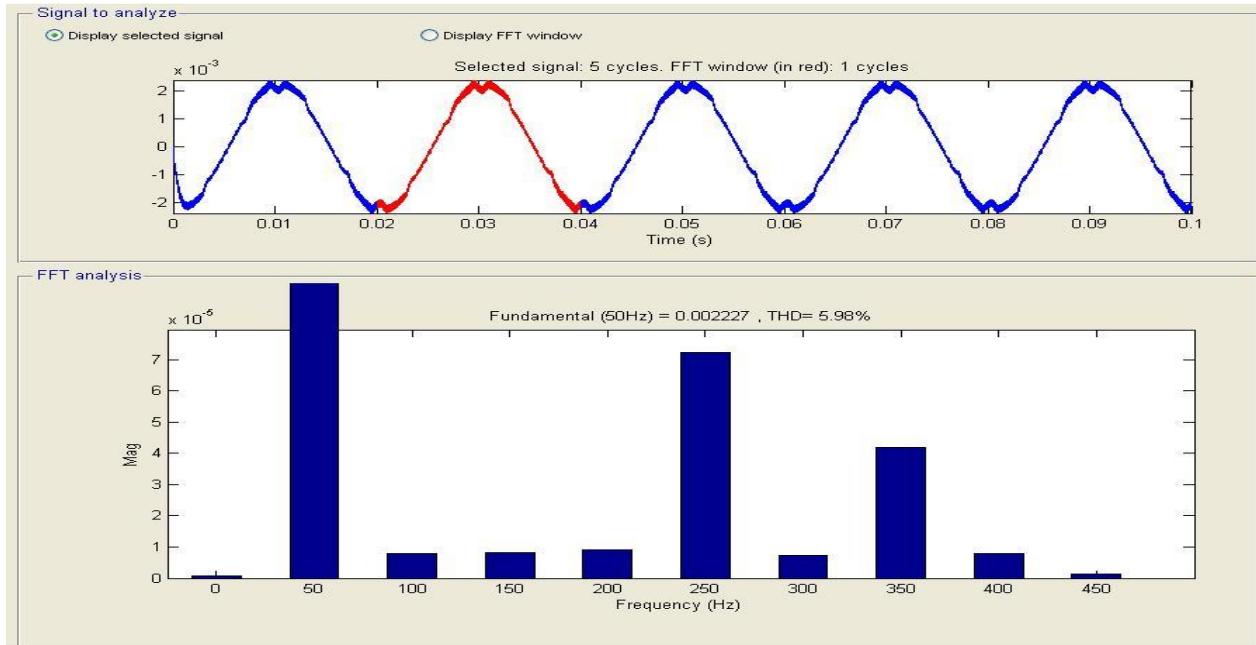


Fig. 5.5 FFT analysis for three-phase inverter showing a THD of 5.98%

5.2 Three-Phase Space Vector Modulated Rectifier with R Load

The simulation control circuit for generating the gate signals is

shown in Fig. 5.6 and the power circuit for variable voltage and variable frequency output at fundamental frequency of a space vector modulated inverter is shown in Fig. 5.7. The generated gate signals for triggering the six switches in an inverter circuit is shown in the Fig.5.8. The ouput dc voltages and currents of the space vector modulated inverter is shown in the Fig. 5.9.

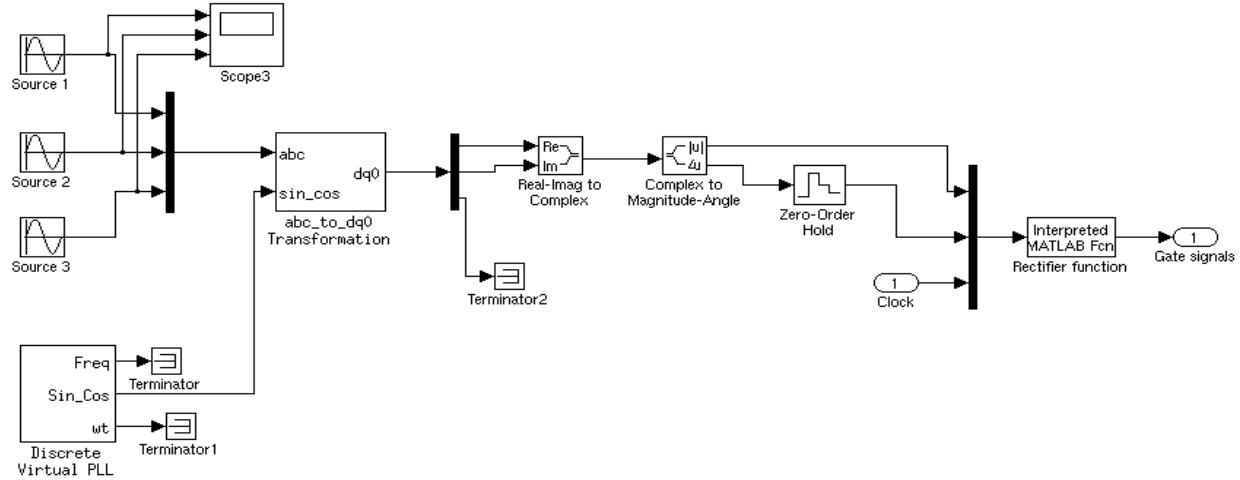


Fig. 5.6 Simulation Control circuit for generation of gate signals in a three-phase rectifier.

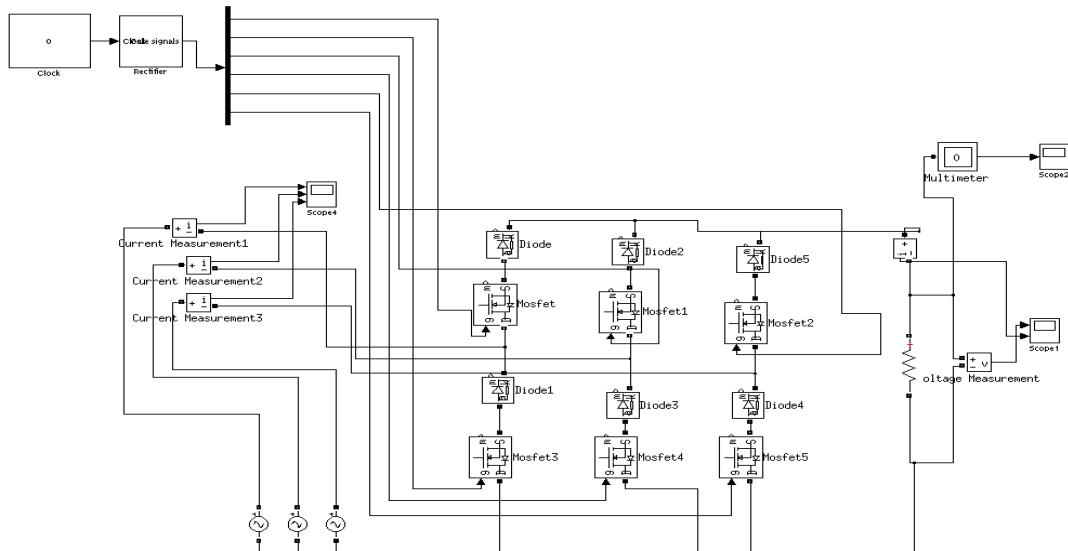


Fig. 5.7 Simulation power circuit for space vector modulated three-phase rectifier a load $R=100 \Omega$

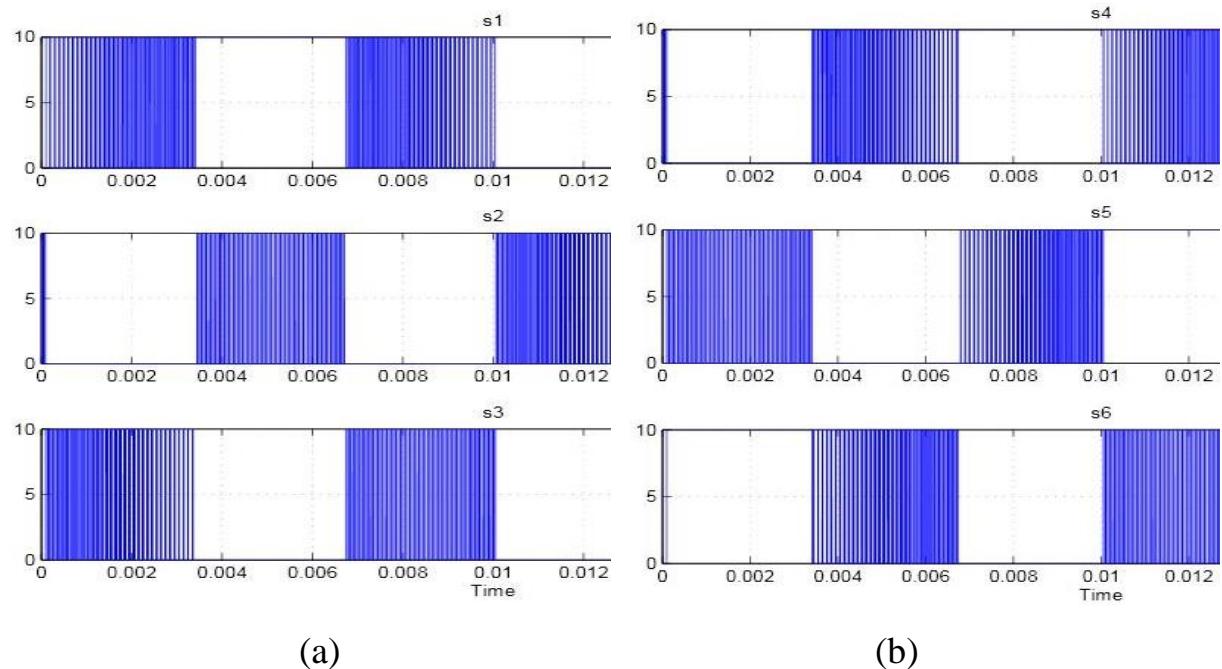


Fig. 5.8 Gate signals for triggering the (a) upper limb and (b) lower limb switches in the rectifier circuit.

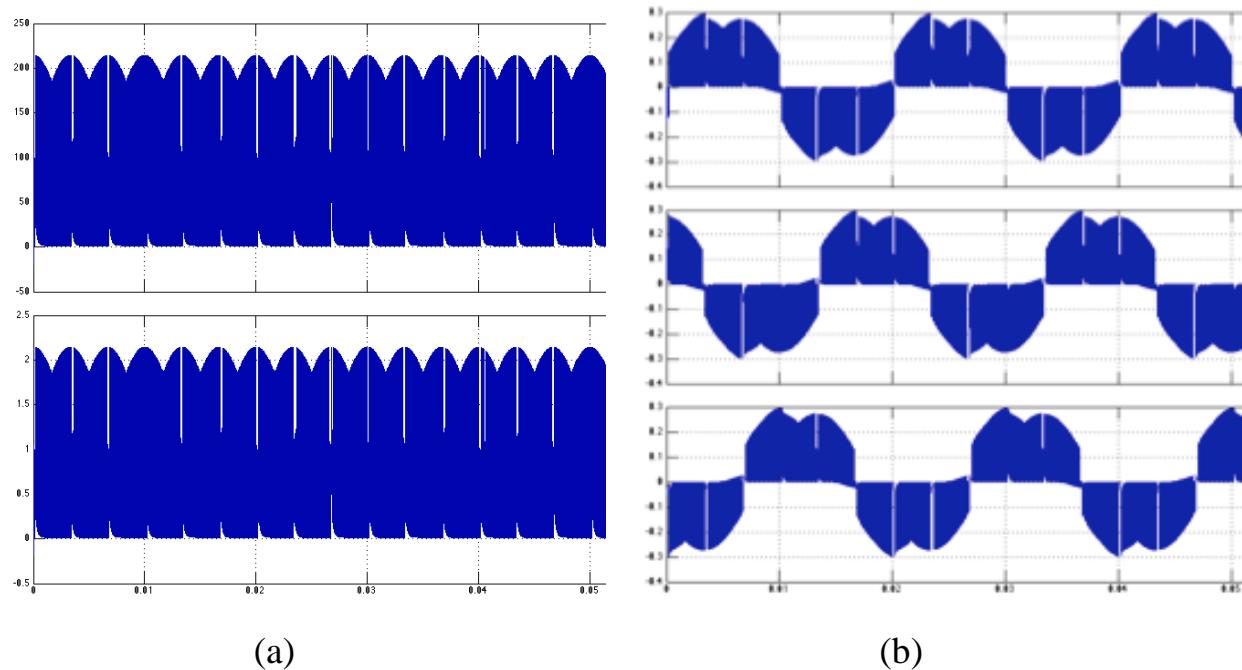


Fig. 5.9 (a) output dc voltage and current (b) Modulated input currents of a three-phase space vector modulated rectifier

5.3 Three-Phase Space Vector Modulated Matrix Converter with R Load

The matrix converter topology consists of nine bi-directional switches which are driven by indirect space vector modulation. The indirect method involves the matrix multiplication of the six gate signals generated by space vector modulated inverter and the six gate signals generated from the space vector modulated rectifier. The simulation power circuit for variable voltage and variable frequency output at fundamental frequency of a space vector modulated inverter is shown in Fig. 5.10 to Fig 5.12. The nine gate signals for the three-phase matrix converter is shown in Fig. 5.13. The ouput line voltage and current of the three-phase space vector modulated matrix converter is shown in Fig. 5.14. The phase current is shown in Fig 5.15. The three-phase output voltages and currents are shown in fig. 5.16. The FFT Analysis for three-phase matrix converter with input filters of $L = 40 \text{ mH}$ and $C = 100 \mu\text{F}$ is shown in fig 5.17

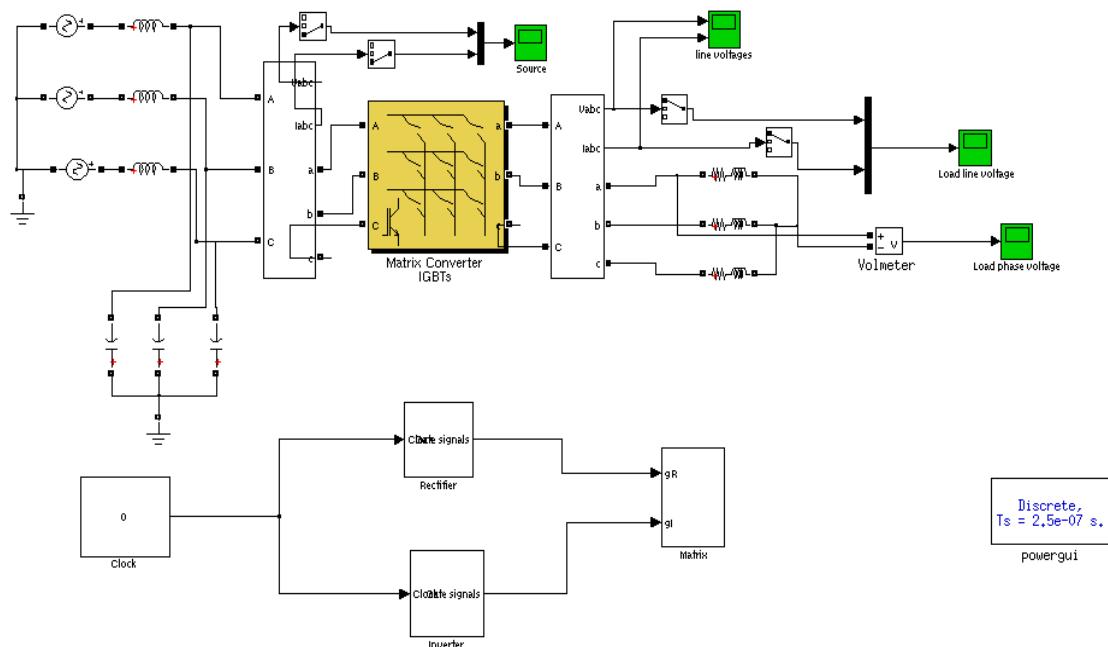


Fig 5.10 Three-Phase space vector modulated matrix converter with $R=100 \Omega$ and

$$L = 40 \text{ mH}$$

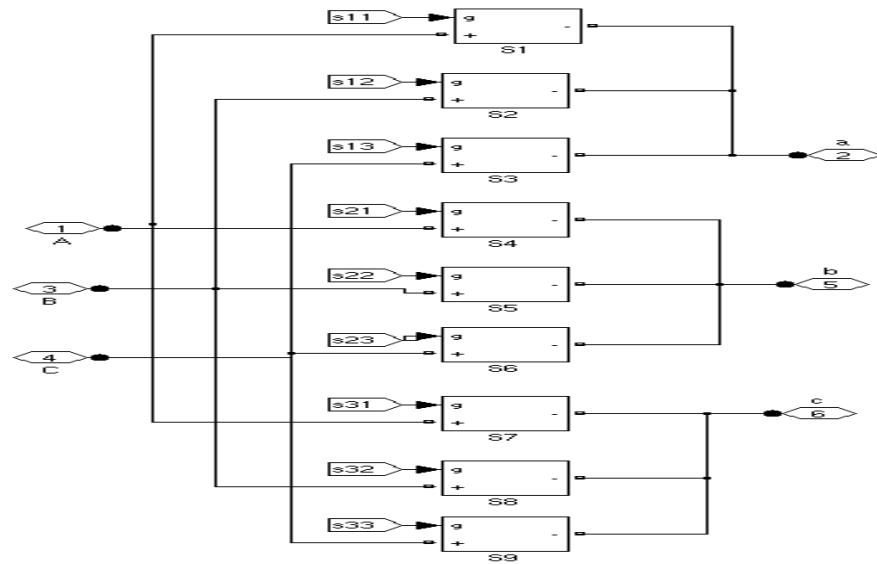


Fig. 5.11 Three-Phase Matrix Converter module

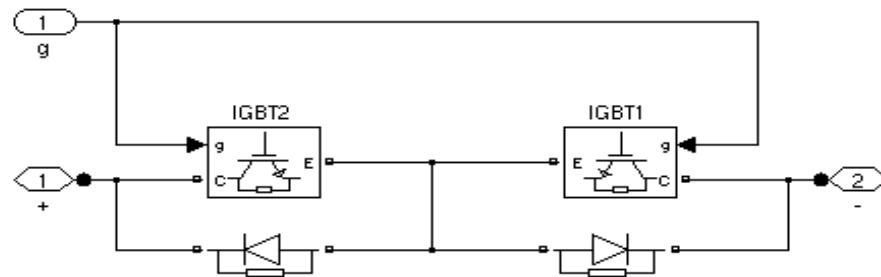
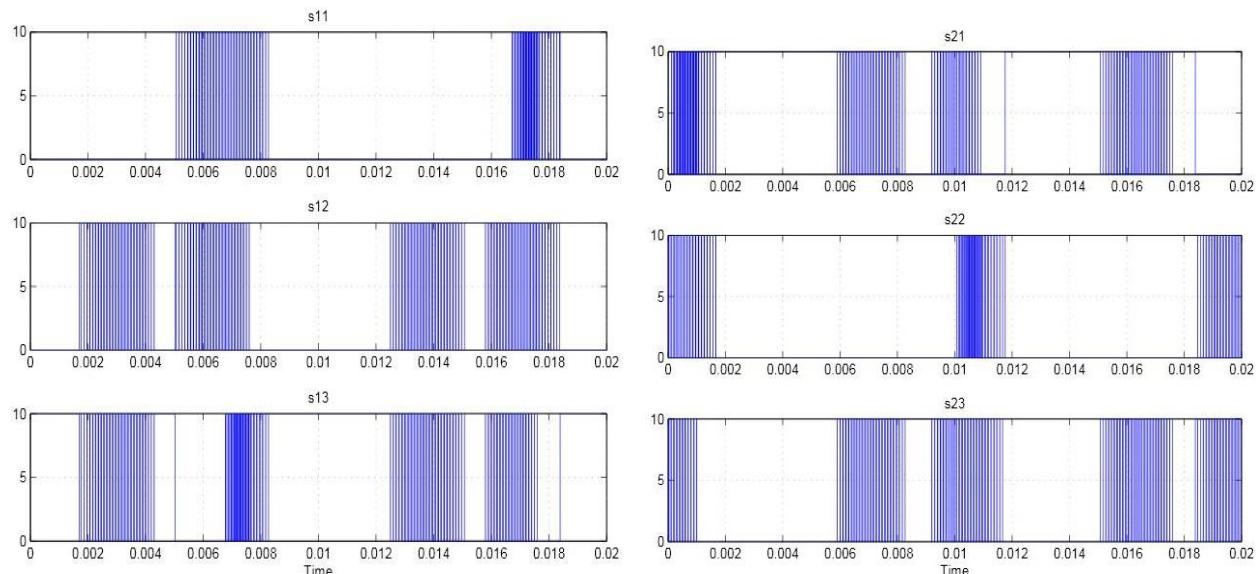
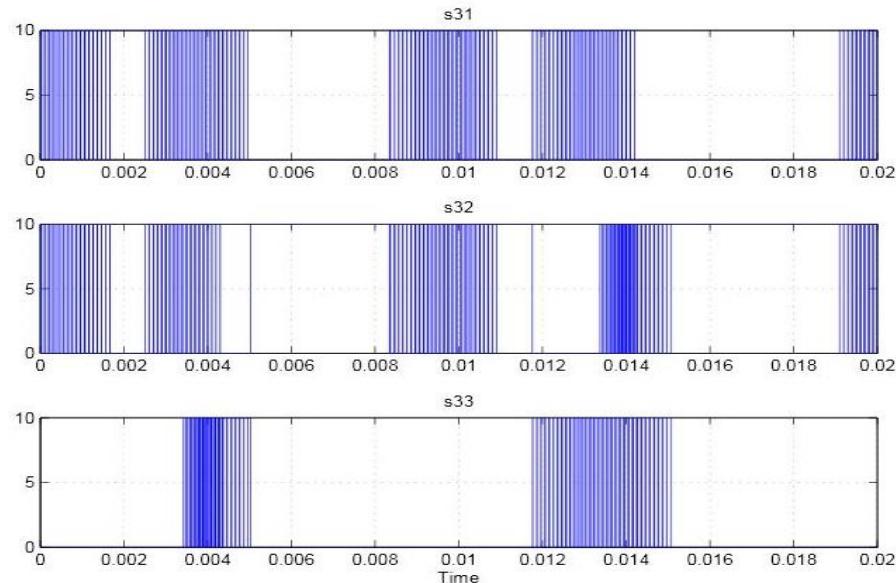


Fig 5.12 Bi-directional switch in the matrix converter module s1



(a) first row

(b) second row



(c) third row

Fig. 5.13 Gate signal for the switches in the matrix converter topology.

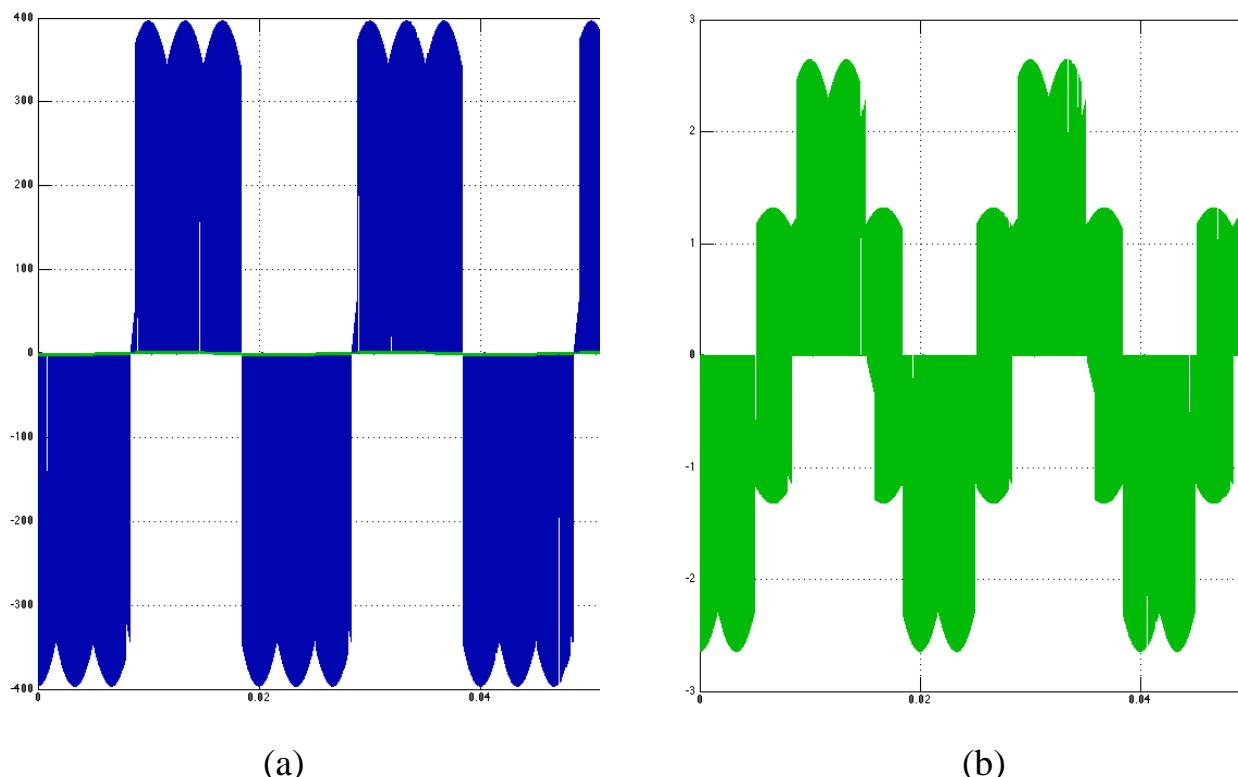


Fig. 5.14 (a) Output line voltage and (b) output current for three phase Matrix converter

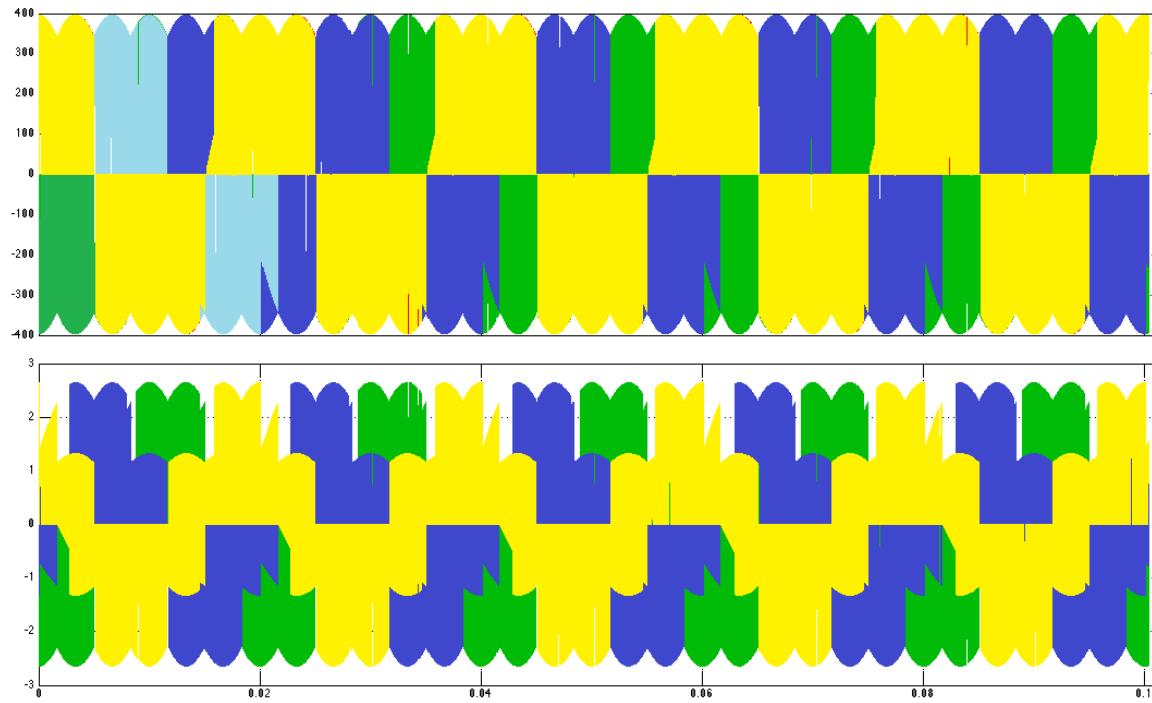


Fig. 5.15 Output line voltages currents for the three-phase matrix Converter

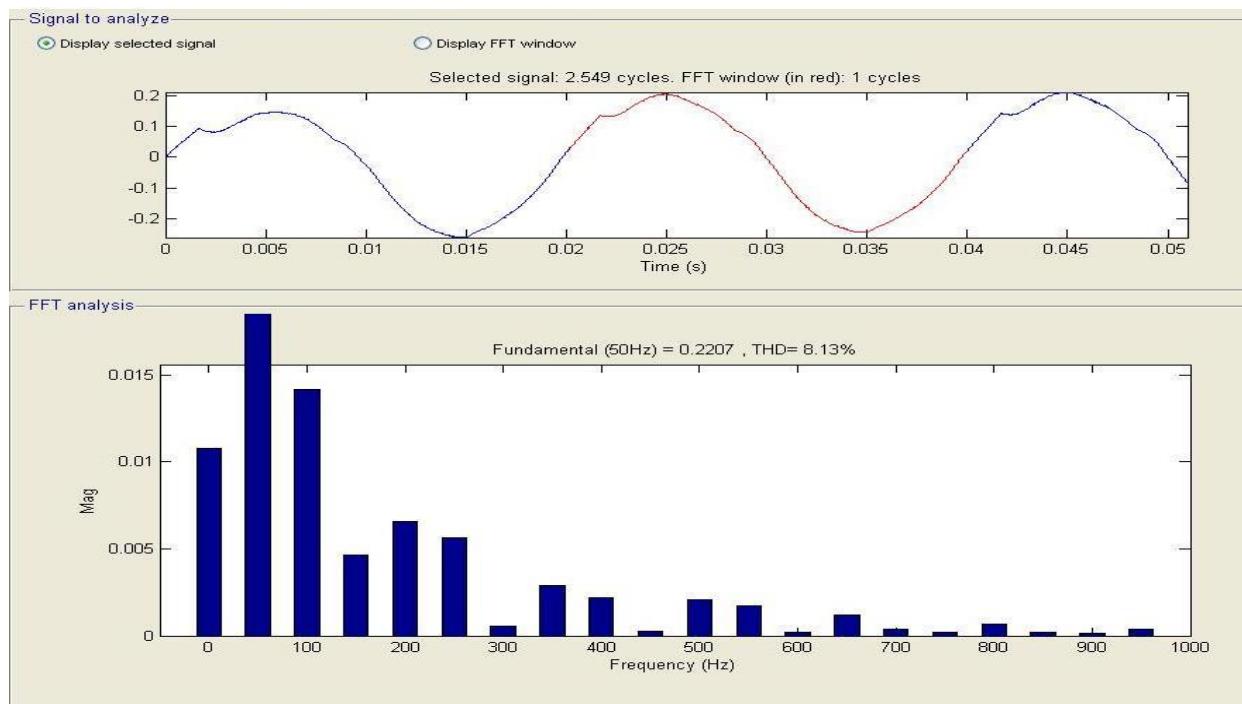


Fig. 5.16 FFT Analysis for three-phase matrix converter

5.4 Hardware Results

5.4.1 Control Circuit

The control circuit hardware is shown in Fig. 5.17 and the practical gate signals for the inverter circuit is shown in Fig 5.18 to Fig. 5.20. The practical gate signals for the rectifier circuit is shown in Fig 5.21 to Fig. 5.23.

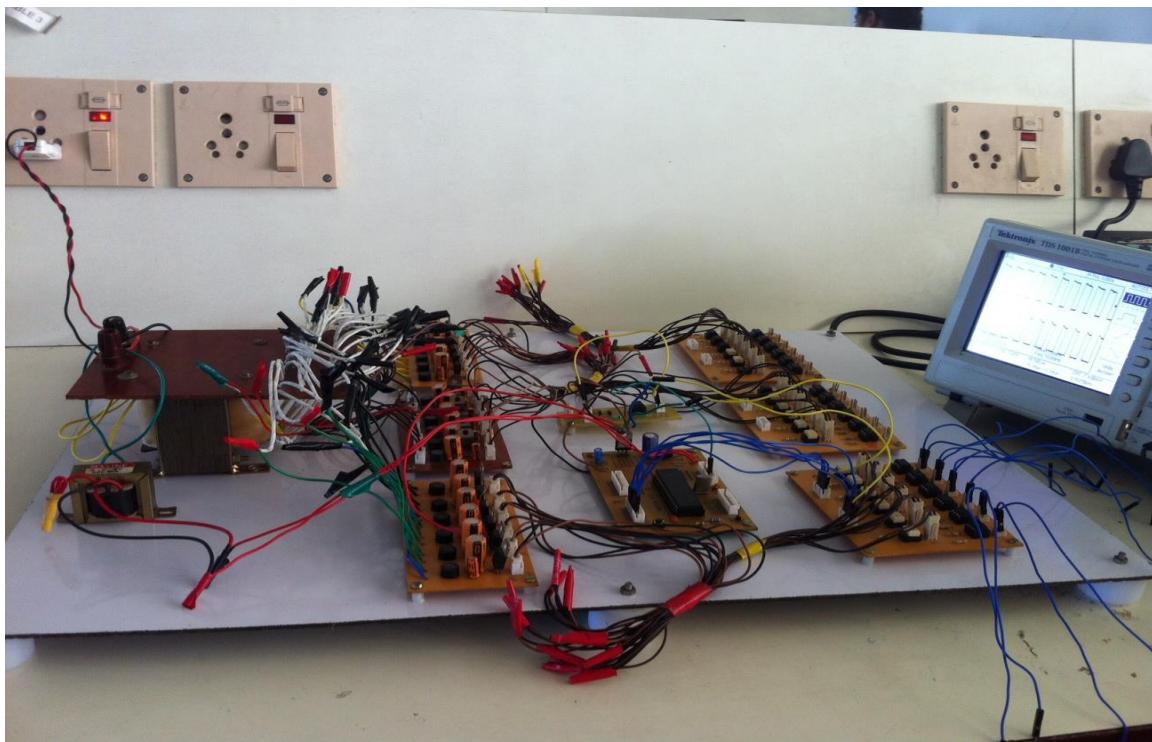


Fig.5.17 Control circuit hardware

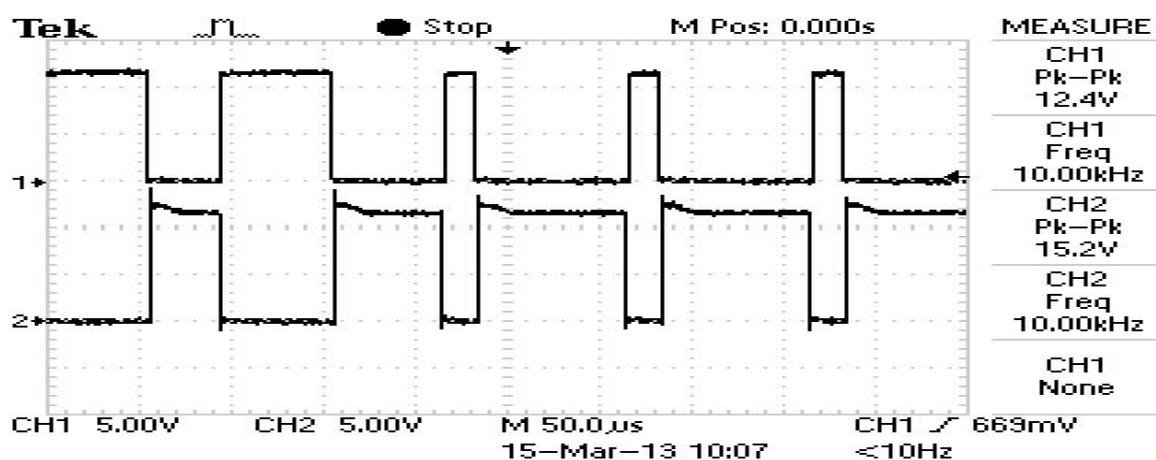
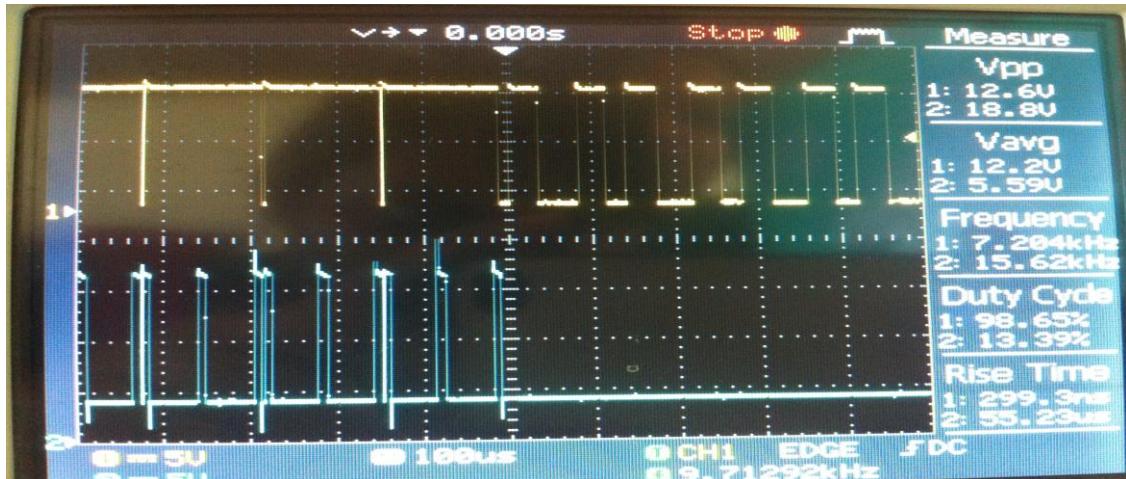
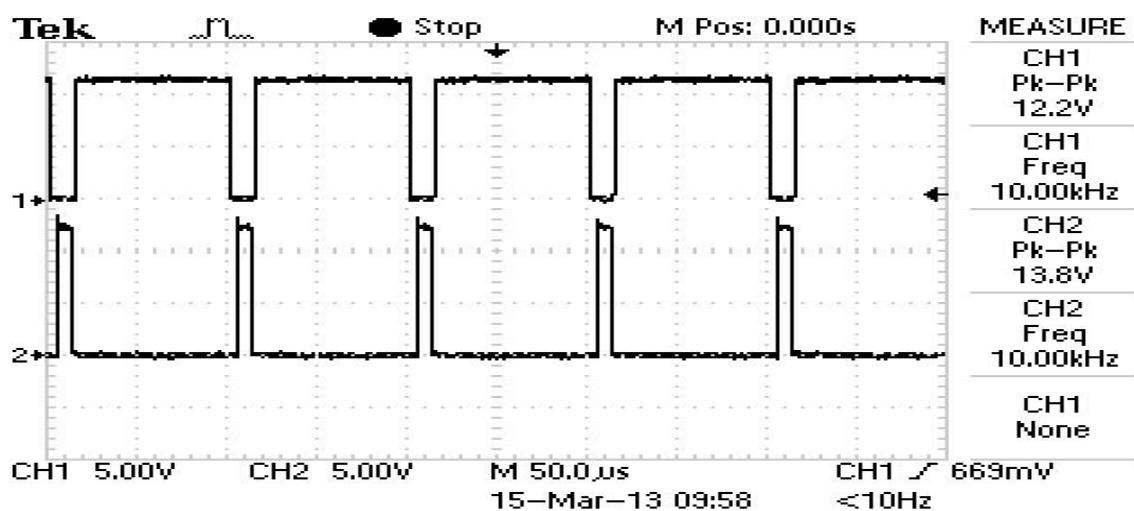
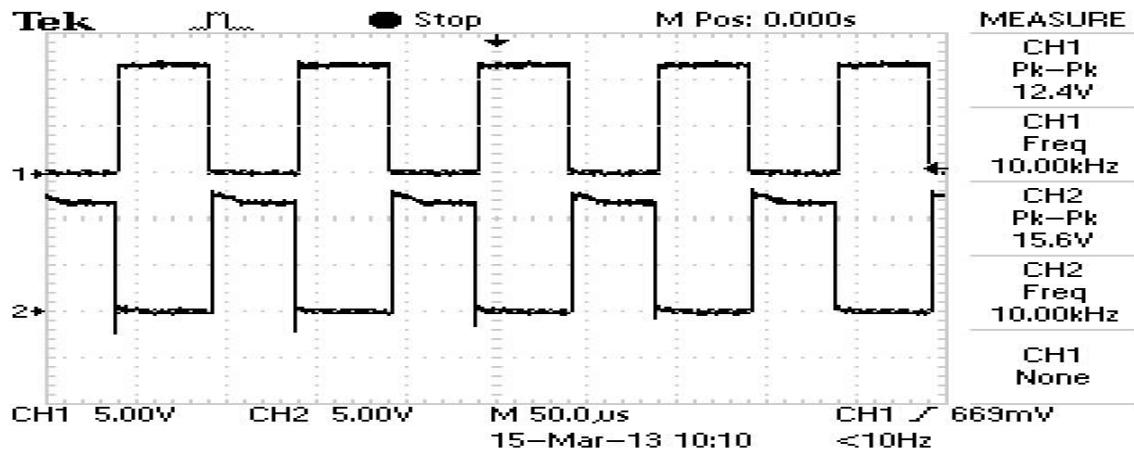


Fig. 5.18 Gate signals for the first limb switches in inverter power circuit



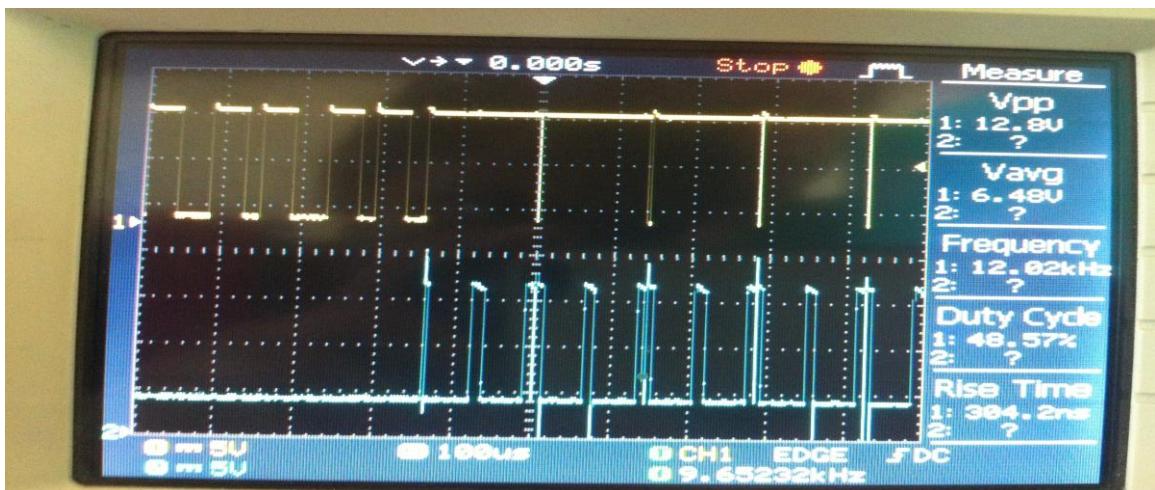


Fig. 5.22 Gate signals for s3 and s4 of the three-phase rectifier

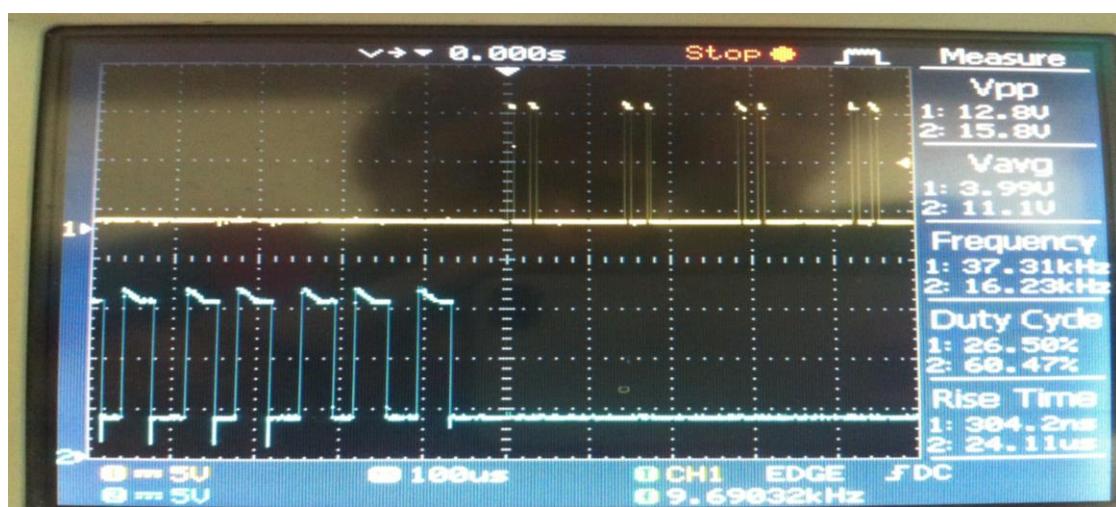


Fig. 5.23 Gate signals for s5 and s6 of the three-phase rectifier

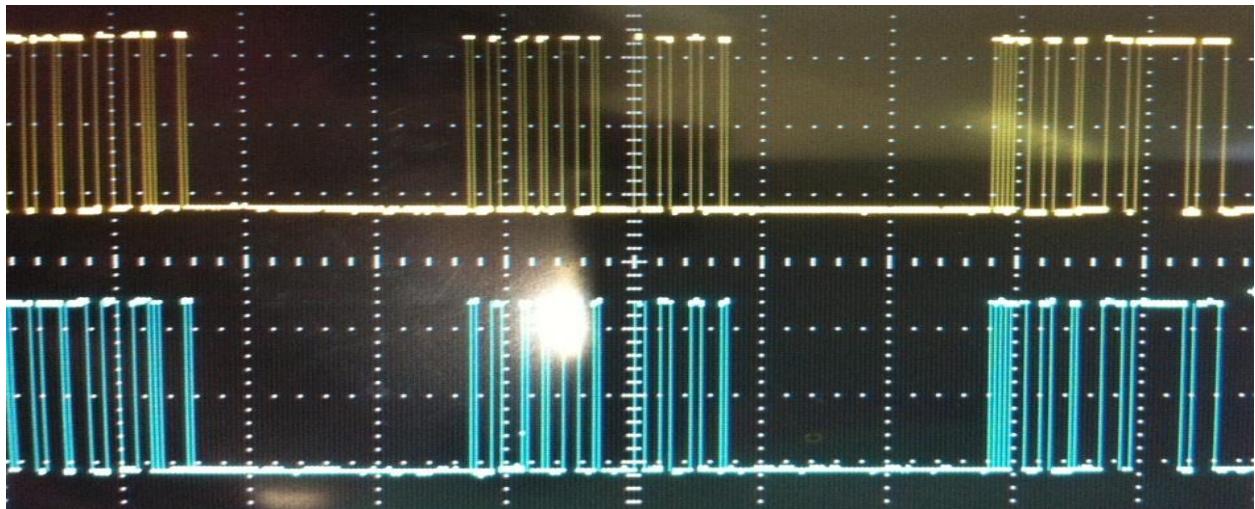


Fig. 5.24 Gate Signal for matrix converter switch s11

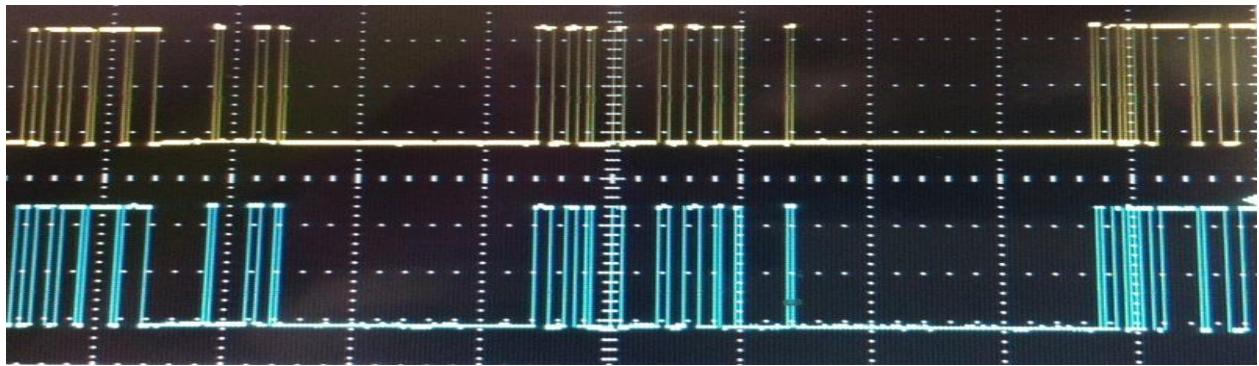


Fig. 5.25 Gate Signal for matrix converter switch s12

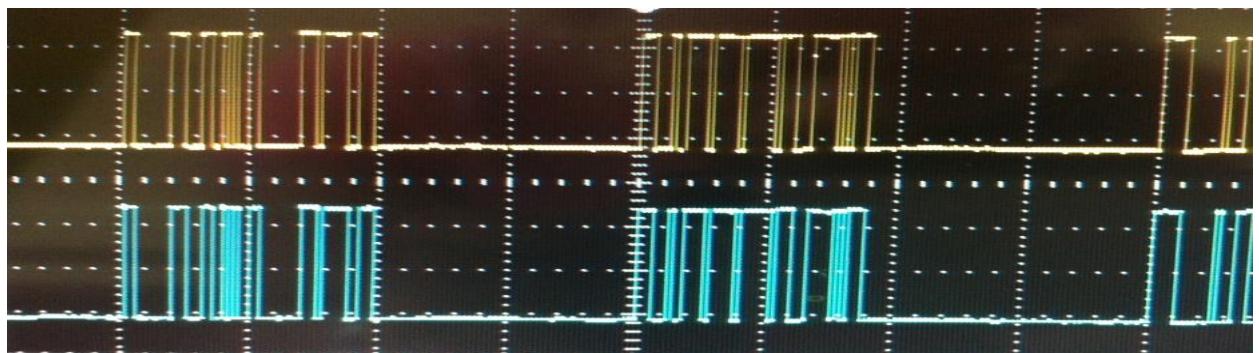


Fig. 5.26 Gate Signal for matrix converter switch s13

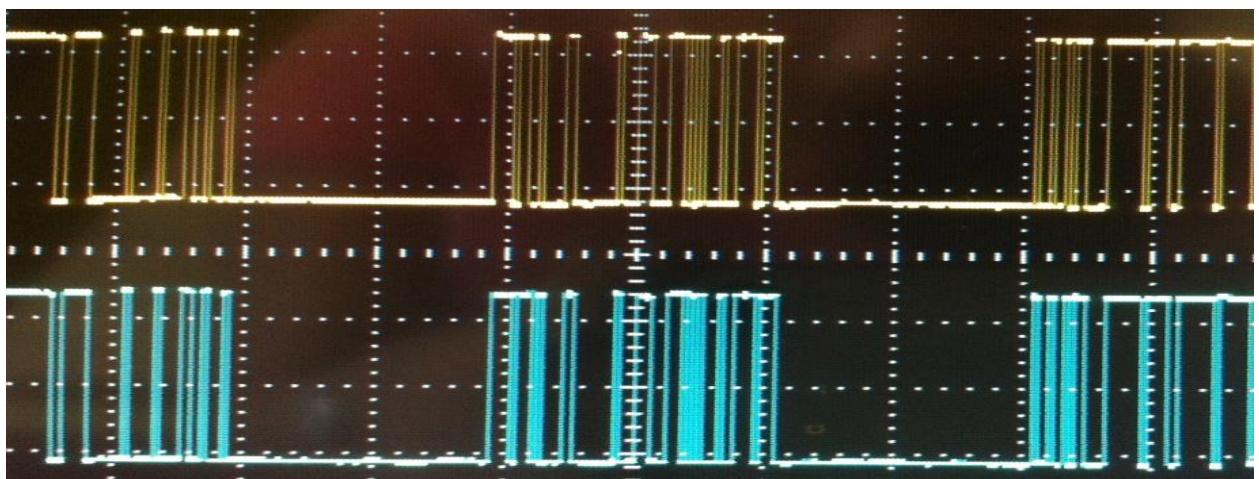


Fig. 5.27 Gate Signal for matrix converter switch s21

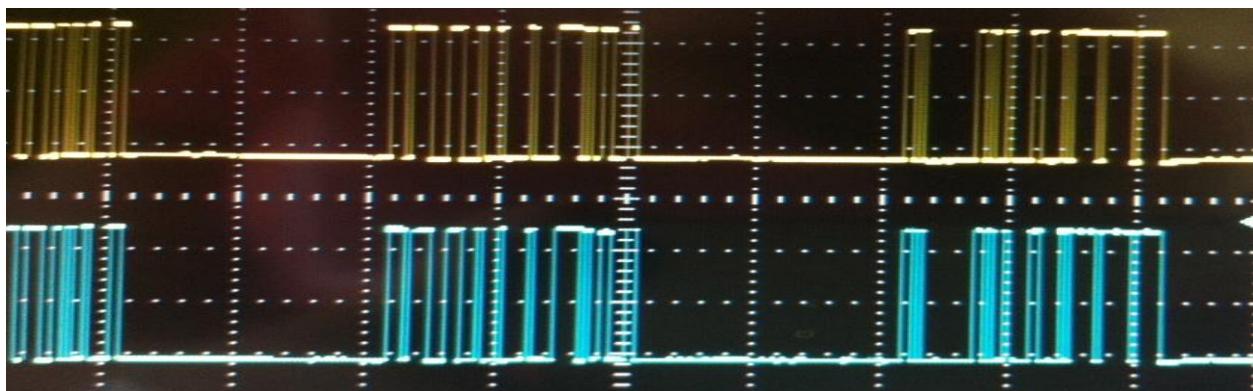


Fig. 5.28 Gate Signal for matrix converter switch s22

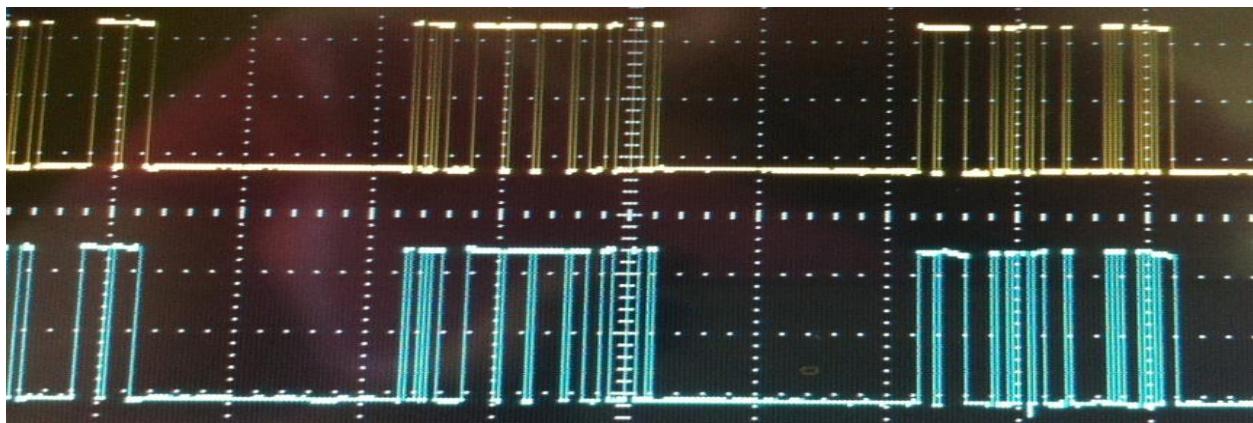


Fig. 5.29 Gate Signal for matrix converter switch s23

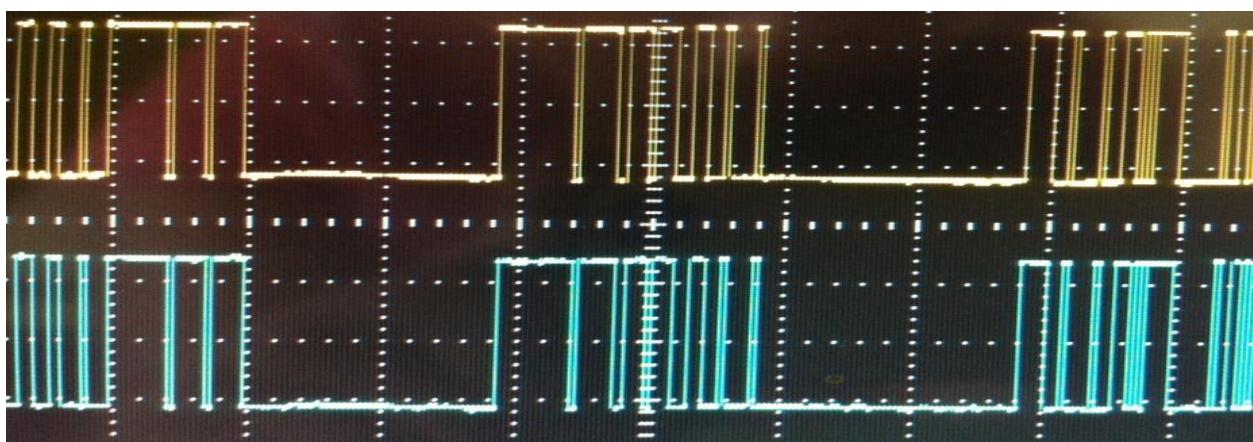


Fig. 5.30 Gate Signal for matrix converter switch s31

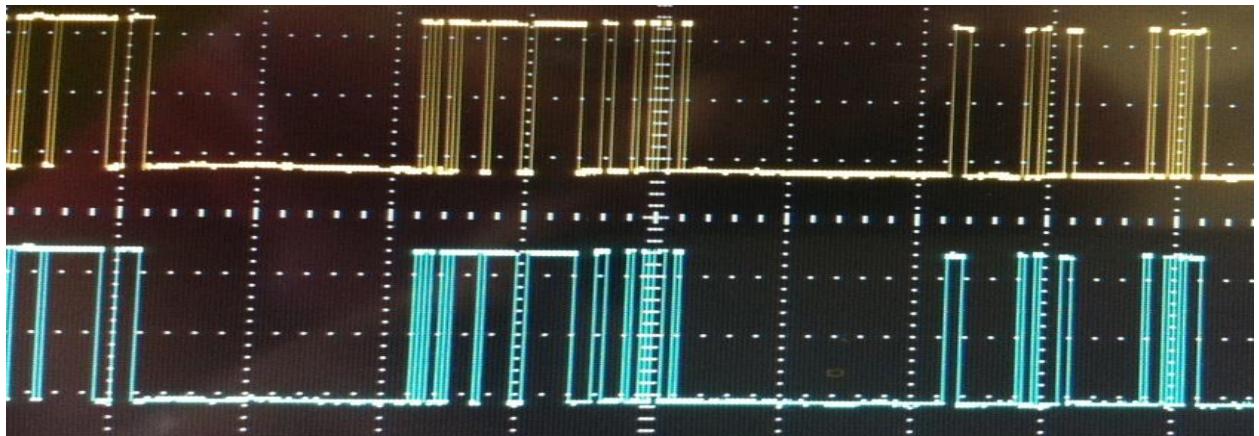


Fig. 5.31 Gate Signal for matrix converter switch s32

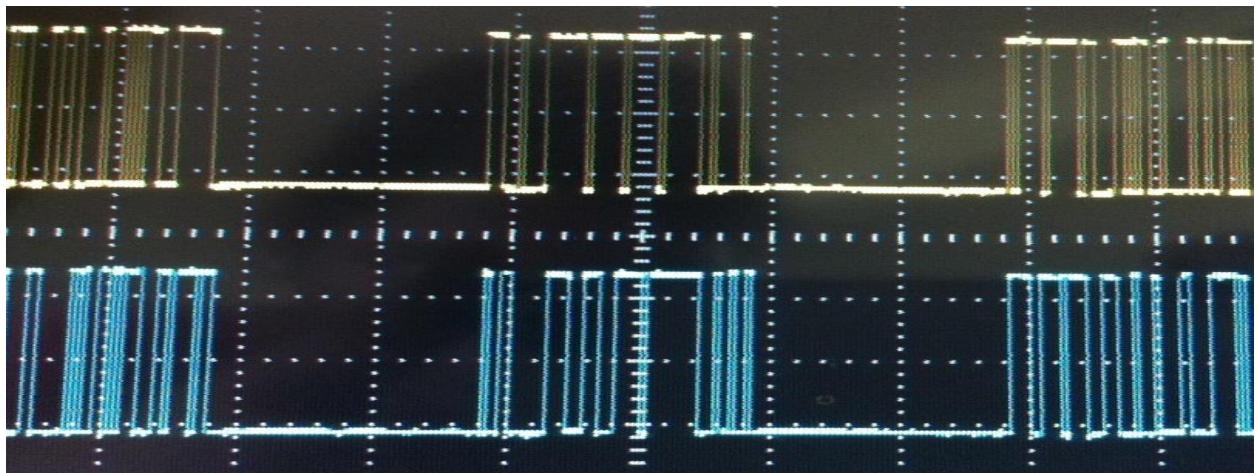


Fig. 5.32 Gate Signal for matrix converter switch s33

5.4.2 Power circuit hardware

The power circuit includes the bi-directional power switches. The power circuit hardware setup for inverter topology is shown in Fig. 5.24 and Fig. 5.25. The corresponding output phase and line voltages of the three-phase inverter are shown in fig 5.26 and Fig. 5.27. The power circuit hardware setup for rectifier topology is shown in Fig. 5.28 and Fig. 5.29. The corresponding output dc voltage for three-phase rectifier is shown in Fig. 5.30. The bi-directional power switches for three-phase matrix converter is shown in fig. 5.31.



Fig. 5.33 Experimental setup for three-phase inverter topology

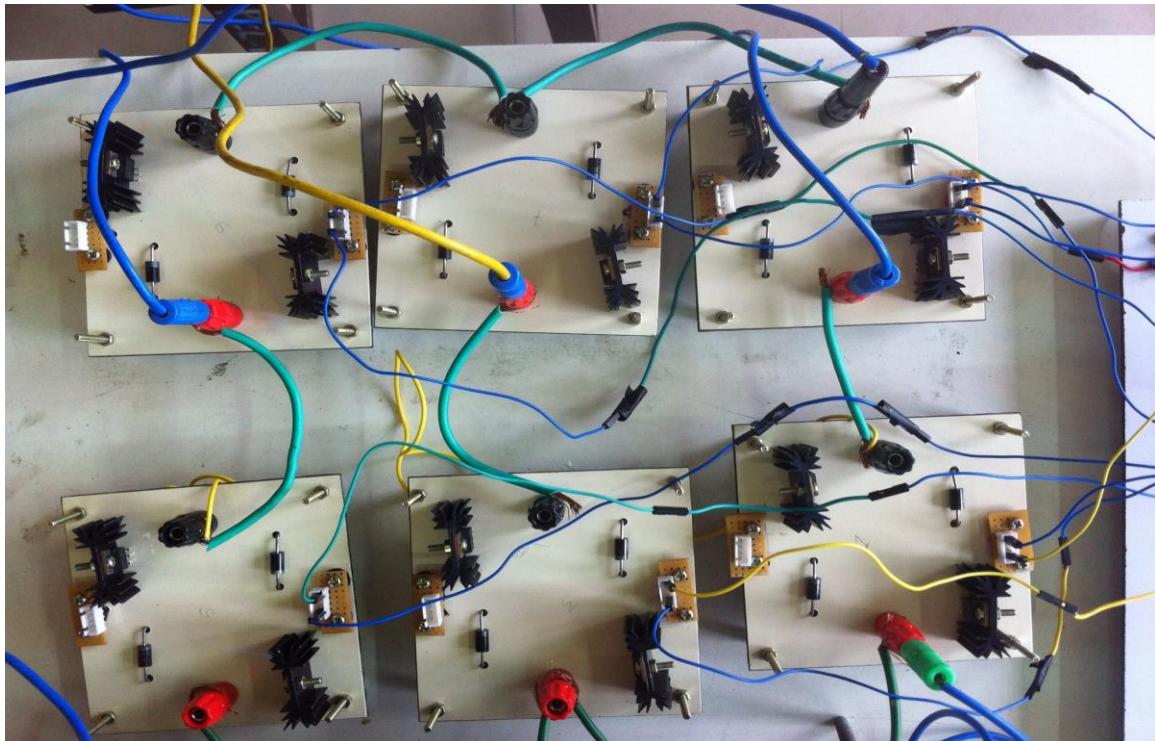


Fig. 5.34 Bi-directional power switches for inverter topology



Fig. 5.35 Output phase voltage for three-phase inverter

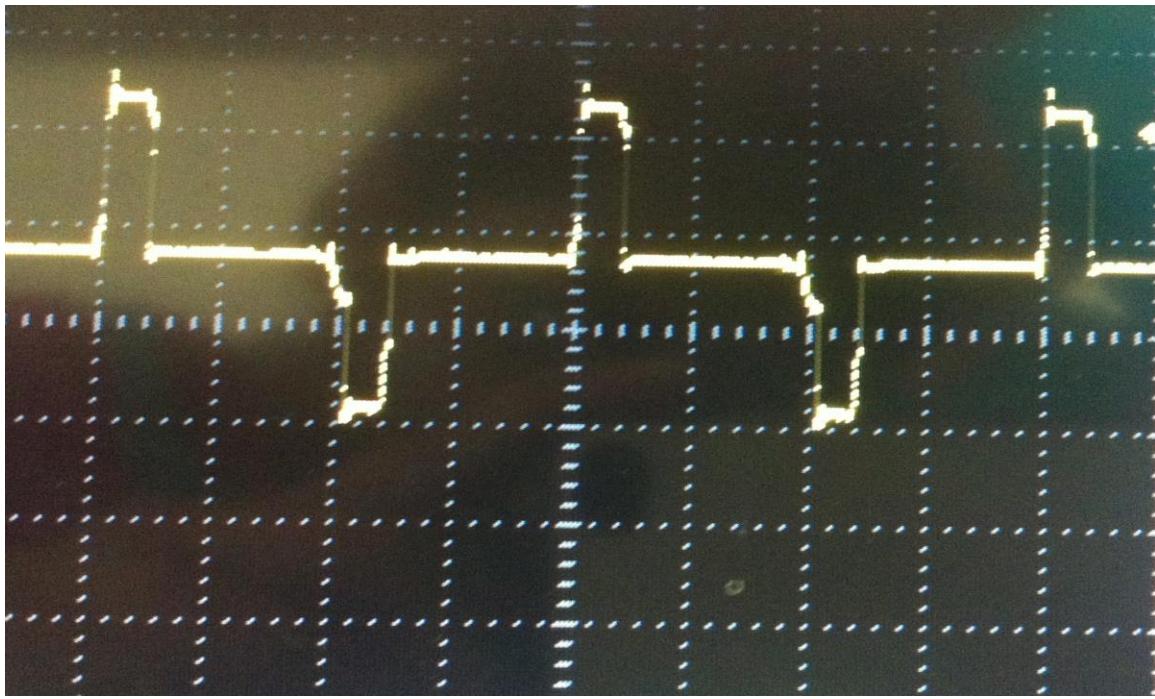


Fig. 5.36 Output line voltage for three-phase inverter

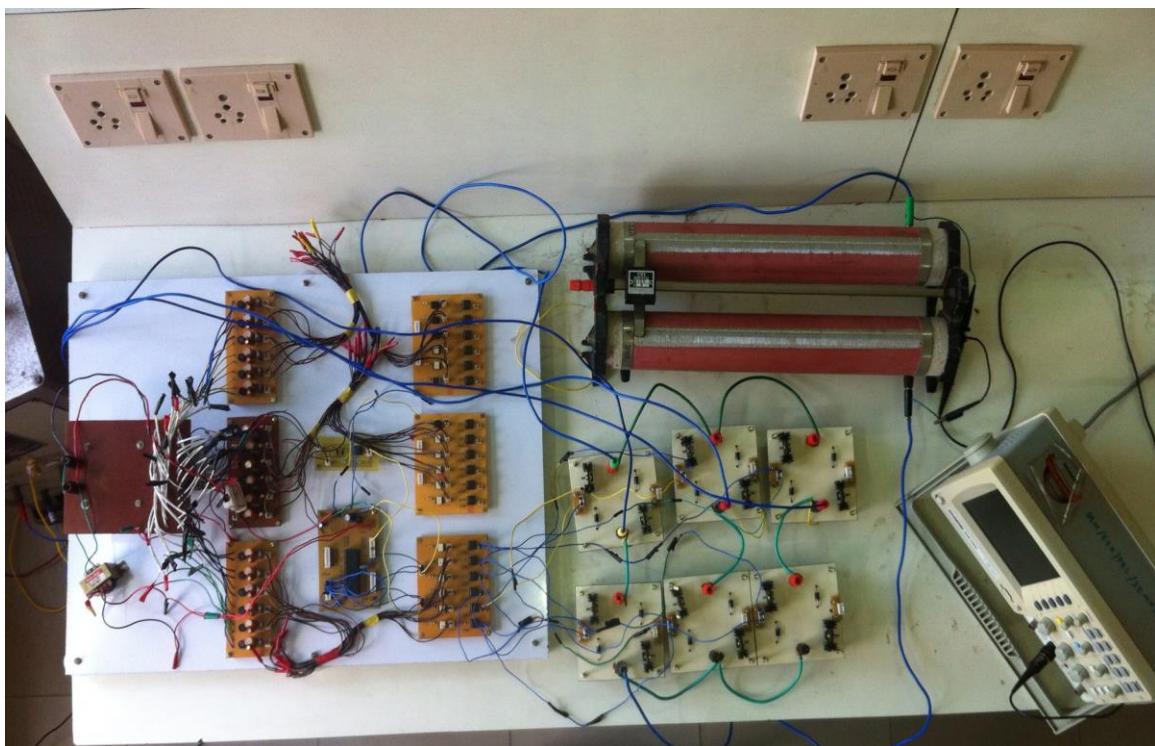


Fig.5.37 Experimental setup for three-phase rectifier

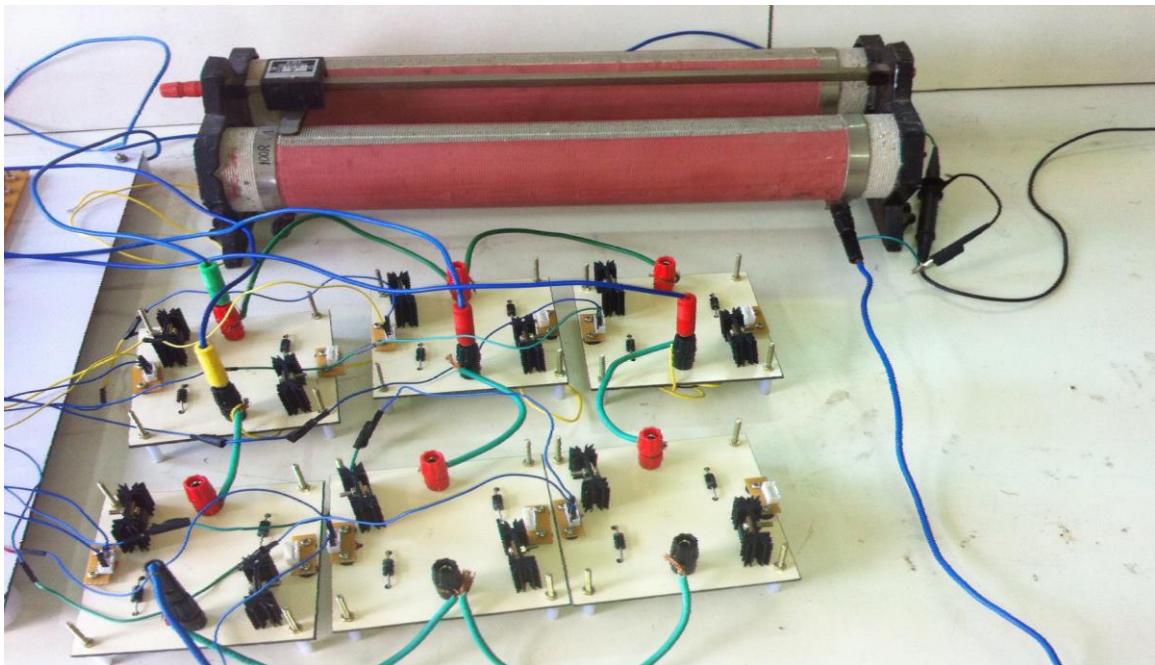


Fig. 5.38 Bi-directional power switches for three-phase rectifier

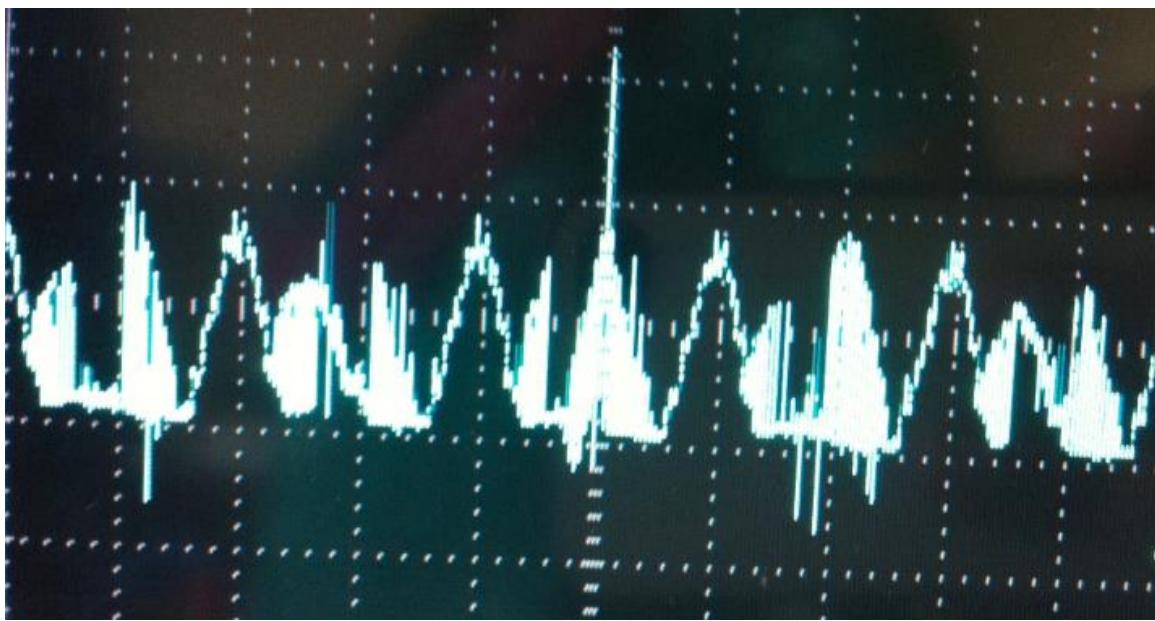


Fig. 5.39 Output dc voltage of three-phase rectifier in comparison with input voltage

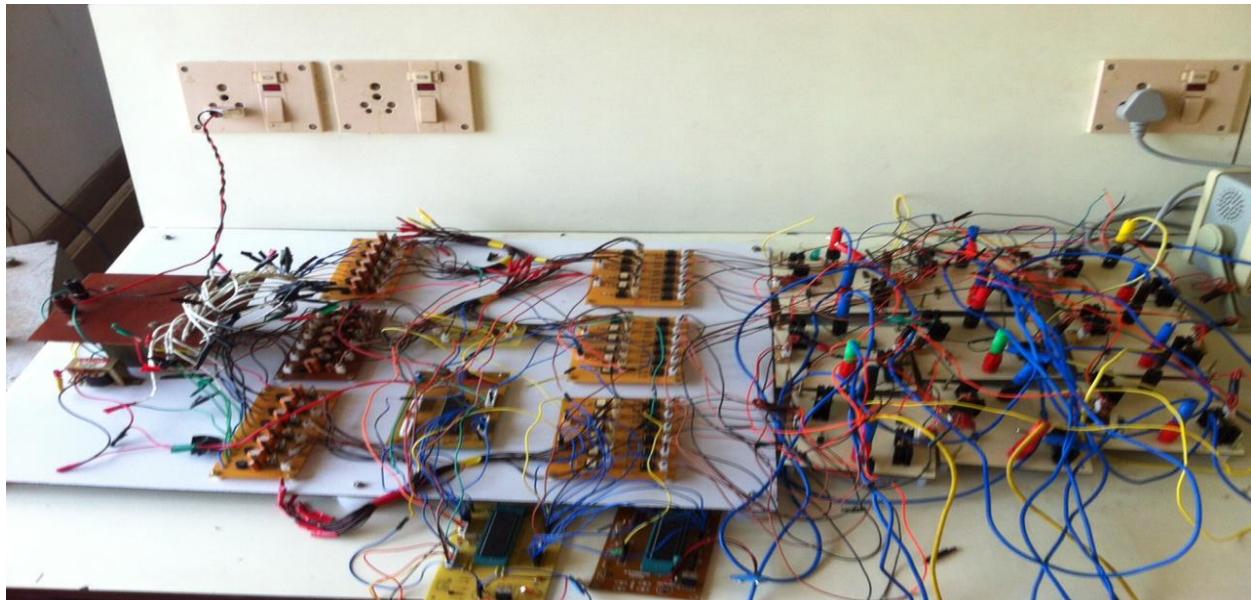


Fig. 5.40 Experimental setup for matrix converter

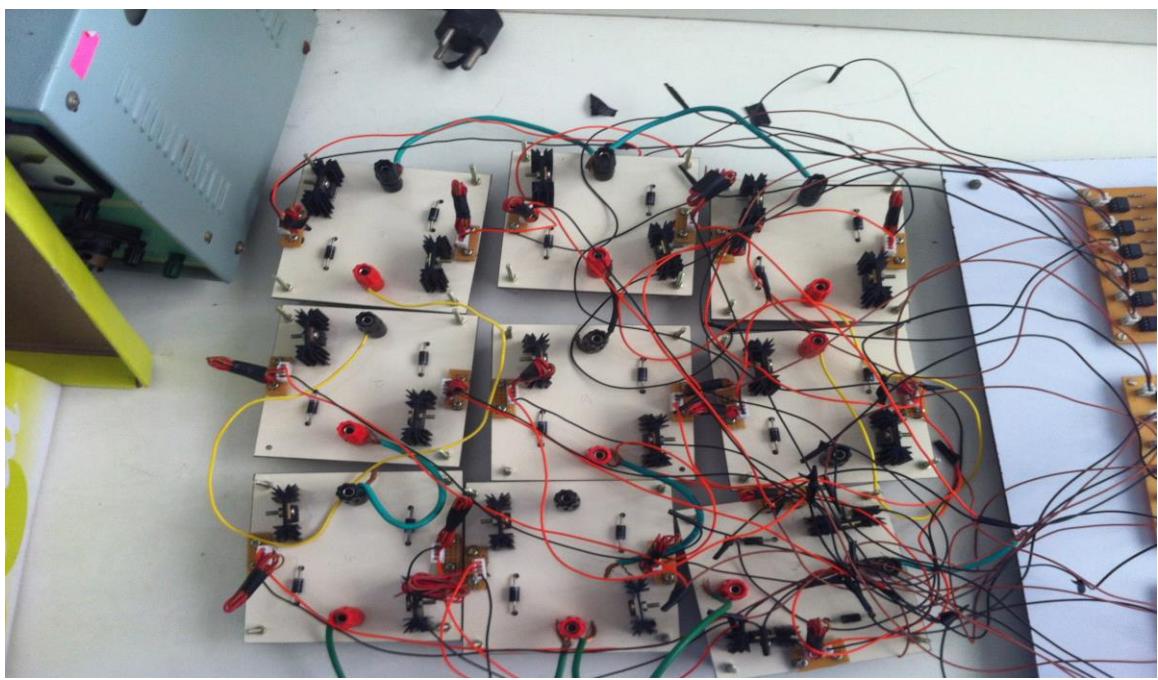


Fig. 5.41 Bi-directional power switches for three-phase matrix converter topology



Fig. 5.42 Output Phase Voltage for Matrix Converter

CHAPTER 6

CONCLUSION

1. A matrix converter with IGBT and power diode, enabling four quadrant operation, is developed and fabricated.
2. A simulation based analysis of Space Vector Modulated Rectifier, Space Vector Modulated Inverter and Space Vector Modulated Matrix Converter has been carried out.
3. It is observed that the harmonic profile is improved by increasing the switching frequency.
4. A three-phase rectifier and inverter are experimentally tested individually for R loads.
5. It is observed that the cost of realization is much lesser when compared to systems involving FPGAs and DSPs. Further commutation circuits are not required when IGBTs are used.

6.1. Scope for future work:

1. The converter may be tested for dynamic loads such as induction motor loads.
2. The control strategy may be improved to provide for input frequency and voltage changes while maintaining output voltage and frequency constant. Such a topology may be tested in a live wind energy conversion system.

APPENDIX – 1

PIC MICROCONTROLLER PROGRAM

1.1 Program for Inverter:

```

dutycycle2L[200]={ 68,92,116,140,164,188,216,240,12,36,64,88,116,144,168,196,
224,252,24,48,76,104,128,156,184,208,236,4,32,56,80,104,128,152,144,120,96,72
88,64,40,12,244,216,192,164,140,112,84,60,32,4,232,204,180,152,124,100,72,44,
20,248,224,196,172,148,124,100,76,84,108,132,156,180,204,232,0,28,52,80,108,1
32,160,188,216,244,12,40,68,96,120,148,176,200,228,252,24,48,72,96,120,144,15
2,128,104,80,56,32,4,236,208,184,156,128,104,76,48,24,252,224,196,168,144,116
,88,64,36,12,240,216,188,164,140,116,92},  

#pragma romdata  

void main(void)  

{  

    //OSCCON=0x77;//Fosc=8MHz  

    INTCONbits.GIE=1;  

    INTCONbits.PEIE=1;  

    INTCONbits.INT0IE=1;  

    INTCON2bits.INTEDG0=1;  

    PIE3bits.PTIE=1;  

    //PDC0H=1;//PDC1H=0;//PDC2H=0;  

    TRISB=0x00;  

    PTPERH=0x00;  

    PTPERL=0xFA;  

    PTCON1=0x00;//reset PTEN in PTCON1 before changing PTMOD in  

PTCON0  

    PTCON0=0b00000010;//continuous up down mode  

    PTCON1=0b11000000;  

    PWMCON0=0b01010000;  

    PWMCON1=0x01;  

    DTCN=0b00010100;

```

```

while(1)
{
if(start==1)
{
INTCONbits.INT0IE=0;//disable ZCD interrupt
PTMRH=PTPERH;
PTMRL=PTPERL;
SVM:
while(i<=33)
{
PWMCON1bits.UDIS=1;
PDC0H=dutycycle1H[i];
PDC0L=dutycycle1L[i];//1
PDC1H=dutycycle2H[i];
PDC1L=dutycycle2L[i];//2
PDC2H=dutycycle3H[i];
PDC2L=dutycycle3L[i];//3
PWMCON1bits.UDIS=0;
}
while(i<=100)
{
PWMCON1bits.UDIS=1;
PDC0H=dutycycle3H[i];
PDC0L=dutycycle3L[i];//3
PDC1H=dutycycle1H[i];
PDC1L=dutycycle1L[i];//1
PDC2H=dutycycle2H[i];
}
}

```

```
PDC2L=dutycycle2L[i];//2
```

```
PWMCON1bits.UDIS=0;
```

```
}
```

```
while(i<=133)
```

```
{
```

```
PWMCON1bits.UDIS=1;
```

```
PDC0H=dutycycle3H[i];
```

```
PDC0L=dutycycle3L[i];//3
```

```
PDC1H=dutycycle2H[i];
```

```
PDC1L=dutycycle2L[i];//2
```

```
PDC2H=dutycycle1H[i];
```

```
PDC2L=dutycycle1L[i];//1
```

```
PWMCON1bits.UDIS=0;
```

```
}
```

```
while(i<=166)
```

```
{
```

```
PWMCON1bits.UDIS=1;
```

```
PDC0H=dutycycle2H[i];
```

```
PDC0L=dutycycle2L[i];//2
```

```
PDC1H=dutycycle3H[i];
```

```
PDC1L=dutycycle3L[i];//3
```

```
PDC2H=dutycycle1H[i];
```

```
PDC2L=dutycycle1L[i];//1
```

```
PWMCON1bits.UDIS=0;
```

```
}
```

```
while(i<200)
```

```
{
```

```

PWMCON1bits.UDIS=1;
PDC0H=dutycycle1H[i];
PDC0L=dutycycle1L[i];//1
PDC1H=dutycycle3H[i];
PDC1L=dutycycle3L[i];//3
PDC2H=dutycycle2H[i];
PDC2L=dutycycle2L[i];//2
PWMCON1bits.UDIS=0;
}
goto SVM;
}
}
}

```

1.2 Program for Rectifier:

```

//RA0--> s1, RA2--> s3, RA4--> s5,
//RA1--> s2, RA3--> s4, RA5--> s6
#include <18F4331.h>
#device adc=8
#FUSES HS           //High speed Osc (> 4mhz)
#use delay(clock=20000000)
#byte porta=0xF80
#byte portb=0xF81
#byte portc=0xF82
#byte portd=0xF83
#byte porte=0xF84
#byte trisa=0xF92

```

```
#byte trisb=0xF93
#byte trisc=0xF94
#byte trisd=0xF95
#byte trise=0xF96
int i;
volatile int start=1;
const int
b[200]={36,35,34,33,32,32,31,30,29,28,27,26,25,24,23,22,20,19,18,17,16,14,13,
18,16,15,14,13,11,10,9,7,6,5,3,2,1,0,0,0,1,2,3,5,6,7,9,10,11,13,14,15,16,18,19,20,2
5,24,23,22,21,20,18,17,16,15,14,12,11,10,8,7,6,4,3,2,0,0,0,0,1,3,4,5,7,8,9,11,12,13
,14,16,17,18,19,20,22,23,24,25,26,27,28,29,30,31,32,32,33,34,35};
const int c[200]
={0,0,3,4,5,7,8,9,11,12,13,15,16,17,18,20,21,22,23,24,25,27,28,29,30,31,32,32,33,
34,35,36,37,37,37,36,36,35,34,33,32,31,30,29,28,27,26,25,24,23,22,20,19,18,17,1
6,14,13,12,10,9,8,6,5,4,0,0,0,0,3,5,6,7,9,10,11,13,14,15,16,18,19,20,21,22,24,25,,2
2,21,20,19,18,16,15,14,13,11,10,9,7,6,5,3,0,0,0,0,4,5,6,8,9,10,12,13,14,16,17,18,1
9,20,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,36,37,37,36,35,34,33,32,32,
31,30,29,28,27,25,24,23,22,21,20,18,17,16,15,13,12,11,9,8,7,5,4,3,0};
const int a[200]
={4,4,4,3,3,3,3,2,2,2,2,2,1,1,1,1,1,1,1,1,2,2,2,2,2,2,3,3,3,4,4,4,4,4,3,3,3,3,2,2,2,
2,2,2,2,1,1,1,1,1,1,2,2,2,2,2,2,3,3,3,3,4,4,4,4,4,3,3,3,2,2,2,2,2,2,1,1,1,1,1,1,1,
3,3,3,3,2,2,2,2,2,2,2,1,1,1,1,1,1,1,2,2,2,2,2,2,3,3,3,3,3,4,4,4,4,4,3,3,3,2,2,2,2,2,2,2,
1,1,1,1,1,1,1,2,2,2,2,2,2,3,3,3,3,4,4};}
void main()
{
    enable_interrupts(INT_EXT);
    enable_interrupts(GLOBAL);
```

```
set_tris_a(0x00);
set_tris_b(0xFF);
set_tris_c(0xFF);
ext_int_edge(0,1);
while(1)
{
if(start==1)
{
disable_interrupts(INT_EXT);
SVM:
i=0;
while(i<=33 && i>=0)
{
output_a(0b001100);
delay_us(a[i]);
output_a(0b011000);
delay_us(b[i]);
output_a(0b001001);
delay_us(c[i]);
output_a(0b001100);
delay_us(d[i]);
output_a(0b001001);
delay_us(c[i]);
output_a(0b011000);
delay_us(b[i]);
output_a(0b001100);
delay_us(a[i]);
```

```
i++;  
}  
while(i<=60 && i>33)  
{  
    output_a(0b000011);  
    delay_us(a[i]);  
    output_a(0b001001);  
    delay_us(b[i]);  
    output_a(0b100001);  
    delay_us(c[i]);  
    output_a(0b000011);  
    delay_us(d[i]);  
    output_a(0b100001);  
    delay_us(c[i]);  
    output_a(0b001001);  
    delay_us(b[i]);  
    output_a(0b000011);  
    delay_us(a[i]);  
    i++;  
}  
while(i<=100 && i>60)  
{  
    output_a(0b110000);  
    delay_us(a[i]);  
    output_a(0b100001);  
    delay_us(b[i]);  
    output_a(0b100100);
```

```
delay_us(c[i]);
output_a(0b110000);
delay_us(d[i]);
output_a(0b100100);
delay_us(c[i]);
output_a(0b100001);
delay_us(b[i]);
output_a(0b110000);
delay_us(a[i]);
i++;
}
while(i<=133 && i>100)
{
output_a(0b001100);
delay_us(a[i]);
output_a(0b100100);
delay_us(d[i]);
output_a(0b000110);
delay_us(c[i]);
output_a(0b100100);
delay_us(b[i]);
output_a(0b001100);
delay_us(a[i]);
i++;
}
while(i<=166 && i>=133)
{
```

```
output_a(0b000011);
delay_us(a[i]);
output_a(0b000110);
delay_us(b[i]);
output_a(0b010010);
delay_us(c[i]);
output_a(0b000011);
delay_us(d[i]);
output_a(0b010010);
delay_us(c[i]);
output_a(0b000110);
delay_us(b[i]);
```

```
output_a(0b000011);
delay_us(a[i]);
i++;
}
while(i<200 && i>166)
{
output_a(0b110000);
delay_us(a[i]);
output_a(0b010010);
delay_us(d[i]);
output_a(0b011000);
delay_us(c[i]);
output_a(0b010010);
delay_us(b[i]);
```

```

output_a(0b110000);
delay_us(a[i]);
i++;
}
goto SVM;
}
}
}

```

1.3 Program for Matrix convereter:

```

#include<p18f4550.h>
#include<delays.h>
#pragma config FOSC = HS
void main(void)
{
    TRISA=0b00111111;//Rectifier
    TRISB=0b00000000;//Matrix
    TRISC=0b00000000;//Matrix last pin
    TRISD=0b00111111;//Inverter
    TRISE=0x00;
    while(1)
    {
        LATBbits.LATB1=(PORTAbits.RA0*PORTDbits.RD0)+(PORTAbits.RA1*POR
TDbits.RD1);
        LATBbits.LATB2=(PORTAbits.RA0*PORTDbits.RD2)+(PORTAbits.RA1*POR
TDbits.RD3);
    }
}

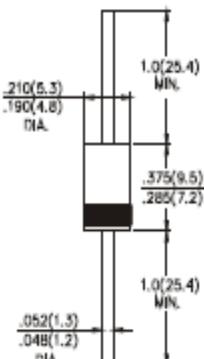
```

```
LATBbits.LATB3=(PORTAbits.RA0*PORTDbits.RD4)+(PORTAbits.RA1*POR  
TDbits.RD5);  
  
LATBbits.LATB4=(PORTAbits.RA2*PORTDbits.RD0)+(PORTAbits.RA3*POR  
TDbits.RD1);  
  
LATBbits.LATB5=(PORTAbits.RA2*PORTDbits.RD2)+(PORTAbits.RA3*POR  
TDbits.RD3);  
  
LATBbits.LATB6=(PORTAbits.RA2*PORTDbits.RD4)+(PORTAbits.RA3*POR  
TDbits.RD5);  
  
LATBbits.LATB7=(PORTAbits.RA4*PORTDbits.RD0)+(PORTAbits.RA5*POR  
TDbits.RD1);  
  
LATCbits.LATC0=(PORTAbits.RA4*PORTDbits.RD2)+(PORTAbits.RA5*POR  
TDbits.RD3);  
  
LATCbits.LATC1=(PORTAbits.RA4*PORTDbits.RD4)+(PORTAbits.RA5*POR  
TDbits.RD5);  
}  
}
```

APPENDIX – 2

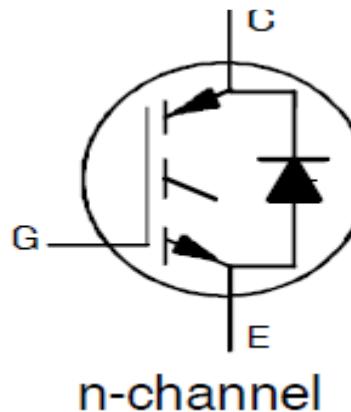
DATASHEETS

2.1. IN5408 Datasheet:

 <p>FEATURE</p> <ul style="list-style-type: none"> • Low forward voltage • High current capability • Low leakage current • High surge capability • Low cost <p>MECHANICAL DATA</p> <ul style="list-style-type: none"> • Case:Mold plastic use UL 94V-0 recognized flame retardant epoxy • Terminals:Axial leads, solderable per MIL-STD-202, method 208 • Polarity: Color band denotes cathode • Mounting Position:Any 	<p>VOLTAGE RANGE 50 TO 1000 Volts CURRENT 3.0 Amps</p> <p>DO-201AD</p>  <p>Dimensions in Inches and (millimeters)</p>																																																																																																																																														
<p>MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS</p> <p>Ratings at 25°C ambient temperature unless otherwise specified. Single phase, half wave, 60Hz, resistive or inductive load. For capacitive load, derate current by 20%.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th><th>IN5400</th><th>IN5401</th><th>IN5402</th><th>IN5403</th><th>IN5404</th><th>IN5405</th><th>IN5406</th><th>IN5407</th><th>IN5408</th><th>UNITS</th></tr> </thead> <tbody> <tr> <td>Maximum Recurrent Peak Reverse Voltage</td><td>50</td><td>100</td><td>200</td><td>300</td><td>400</td><td>500</td><td>600</td><td>800</td><td>1000</td><td>V</td></tr> <tr> <td>Maximum RMS Voltage</td><td>35</td><td>70</td><td>140</td><td>210</td><td>280</td><td>350</td><td>420</td><td>560</td><td>700</td><td>V</td></tr> <tr> <td>Maximum DC Blocking Voltage to TA = 150°C</td><td>50</td><td>100</td><td>200</td><td>300</td><td>400</td><td>500</td><td>600</td><td>800</td><td>1000</td><td>V</td></tr> <tr> <td>Maximum Average Forward Rectified Current .5", (12.5mm) Lead Length at TA = 75°C</td><td></td><td></td><td></td><td></td><td></td><td>3.0</td><td></td><td></td><td></td><td>A</td></tr> <tr> <td>Peak Forward Surge Current 8.3 ms single half sine-wave</td><td></td><td></td><td></td><td></td><td></td><td>150</td><td></td><td></td><td></td><td>A</td></tr> <tr> <td>Maximum Forward Voltage at 3.0A Peak</td><td></td><td></td><td></td><td></td><td></td><td>1.2</td><td></td><td></td><td></td><td>V</td></tr> <tr> <td>Maximum Reverse Current, TA ~25°C at Rated DC Blocking Voltage TA = 55°C</td><td></td><td></td><td></td><td></td><td></td><td>10</td><td></td><td></td><td></td><td>µA</td></tr> <tr> <td></td><td></td><td></td><td></td><td></td><td></td><td>500</td><td></td><td></td><td></td><td>µA</td></tr> <tr> <td>Maximum Full Load Reverse Current, Full Cycle Average, .5", (12.5mm) Lead Length TA = 105°C</td><td></td><td></td><td></td><td></td><td></td><td>500</td><td></td><td></td><td></td><td>µA</td></tr> <tr> <td>Typical Junction Capacitance (Note 1)</td><td></td><td></td><td></td><td></td><td></td><td>50</td><td></td><td></td><td></td><td>pF</td></tr> <tr> <td>Storage Temperature Range TA</td><td></td><td></td><td></td><td></td><td></td><td>-65 to +175</td><td></td><td></td><td></td><td>°C</td></tr> <tr> <td>Operating Temperature Range TJ</td><td></td><td></td><td></td><td></td><td></td><td>-65 to +170</td><td></td><td></td><td></td><td>°C</td></tr> </tbody> </table> <p>Notes : 1. Measured at 1.0 MHz and applied reverse voltage of 4.0 Vdc * JEDEC Registered Value.</p>		IN5400	IN5401	IN5402	IN5403	IN5404	IN5405	IN5406	IN5407	IN5408	UNITS	Maximum Recurrent Peak Reverse Voltage	50	100	200	300	400	500	600	800	1000	V	Maximum RMS Voltage	35	70	140	210	280	350	420	560	700	V	Maximum DC Blocking Voltage to TA = 150°C	50	100	200	300	400	500	600	800	1000	V	Maximum Average Forward Rectified Current .5", (12.5mm) Lead Length at TA = 75°C						3.0				A	Peak Forward Surge Current 8.3 ms single half sine-wave						150				A	Maximum Forward Voltage at 3.0A Peak						1.2				V	Maximum Reverse Current, TA ~25°C at Rated DC Blocking Voltage TA = 55°C						10				µA							500				µA	Maximum Full Load Reverse Current, Full Cycle Average, .5", (12.5mm) Lead Length TA = 105°C						500				µA	Typical Junction Capacitance (Note 1)						50				pF	Storage Temperature Range TA						-65 to +175				°C	Operating Temperature Range TJ						-65 to +170				°C
	IN5400	IN5401	IN5402	IN5403	IN5404	IN5405	IN5406	IN5407	IN5408	UNITS																																																																																																																																					
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Maximum Full Load Reverse Current, Full Cycle Average, .5", (12.5mm) Lead Length TA = 105°C						500				µA																																																																																																																																					
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2.2 IRG4BC15UDPBF (IGBT WITH ULTRAFAST SOFT RECOVERY DIODE) Datasheet:

2.2.1 Pin Diagram:

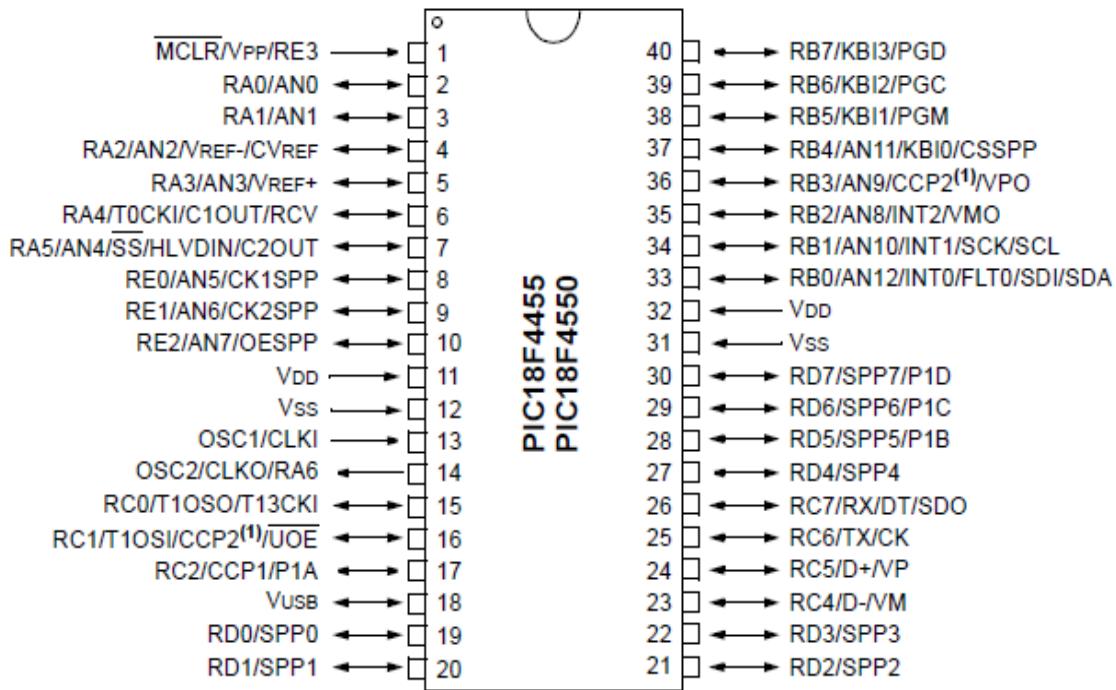


2.2.2 Ratings Table:

	Parameter	Max.
V_{CES}	Collector-to-Emitter Voltage	600
$I_C @ T_C = 25^\circ\text{C}$	Continuous Collector Current	14
$I_C @ T_C = 100^\circ\text{C}$	Continuous Collector Current	7.8
I_{CM}	Pulsed Collector Current ①	42
I_{LM}	Clamped Inductive Load Current ②	42
$I_F @ T_C = 100^\circ\text{C}$	Diode Continuous Forward Current	4.0
I_{FM}	Diode Maximum Forward Current	16
V_{GE}	Gate-to-Emitter Voltage	± 20
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	49
$P_D @ T_C = 100^\circ\text{C}$	Maximum Power Dissipation	19
T_J	Operating Junction and	-55 to +150
T_{STG}	Storage Temperature Range	
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)
	Mounting Torque, 6-32 or M3 Screw.	10 lbf•in (1.1 N•m)

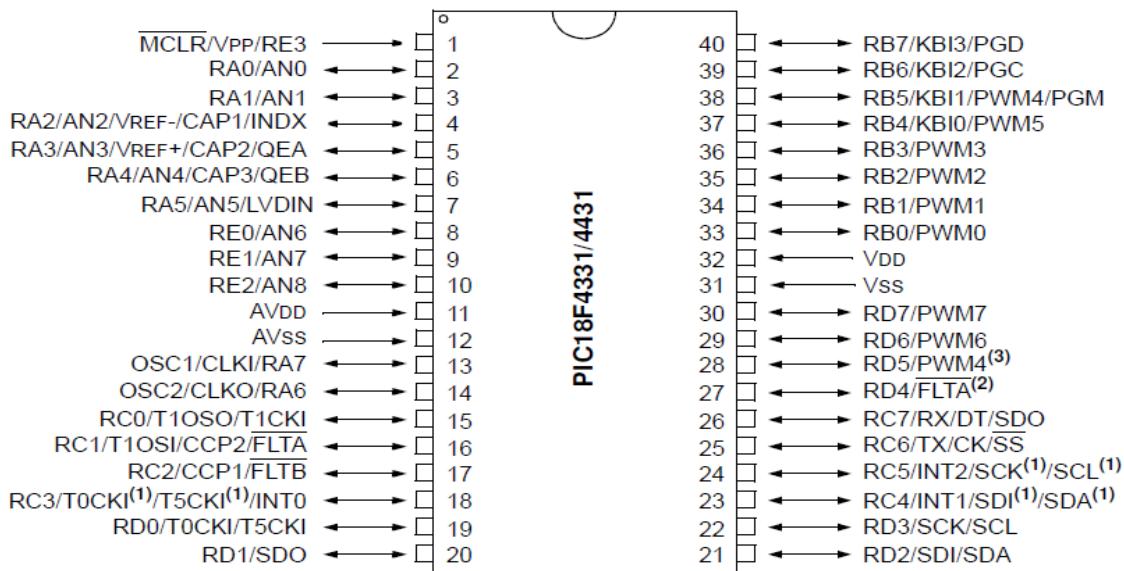
2.3. PIC18F4550:

2.3.1 Pin Diagram:



2.3. PIC 18F4331:

2.3.1 Pin Diagram:



APPENDIX – 3

GRANT LETTER FOR FUNDING

**SSN COLLEGE OF ENGINEERING
KALAVAKKAM–603110**

Kala Vijayakumar
President

19-10-2012

Dear Ms.Jeevitha, Ms. Kavitha and Mr. Manu Prasad,

I am glad to inform you that the following project submitted by you is approved, after careful evaluation, for internal funding.

“Harnessing wind energy via modern three-phase matrix converter topology”

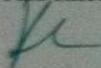
PROJECT MEMBERS: Ms.B. Jeevitha Final Year EEE (U.G)
Ms. V. Kavitha Final Year EEE (U.G)
Mr. M. Manu Prasad,Final Year EEE (U.G)

SUPERVISOR: Dr. A.N. Aravindan, EEE

I am sure that you will put your very best efforts to carry out the project successfully and will produce excellent results.

With my very best wishes.

Yours sincerely,



To

Ms.B. Jeevitha
Ms. V. Kavitha
Mr. M. Manu Prasad
Final Year EEE (U.G)

Copy to:

1. SUPERVISOR: Dr. A.N. Aravindan, EEE
2. H O D, EEE



REFERENCES

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- [2] Alesina, Alberto, and Marco GB Venturini. "Analysis and design of optimum-amplitude nine-switch direct AC-AC converters." *Power Electronics, IEEE Transactions on* 4.1 (1989): 101-112.
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- [9] Parekh, Rakesh. "VF control of 3-phase induction motor using space vector modulation." *Microchip Technology Inc., AN955, USA* (2005).