EXPT NO. : **DESIGN OF HALF ADDER AND FULL ADDER**
DATE :

AIM:

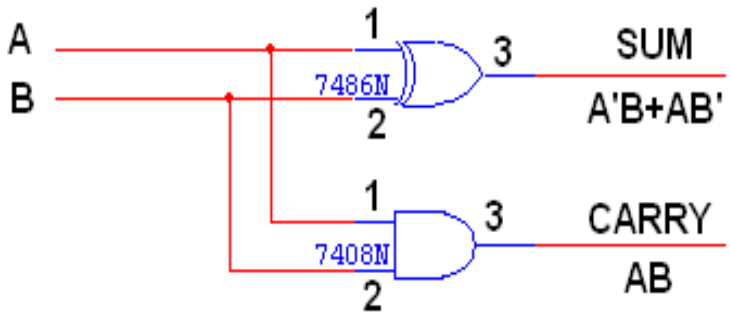
To design and simulate half adder and full adder verify the truth table using logic gates.

Tools Used:

LTSPice

LOGIC DIAGRAM:

HALF ADDER



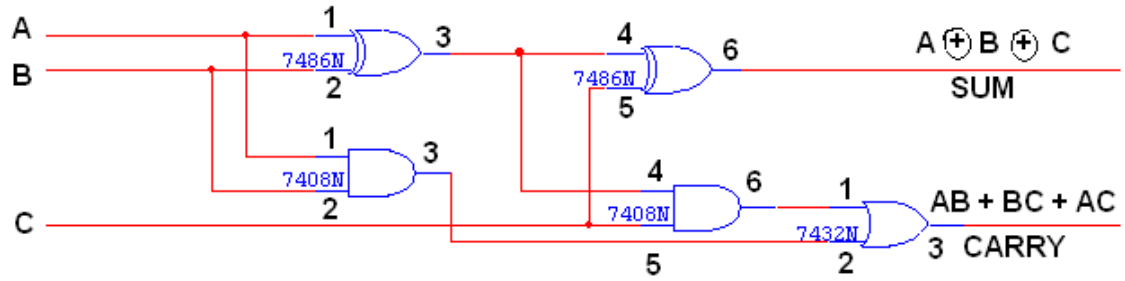
TRUTH TABLE:

A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

LOGIC DIAGRAM:

<u>FULL ADDER</u>

FULL ADDER USING TWO HALF ADDER



TRUTH TABLE:

A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

PROCEEDURE:

RESULT: