Betatron tune measurement in the LHC damper using GPU

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January 3, 2013

Abstract

This paper describes the betatron tune measurement in the Large Hadron Collider (LHC) at the European organization for nuclear research (CERN) including the present hardware and the future possible implementations using the Accelerating Damper Transverse (ADT) acquisitions. The ADT data have to be processed to be able to extract the betatron tune. This paper studies the use of Graphic Processing Units (GPUs) to process bunch position acquisition data.

Acknowledgements

Thanks everyone from CERN and from Heppia (TODO).

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 State of knowledge

In a particle accelerator, the charged particles circulate around the ring and oscillate due to the magnets and the accelerating structures. The accelerating structures, in the LHC supra-conducting cavities apply a strong electrical field that oscillates at the RF frequency (f_0) to particles in order to collect and accelerate particles in bunches inside a frequency bucket.

The particles inside a bucket are oscillating longitudinally along the ring and transversally in the vertical and horizontal plane. The longitudinal oscillations are damped by the beam control system. But the transversal oscillations must be damped by a separate system : the ADT[4, 8].

One of the key parameters of the accelerator is the betatron tune. The betatron tune, Q, is the quotient of the betatron oscillation and the particle frequencies.

$$f_\beta = Q * f_0$$

This value allow us to check if the particle beam is stable and don't reach any dangerous instabilities.

1.2 Tune measurement in the LHC

In order to measure the betatron tune in an accelerator we use Beam Position Monitors (BPMs). These monitors are able to measure the position of the beam in the vacuum chamber.

In the present setup Beam Instrumentation (BI) group is using their diode-based base-band-tune (BBQ) [2] system to acquire the tune over a certain number of machine turn (256 to 128'000). This can work as a passive instrument or as an on demand system by exciting 12 bunches in the beam with the tune kicker (MKQA). ADT has also been used for tune measurement excitation[3].

In normal operation, as the ADT is active, it is difficult to have a good picture of the excited bunches and make a fine tune measurement : the oscillations created by the MKQA are damped by the ADT. There have been studies to disable the ADT for a certain number of bunches in order to get a better tune measurement[5], but this may not be sufficient.

1.3 Proposed system

The ADT also have BPMs and these can have per bunch measurement[7]. This could allow a much precise measurement. But due to the high among of data to be processed (estimated to 640 mega bytes per seconds for each BPM) dedicated hardware is needed to compute the correct tune[6].

In order to be able to apply direct correction to beam oscilliation the betatron tune has to be measured at a high frequency, this has been estimated by BI to be between 5 and 10[Hz], once every 100 to 200[ms].

During the 2012 normal operation of the LHC, data has be acquired using the ADT acquisition system and data processing techniques has been tried to asses the modification that will be needed in order to make a reliable betatron tune measurement at a reasonable rate[6].

The current VMEbus implementation has some serious issues in particular the bus is quite slow the data rate of the bus is around 40 megabits per seconds. The data need to either be processed on the acquisition board or to be off-loaded to another computer using the serial link available on the board[1].

1.3.1 DSP on VME board

Digital Signal Processors (DSPs) are able to compute Fast Fourier Transforms (FFTs) at high rate and these are used already in the machine at different places to make high speed feedback loops. The question is : is it fast enough to compute all the FFTs needed, DSPs are two orders of magnitude slower than GPUs. We also would have to develop a completely new system in order to be able to use them, in fact we don't have DSPs in the present ADT. The cost of development and the complexity of the deployment should also be studied.

1.3.2 FPGA pre-processing on VME board

Like in the approach using DSPs on VME boards, the question of computing power is still unsolved. We already have in house experience and we already have a lot of Field-Programmable Gate Array (FPGA) installed in the ADT. But if we want to do it we will have to create a new card able to replace the existing one and to make the computation. This mean create a potential problem in the existing setup. The cost is also to be studied we have to develop a new card, test it and install it in the LHC. Also the number of card and FPGA is not well understood, it could be anywhere between 4 and 3000 (FIXME).

1.3.3 GPU off-board computing

This solution can be integrated easily in the present setup. The present acquisition cards already have a digital output and could be used to transfer the data in another crate that could do the computations. The GPUs are cheap (compare to the price of developing a new VMEbus card) and easily scalable. The GPU should have largely enough computing power to be able to make the FFTs. Another interesting aspect of this solution is the ability to test it using Central Processing Unit (CPU).

1.4 Problem definition

1.4.1 Algorithm

1.4.2 Hardware

1.4.3 Timing

Chapter 2

Results

2.1 Implemented System

2.2 Notch filter

2.3 FFT

2.3.1 FFTW

2.3.2 FFT with OpenCL on GPU

2.3.3 FFT with OpenCL on CPU

2.4 Amplitude

2.5 SVD

2.6 Performances

2.6.1 Pipelining

Pipelining was tested and used in the process and it was possible to win around 15% in performances around it.

2.6.2 Memory

2.6.3 Time

Figure 2.1: Time flow with different implementations and with 3000 bunches of 2048 points each.

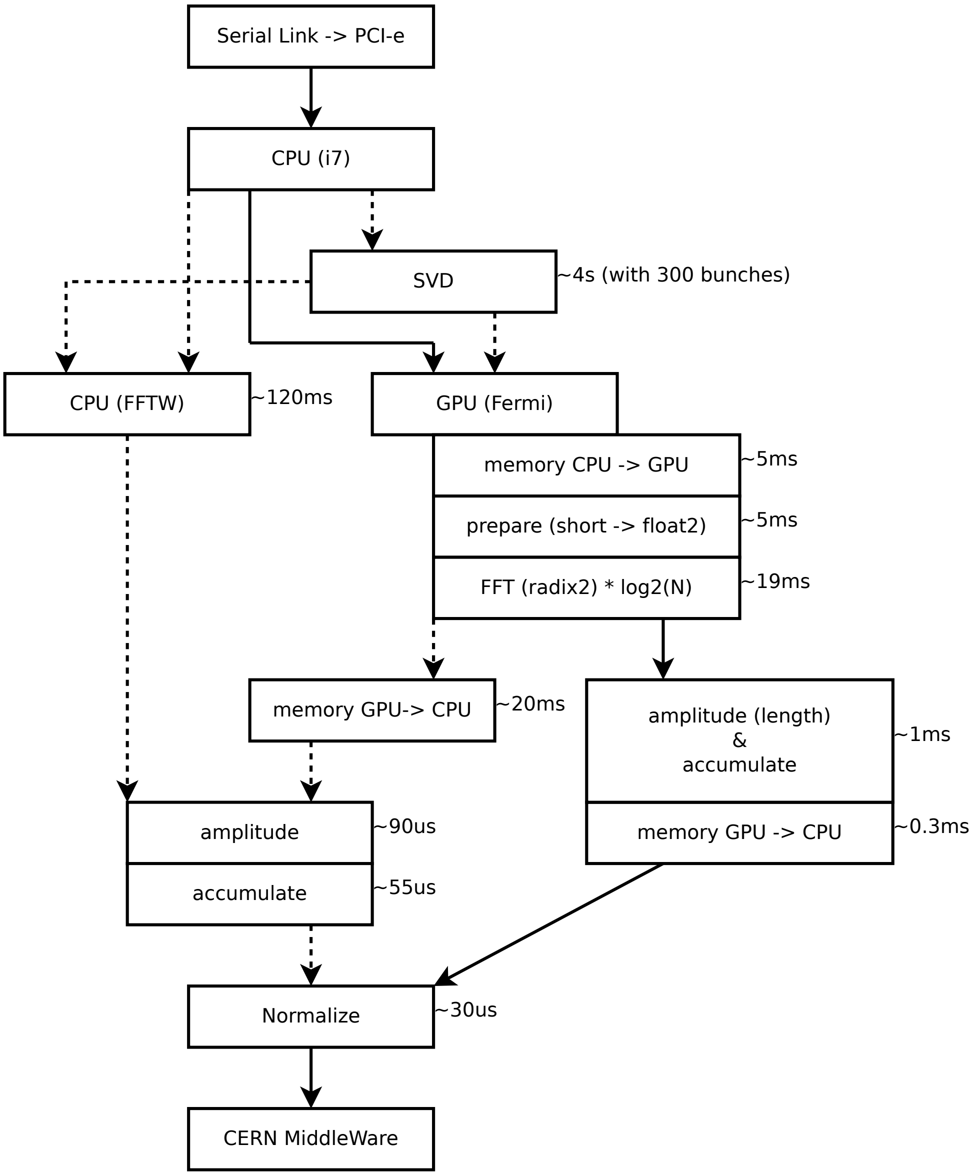
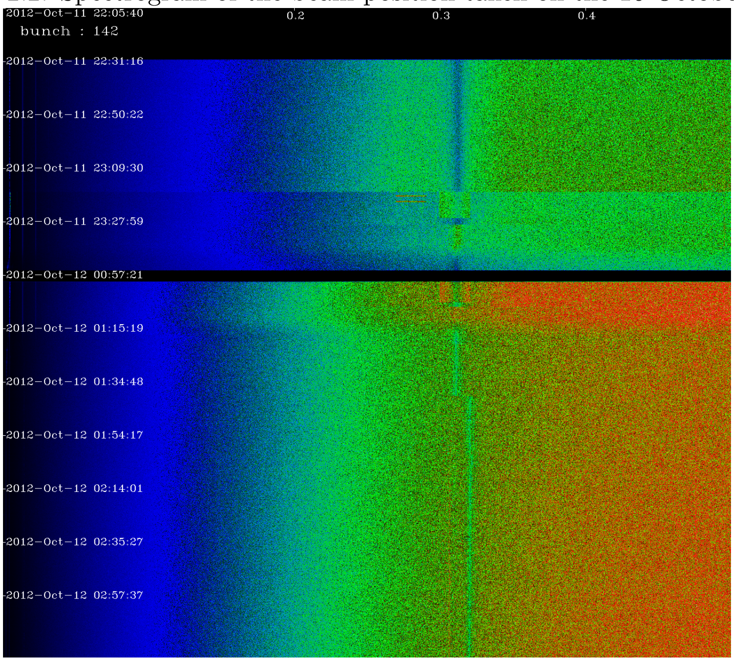


Figure 2.2: Spectrogram of the beam position taken on the 16 October 2012



Chapter 3

Discussion

Chapter 4

Conclusion

This project looks like a nice place to try using GPUs in accelerators. The possibilities are promising and the gain for the stability of the LHC could allow more physic time. GPUs could prove to be useful and be used in other places in accelerators where computing power is needed.

Chapter 5

Experimental

5.1 Estimation of the amount of data

Presently the LHC is working with an interval of 50ns between bunches this correspond to a bunch every 10 buckets. But the Operation (OP) is planning to move to 25ns bunches spacing this would mean 5 buckets between bunches. With the RF frequency (f_0) we can compute the number of acquisitions per seconds.

$$for\ 50\ ns\ :\frac{400.789M}{20} = 20'039'450 \leq 2^{25}$$

$$for\ 25\ ns\ :\frac{400.789M}{10} = 40'078'900 \leq 2^{26}$$

This represent the amount of data for one pickup (BPM), in the case of ADT we have two of them per beam and per plane so as the LHC has two rings and for each ring there are two transversal plane and there are two pickups per plane. This means we still have to multiply this value by eight.

$$for\ 50\ ns\ : 2^{25} * 8 = 2^{28}$$

$$for\ 25\ ns\ : 2^{26} * 8 = 2^{29}$$

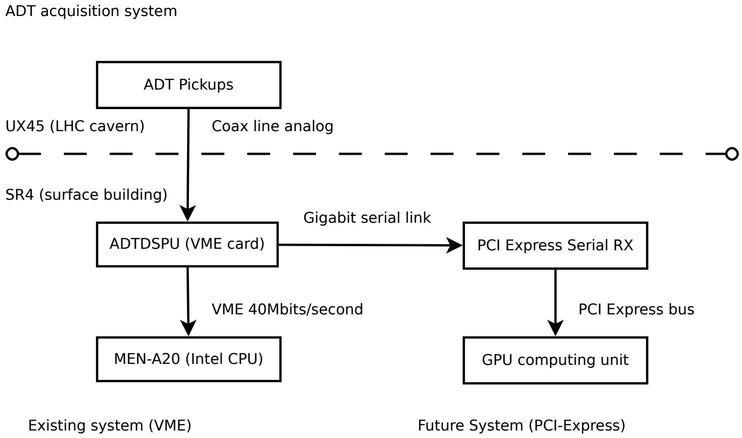
As FFTs on GPUs start to be be faster than CPUs around 2^{15} acquisitions it seems interesting to study this kind of system to compute the betatron tune.

5.2 Measurement with the ADT

In order to check the feasibility of the system and to have a good prototype the first test will be to excite some of the bunches and acquire the betatron tune using the ADT during the end of 2012 run.

A piece of software has been developed that will acquire the bunch by bunch acquisition and compute various algorithm on the data using the CPU and the FFTW library in the CERN infrastructure using Control (CO) group control system and the OP group infrastructure.

Figure 5.1: ADT acquisition hardware



5.3 Experimental Set-up

5.3.1 Hardware

5.3.2 Estimated Bandwith

5.3.3 Software

5.4 FFT

5.5 SVD

5.6 Machine development sessions

Using the ADT BPMs we acquired data in the machine during 3 independant Machine Developments (MDs). Most of the data taking was done in parallel to other normal LHC operation or during ADT dedicated MD time.

5.6.1 First session

Night session of the 11 october 2012.

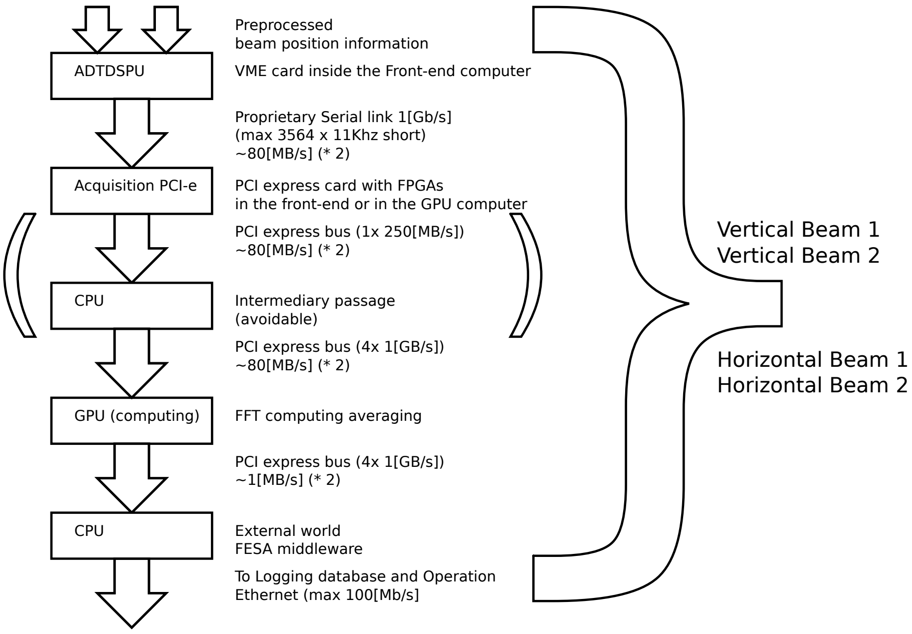
5.6.2 Second session

Parasitic session of the 16 october 2012

5.6.3 Third session

Ramp acquisition of the 14 november 2012

Figure 5.2: Acquisition data flow



Glossary

betatron tune the betatron tune is the frequency of the oscillations of the bunches divided by the RF frequency (f_0). 1, 5, 6

bucket at every Radio Frequency (RF) period in the RF frequency (f_0) there is a bucket, in each of these bucket a particles bunch can potentially be stored in the ring. 4, 6

bunch particules trapped inside an RF bucket circulating in the machine. 1, 4, 6, 13

cavity RF structure made to accelerate the particles, it uses a high power radio frequency into a resonating structure to increase the energy of the particles. 4, 13

damper machine in an accelerator that damp the transverse oscillation of the beam by applying a transverse electric field. 1, 14

FFTW is a C subroutine library for computing the discrete Fourier transform (DFT) in one or more dimensions, of arbitrary input size, and of both real and complex data (as well as of even/odd data, i.e. the discrete cosine/sine transforms or DCT/DST). 6

kicker machine in an accelerator that can kick the beam transversally, used to kick the beam in or out (injection or extraction kicker) of the beam pipe but also in our case excite the beam transversally. 4, 14

RF frequency (f_0) the base frequency of the RF in the cavities in the case of the LHC this frequency is 400.789MHz, this frequency dictate the number of bucket that the machine can have. 4, 6, 13

VMEbus a computer bus standard widespread at CERN, in the case of the LHC RF the bus has a larger board and some of the pins are used to route custom signals between cards. 5

Acronyms

ADT Accelerating Damper Transverse. 1, 4–6

BBQ diode-based base-band-tune. 4

BI Beam Instrumentation. 4

BPM Beam Position Monitor. 4–6

CERN European organization for nuclear research. 1, 6

CO Control. 6

CPU Central Processing Unit. 5, 6

DSP Digital Signal Processor. 5

FFT Fast Fourier Transform. 5, 6

FPGA Field-Programmable Gate Array. 5

GPU Graphic Processing Unit. 1, 5, 6, 12

LHC Large Hadron Collider. 1, 4–6, 12

MKQA tune kicker. 4

OP Operation. 6

RF Radio Frequency. 13

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