Department of Computer Science
Faculty of Computing
UNIVERSITI TEKNOLOGI MALAYSIA

SUBJECT NAME: **DIGITAL LOGIC**

SUBJECT CODE: **SECR 1013**

SEMESTER: **SEMESTER 1**

TITLE: **CASE STUDY**

GROUP MEMBER:

1. **Name: ALISYA HUMAYRAA BT MOHD KHAIRANI**
   No. Matrics: A24CS0043
2. **Name: ALLISYA MAISARAH BT SUHAIZAL**
   No. Matrics: A24CS0044
3. **Name:NUR ANISAH SOLEHAH BINTI MOHD HAMIM**
   No. Matrics: A24CS0157
4. **Name:NAJIHAH BINTI AZHAN KHAN**
   No. Matrics: A24CS0144

SUBMITTED DATE: **31 JANUARY 2025**

COMMENTS:

1.0 DEDICATION AND ACKNOWLEDGEMENT

In performing our case study, we have to take the help and guidelines of some respected persons, who deserves our greatest gratitude. The completion of these assignments gives our much pleasure. Firstly, we would like to show our gratitude to Mr. Fariz Ali, Digital Logic Lecturer, UTM for giving us a good guideline for assignment throughout numerous consultations. Secondly, we would like to appreciate the immense patience shown by ourselves while We was working on this. Also, we would like to thank ourselves for courage and patience while working for this assignment. We would also like to expand our deepest gratitude to all those who have directly and indirectly guided we in writing this case study. Many people, especially our classmates have made valuable comments, suggestions on this case study which gave us the inspiration to improve our case study. We thank all the people for their help directly and indirectly to complete our assignment Digital Logic case study.

2.0 OBJECTIVES

The objective of this project is to:

1. Design and implement a system to transmit data between two labs, each lab consists of 8 computers.
2. Integrate a 3-bit synchronous counter to manage the data transfer.
3. Utilize sequential circuit elements.
4. Validate the circuit design and functionality using the Digital Electronics Deeds Simulator.
5. Demonstrate the application of digital electronics principle for communications between the two labs.

TABLE OF CONTENT

3.0 Background

In this project, we aim to develop a system for data transfer between two labs, with each lab consists of 8 computers. The system focuses reliable synchronization of data across the labs. By incorporating components like 3-bit synchronous counter and D flip-flop, this project will highlight the use of sequential and combinational circuits in managing data flow efficiently. We will use Digital Electronics Deeds Simulator to carry out the design and simulation.

Combinational Circuit Components

- 3-bit synchronous counter
- Basic gates
- LEDs
- 4-bit comparator

Sequential Circuit Components

- D flip-flop
- Clock enabler

Extra Features

- Able to set our own passwords

4.0 Problem Statement

In many systems today, there is often lack of structured and efficient data transmission between two computers network. This can lead to delays, synchronization issues and unreliable communication, especially when multiple devices are involved.

The challenge arises when there is no synchronized method to transfer data across multiple computers such as labs. Without a proper system, the flow of information may be disrupted that can lead to errors.

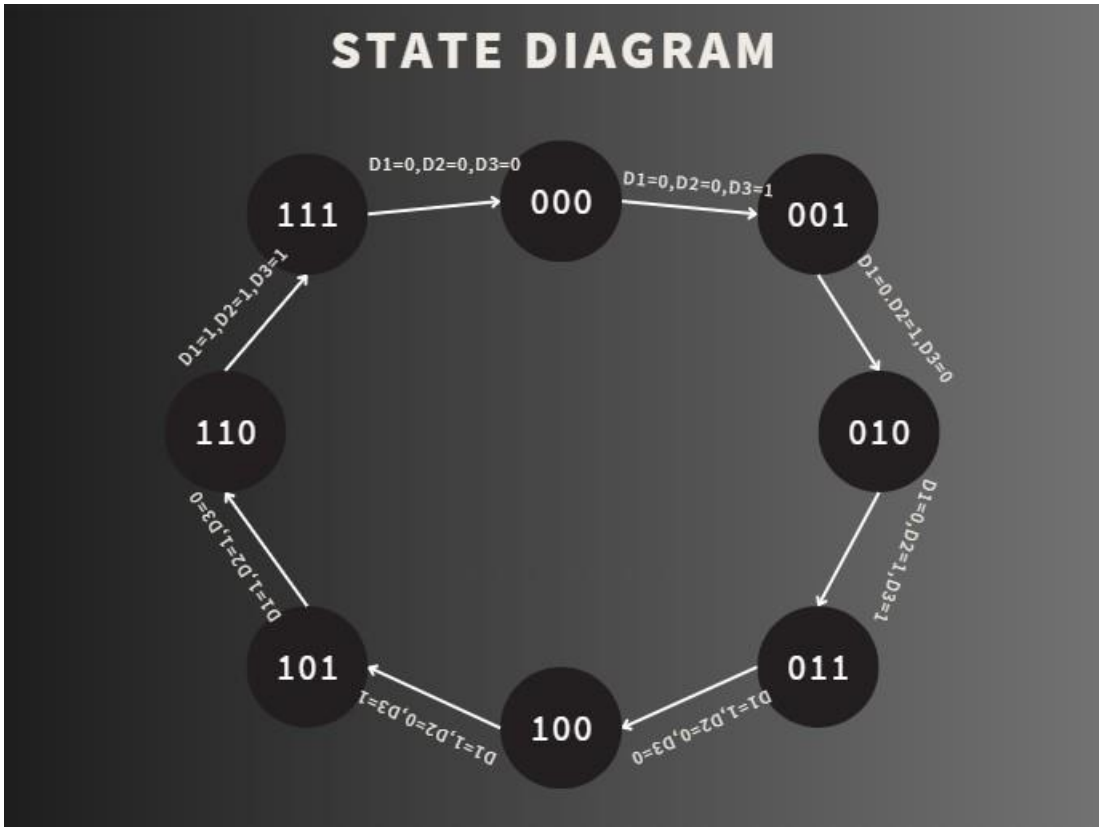
To address this issue, we propose a solution using a 3-bit synchronous counter and D flip-flop to allow synchronized communication between two labs. We will design and test using Deeds Electronics Deeds Simulator to ensure the data transfer is efficient.

5.0 Suggested Solution

To address the transmission data problem, we propose a solution using 3-bit synchronous counter, which sequences the flow of data to ensure organized communication. The D flip-flop will be used to maintain data synchronization during transmission process.

Each lab will have set of switches of input, which will initiate data transfer, LEDs that will provide visual feedback for monitoring. The synchronous counter allows computers in Lab A communicate with Lab B. Moreover, clock signals are used to enable precise timing and prevent error during data transmission.

6.0 State Diagram



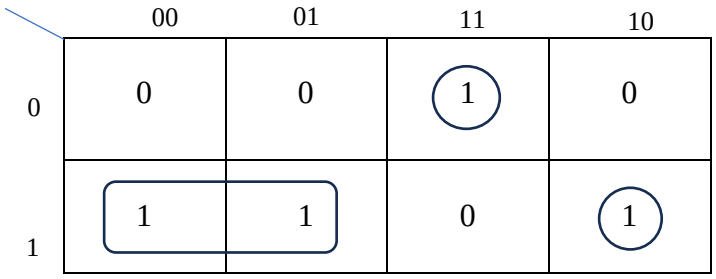
7.0 REPORT CASE

7.1 TRUTH TABLE

PRESENT STATE			NEXT STATE			D1	D2	D3
Q1	Q2	Q3	Q1	Q2	Q3			
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0

7.2 KARNAUGH MAPS (K-MAP)

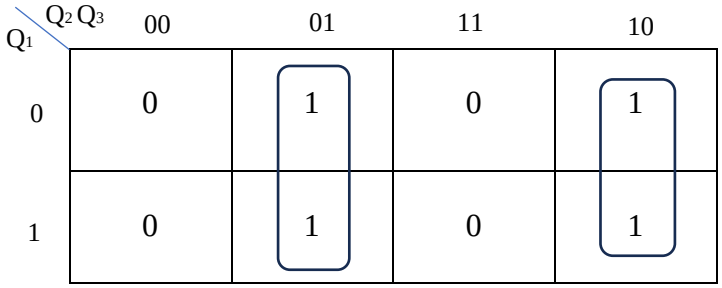
D1



EQUATION

$D1 = Q_1 Q_2' + Q_1' Q_2 Q_3 + Q_1 Q_2 Q_3'$

D2

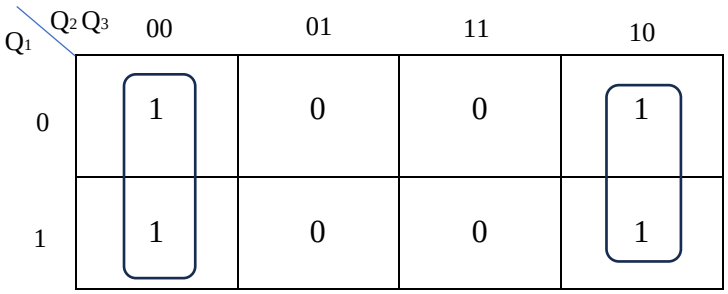


EQUATION

D2 = $Q_2'Q_3 + Q_2 Q_3'$

= $Q_2 \oplus Q_3$

D3



EQUATION

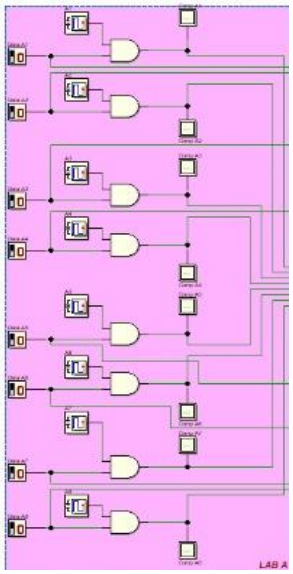
D3= $Q_2' Q_3' + Q_2 Q_3'$

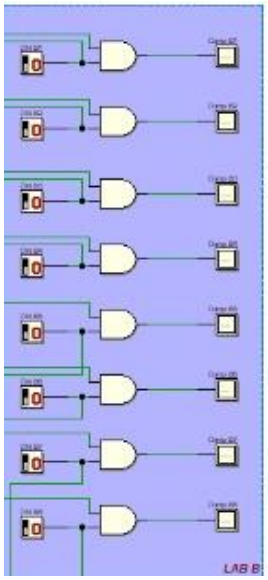
8.0 Implementation

8.1 Input switch

The input switches for Lab A and Lab B designed for user to enter the data manually which the user set the binary data that will transmit data. Each lab is equipped with 8 switches where each of the switch represent one bit where the first switch represents the Most Significant Bit (MSB) and the last switch represent the Least Significant Bit (LSB).

The input switches are simple to use. There is also LEDs that connect to each bit which provide real time feedback. The LEDs light up based on switch positions, allowing users to confirm the input values visually. This will ensure accuracy before transmission of data from Lab A and Lab B. By using this setup, the system is easy to operate and data will be synchronized between two labs.



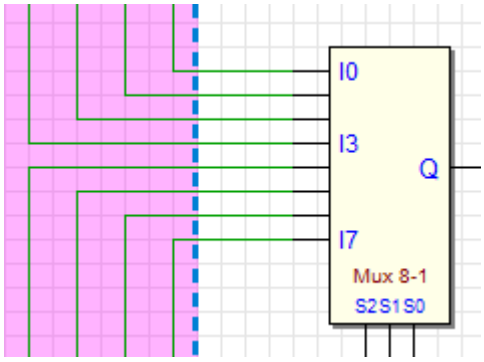


8.2 Multiplexer and Demultiplexer

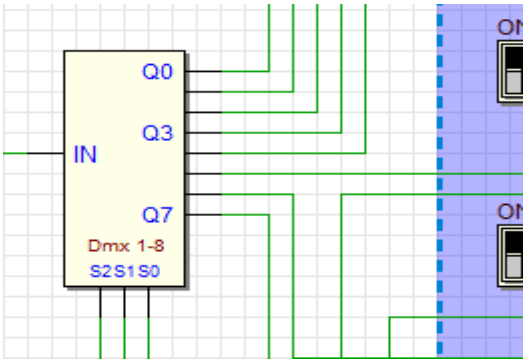
The multiplexer (Mux) in the circuit is used to select one signal from multiple input lines and foward it to a single output. The primary function of the multiplexer is to combine multiple signals into a single line, enabling efficient transmission of data from one part of circuit to another. In this circuit, the multiplexer in Lab A reduce the complexity of wiring by transmitting selected input signals to Lab B.

As for demultiplexer (Demux), it performs the reverse operation of the multiplexer. It takes a single input signal and distributes it to one of several output lines based on control signals. In this circuit, the demultiplexer in Lab B ensures that the transmitted signal from the multiplexer is routed to the correct output line. This allows the data sent from Lab A to be correctly distributed and used by the components in Lab B.

Together, the multiplexer and demultiplexer enable efficient and organized data routing between Lab A and Lab B.



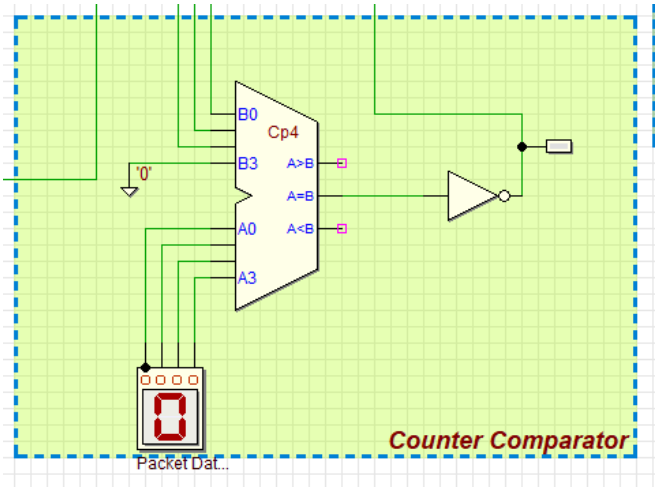
Multiplexer (Mux)



Demultiplexer (Demux)

8.3 Comparator

The comparator in this circuit compares the current 4-bit counter value with a preset reference value. It takes inputs from the counter (A0 to A3) and the preset value (B0 to B3) and produces three outputs: `A > B`, `A = B`, and `A < B`. The `A = B` output is inverted to control specific actions, such as stopping the counter or activating other modules when the counter matches the preset. A seven-segment display is included to show the preset value, making it easier to monitor the comparison. This ensures the system responds accurately when the desired condition is met.

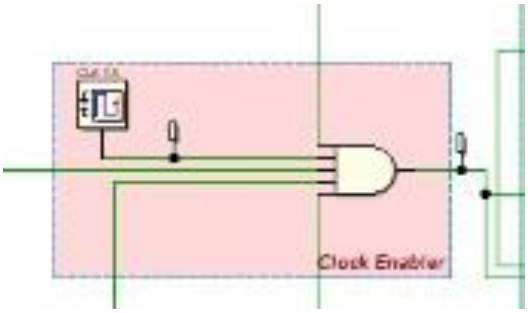


Counter Comparator

8.4 Clock Enabler

The clock enabler is built using a 5 input AND gates to ensure that clock signal is activated only when all conditions are met. The five inputs to AND gates are from power on switch, start switch, password output, comparator signal and a push buttons. All five input must be high in order for the clock to enable the system.

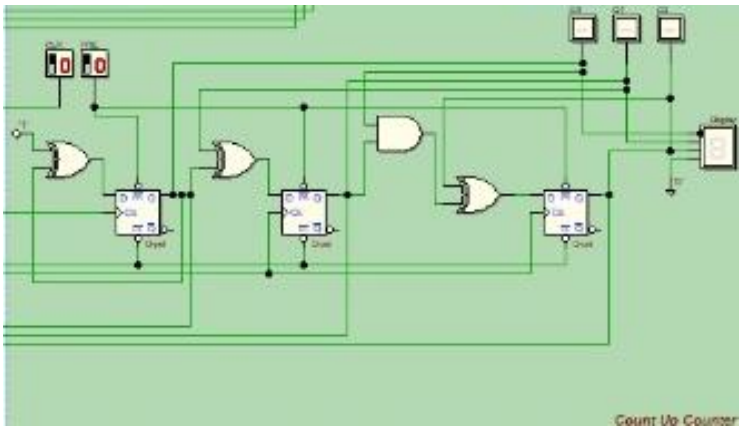
The output for the AND gate is connected to the clock output of the D flip-flop. This setup allows the system runs under the right conditions only.



8.5 D Flip-flop

We implement a 4-bit D flip-flop in this data transmission project. The counter operates based on a clock generator (PUSH button) and determine whether the data transmission should continue or stop. The counting starts when the D input receives a high state (1) signal from the Clock Enabler.

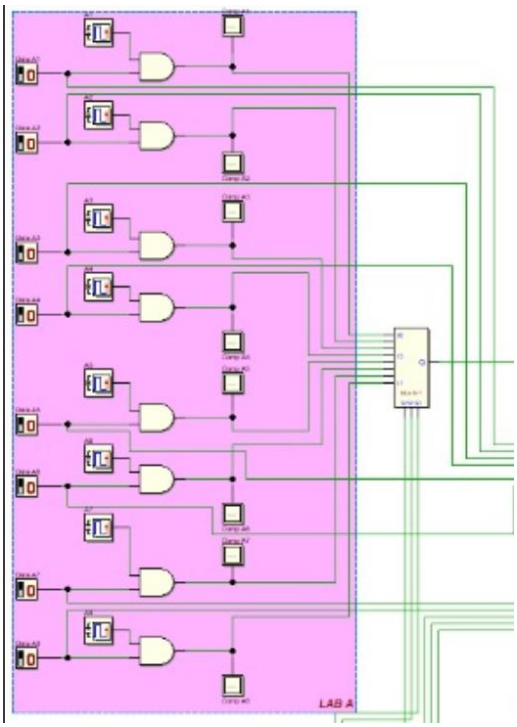
When the conditions are met, the system will activate the counting process. However, if the conditions are not met the counter remains inactive. The counting will stop process when either the pulse is no longer active or when the system successfully completes the user specified enter data.



8.6 Full duplex & Simple duplex

We implemented the full duplex and simple duplex as the full duplex communication systems enable simultaneous two-way data transmission, allowing both sending and receiving of information at the same time. This capability significantly enhances the efficiency of real-time communication applications, such as telephone systems, video conferencing, and modern internet-based technologies, where uninterrupted interaction is essential . Full duplex systems make use of FDD or TDD and similar techniques for smooth, uninterrupted flow of data without interference. These are essential in applications requiring very high-speed real-time communications.

LAB A have multiple inputs and outputs that are interconnected to the central logic bus. If LAB A can both **send and receive data simultaneously**, then this section operates as **Full Duplex**.



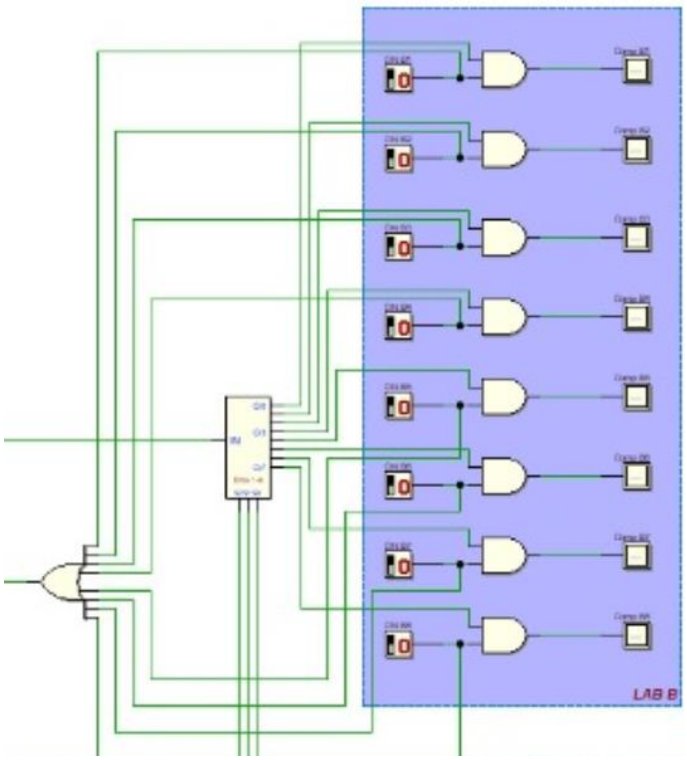
LAB A (refers to the diagram in deeds)

Simple duplex

We implemented in the circuit that has full and half duplex. Main reason we included simple duplex is half duplex communication systems facilitate bidirectional data transfer but restrict

the flow of information to one direction at a time. Unlike full duplex systems, half duplex devices alternate between sending and receiving data, which can result in slower communication speeds but is more cost-effective and simpler to implement. This system is widely used in applications where simultaneous communication is unnecessary, such as walkie-talkies, two-way radios, and older Ethernet networks. Despite its limitations, half duplex remains a practical solution for scenarios requiring basic communication or constrained bandwidth environments

LAB B are connected to the central logic bus in such a way that it could support unidirectional communication in certain cases. LAB B is configured to either send or receive data-but not at the same time-then this section operates as Simple Duplex .



LAB B (refers to deeds diagram)

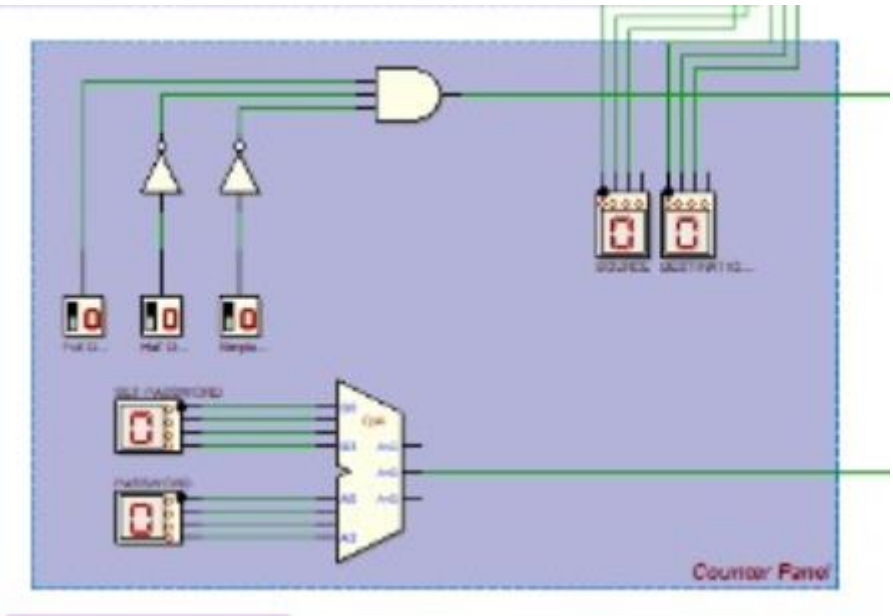
8.7 Counter Panel

Duplex Counter Panel is located in the blue section of the diagram. It is the module that executes counting operations either upwards or downwards. It communicates with other control circuitry, as illustrated in this diagram, in the form of clock enable block in red, and

the comparator of the counter in light green. The clock enables controls timing to ensure the counter is allowed to operate during active clock cycles. Meanwhile, a counter comparator looks for the prevailing count value being within predetermined boundaries or thresholds.

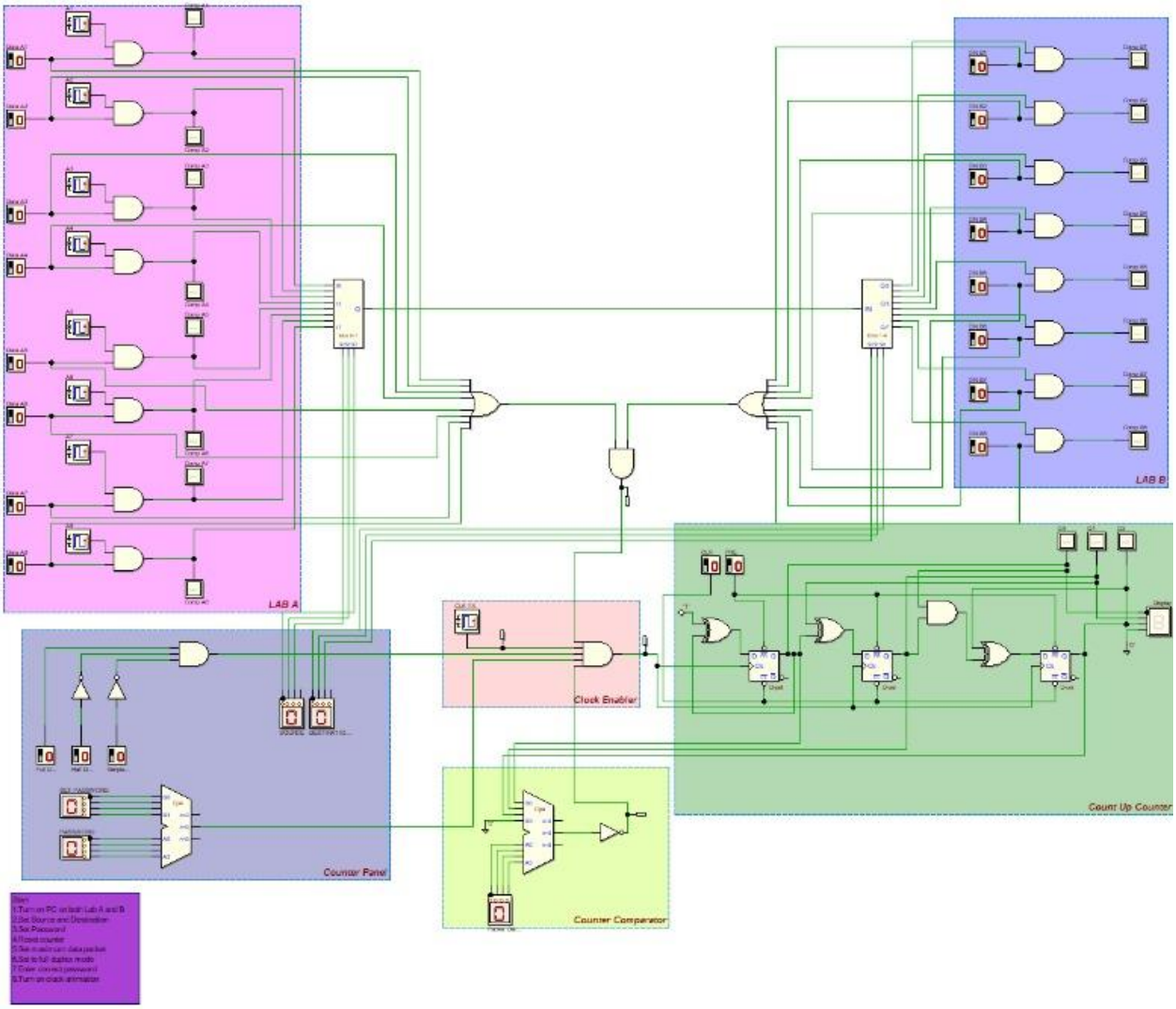
This panel accepts signals from other modules like LAB A and LAB B B that make the choice of increasing or decreasing the count. If an “up” signal is coming in, it increases its count conversely, the case for “down” commands
that reverse this whole process is when the duplex feature comes into operation supported by logic gates along with the controlling signals present within the panel.

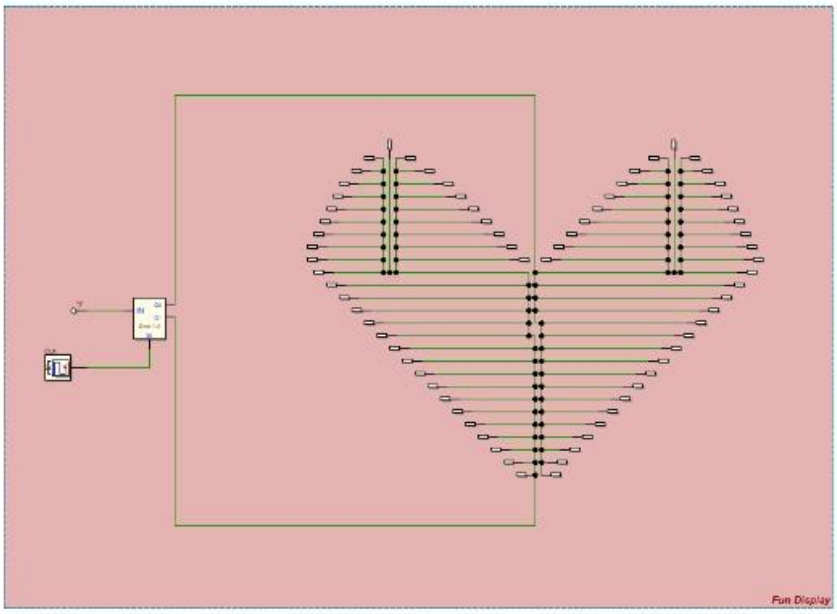
The counter panel is probably connected to the heart-shaped fun display, which visually represents the current count state. As the counter value changes, the display updates to reflect these changes dynamically. This integration of up-and-down counting functionality with visual output highlights the versatility of the Duplex Counter Panel in managing bidirectional counting tasks.



Counter Panel (blue section) refers to deeds diagram

Full Digital Electronics Deeds Circuit





9.0 CONCLUSION

In conclusion, the project demonstrates an efficient design for transmitting data between two labs

where each lab consists of 8 computers. The circuit incorporate components such as a 3-bit synchronous counter for data flow and D flip-flops to make sure data storage and synchronization are reliable. The use of switches, LEDs for visual outputs, and the Digital Electronics Deeds Simulator allow a thorough validation of the system's functionality.

It is an accomplishment when was successfully integrating the synchronous counter to manage the data transfer process. One challenge we faced was ensuring accurate synchronization and addressing timing issues when implementing the D flip-flops.

In future projects, we aim to expand the complexity of our designs by incorporating more advanced components and features. We are excited to continue applying our knowledge of digital logic for future projects.

10.0 REFERENCES

Admin. (2022, December 28). ***4 Examples of acknowledgement for case studies*****. Acknowledgement World.** https://acknowledgementworld.com/acknowledgement-for-case-study/

GeeksforGeeks. (2021, May 26). ***Synchronous 3 bit Up/Down counter*****. GeeksforGeeks.** https://www.geeksforgeeks.org/synchronous-3-bit-up-down-counter/

A synchronous counter design using D Flip-Flops and J-K Flip-Flops**. (2017, June 21). K.L. Craft - Website And Blog. https://klcraft.net/2017/06/21/a-synchronous-counter-design-using-a-d-flip-flop-and-a-j-k-flip-flop/**

11.0 APPENDICES

Task Distributions

Members	Task
Nur Anisah Solehah	**-Report (make the implementation for full duplex, simple duplex and duplex counter panel (explanation , elaborations for circuit and flow of the function))** **-slide for presentation (based on the report)**
Alisya Humayraa	**-Make circuit** **-Report (Dedication and Acknowledgement, Truth Table)**
Allisya Maisarah	**-Report (implementation for multiplexer, demultiplexer and 4-bit comparator)** **-slide for presentation (based on the report)**
Najihah	**-Report (Objectives, Background, Problem Statement, Solution Suggested, Conclusion, Table of Content, Implementation [input switch, clock enabler, D flip flop])**