

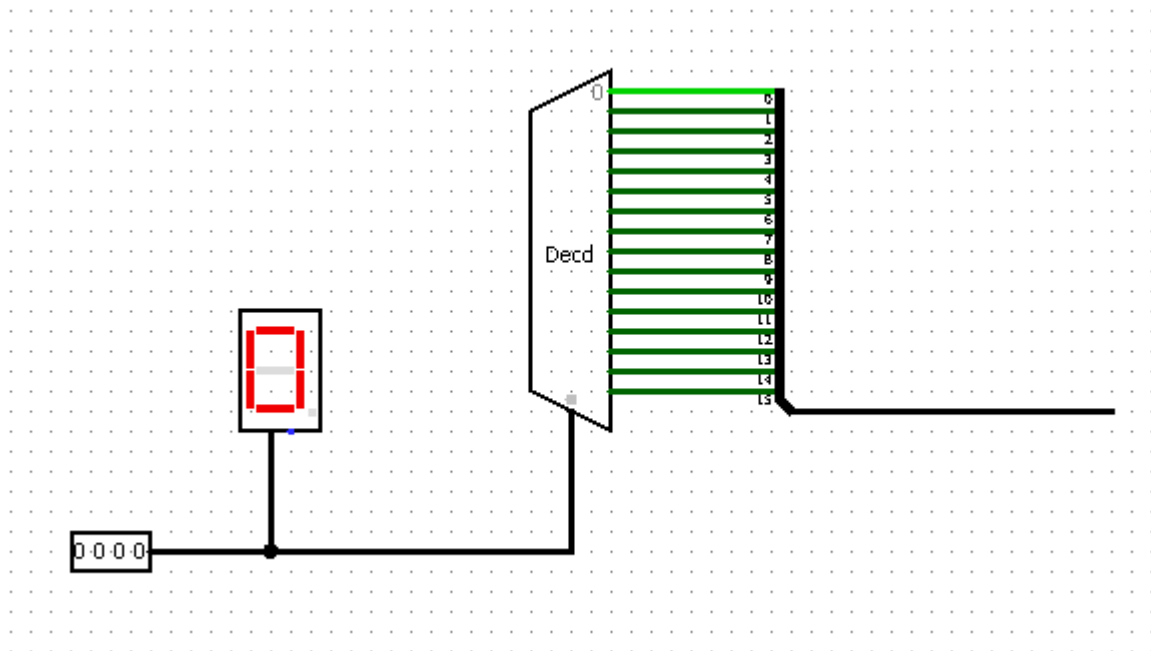
Simulation Lab 4 Answer Sheet
The Microprocessor

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Date: 3/27/18

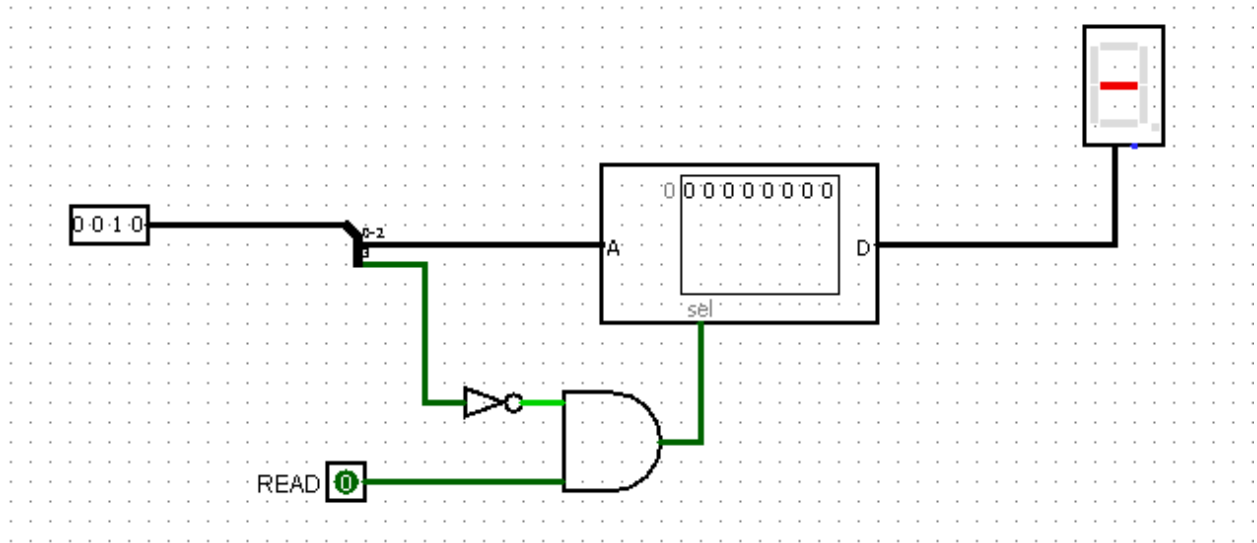
Task 4-1: Build the Addressing Logic

Include a picture of your Logisim addressing logic circuit here:



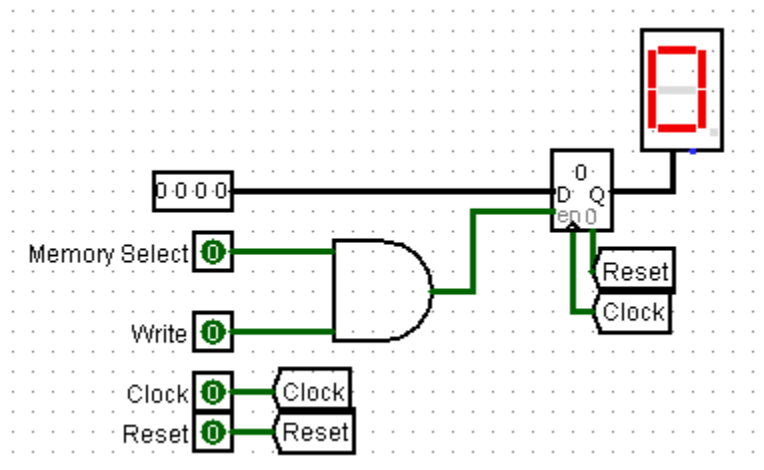
Task 4-2: Build a 4-Bit ROM Memory Cell

Include a picture of your Logisim 4-bit ROM circuit here:



Task 4-3: Build 4-Bit Output Port

Include a picture of your Logisim 4-bit output port circuit here:

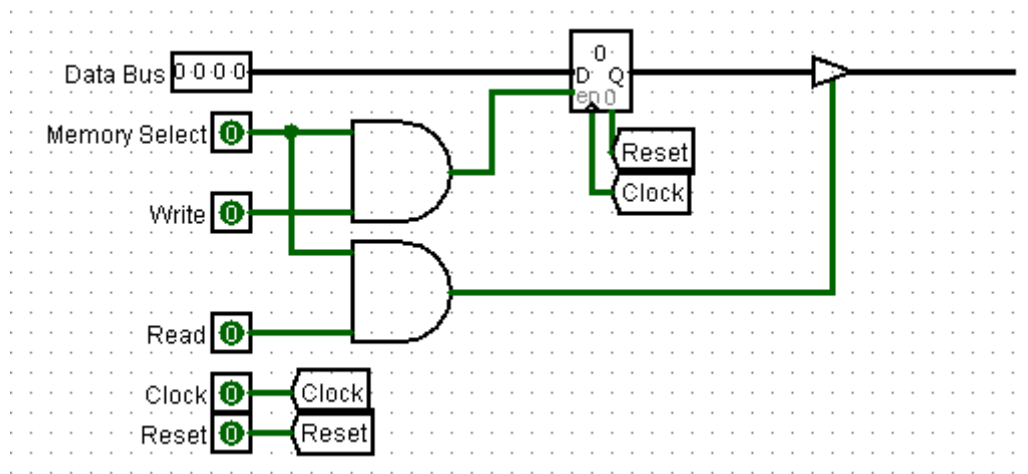


Test your circuit and record the results in **Table** .

| Table 1 | | | |
|----------------------------|-------|------------------|---|
| Data Bus (4-bit binary) | Write | Memory Select | Q |
| 1101 | 1 | 1 | d |
| 0001 | 0 | 1 | d |
| 0001 | 1 | 1 | 1 |
| 1100 | 1 | 1 | C |

Task 4-4: Build the 4-Bit RAM Cell

Include a picture of your Logisim 4-bit RAM circuit here:



Test your circuit and record the results in **Table** . Include a picture of your Logisim 4-bit RAM circuit testing set up.

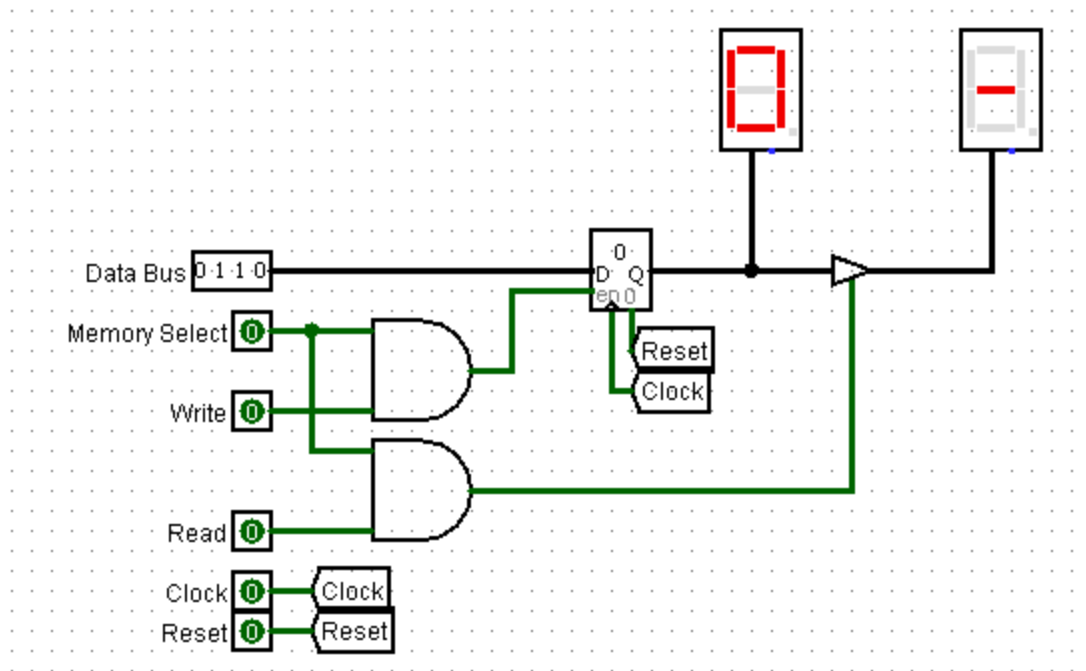
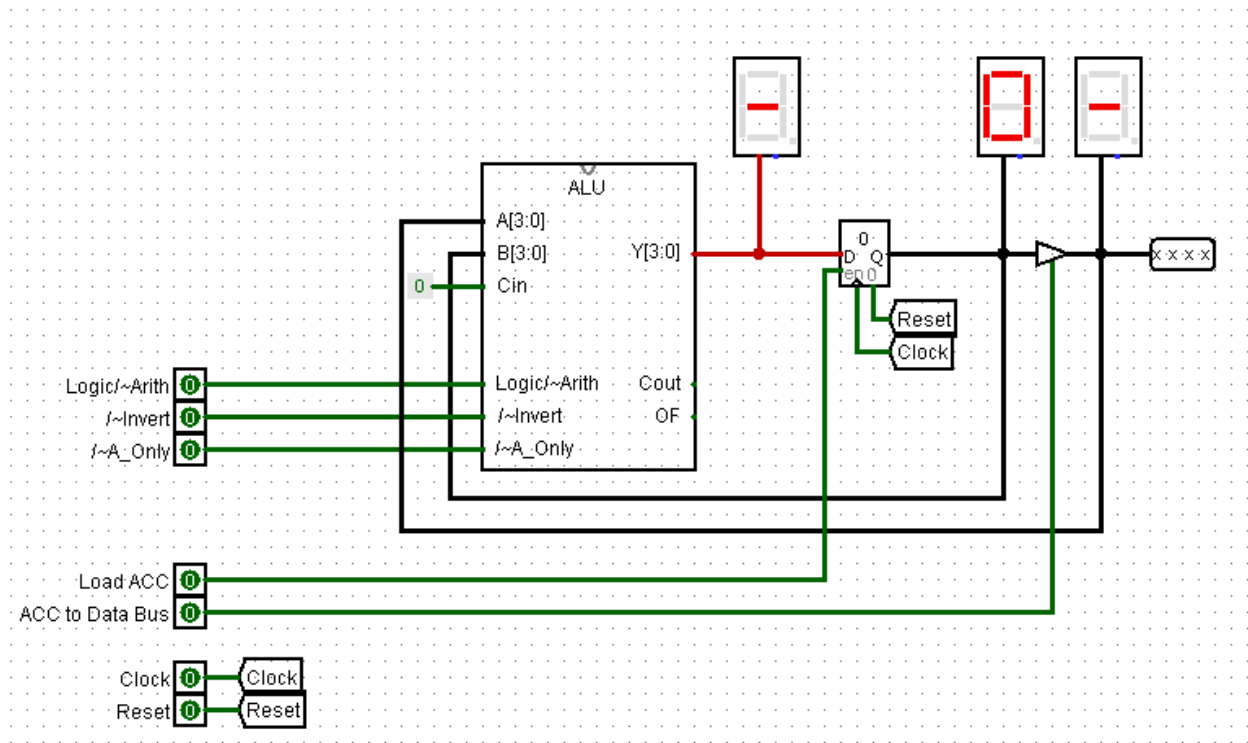


Table 2

| Data Bus (4-bit binary) | Write | Memory Select | Read | Q {between register and buffer} | Data Bus {after buffer} |
|----------------------------|-------|------------------|------|------------------------------------|----------------------------|
| 0111 | 0 | 1 | 0 | 7 | - |
| 0111 | 0 | 1 | 1 | 7 | 7 |
| 0110 | 1 | 1 | 1 | 6 | 6 |
| 1111 | 1 | 1 | 0 | f | - |
| 1111 | 0 | 1 | 1 | f | f |
| 1001 | 1 | 1 | 0 | f | - |

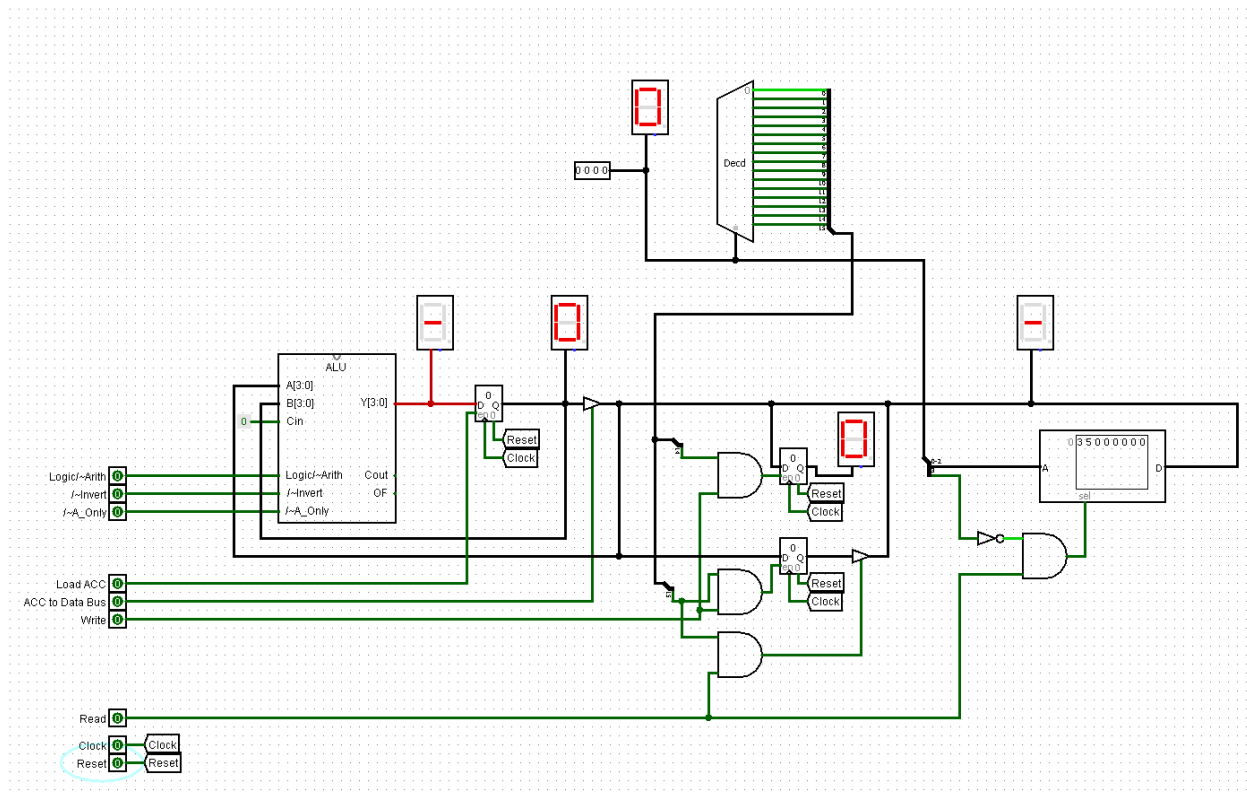
Task 4-5: Build the Brainless Central Processing Unit

Include a picture of your Logisim Brainless Central Processing Unit circuit here:



Task 4-6: Build the Brainless Microprocessor

Include a picture of your Logisim brainless microprocessor circuit here:



Task 4-7: Testing and Controlling the Brainless Microprocessor

Follow steps 1 through 3 outlined in the laboratory manual to test your brainless microprocessor circuit. It might be helpful to review the ALU Function Table from Sim lab 3. Table 3 is an example, for the ADD command, of how to fill out tables to record the values of the control lines during every clock cycle.

| Table 3 | |
|--|--------------------|
| Instruction [Add operand to Accumulator (ACC)] | |
| Control Line | Value |
| 4-bit Binary Keyboard (Address Bus) | Address of operand |
| Write | 0 |
| Read | 1 |
| ACC to Data Bus | 0 |
| Load ACC | 1 |
| /~A_Only | 1 |
| /~Invert | 1 |
| Logic/~Arith | 0 |

For all of the instructions you performed (i.e. Subtract, Load ACC, etc.) record the values of the control lines during every clock cycle in Table 4 and Table 5.

| Table 4 | |
|---------------------------------------|-------|
| Instruction [Load ACC with operand] | |
| Control Line | Value |
| 4-bit Binary Keyboard (Address Bus) | 0000 |
| Write | 0 |
| Read | 1 |
| ACC to Data Bus | 0 |
| Load ACC | 1 |
| /~A_Only | 0 |
| /~Invert | 1 |
| Logic/~Arith | 0 |
| | |
| Instruction [AND operand with ACC] | |
| Control Line | Value |
| 4-bit Binary Keyboard (Address Bus) | 0000 |
| Write | 0 |
| Read | 1 |

| | |
|--|-------|
| ACC to Data Bus | 0 |
| Load ACC | 1 |
| /~A_Only | 1 |
| /~Invert | 1 |
| Logic/~Arith | 1 |
| Instruction [Store ACC to RAM] | |
| Control Line | Value |
| 4-bit Binary Keyboard (Address Bus) | 1111 |
| Write | 1 |
| Read | 0 |
| ACC to Data Bus | 1 |
| Load ACC | 0 |
| /~A_Only | 0 |
| /~Invert | 0 |
| Logic/~Arith | 0 |
| Instruction [Subtract operand from ACC] | |
| Control Line | Value |
| 4-bit Binary Keyboard (Address Bus) | 1111 |
| Write | 1 |
| Read | 0 |
| ACC to Data Bus | 0 |
| Load ACC | 1 |
| /~A_Only | 1 |
| /~Invert | 0 |
| Logic/~Arith | 0 |

Describe any other tests that you performed. NOTE: the laboratory manual gives you a minimum set of items to test

| Table 5 | |
|--|-------|
| Instruction [Not (operand) to ACC] (1's complement) | |
| Control Line | Value |
| 4-bit Binary Keyboard (Address Bus) | 1111 |
| Write | 1 |
| Read | 0 |

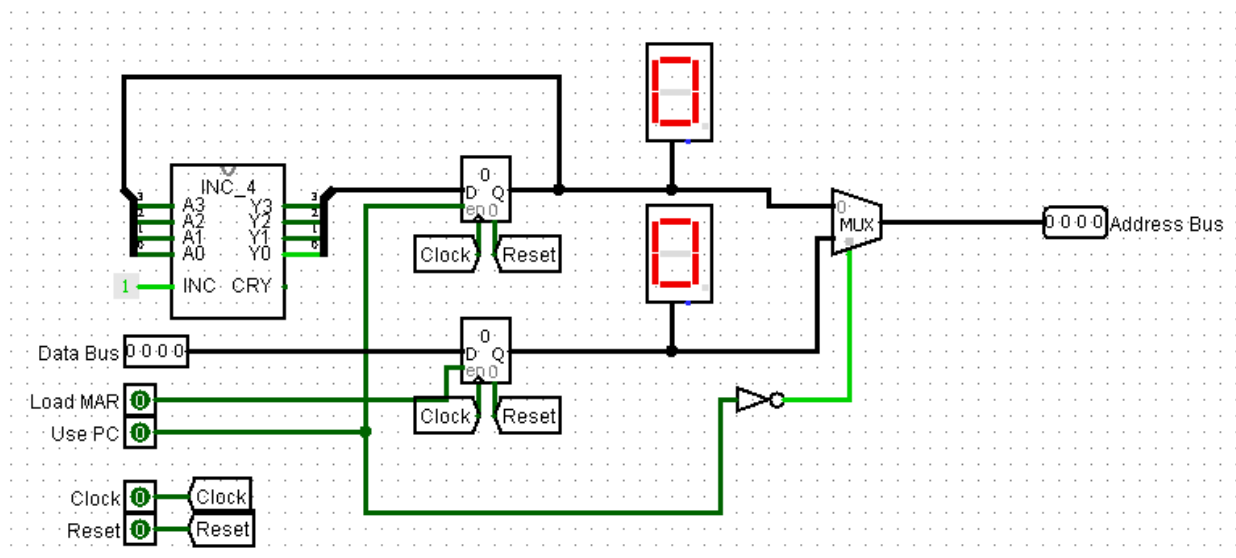
| | |
|--|-------|
| ACC to Data Bus | 0 |
| Load ACC | 1 |
| /~A_Only | 0 |
| /~Invert | 0 |
| Logic/~Arith | 1 |
| Instruction [Negate(operand) to ACC] (2's complement) | |
| Control Line | Value |
| 4-bit Binary Keyboard (Address Bus) | 1111 |
| Write | 1 |
| Read | 0 |
| ACC to Data Bus | 0 |
| Load ACC | 1 |
| /~A_Only | 0 |
| /~Invert | 0 |
| Logic/~Arith | 0 |

Why do you think the register at the output of the ALU is called the 'accumulator'?

It is where results of the ALU accumulate.

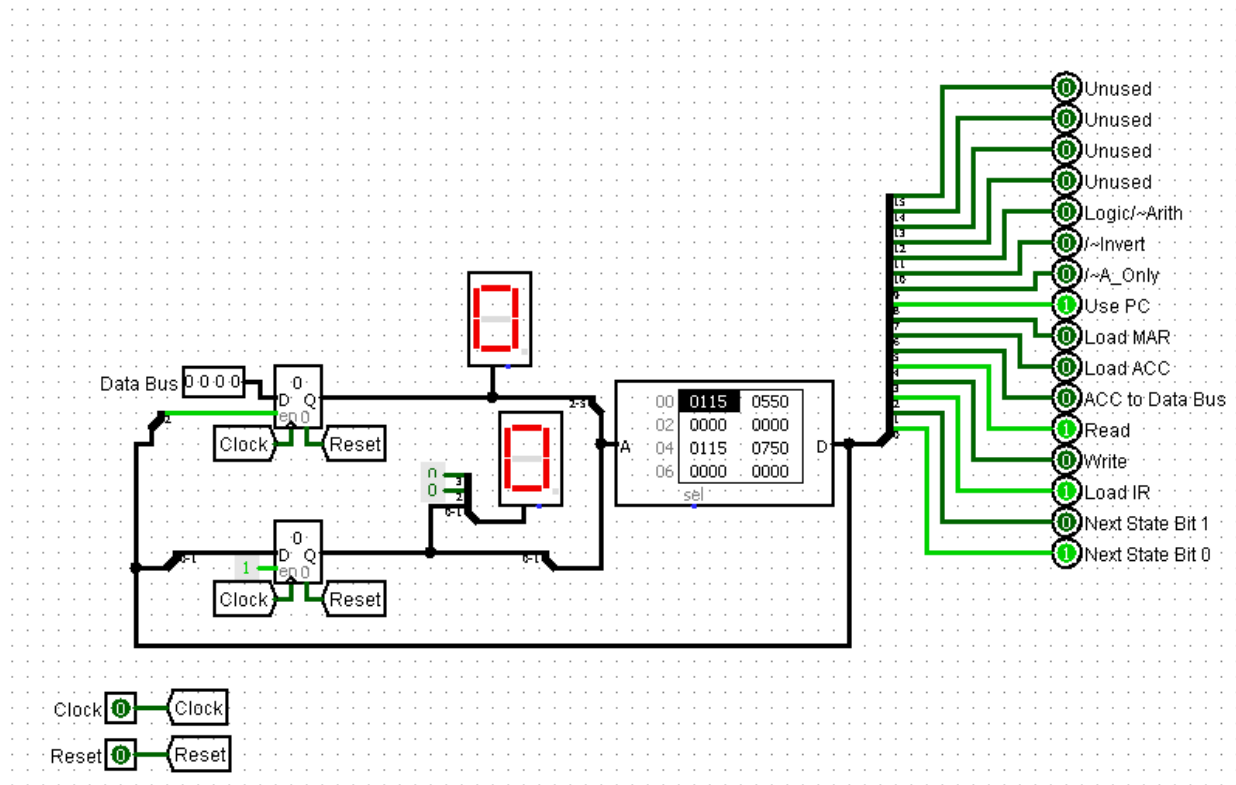
Task 4-8: Build the Memory-Address-Generation Circuit

Include a picture of your Logisim memory address generation circuit here:



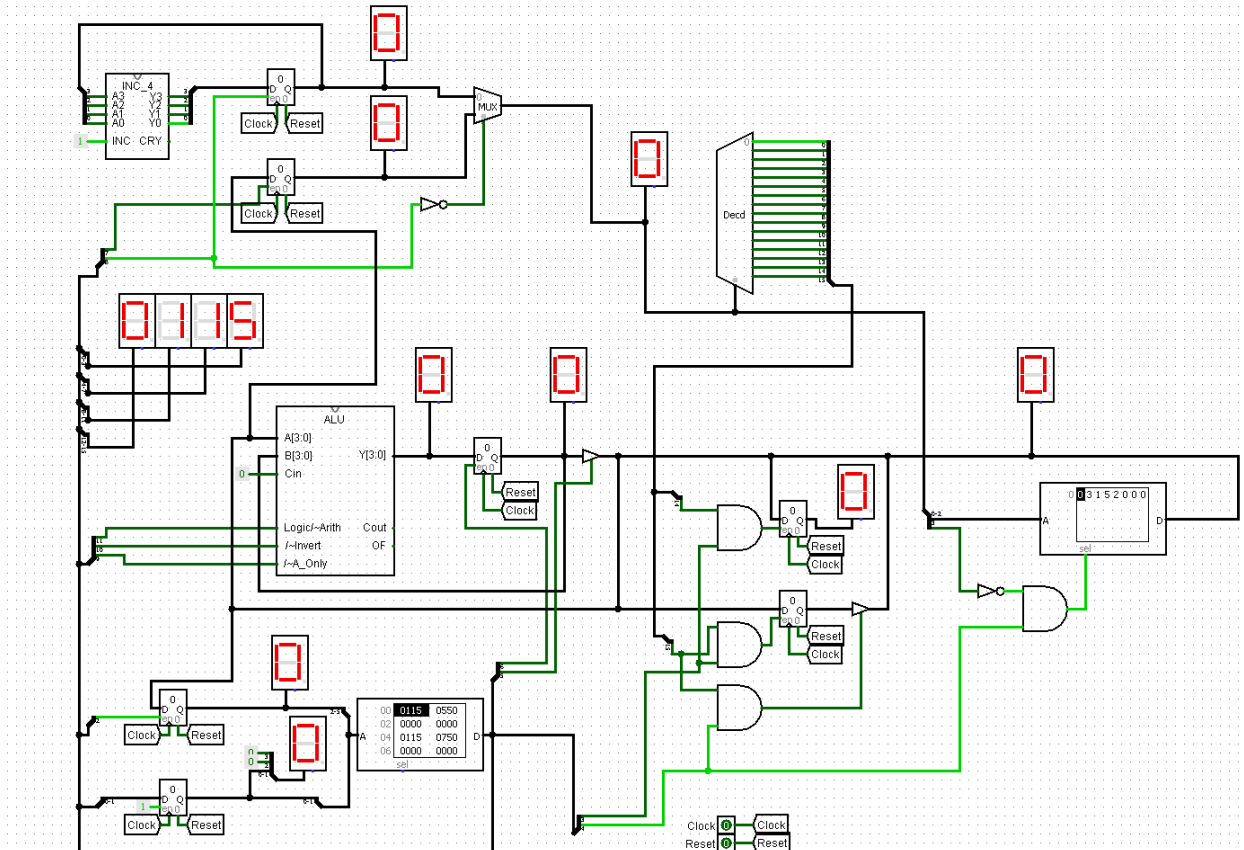
Task 4-9: Build the Controller Circuit

Include a picture of your Logisim controller circuit here:



Task 4-10: Build the Complete Microprocessor Circuit

Include a picture of your Logisim complete microprocessor circuit, with controller, here:



Task 4-11: Write and Execute a Simple Program for Your Microprocessor

Write the program given in your laboratory manual into the appropriate memory locations. Observe the operation of each step of your program (i.e. observe the values of the control lines and record whether data is being moved properly according to those control line settings). Did you get an 8 stored into the accumulator with you initial test?

If not, what error(s) did you find during your debugging process?

Yep! Worked on the first try.

Task 4-12: Add the 'AND', 'Zero', 'Subtract', and 'Store ACC' Instructions