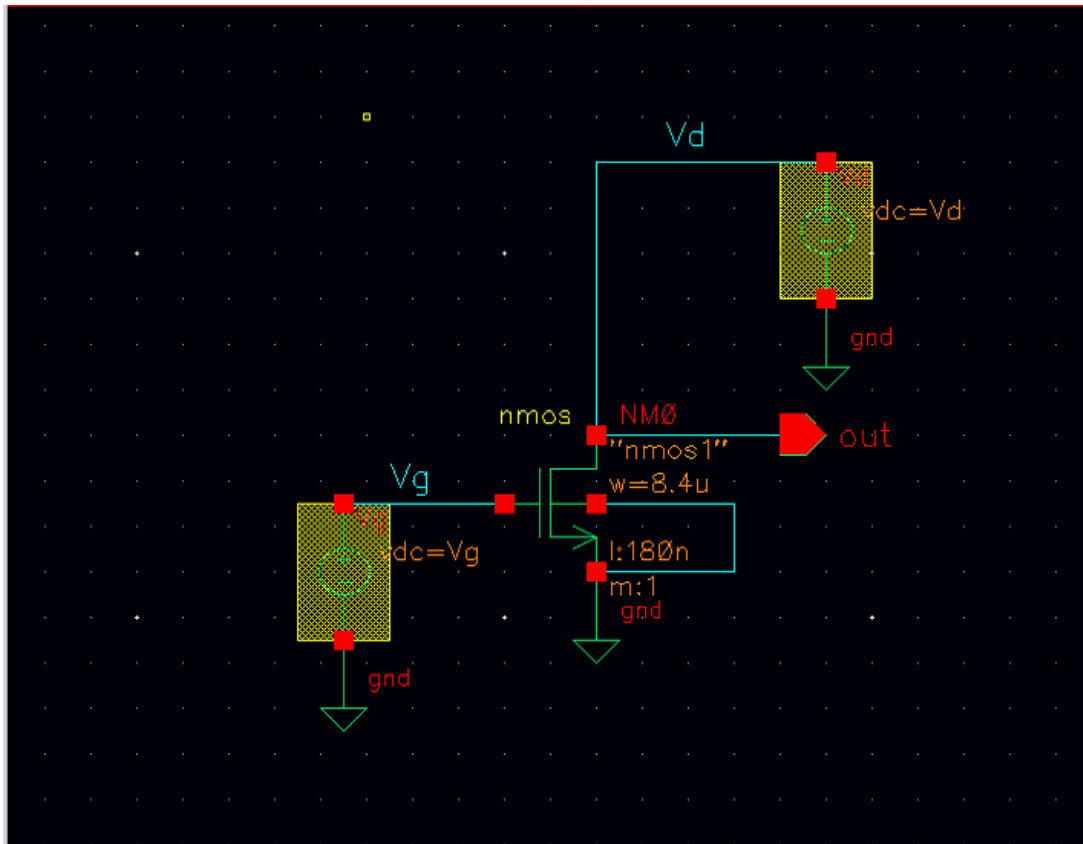


MOS Amplifier

Part 1: Checking the parameters of the nmos in gpdk 180nm file:



I created a schematic: check_param where I check the following parameters for Vdc sweep of 0 to 5 V and Vgs = 1, 2, 3, 4, 5V for different W/L ratios:

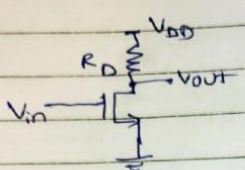
1. Threshold voltage: It is about 0.53V.
2. Drain Current
3. Transconductance (gm)
4. $U_n \cdot C_{ox}$ (I had a doubt as to whether $U_n \cdot C_{ox}$ is represented as Beff in cadence virtuoso)

I used this schematic as a reference for the other amplifiers in their DC operating point stage.

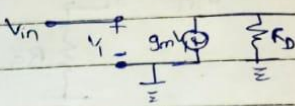
Part 2: Common source amplifier

PAGE No.
 DATE / /

Common Source



Small signal model →



$V_i = V_{in} \quad V_{out} = -g_m V_i R_D$
 $\therefore A_v = -g_m R_D$

The gain desired is $A_v = -5$.

$W = 2 \mu m \quad L = 180 nm$

$V_{gs} = 2V$ (DC operating point).

If $V_d = 2V$ then $g_m = 979.60 \mu S \quad \therefore R_D = 10^4 \Omega$

$\therefore W \rightarrow 0.98 \mu m$. (to reduce g_m). $(g_m \propto \frac{W}{L})$

For $\frac{W}{L} = \frac{0.98 \mu m}{180 nm}$ we need $V_d = 1.9V$ to $2V$.

→ We need $V_d = 1.9V$ to $2V$.

At $V_{ds} = 2V \quad V_{gs} = 2V \rightarrow i_d = 0.71768 mA$

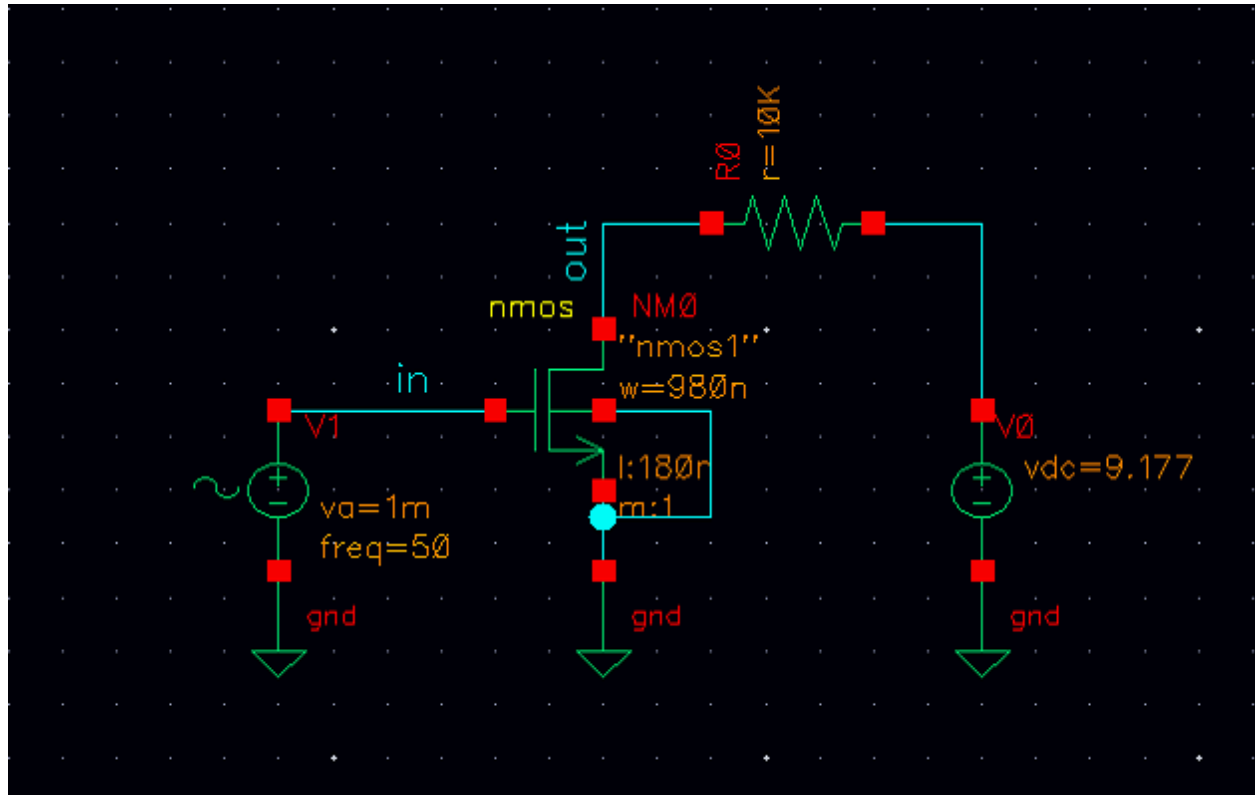
$\therefore V_{dd} = V_d + i_d R_D = 2 + 0.71768 \times 10 = 9.1768V$

Input signal : 1mV sine signal of frequency 50Hz.

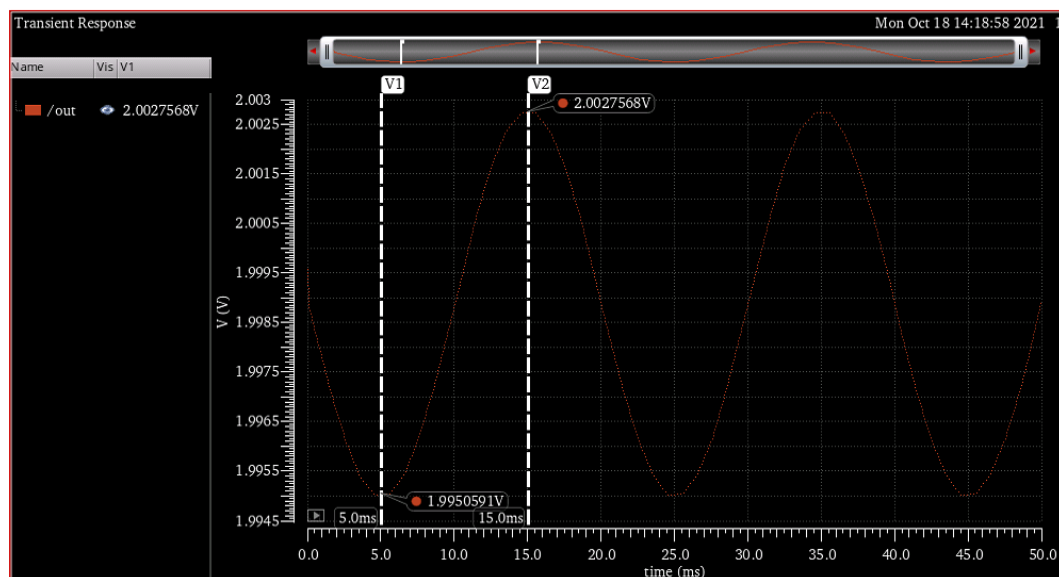
Here in this circuit, I made the error of not taking frequency into consideration. This is why I am getting a gain of 4 instead of 5, which I wanted. The same mistake was made for the common gate amplifier (where I took a small signal frequency of 1KHz). This

mistake is rectified for the common drain amplifier where I took a frequency of only 50Hz. And later on corrected for all of the other amplifier circuits.

Circuit and Plot:



Output:

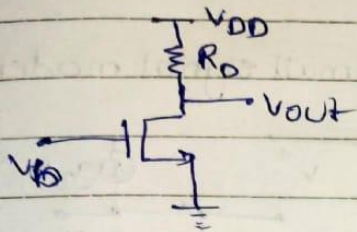


Part 3: Common gate amplifier

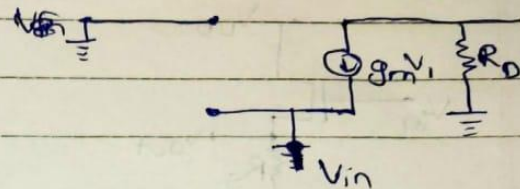
Required Drain at DC: 0.8 V/V

Input signal : 1mV sine signal of frequency 50Hz.

Common gate \Rightarrow



Small signal model



DC operating point $\Rightarrow V_{GS} = 2V$

$$V_{DS} = 2V$$

$$\frac{W}{L} = \frac{2 \mu m}{180 nm}$$

$$V_s = -v_{in}$$

$$v_{out} = -g_m v_s R_D$$

$$A_v = +g_m R_D$$

$$A_v = +g_m R_D \quad A_v = +5 \text{ (required)}$$

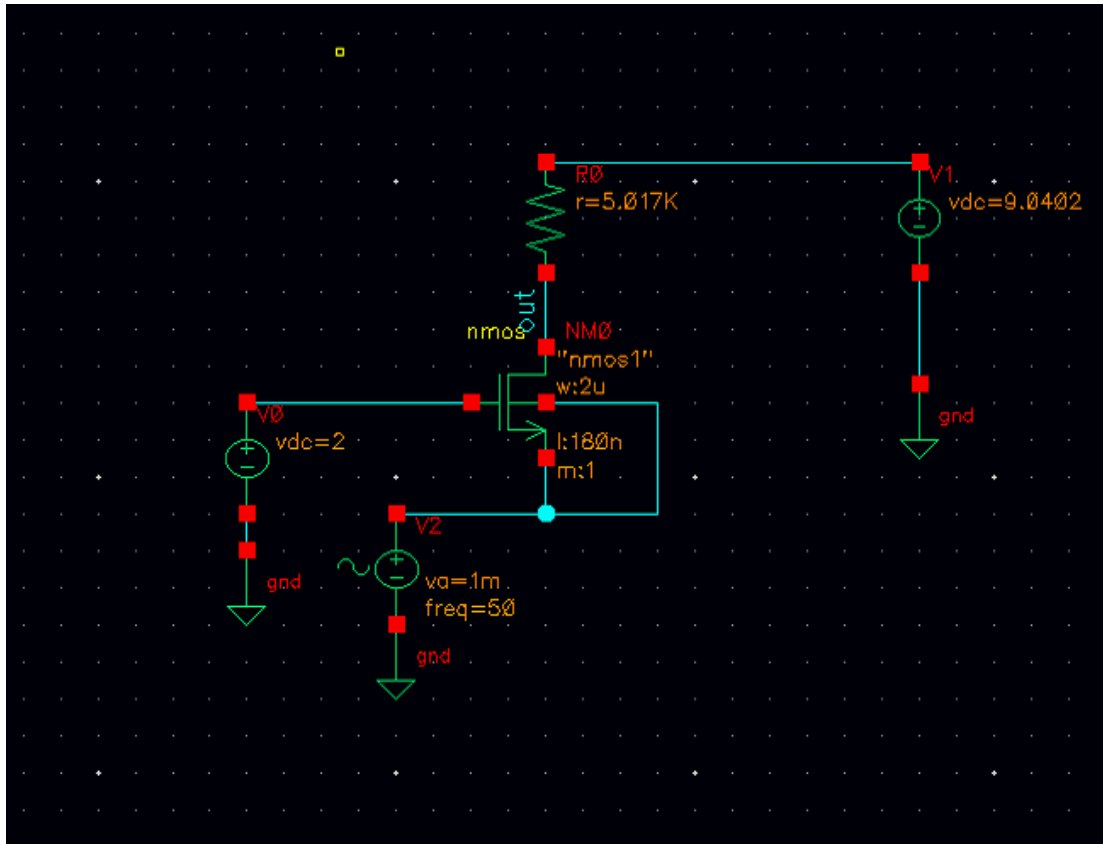
At above DC operating point $\Rightarrow i_d = 1.4031 mA$

$$\hookrightarrow g_m = 996.49 \mu S$$

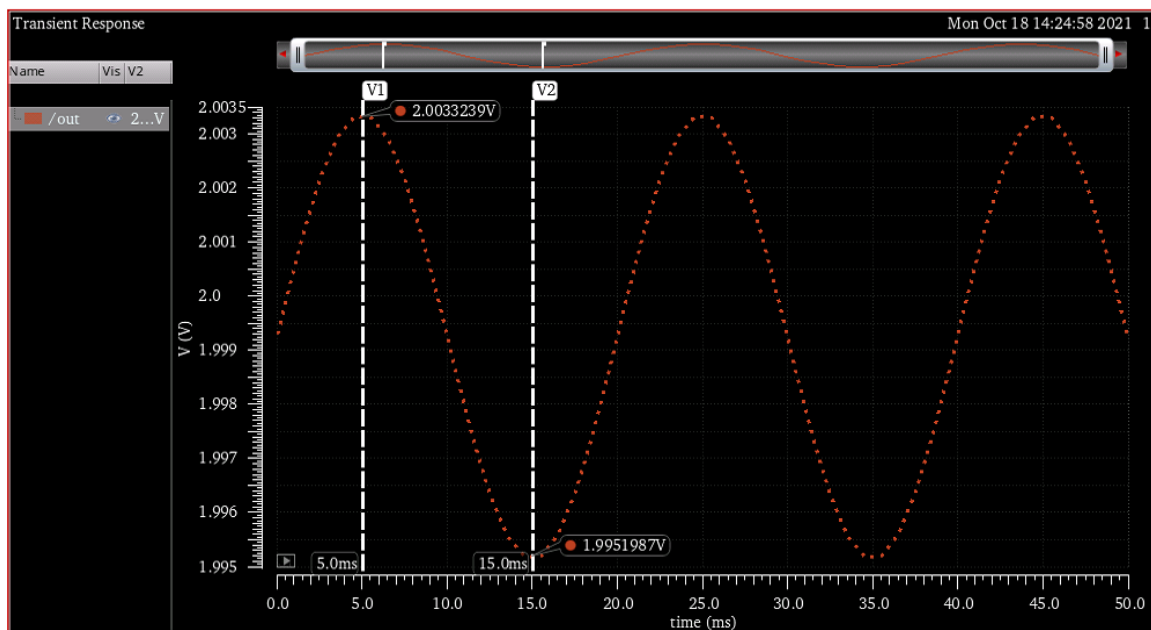
$$\therefore R_D = \frac{5}{i_d} = 5017.6 \Omega$$

$$\therefore \text{required } v_{dd} = v_d + i_d R_D = 9.0402 V$$

Circuit:



Plot of Output:



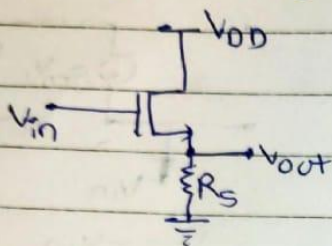
Part 4: Common drain amplifier:

Required Drain at DC: 0.8 V/V

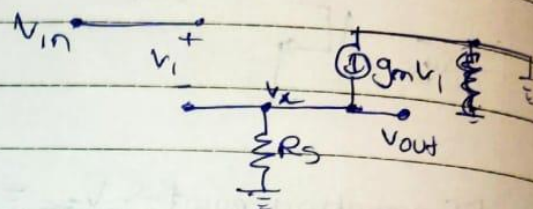
Input signal : 1mV sine signal of frequency 50Hz.

Common Drain \rightarrow

Aiming for a gain of 0.8 V/V.



Small signal model



$$\frac{g_m R_S}{1 + g_m R_S} = 0.8$$

$$\therefore g_m R_S = 4$$

$$\text{At } \frac{W}{L} = \frac{2 \mu\text{m}}{180 \text{ nm}} \rightarrow g_m = 1 \text{ mS}$$

\therefore We need 4-times higher W/L . (if R_S is fixed at 1Ω)

$$\therefore \frac{W}{L} = \frac{8.4 \mu\text{m}}{180 \text{ nm}}$$

\rightarrow DC operating point $V_{GS} = 2\text{V}$

$$V_D = ? = V_{DD}$$

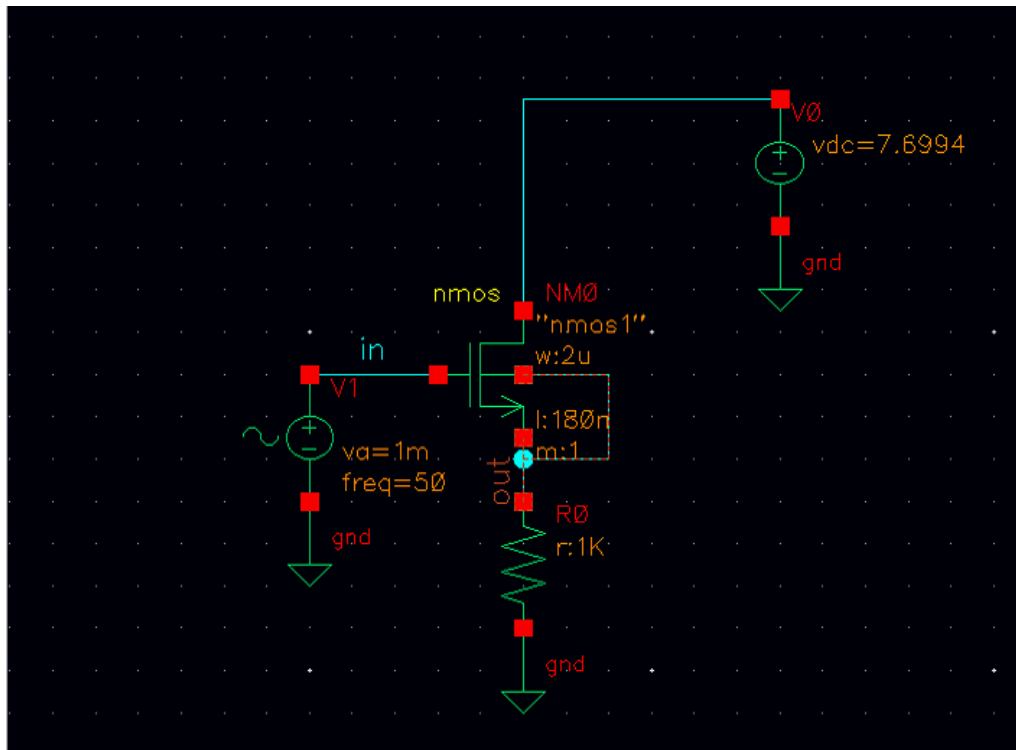
$$V_{DS} = 2\text{V}$$

$$\therefore \text{For } V_{DS} = 2\text{V} \rightarrow g_m \rightarrow 4 \times 10^{-3} \text{ S}$$

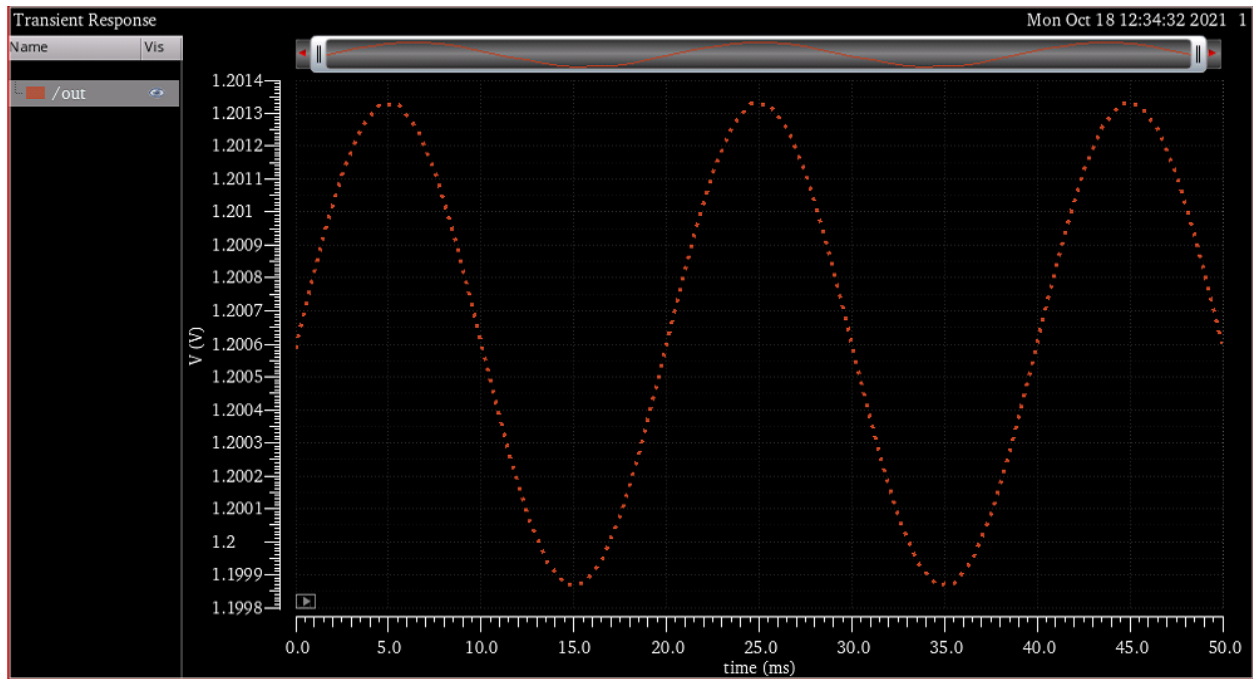
$$\rightarrow I_{DS} \rightarrow 5.6944 \text{ mA}$$

$$\therefore V_{DD} = V_{DS} + I_D R_S = 2 + 5.6944 \times 1 = 7.6944$$

Circuit:



Plot:



We have a gain of 0.8 with voltage swing of 0.8mV.