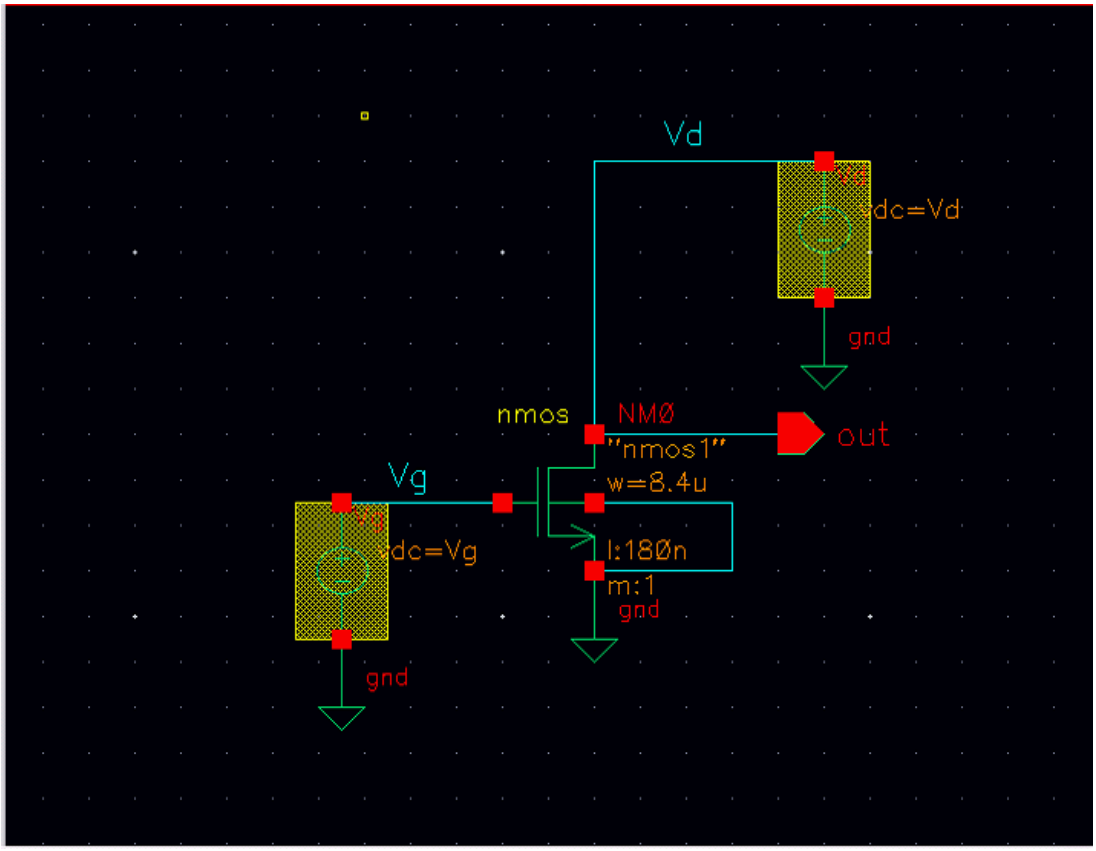
MOS Amplifier

Part 1: Checking the parameters of the nmos in gpdk 180nm file:

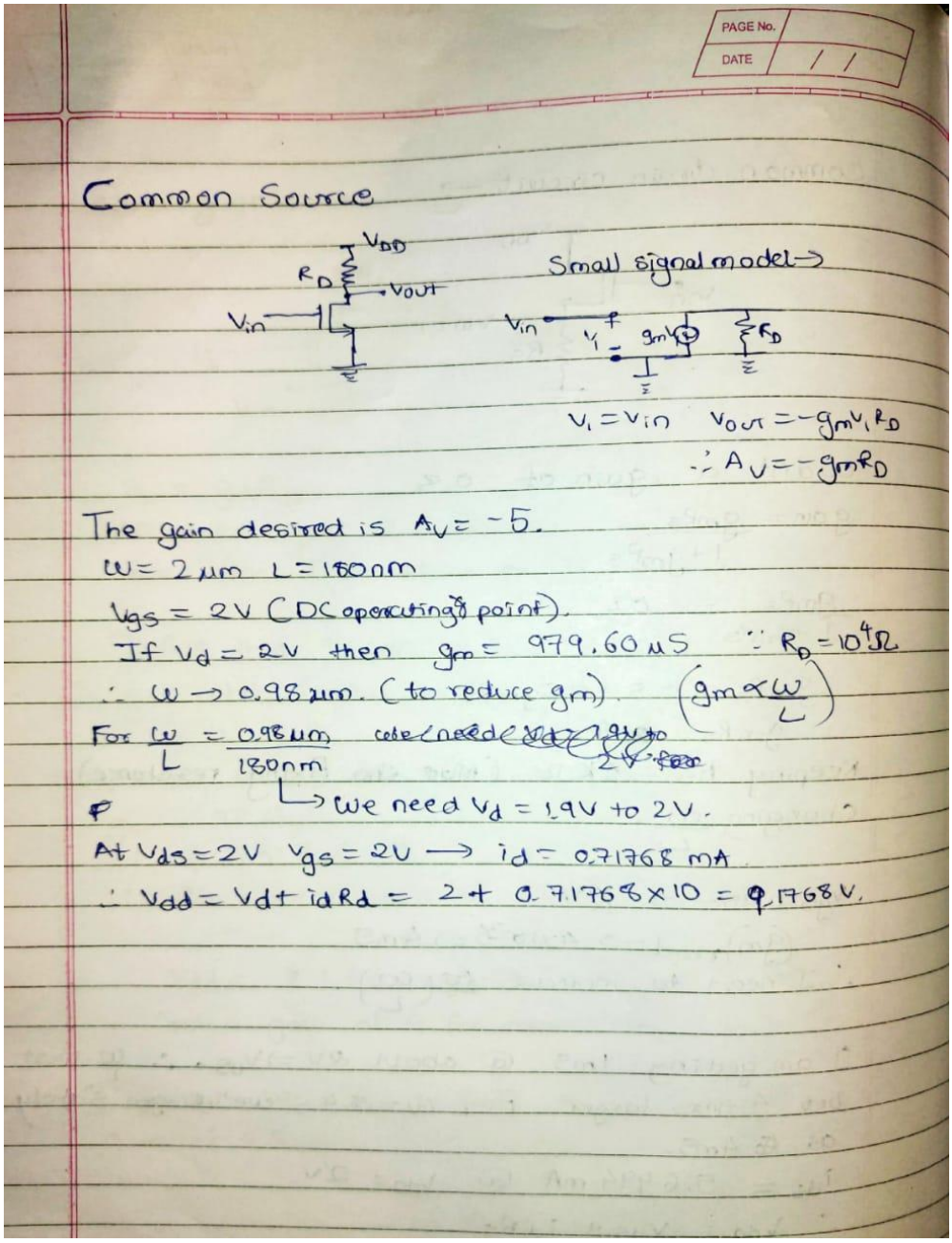


I created a schematic: check_param where I check the following parameters for Vdc sweep of 0 to 5 V and Vgs = 1, 2, 3, 4, 5V for different W/L ratios:

1. Threshold voltage: It is about 0.53V.
2. Drain Current
3. Transconductance (gm)
4. U_n*C_ox (I had a doubt as to whether U_n*C_ox is represented as Beff in cadence virtuoso)

I used this schematic as a reference for the other amplifiers in their DC operating point stage.

Part 2: Common source amplifier

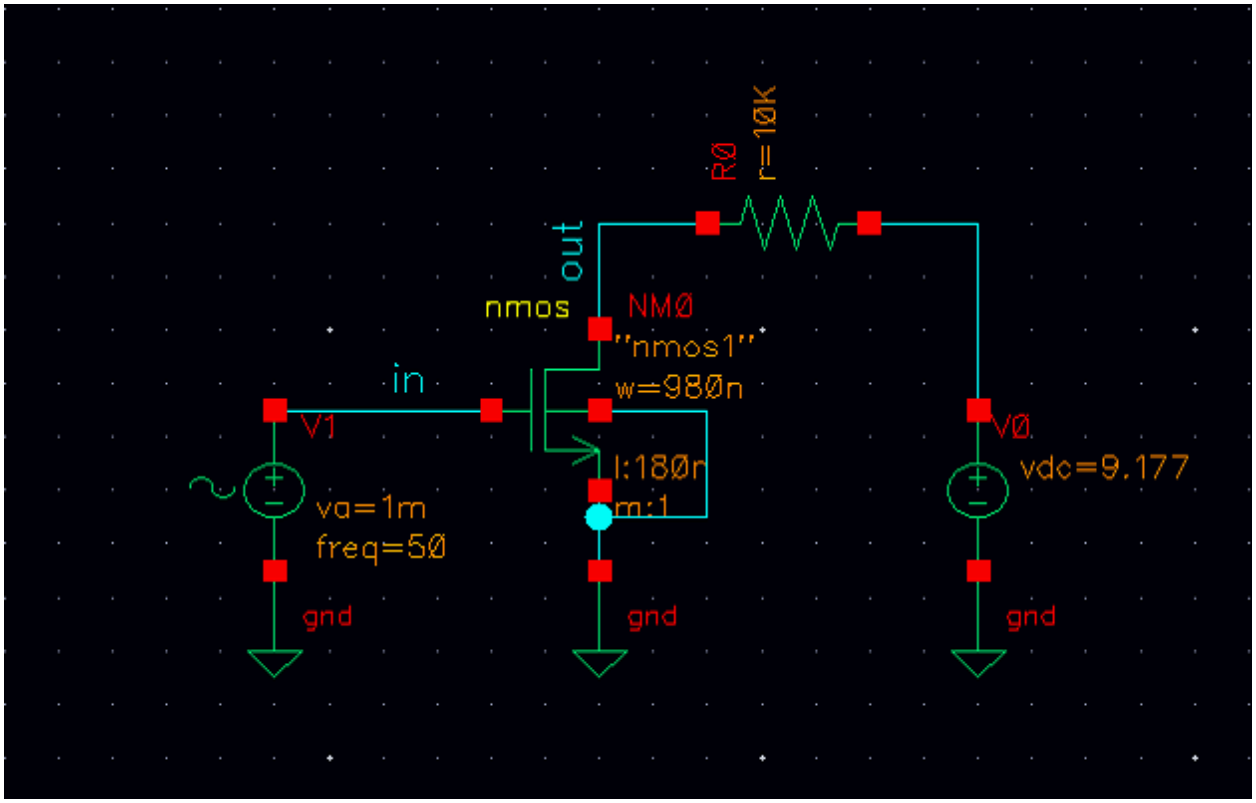


Input signal : 1mV sine signal of frequency 50Hz.

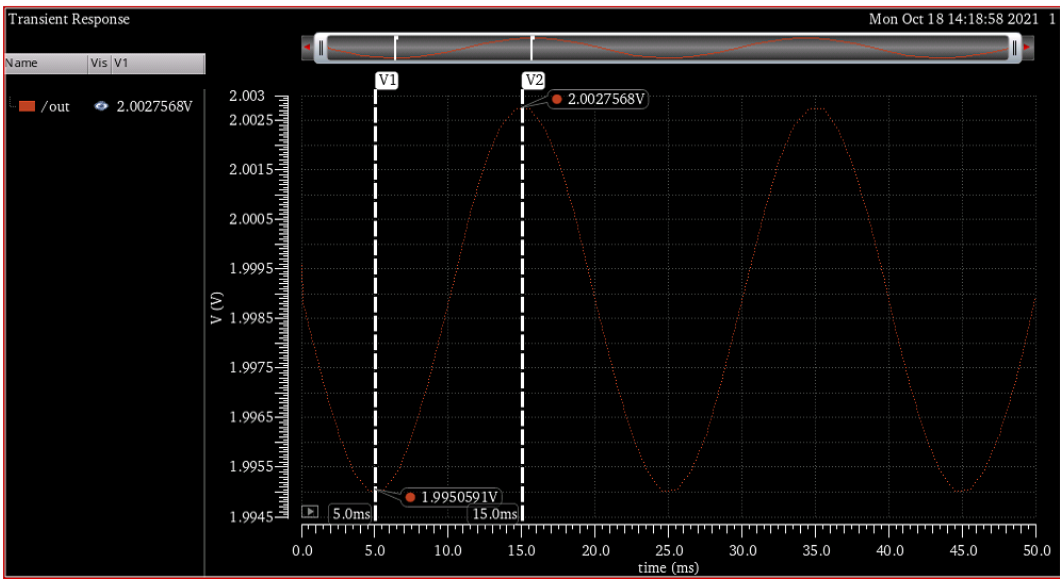
Here in this circuit, I made the error of not taking frequency into consideration. This is why I am getting a gain of 4 instead of 5, which I wanted. The same mistake was made for the common gate amplifier (where I took a small signal frequency of 1KHz). This

mistake is rectified for the common drain amplifier where I took a frequency of only 50Hz. And later on corrected for all of the other amplifier circuits.

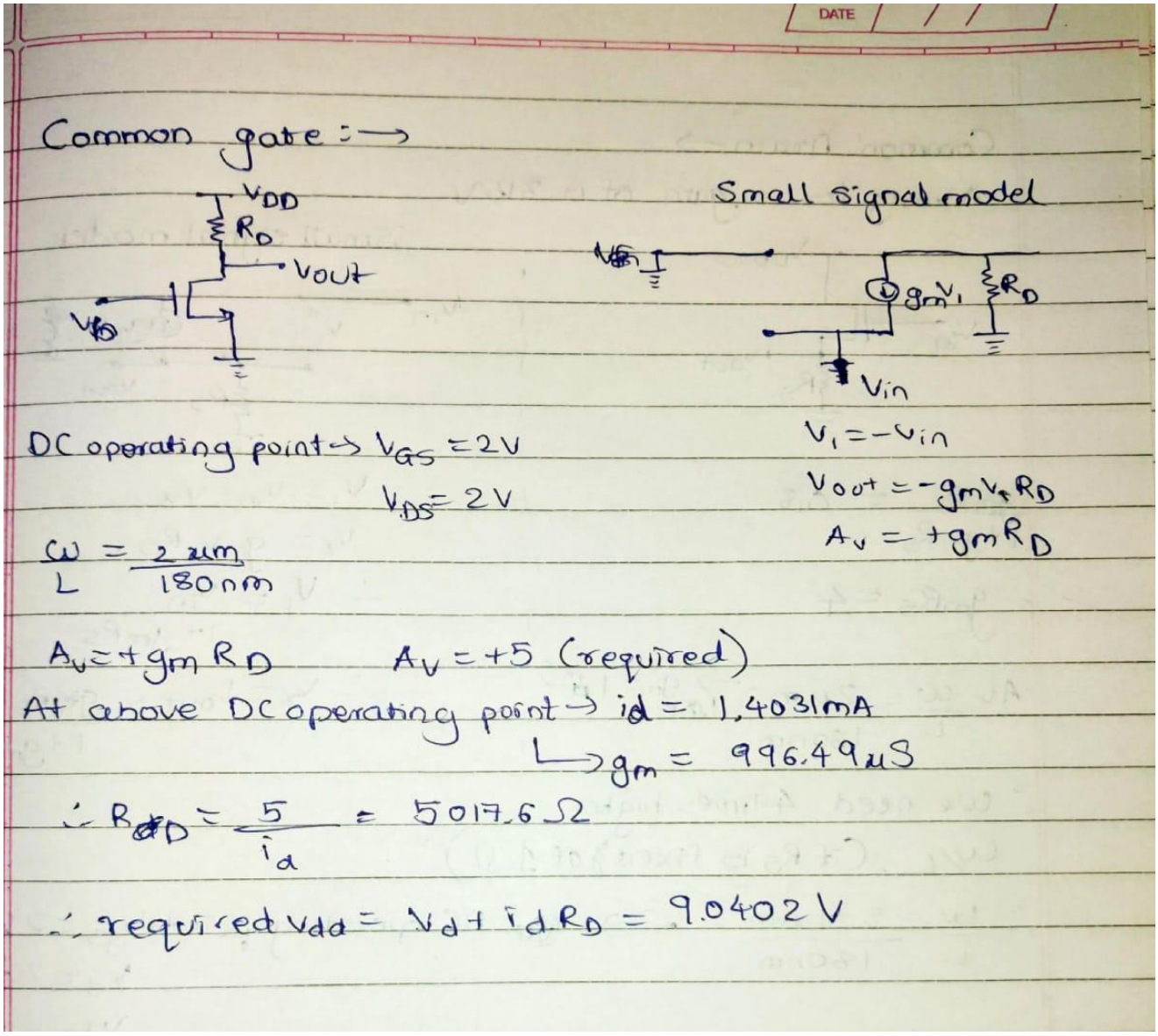
Circuit and Plot:



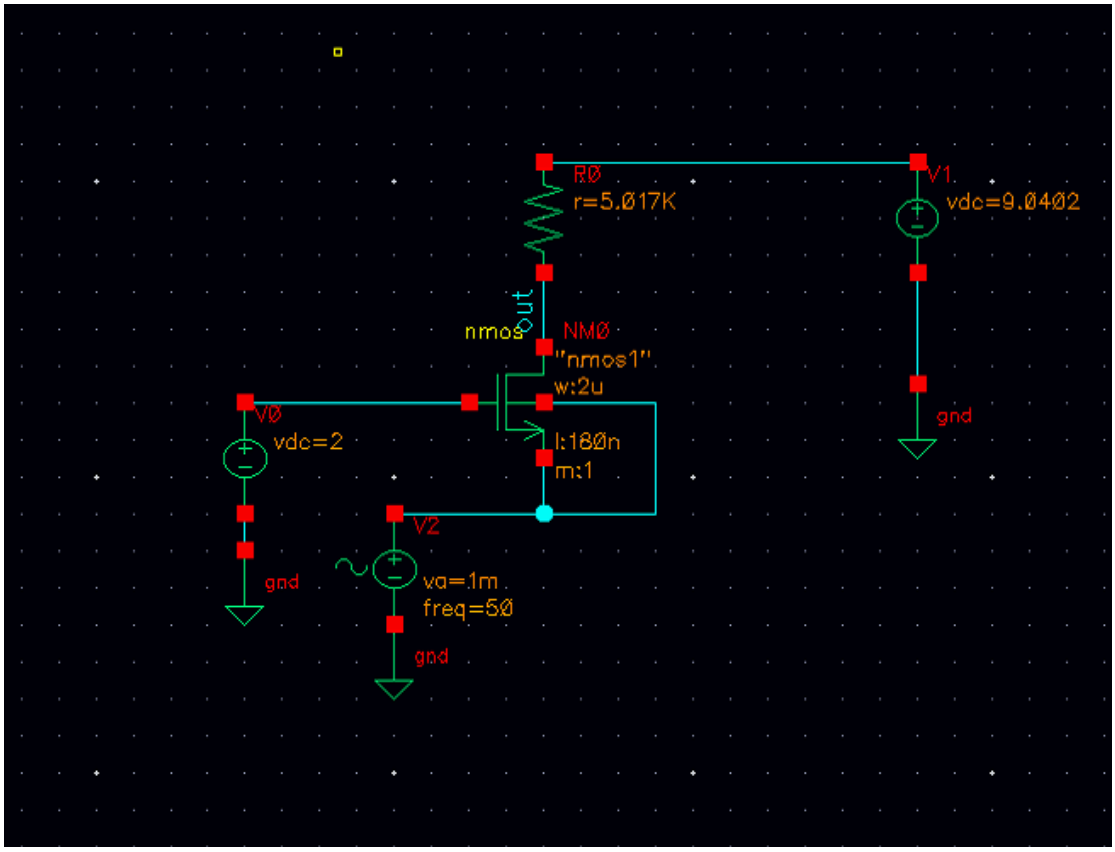
Output:



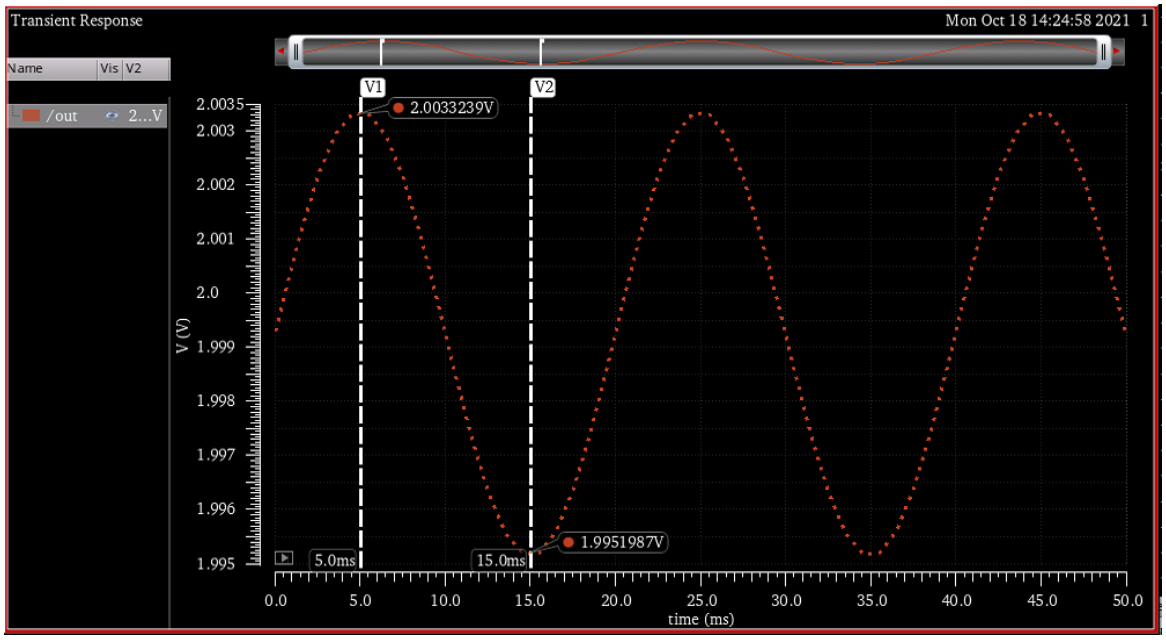
Part 3: Common gate amplifier
Required Drain at DC: 0.8 V/V
Input signal : 1mV sine signal of frequency 50Hz.



Circuit:



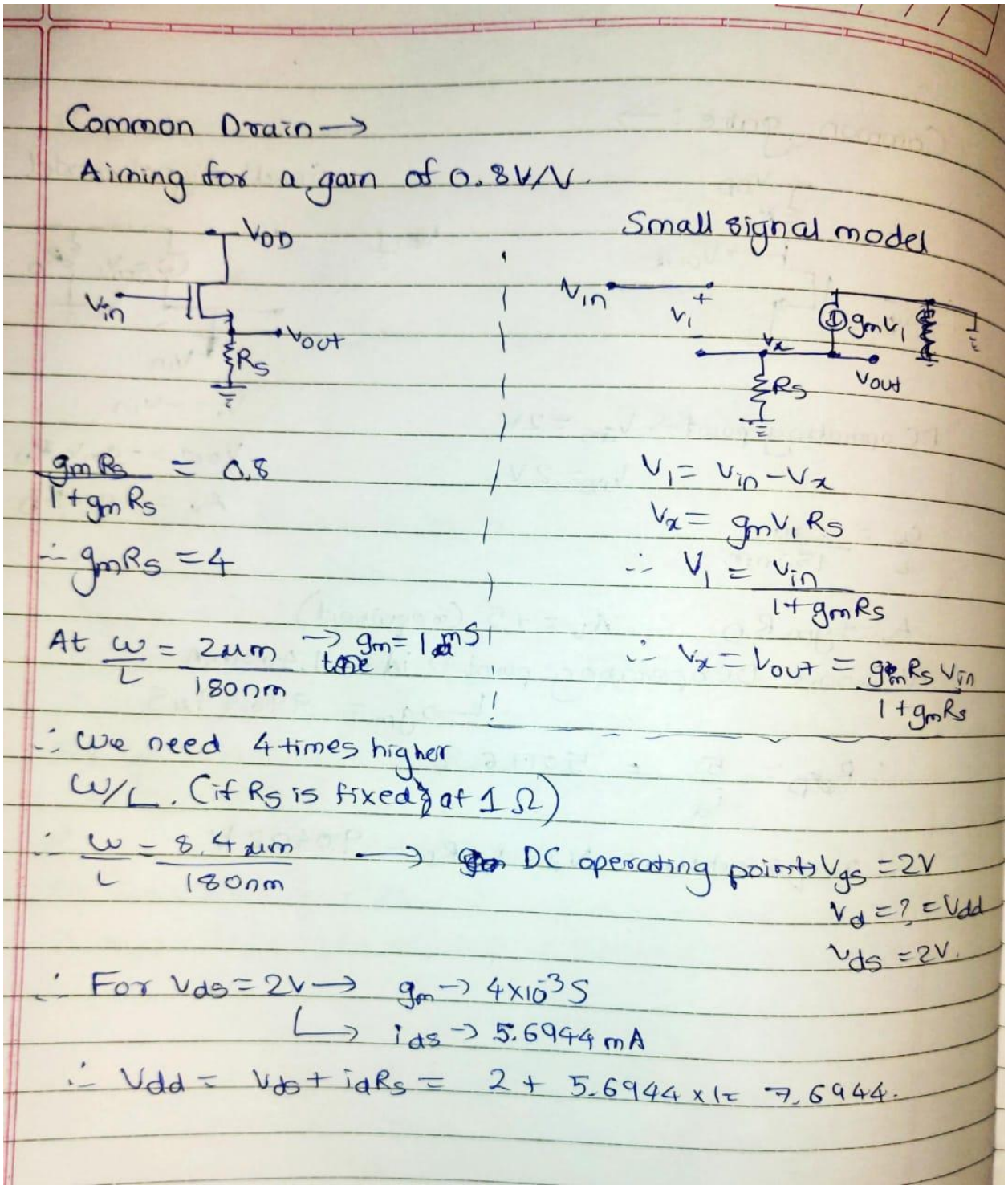
Plot of Output:



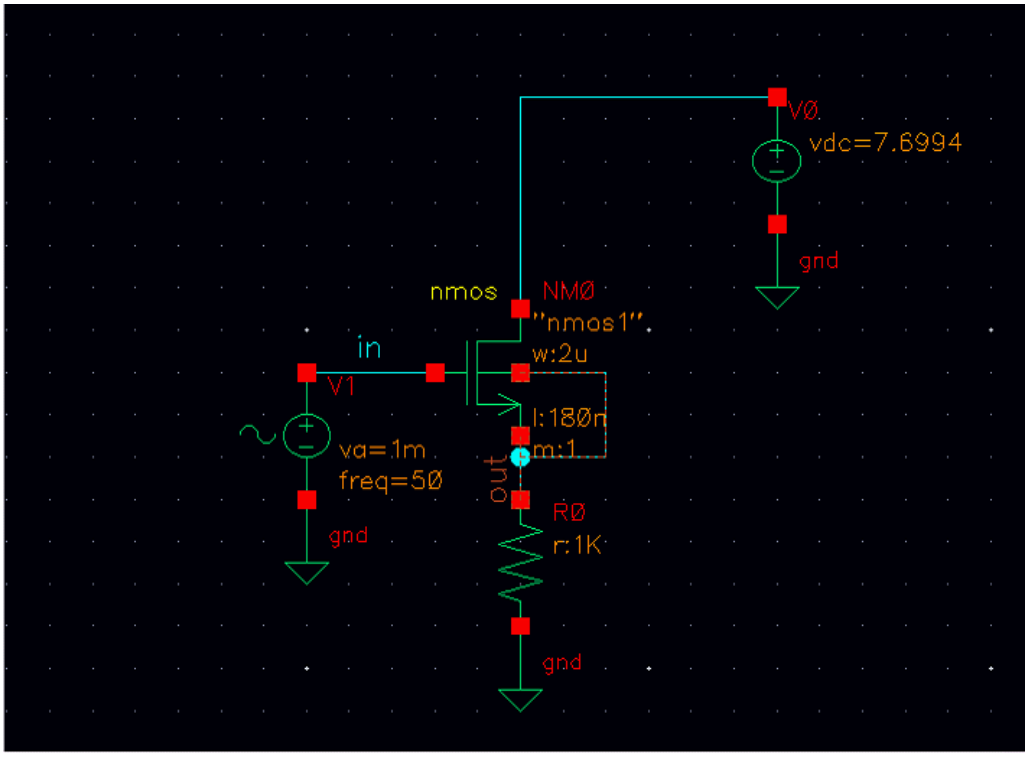
Part 4: Common drain amplifier:

Required Drain at DC: 0.8 V/V

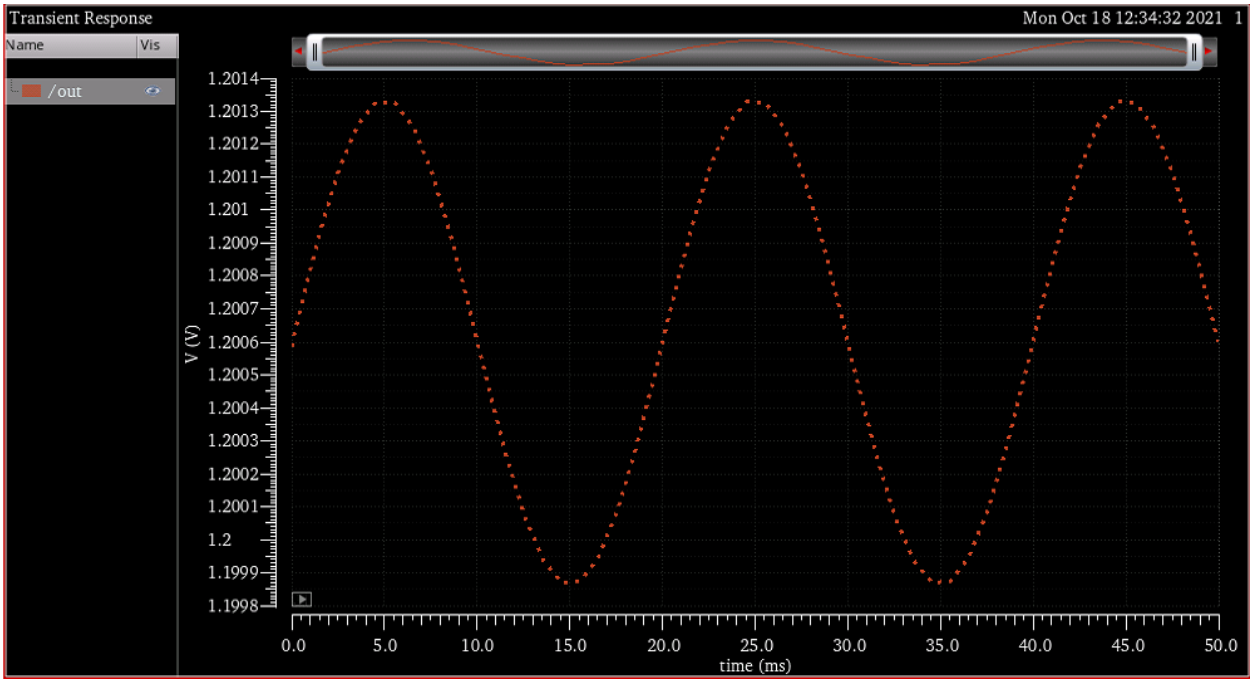
Input signal : 1mV sine signal of frequency 50Hz.



Circuit:



Plot:



We have a gain of 0.8 with voltage swing of 0.8mV.