

ANISH KUMAR SHARMA

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Objective

I would like to be a part of an organization where I could contribute and enhance my knowledge and hone my talents for the development of both the organization and myself.

Technical Experience:

- Working for Processware system as Design and Verification Engineer 15'Feb,2021.
- 3.5 year of experience working SMDPC2SD as Design and Verification/SoC (1'Aug,2017-30'Jan,2019 with NIT Delhi) (1'Feb,2019-11'Feb,2021 with IIT Roorkee).
- 5 year of experience working with ITM Gurgaon as a Lab Engineer in VLSI/Embedded lab for developing projects.(31,May 2012-31,June 2017).

Technical Skills

- Vivado Software for FPGA logic design, synthesis, and bit stream generation.
- Knowledge of Git for Project Management.
- Work on aldec tool dedicated to avionics std DO-254, FPGA Design and Verification(Active_HDL,Alint_Pro).
- Knowledge of DO-254.
- Knowledge of Hardware Development Cycle document like PHAC, HCMP,HCS,HRS etc.
- Knowledge of TCL script for Design Compiler gen. netlist and set constrain for design.
- Work on full and semicustom layout design for area reduction on diff. tech node.
- Designing FSM asic. Vivado Software for FPGA logic design, synthesis, and bit stream generation.
- Knowledge of full flow till GDSII Tapout(Analog/Digital) .

Technical Language

- Hands on experience in Verilog Coding and Test Bench Design.
- Knowledge of C and C++ ,Python programming language.
- Good knowledge of Oop's concept.
- Good in RTL Digital design.
- Work with embedded soc (ardino, raspberry pi, Tiva C Series Arm4).

Career Summary

- Attended a workshop VLSI Design Tool at IISC Bangalore “Full ASIC Mix Tap-Out” June'2019.
- Attended a workshop VLSI Design Tool at NIT Delhi “Layout Design” Feb' 2018.
- Hand on experience on Layout design DRC, LVS, QRC extraction and Post Layout simulation on Cadence Virtuoso tool.
- Hand on experience on basys-3 board for FPGA logic design, synthesis, implementation and bit-stream generation.
- Hand on experience on spartan-6 board for FPGA logic design, synthesis, implementation and bit-stream generation.

Education

2005-2008	Diploma in Electrical Engineering from SBCMS Poly. Punjab state board of technical education and training, Chandigarh. with 73.14%
2008-2012	B.Tech. in Electrical Engineering from Chitkara College, Chandigarh with 67.8%
2013-2016	M-Tech in Embedded/VLSI from NCU University Gurgaon With 7.33 CGPA

References

- Karan Kumar
Processware System
Design and Verification Engineering
9958493432
- Somit Sharma
IIT Roorkee
Lab Engineer
9849197704
- Nittin
Entuple Technologies
Application Engineer
8130992206

Place: Delhi
Date: July' 2021

Anish Kumar