

## EE593 : Low Power VLSI Design

### GCD Processor Design

## GCD Calculator Design

Design a 16-bit GCD calculator. The top module is as follows.

```
module gcd(  
    input clk,    // System clock  
    input reset,  // To reset the GCD calculation  
    input start,  // To start the GCD calculation  
    input [15:0] A, B // Inputs A, B  
  
    output ready, // ready to take next inputs  
    output [15:0] result, // GCD result  
);
```

- The GCD calculator, calculate the GCD of two 16-bit numbers.
- Depending on the range of values, the number of iterations may vary.
- Upon completion of the calculation, you should be known about the result is ready.
- You should have an input signal to start the computation for next round of GCD calculation.

## GCD Processor Design

The GCD inputs should be loaded into a FIFO (*FIFO\_A*, *FIFO\_B*) and the result should be loaded into another FIFO (*FIFO\_result*) as shown in Figure 1. The FIFO size can be any value (8, 16 etc). The GCD calculator should take inputs from two input FIFO and the result should be available in output FIFO.

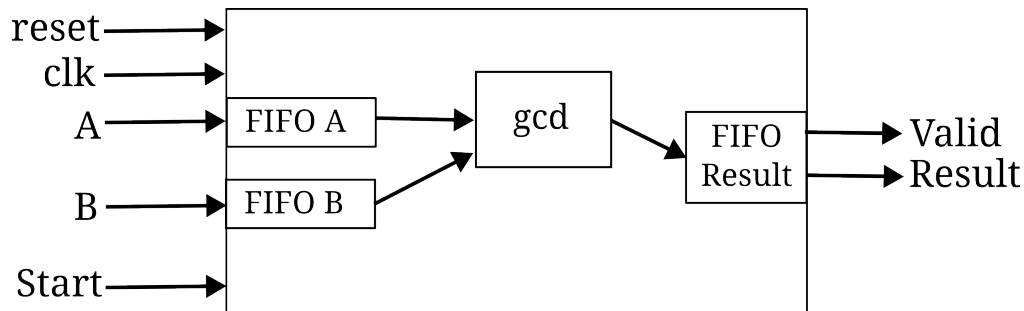


Figure 1: GCD Processor Block Diagram

When ever a new data comes for calculating GCD, the data can be loaded into FIFO. The calculation of the GCD can be started whenever the GCD circuit is free.

**Note:**

- You can make your own assumptions.
- If required create extra control signals.
- The code should be synthesised properly.
- You can create extra blocks, if required.

Write test bench for gcd, and gcd processor modules. Check the functionality of these modules and do synthesis to estimate the area, delay and power. **Submission:**

1. Prepare a report (in latex) and submit a pdf in Moodle. Keep a clear simulation plot and RTL schematic (to show blocks used in the design) in report.
2. Draw a table with values of results of your internal registers to show the GCD calculation of 27 and 15. Include cycle number as well in the table.
3. Submit your codes in Moodle.
4. Synthesize the code and prepare area, delay and power reports. Study and comment on the power, area and delay values.

*Extra marks will be given to those who present results and justifications effectively through plots and tables.*

**Marks - 50**