Implementation of Sense Amplifier

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I. Abstract

In this report we have and design and simulated the positive edge-triggered register based on sense amplifier. Setup time, hold time and propagation delay was calculated using EDA tool Cadence virtuoso spectre.

Index Terms = PMOS, NMOS , propagation delay, analoglib, TSMCn65, Mask, Via, Layout, DRC.

II. Introduction

We use technique that uses a sense amplifier structure to implement an edge-triggered register that is called as Sense Amplifier. Sense-amplifier circuits accept small input signals and amplify them to generate rail-to-rail swings. As we will see, sense amplifier circuits are used extensively in memory cores and in low swing bus drivers to amplify small voltage swings present in heavily loaded wires.

There are several approaches for building these amplifiers, with one popular approach being the use of feedback (e.g., cross-coupled inverters). Figure 1 depicts a design that employs a pre-charged front-end amplifier to sample the differential input signal on the rising edge of the clock signal.

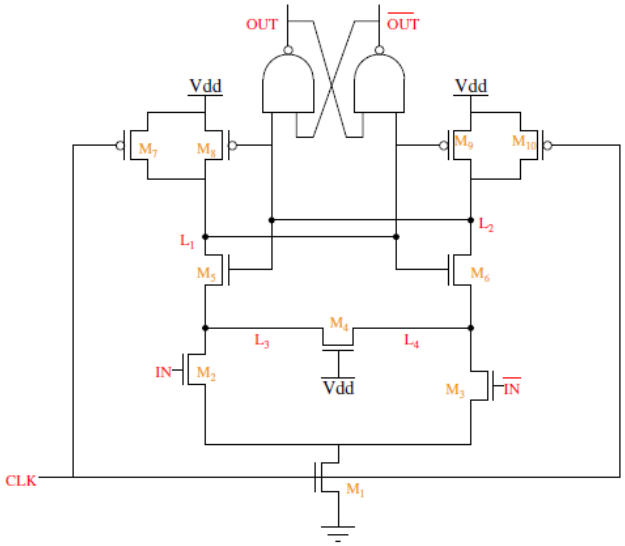

Fig. 1: Positive edge-triggered register based on sense-amplifier.

The main aim of the register or a latch is to store the data. The sense amplifier circuits accept small input signals and amplify them to generate rail-to-rail swings alike from degrading the signal and producing a false value. In the circuit depicted in the image, a front-end amplifier samples the differential input signal on the clock signal's rising edge. The SR flip flop receives the outputs from the front-end circuit and holds the data there while ensuring that the outputs only switch once every clock cycle.

The main objectives covered in this experiment are

- Implement Sense Amplifier design in cadence.
- Do the sizing and optimize the design.
- Performing the transient analysis to find the setup and hold times.
- Make a layout for our design.

III. Working and Construction

Construction of PDN in psedo nmos logic is same as in CMOS logic but in PUN there is only one PMOS which is grounded.

A. Schematic of Sense Amplifier based register:-

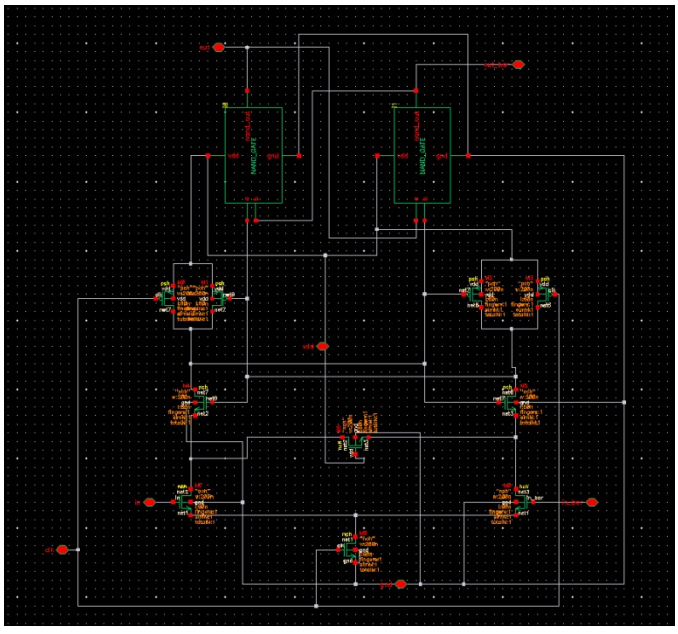

Fig. 2: Sense Amplifier design.

B. Test Bench of Sense Amplifier based register:-

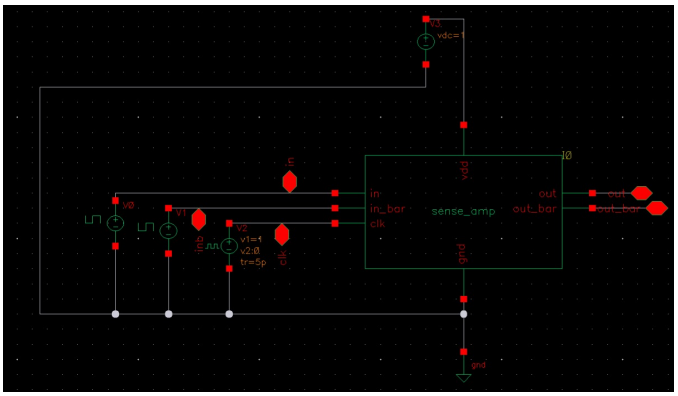

Fig. 3: Testbench of Sense Amplifier

IV. The Simulation Results and Discussions

A. Transient analysis of the 28T FA:-

By simulating the circuit using the given bit sequence, we the the following results .

Inferences:

• From the schematic we can observe that the design consists of an amplification circuit cascaded with an SR flipflop.
• The swing of the results is from 400nV to 500mV.
• The setup time is of 8.1ns which is the time for which the data must be stable before the clock trigger.
• The sizing of the PMOS are made 2.2 times that of NMOS. So the width of NMOS and PMOS remains 200nm and 440nm respectively.
• There is a difference in swing of the input and input.

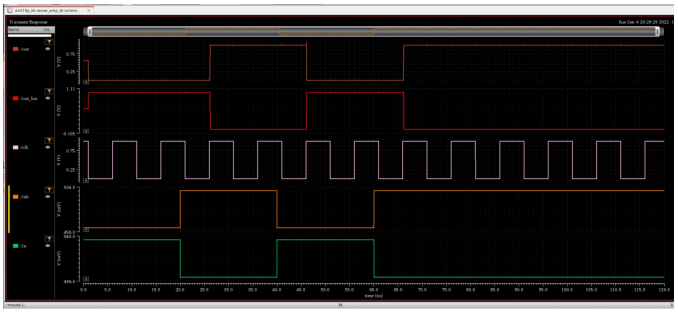

Fig. 4: Transient analysis results

B. Setup Time:-

Setup time achieved is negative.

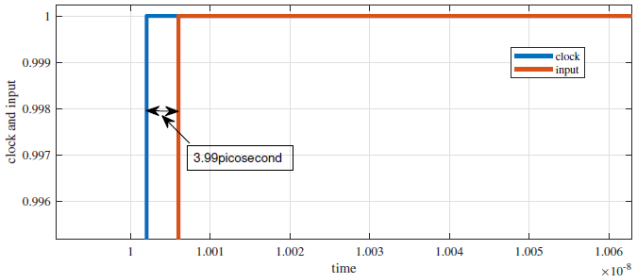

Fig. 5: Setup Time for register

C. Propagation Delay:-

The calculation of propagation delay is done from the graph shown below:
tpHL = 10.0584ns - 10.0015ns = 0.0569ns
tpLH = 20.04ns - 20.0015ns = 0.0384ns
therefore
tp = 47.7ps

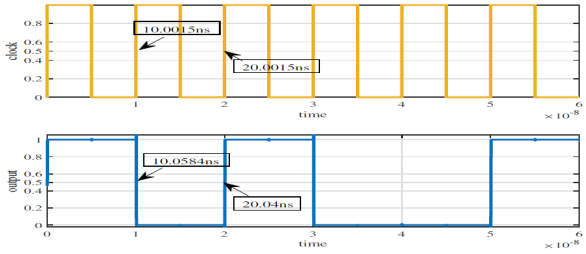

Fig. 6: Propagation delay for register

V. Layout and Packaging

The layout for the design is made as follows:

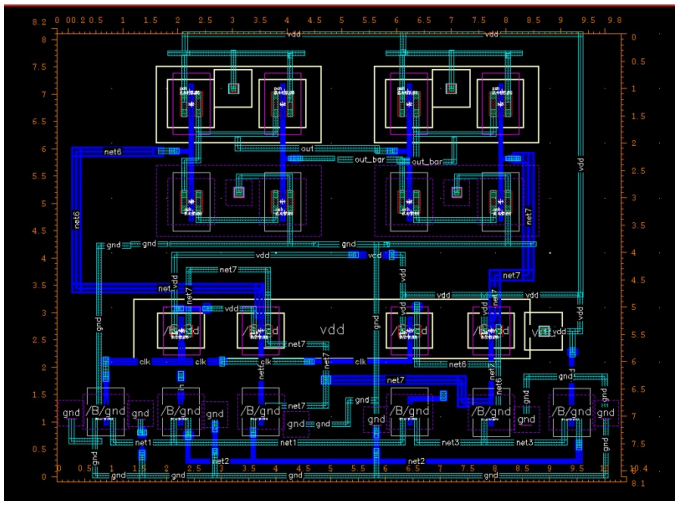

Fig. 7: Layout of Sense Amplifier

VI. Conclusions

We explored the design, analysis and layout making of the sense amplifier. By this we understood that there are some trade offs which we need to study before committing our design. Like the best performance logic design might not be able to have the better area efficiency. The main interesting pros of this sense amplifier is it's amplification and storing instead of just storing a false value. There are various leakages which are decays our signal in the real life application, so at large scale storing device manufacturing this sense amplifier can be one of the best possible solution than the simple registers. Apart from this we also learnt the following:

• Use the Cadence Virtuoso for making Sense Amplifier schematic.

• Using the nch and pch MOSFETS from TMSCn65 library and some basic sources from analoglib.

• Performing the simulation and the timing analysis to measure delays and timing aspects.

• We alse learnt how to make a DRC error free layout of our design.

VII. Refernces

1. Digital Integrated Circuits by Jan M.Rabaey

2. Design of Sense Amplifier in the High Speed SRAM