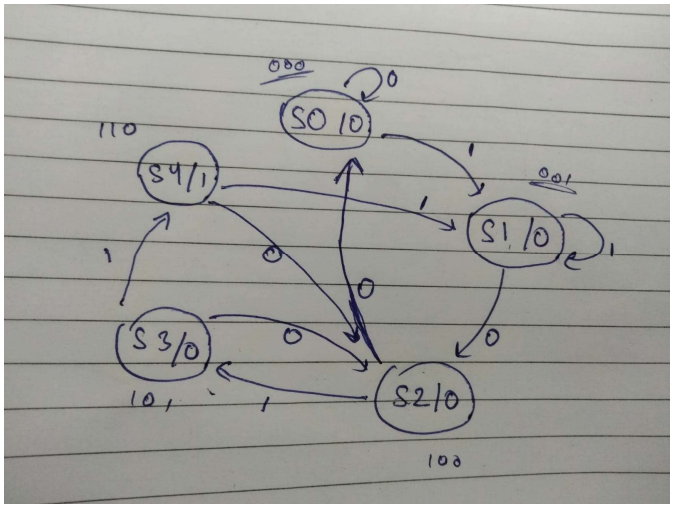
Sequence Detector

This Verilog project is to present a full Verilog code for Sequence Detector using Moore FSM. A Verilog Testbench for the Moore FSM sequence detector is also provided for simulation.

The Moore FSM keeps detecting a binary sequence from a digital input and the output of the FSM goes high only when a "1011" sequence is detected. The state diagram of the Moore FSM for the sequence detector is shown in the following figure.



It is noted that the Moore FSM output depends on only the current state of the FSM.

Output of the Simulations are :