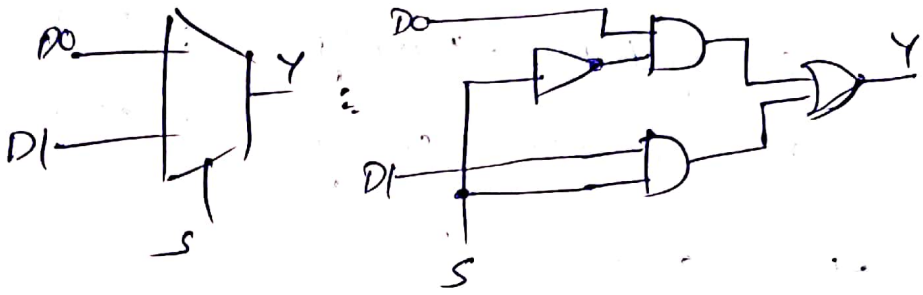
Given:

NOT gate : 2ns

AND gate : 4ns

OR gate : 4ns

wires : na



2x1 : Mux delay = NOT + AND + OR

= 2ns + 4ns + 4ns

= 10ns

(1) Registers

① Loading (storing data)

Delay path : Input to latch

Delay = Inverter + AND + AND + MUX + MUX + MUX + Latch

= 2ns + 4ns + 4ns + 10ns + 10ns + 10ns = 40ns.

② Dumping (Retrieving).

Delay : Inverter + AND + AND + MUX + MUX + Tristate buffer

= 2ns + 4ns + 4ns + 10ns + 10ns + 4ns = 34ns.

(2) ~~MUX~~ ALU

Delay : max(AND, XOR, NOT, OR gates) + MUX (8x1) + latch

= 4ns + 10ns x 3 + 4ns = 38 ns.

(3) FSM:

Delay : MUX (16x1) + Latch + NOT + AND + MUX (16x1) + latch + NOT

= 4x10ns + 4ns + 2ns + 4ns + 4x10ns + 4ns + 2ns = 98 ns.

Processor

① mv - 0,1,6,9

0 - Din to Bus : Register Dumping : 34ns

1 - Bus to IR : Register storing : 40 ns

6 - Ry to Bus : Dumping : 34ns.

9 - Bus to Ry : storing : 40ns.

AFSM : 96ns

MUX : 38ns

Delay Total : 34+40+34+40+96+38 ns = 282ns.

② mvi - 0,1,2,3.

similar to mv : Delay : 282ns [2x(Dumping + storing)]

③ Operations - 0,1,4,5,6,7,8,9
(Others).

Delay = Data Register Duming + Register storing + Data Dumping + Data storing + Data Dumping + ALU delay + Data Dumping + Data storing

= 4 x 34ns + 3 x 40 ns + 38ns

= 294 ns.

Total Delay = 96 ns + 38 ns + 294 ns

= 428 ns.