Schedulers & Dispatcher

→ Schedulers are the components of O.S (Process Manager) that makes decisions;

Schedulers
- → Long Term Scheduler (LTS)
- → Short Term " (STS)
- → Medium Term " (MTS)

1) Long Term Scheduler : operates on Job-Q & decides which programs to be Loaded in Memory

2) Short Term Scheduler : operates on Ready-Q, to decide which ready Process Should run onto cpu-Next

cpu-Scheduler

3) Medium Term Scheduler: operates on Suspend 'Q' to Swap-out & Swap-in Processes;

Which Scheduler controls degree of Multiprogramming?

→ No. of registered Process with OS

a) LTS b) MTS c) STS

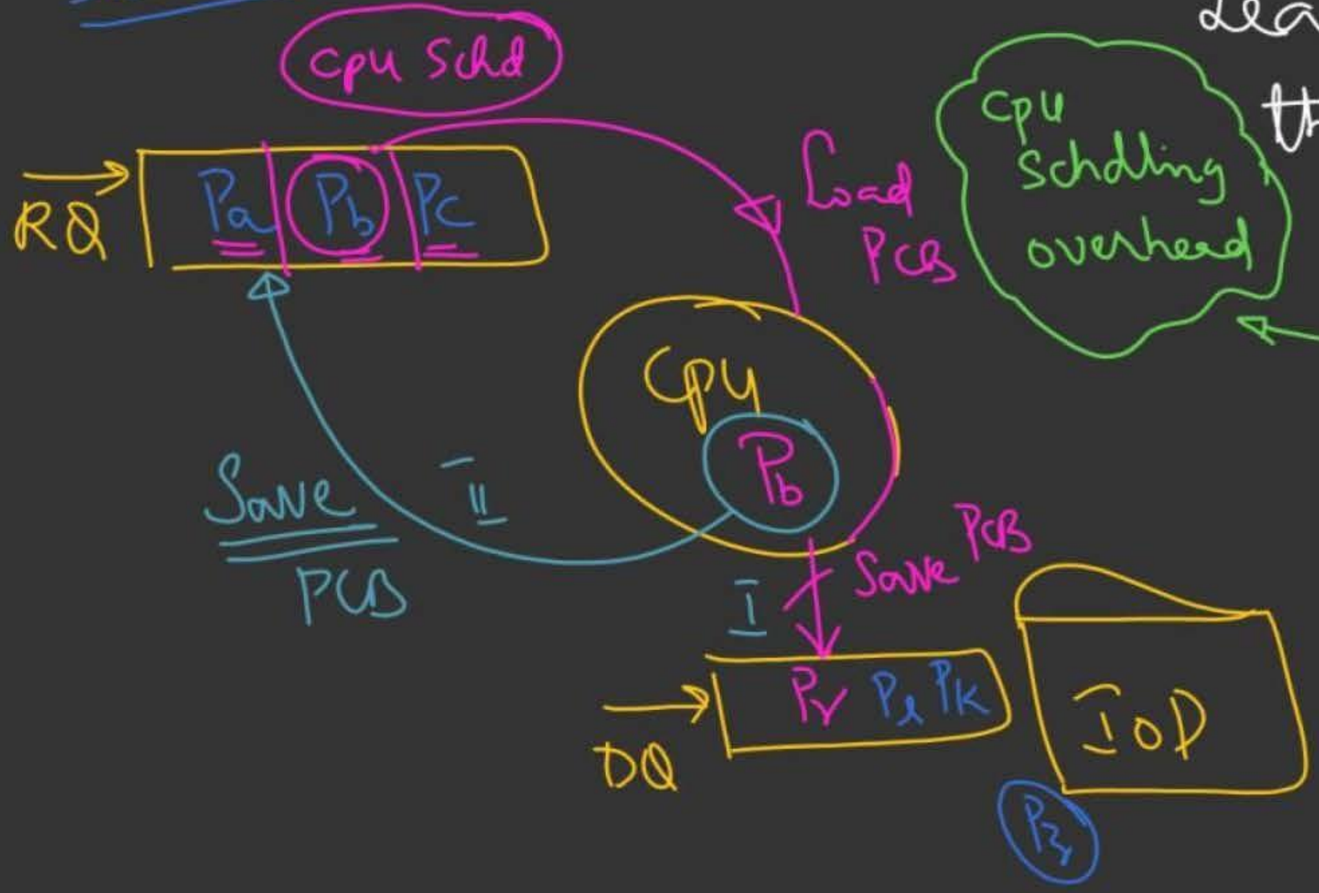
Q) Does uniprogrammed O.S need a Scheduler?

No Suspend Q No Ready Q No Block Q

⑧ CONTEXT – SWITCHING : (is an activity carried out by DISPATCHER, that involves Saving the PCB of process leaving the cpu and Loading the PCB of Next Ready Process onto cpu;) < Process Switching

(Dispatcher)

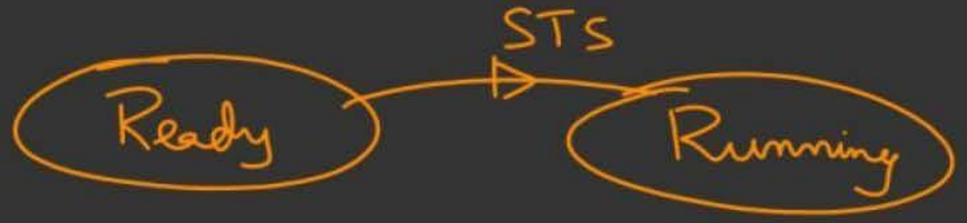
Scenario



Total time to Load & Save PCB ≡ Content Switching Time

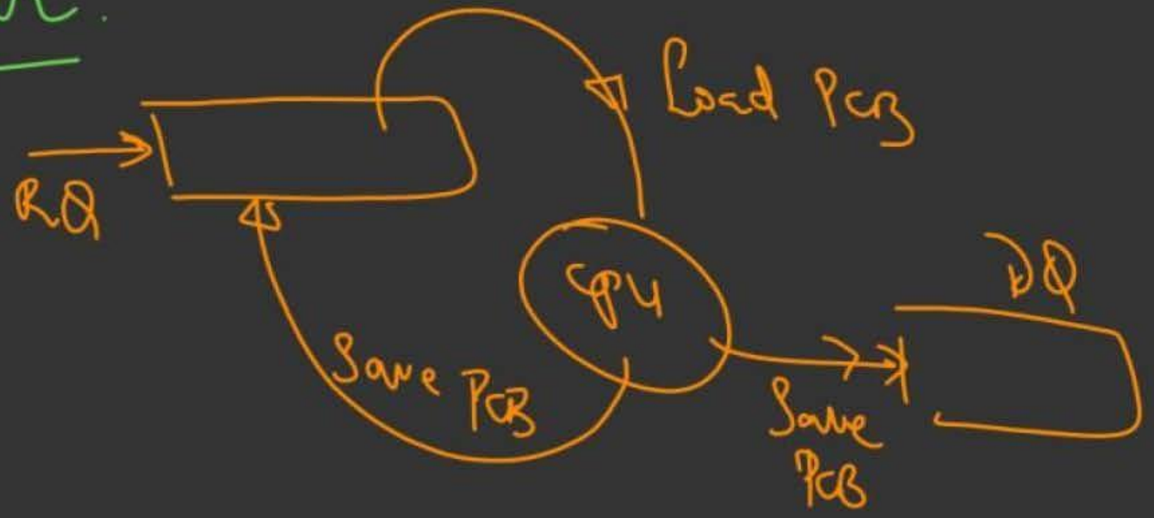
1) LTS :

2) STS :



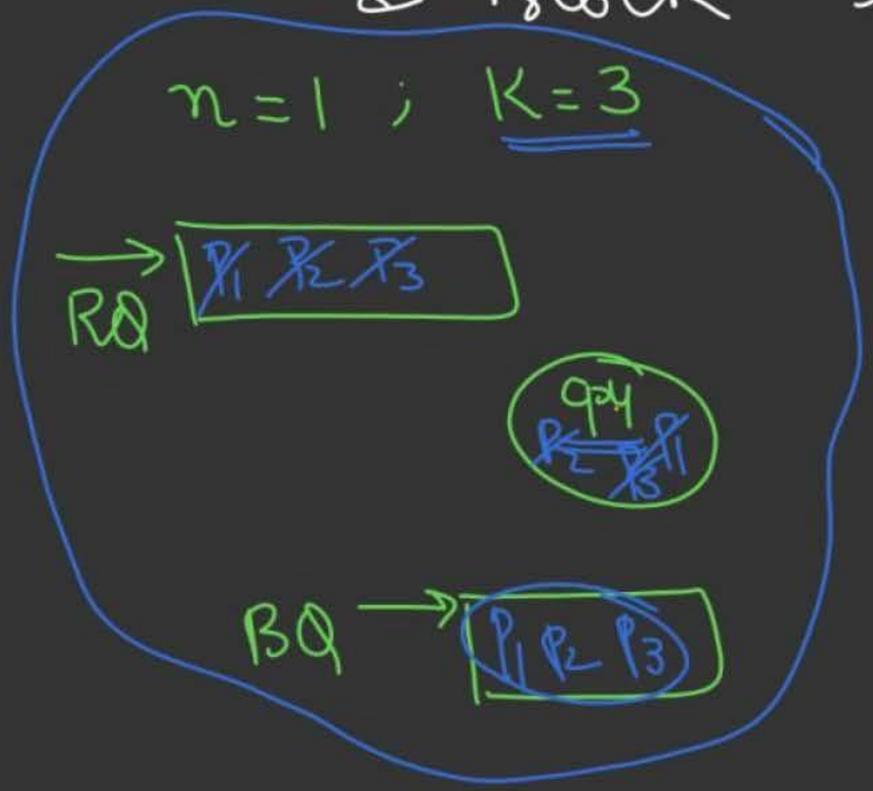
3) MTS :

4) Dispatcher :



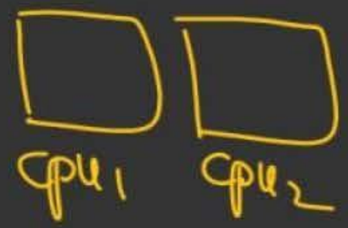
2m

Q) Consider a System having n - cpu's ($n \geq 1$) and 'K' processes ($K > n$); What is the Lower Bound (Min) and upper Bound (Max) of the no. of Processes that can be in Ready, Running & Block States?



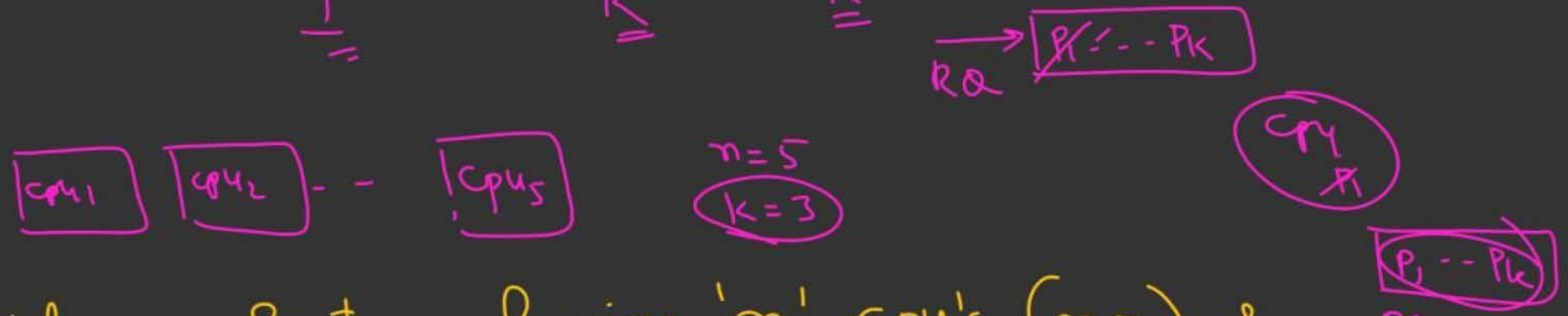
	LB	UB
Ready	0	K
Running	0	n
Block	0	K

Max: 2



Q2) Consider a System having a single cpu & 'K' processes ($K > 1$); What is the UB of Running, Ready, Block?

Running: 1 ≤ , Ready: K ≤ , Block: K ≤

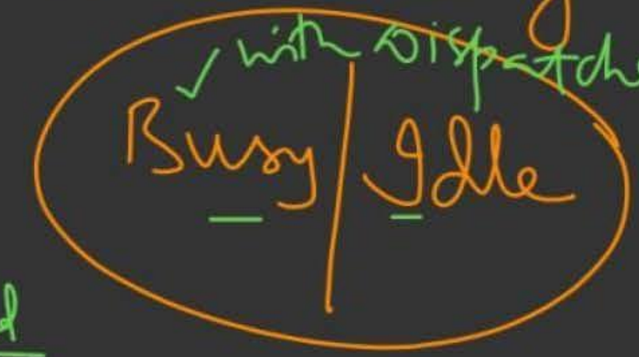


Q3) Consider a System having 'n' cpu's ($n \geq 1$) & K-processes ($k < n$); Calculate UB of Ready, Running & Block processes;

Ready: K, Running: K, Block: K

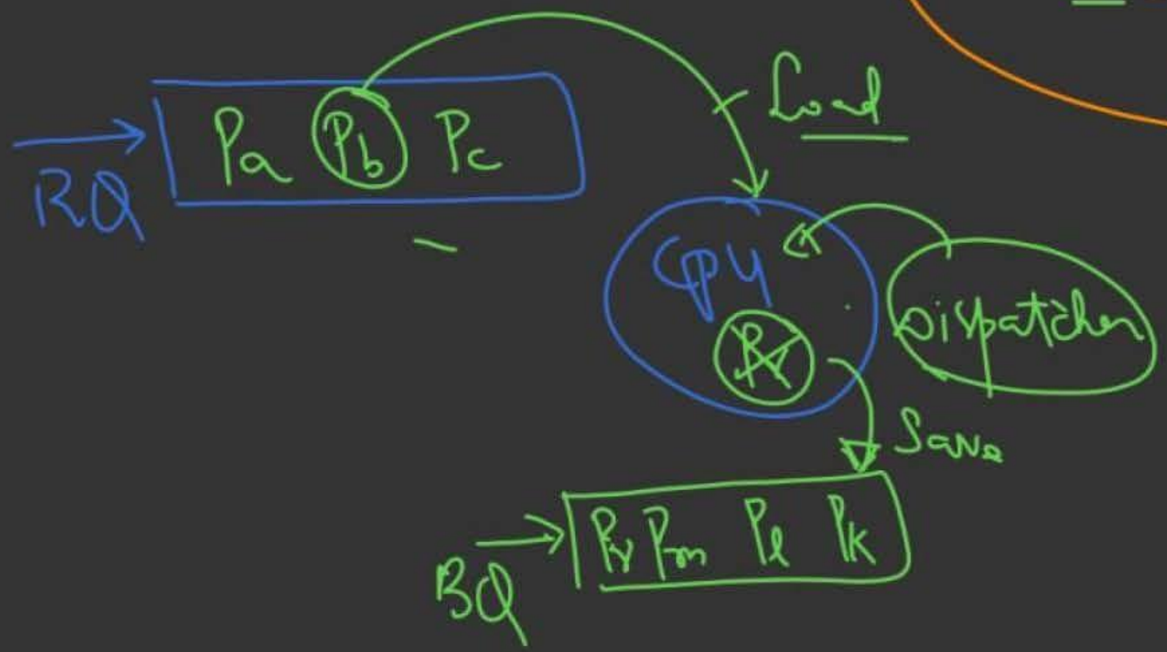
9) What will be the State of cpu, during Content-Switching?

Ans:



× Ideal

Idle



Dispatcher is running on cpu to Save the PCB, has to Load the PCBs from RQ onto cpu

During Content-Switching (dispatcher), no useful (user Process) activity takes place on cpu (overhead)

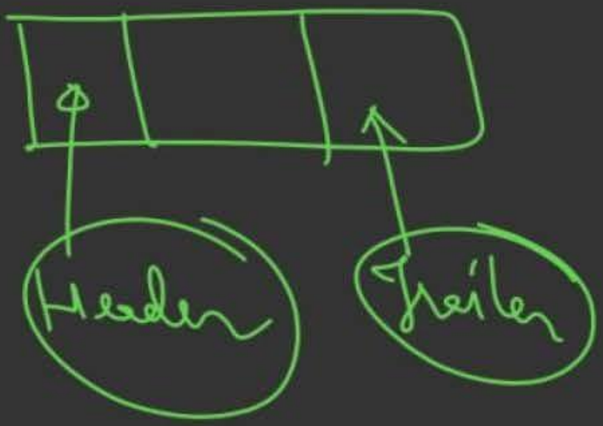
Content-Switching-time

=

cpu Scheduling overhead

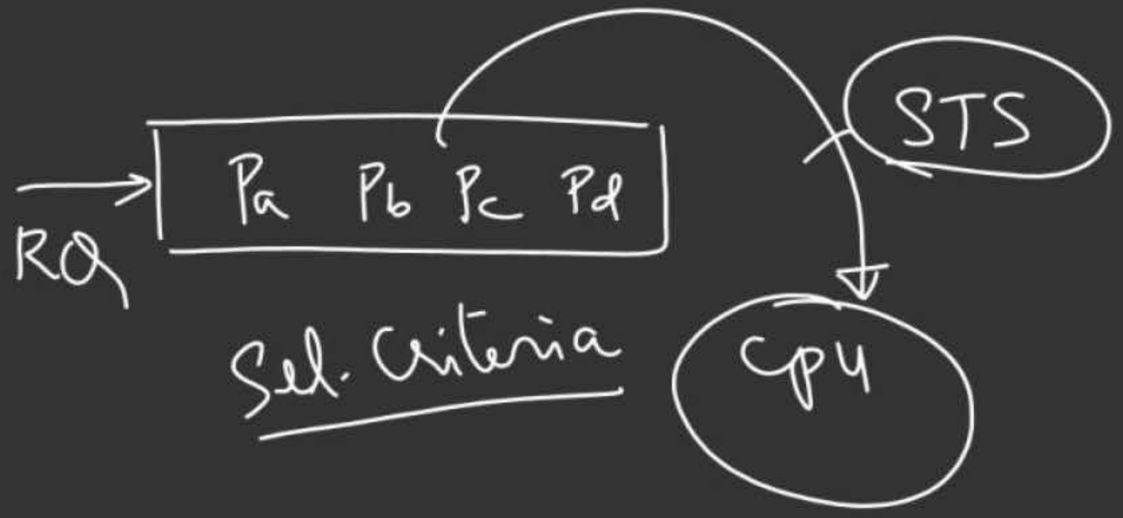
=

Dispatch Latency



2) CPU Scheduling

(*) Process Scheduling



Function

320 m — 20
1 m — ?

Throughput = $\frac{20}{320} * 100$ %

[Design of Short Term Scheduler]

Goals of CPU Scheduler

1. Max. CPU utilization
   - Max. Throughput = No. of Process Completed Per unit-time
2. Minimize Turn-Around_time (TAT), waiting_time (WT), Response_time (RT)

Process_times:

1. Arrival time (AT):

Submission time

2. Waiting_time (WT)

3- Scheduling_time (ST)

4 Burst_time (BT)

[CPU-BT]

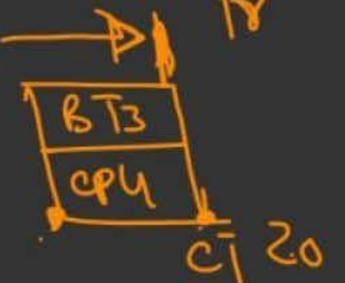
6) Completion time (CT):

7) Turn_Around Time (TAT)

(CT-AT)

5) State_Timing diagram

5) IO-Burst_time (IOBT)



1. Arrival time (AT) : Time at which process makes entry into Ready 'Q' from New State

2. Waiting time (WT) : Time Spent by Process in R.Q, waiting for cpu is W.T

3. Burst time (BT) : Time Spent by process running on cpu is B.T

4. Io Burst Time (IoBT) : Time Spent by Process in perf. Io

5. Completion Time (CT) : Time at which process Complete its execution & Leave (Terminate)

6. Turn-Around Time (TAT) : Total Time Spent by Process from Arrival to Completion;

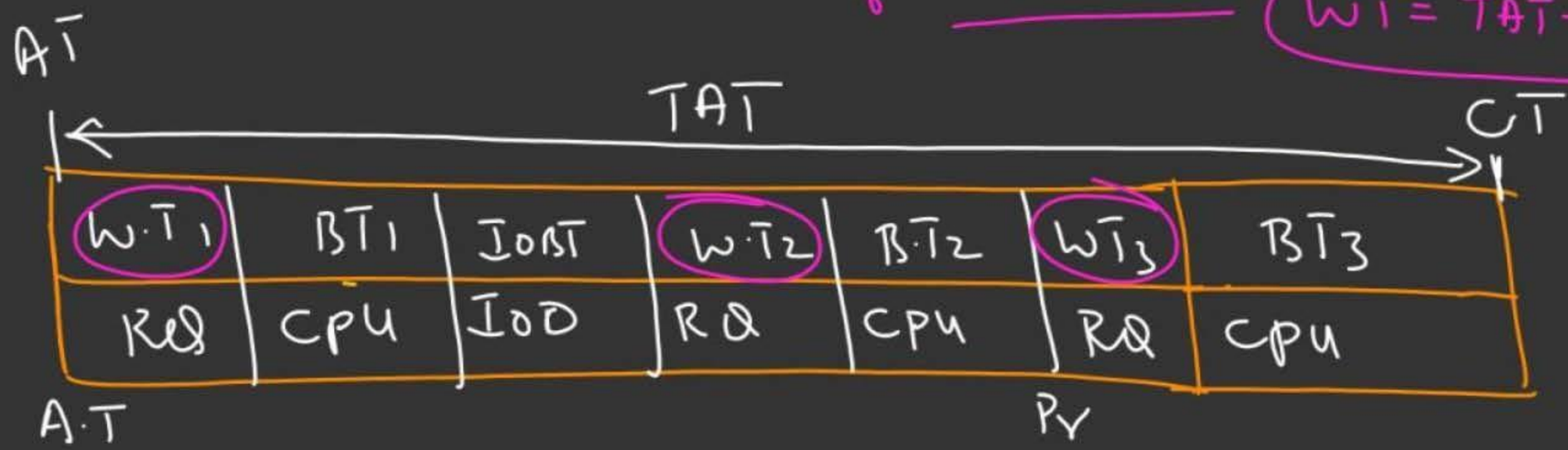
Waiting-time(WT) = TAT − (BT + IOBT)

*

B.T = BT1 + BT2 + BT3

if IOBT = 0

WT = TAT − BT



TAT = CT − AT

*

Process Concepts

- Program vs Process
- Process as an ADT
- Process Structure
- Process States
- State Transition diagram
- Scheduling Q's
- Queuing diagram
- L.T.S + S.T.S + M.T.S
- Dispatcher & Context Switching

→ Goals of S.T.S

→ Process Times

- A.T
- W.T
- B.T
- ZOBT
- C.T
- T.A.T