Chapter-2

HARDWARE DESCRIPTION

GENERAL

The system has got 8085 as the Central Processing Unit. The clock frequency for the system is 3.07 MHz and is generated from a crystal of 6.14 MHz.

8085 has got 8 data lines and 16 address lines. The lower 8 address lines and 8 bit data lines are multiplexed. Since the lower 8 address bits appear on the bus during the first clock cycle of a machine cycle and the 8 bit data appears on the bus during the 2nd and 3rd clock cycle, it becomes necessary to latch the lower 8 address bits during the first clock cycle so that the 16 bit address remains available in subsequent cycles. This is achieved using a latch 74-LS-373.

MEMORY

VMC-850X provides 8/32K bytes of RAM using 6264/62256 chip and 8K bytes of EPROM for monitor. There is one memory space provided on VMC-850X. This one space can be defined any address slots from 8000 - DFFF depending upon the size of the memory chip to be used. Total onboard memory can be extended to 64K bytes.

I/O DEVICES

The various I/O chips used in VMC-8501 are 8279, 8255 & 8253 and VMC-8502 are 8279, 8255, 8253 & 8155. The functional role of all these chips is given below:

8279 (Keyboard & Display Controller)

8279 is a general purpose programmable keyboard and display I/O interface device designed for use with the 8085 microprocessor. It provides a scanned interface to 28 contact key matrix provided in VMC-850X and scanned interface for the six seven segment displays. 8279 has got 16 x 8 display RAM which can be loaded or interrogated by the CPU. When a key is pressed, its corresponding code is entered in the FIFO queue of 8279 and can now be read by the microprocessor. 8279 also refreshes the display RAM automatically.

8255 (Programmable Peripheral Interface)

8255 is a programmable peripheral interface (PPI) designed to use with 8085 Microprocessor. This basically acts as a general purpose I/O device to interface peripheral equipments to the system bus. It is not necessary to have an external logic to interface with peripheral devices since the functional configuration of 8255 is programmed by the system software. It has got three Input/Output ports of 8 lines each (PORT-A, PORT-B & PORT-C). Port C can be divided into two ports of 4 lines each named as Port C upper and Port C lower. Any Input/Output combination of Port A, Port B, Port C upper and lower can be defined using the appropriate software commands. The port addresses for these ports are given in Chapter-6. VMC-850X provides 24 Input/Output ports using 8255 chips.

8253 (Programmable Internal Timer)

This chip is a programmable interval Timer/Counter and can be used for the generation of accurate time delays under software control. Various other functions that can be implemented with this chip are programmable rate generator, Even Counter, Binary rate Multiplier, Real Time Clock etc. This chip has got three in dependent 16 bit counters each having a count rate of up to 2KHz. The first Timer/Counter (i.e. Counter 0) is being used for Single Step operation. However, its connection are also brought at connector space C4. For single step operation CLK0 signal of Counter 0 is getting a clock frequency of 1.535 MHz. The counter 1 is used to generate clock for 8251. Counter 1 & Counter 2 are free for the user. Clock for the CLK1, CLK2 is to be given externally.

8155 (Programmable I/O Port & Timer Interface) Optional (only in Model VMC-8502)

8155 is a programmable I/O ports and timer interface designed to use with 8085 Microprocessor. The 8155 includes 256 bytes of R/W memory, three I/O ports and a Timer. This basically acts as a general purpose I/O device to interface peripheral equipments to the system bus. It is not necessary to have an external logic to interface with peripheral devices since the functional configuration of 8155 is programmed by the system software. It has got two 8-bit parallel I/O port (Port-A, Port-B) and one 6-bit (Port-C). Ports A & B also can be programmed in the handshake mode, each port using three signals as

handshake signals from Port-C. The timer is a 14 bit down counter and has four modes. VMC-8502 optionally provides 22 I/O ports & a 14 bit timer/counter.

8251 (USART)

This chip is a programmable communication interface and is used as a peripheral device. This device accepts data characters from the CPU in parallel format and then converts them into serial data characters for the CPU. This chip will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character from the CPU. The CPU can read the complete status of it at any time. One such chip is used in VMC-8503A Kit and these can be used for interfacing any serial device. The connections of 8251 is brought at connector C5.

DISPLAY

VMC-850X provides six digits of seven segment display. Four digits are for displaying the address of any location or name of any register, whereas the rest of the two digits are meant for displaying the contents of a memory location or of a register. All the six digits of the display are in hexadecimal notation.