ECE 465
Digital Systems Design
Fall 2025

Design of Arithmetic Logic Unit using Reversible Logic Gates

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UIC ENGINEERING

Motivation

- Traditional ALUs lose information → energy dissipation.
- Reversible logic supports low-power, green computing.
- Essential for nano, quantum, and IoT hardware.
- Key stepping stone toward quantum ALUs.

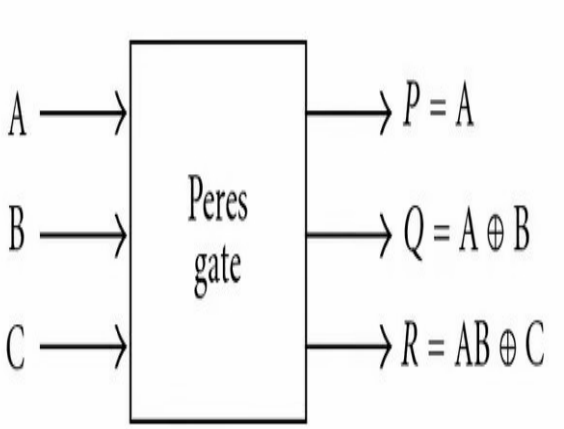
Problem Statement

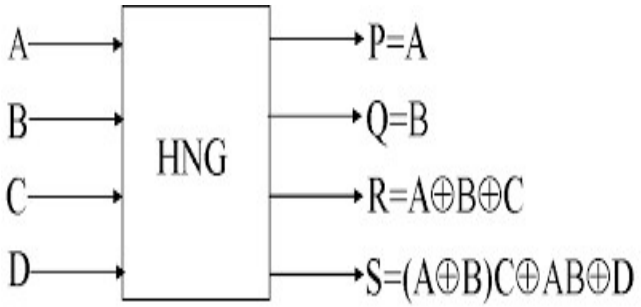
- Irreversible logic loses information, so it always wastes some energy.
- Power and thermal limits worsen with scaling.
- Need reversible architectures to minimize energy loss.
- Proposed: Optimized reversible ALU with minimal garbage outputs.

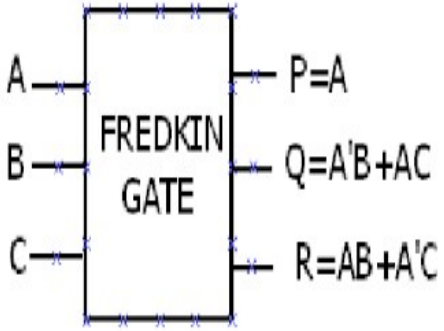
Techniques

- Peres Gate for XOR and partial carry with low hardware cost.
- HNG Gate for full adder with only one gate.
- Fredkin Gate for OR and multiplexing.

Reversible Gates:

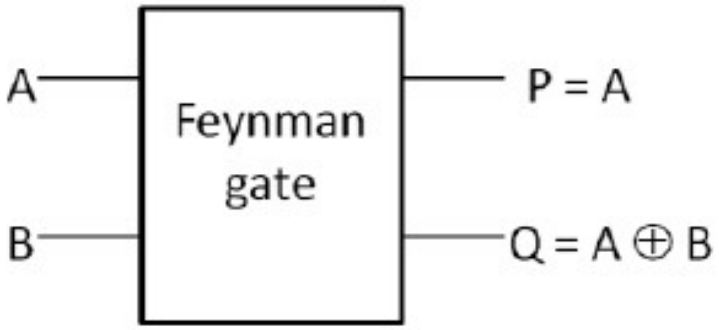




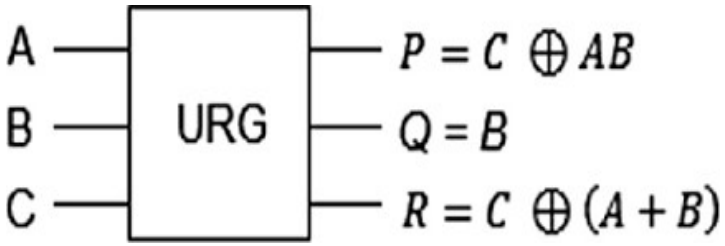


Reversible Gates:

Feynman gate performs a bitwise XOR operation on one of its inputs when a control bit is set to 1.

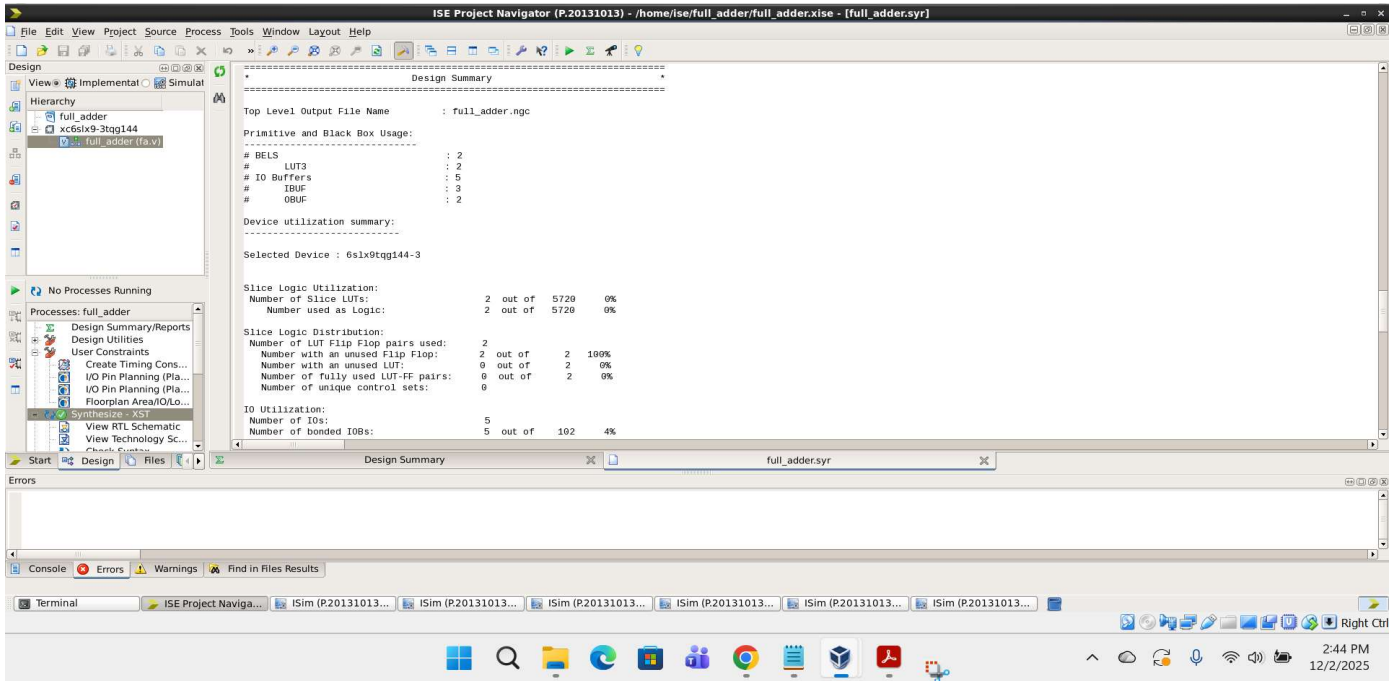


Any reversible logic function can be constructed solely using copies of this single gate type.



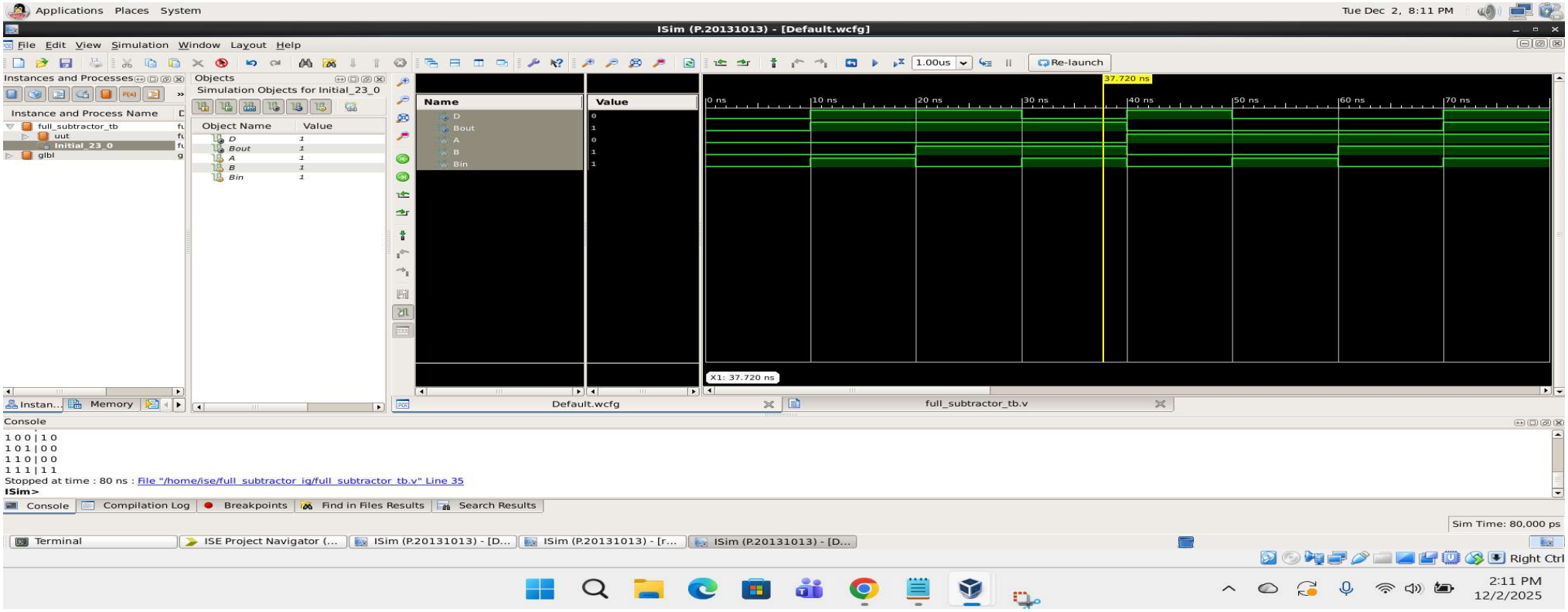
Results

- Area is minimal compared to irreversible gate.
- Very low power due to reversible design.
- Less delay as gates are compact.

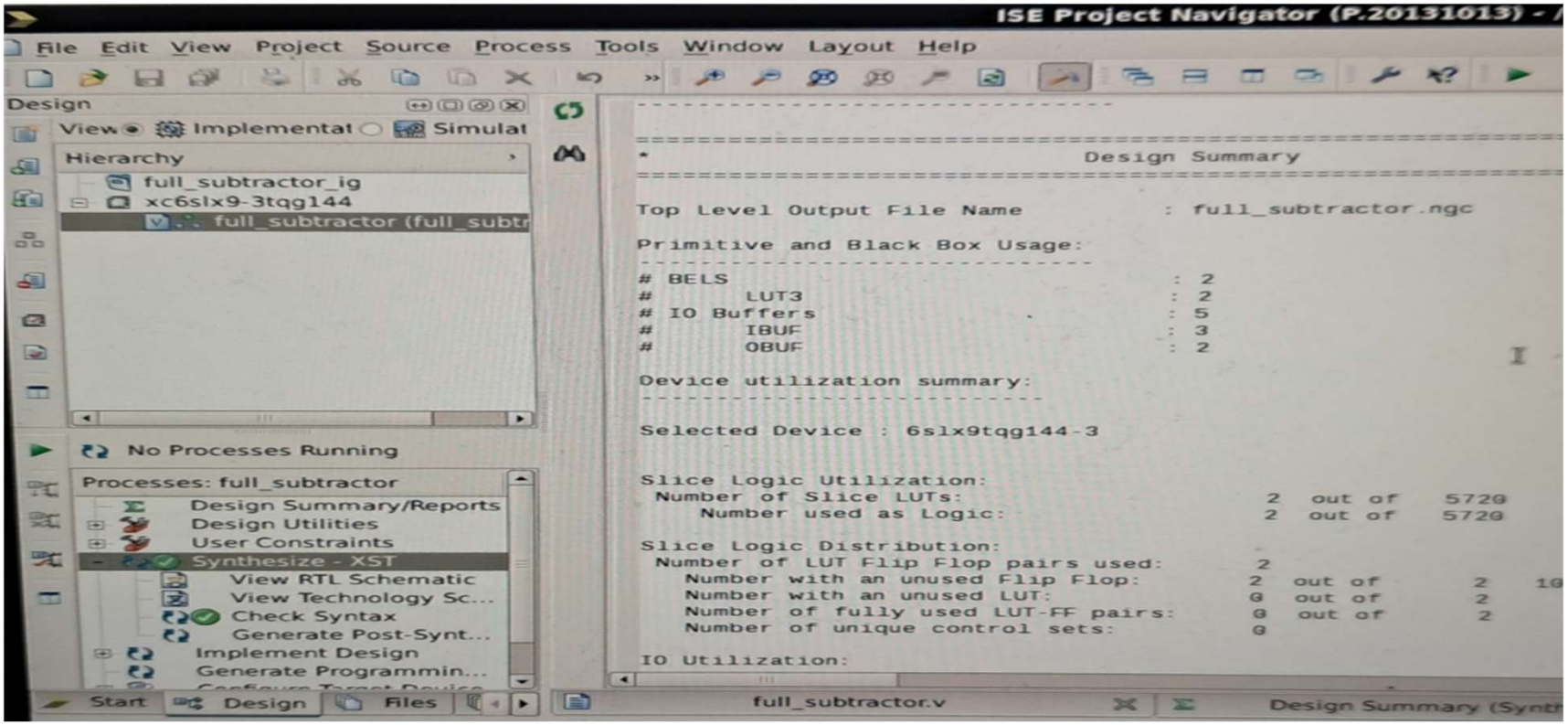


Results

- This is full subtractor circuit using irreversible gates.



Results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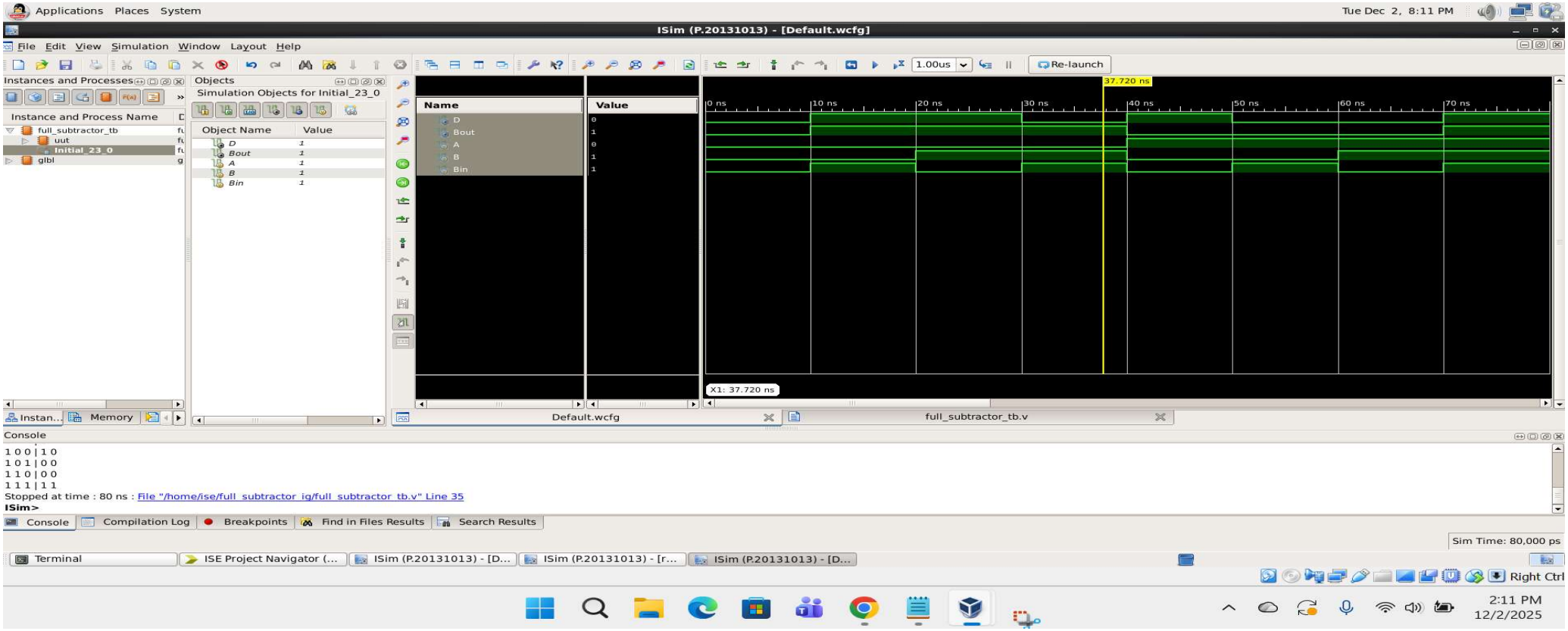
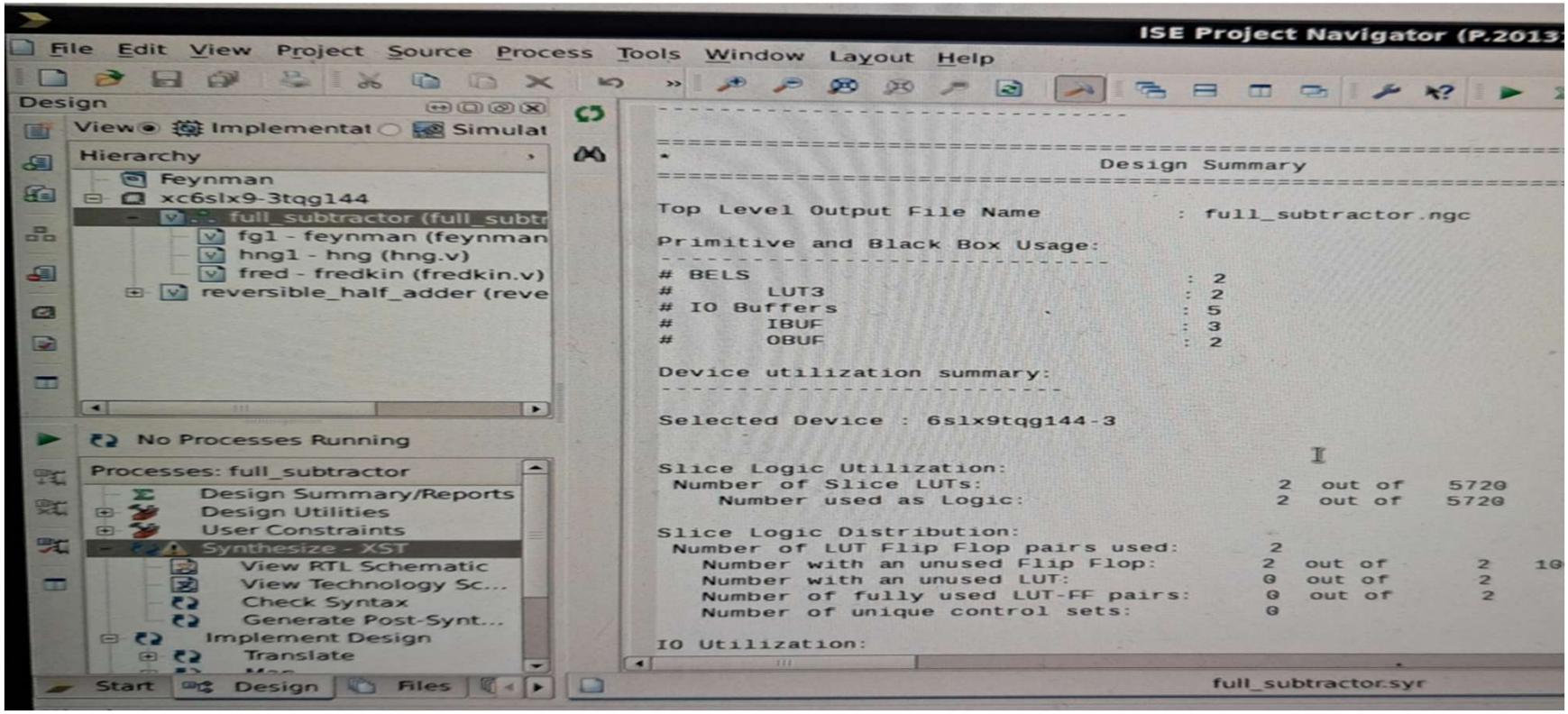
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Sc...
Check Syntax
Generate Post-Synt...
Implement Design
Generate Programmin...
Start Design Files
Design Summary
Top Level Output File Name : full_subtractor.ngc
Primitive and Black Box Usage:
BELS : 2
LUT3 : 2
IO Buffers : 5
IBUF : 3
OBUF : 2
Device utilization summary:
Selected Device : 6slx9tqg144-3
Slice Logic Utilization:
Number of Slice LUTs: 2 out of 5720
Number used as Logic: 2 out of 5720
Slice Logic Distribution:
Number of LUT Flip Flop pairs used: 2
Number with an unused Flip Flop: 2 out of 2
Number with an unused LUT: 0 out of 2
Number of fully used LUT-FF pairs: 0 out of 2
Number of unique control sets: 0
IO Utilization:
full_subtractor.v
Design Summary (Synth

Results

- This is the full subtractor circuit with reversible gates.



Results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Hierarchy
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hng1 - hng (hng.v)
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No Processes Running
Processes: full_subtractor
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Sc...
Check Syntax
Generate Post-Synt...
Implement Design
Translate
Start
Design
Files
Design Summary
Top Level Output File Name : full_subtractor.ngc
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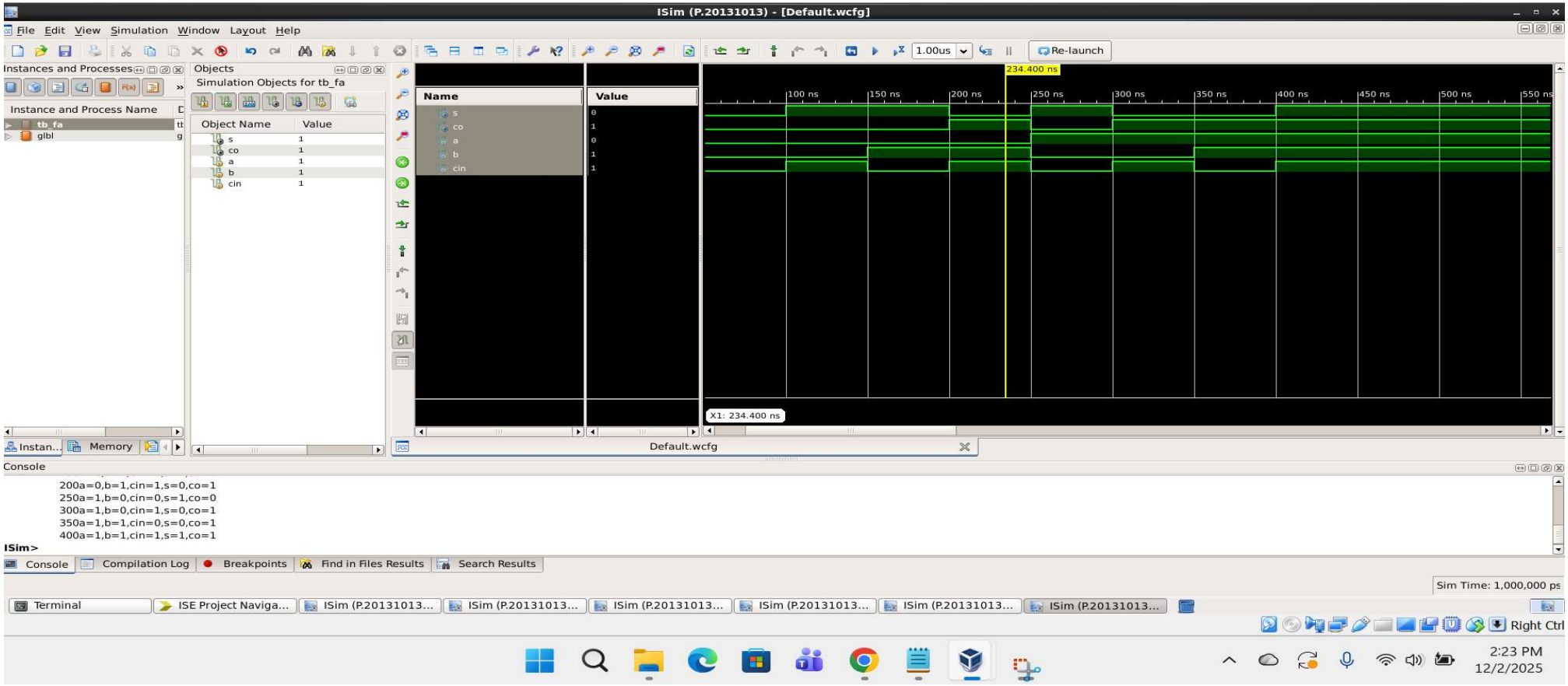
full_subtractor.syr

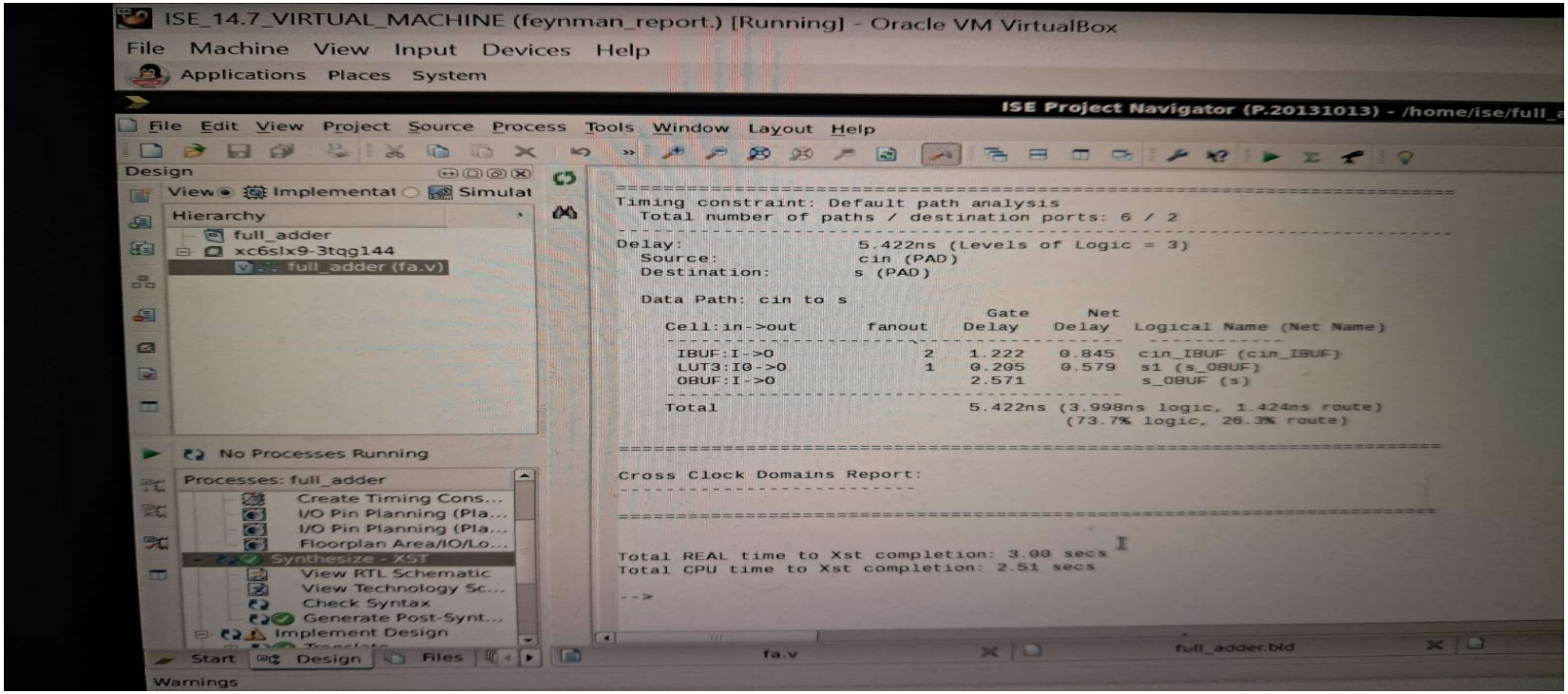
Results

- Full adder circuit with irreversible gates.



Results

- Timing summary for full adder with irreversible gates.



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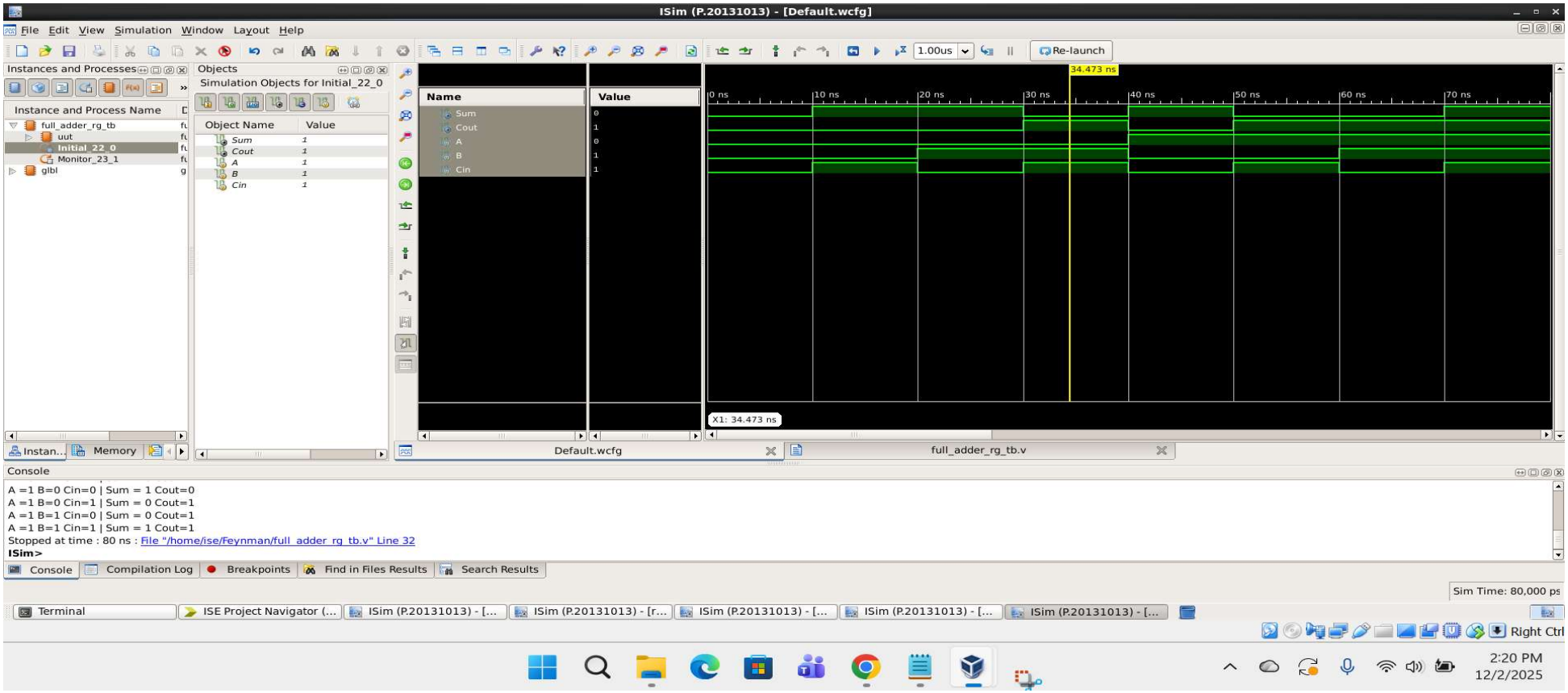

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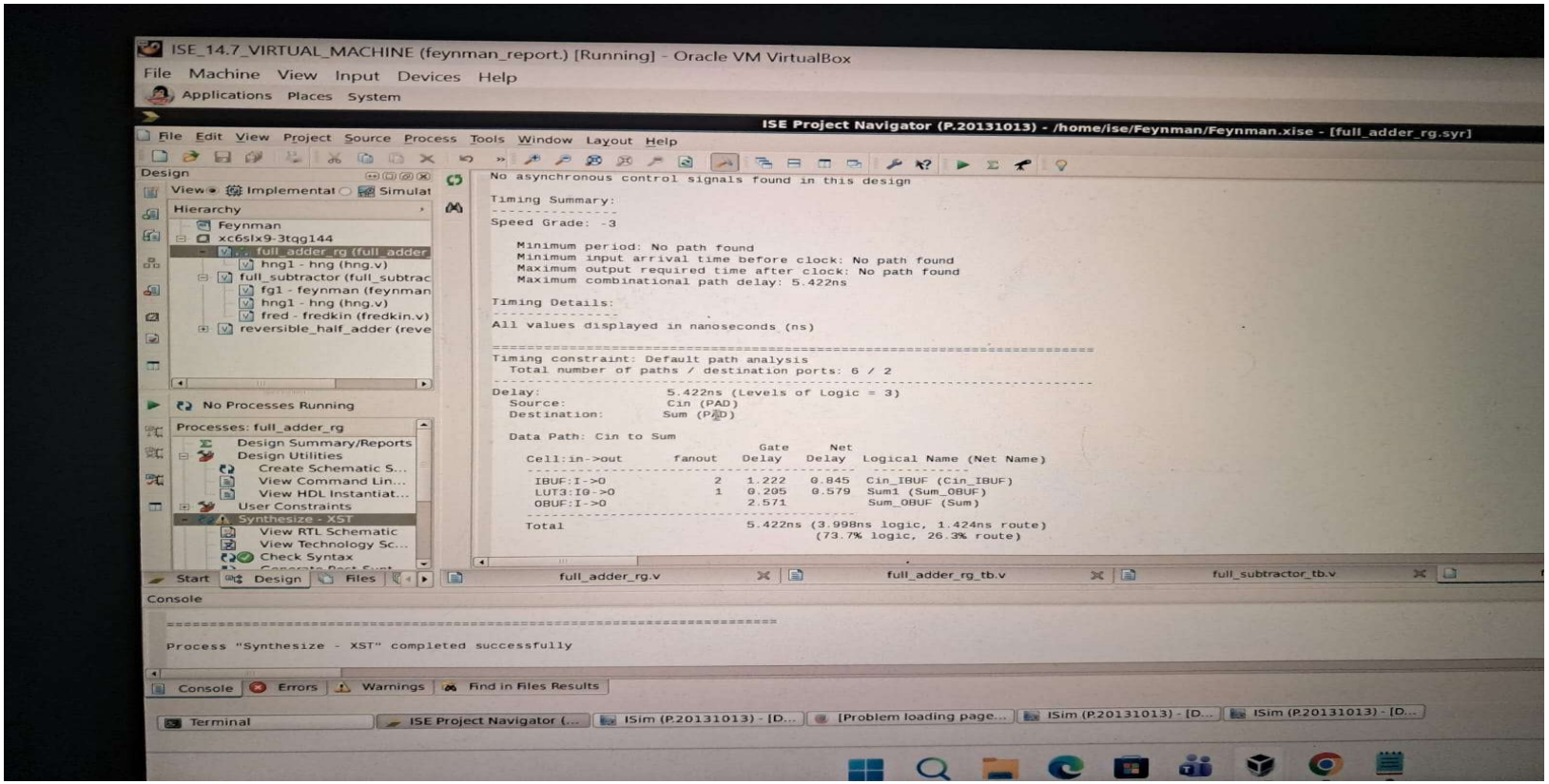

Contribution Map Per Group Member

- • Anish Ramachandra Jois: Gate-level design, Testing, Results.
- • Achanta Sasidhar Naga Vital: ALU integration, Logic blocks, Documentation.

Conclusion

- Completed an optimized reversible ALU architecture.
- Used Peres, HNG, Fredkin gates for minimal garbage outputs.
- Energy Efficiency.
- Information conservation.
- Power and time delay