BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI II SEMESTER 2014-2015 CSF241/ECEF241/EEEF241/INSTRF241MICROPROCESSOR PROGRAMMING AND INTERFACING TEST I (OPEN BOOK) TIME: 60 Min. 28/02/2015 MM: 40 IDNO: Name: Q1. In an 80486 processor that is working in real mode and 16-bit mode: Suppose that: CS =1000_H,

Q1. In an 80486 processor that is working in real mode and 16-bit mode: Suppose that: $CS = 1000_H$, $ES = 8000_H$, $DS = 4000_H$, $ES = 7000_H$, $ES = 0000 0200_H$, $EDI = 0000 0410_H$, $EBP = 0000 2300_H$, $EBX = 0000 0200_H$ EAX=0000 0400_H, $ECX = 0000 0020_H$, $EDX = 0000 0008_H$ For the instructions given below determine the following. [Give Values only in Hex only] [4]

MOV [BP+SI+2000 _H],CX	
Memory Address	
Addressing Mode	
Machine Code	
	Memory Address Addressing Mode

Q2. Replace the following program segments by <u>a single instruction</u> of 80486. You can assume that all flags (except Trap and Interrupt) are reset at the beginning of each of these program segment [Clarification: Each program segment achieves a certain final result. You need to give a single instruction that will achieve the same result. The single instruction needs only achieve the final result]

	Program	Instruction		Program	Instruction
Α	PUSH AX		В	PUSHF	
	PUSH BX			PUSH BP	
	POP AX			MOV BP,SP	
	POP BX			MOV AH,[BP+2]	
				POP BP	
				POPF	
С	CMP EBX,EAX		D	MOV [0200],ESP*	
	JNE X1			PUSH EAX	
	MOV EBX,ECX			PUSH ECX	
	JMP X2			PUSH EDX	
	X1: MOV EAX,EBX			PUSH EBX	
	X2:			PUSH DWORD PTR[0200]	
				PUSH EBP	
				PUSH ESI	
				PUSH EDI	
E	PUSHF		F	PUSHF	
	MOV BH,FF			PUSH AX	
	CMP BL,0			MOV AX,[SI]	
	JL X1			MOV ES: [DI],AX	
	NOT BH			POP AX	
	X1: POPF			INC SI	
				INC SI	
				INC DI	
				INC DI	
				POPF	

^{*}DS: [0200] – is just a temp location – what happens to it does not matter in the final result.

	cycles in proper or	der				[4]
	Instruction	Cycles		Instruction	Cycles	
Α	ADD	- Cy 6.66	В	XCHG AX,[BX]		
	[BX+SI+1000], CX					
_						
С	NOP		D	CMP [SI],AX		
	L		<u> </u>			
Q4.	. If a processor is	working at 5 MHz	and the	memory access tim	e is 750ns. The nu	mher of w
٠.	•	_		•		
	states required w	vill be		, considering a	n address set-up ti	me of 110r
	data set-up time	of 40ns with a latc	hing and b	uffer delays of 30ns		[2]
	·		J	•		
Q5.	. What will be the	effect of executing	the follow	ving code snippet or	n an 8086 processor	? [2]
•	MOV BX, FFF				·	
	AND BX, 070					
	PUSH BX					
	POPF					
ე6.	. Write an 8048	36 ALP that will ex	amine a s	eries of memory lo	cations for small a	phabets. I
Q6.	memory location	has a small alphal	oet it will o	convert it into capit	als. If the memory	ocation do
Q6.	memory location not have a small	has a small alphal alphabet it will no	pet it will on the control of the co	convert it into capit the contents of the	als. If the memory memory location.	ocation do
Q6.	memory location not have a small memory location	has a small alphal alphabet it will no to be examined st	oet it will o ot modify art at <i>alph</i>	convert it into capit	als. If the memory memory location. mory locations to be	location do The series e examined
Q 6.	memory location not have a small memory location stored in <i>cnt1</i> an	has a small alphal alphabet it will no to be examined st d will not exceed 2	pet it will on t modify art at alph 1000 _d . The	convert it into capit the contents of the 1. The count of mer	als. If the memory memory location. mory locations to be onversion of one si	location do The series e examined
Q 6.	memory location not have a small memory location stored in <i>cnt1</i> an to one capital alp	has a small alphal alphabet it will no to be examined st d will not exceed a shabet must be dor	oet it will o ot modify art at <i>alph</i> 1000 _d . The ne using a	convert it into capit the contents of the 1. The count of mer checking and the c	als. If the memory memory location. mory locations to be onversion of one selections.	ocation de The series e examine mall alpha

Q3. For the following Instructions what will be the machine cycles executed by 8086. Enter the machine