# SET 'A'

### BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI Hyderabad Campus, Second Semester 2014-2015 CS/ ECE /EEE/ INSTR F241 Microprocessor Programming & Interfacing

Quiz-3 (Closed Book)

	24/04/15 Marks : 20	Day: Friday	Time:1	<b>2.00</b> – 1	12.30 PM
NAM	IE:	I	D:		
Answe	er all the questions.				
1.	Which microprocessor pins (A) RESET and READY	(B) READY and	l WAIT		
	(C) HOLD and HLDA	(D) None of thes	se	[	] [1M]
2.	The no. of address lines requ (A) 15 lines (B) 16 lines (		of size 256 K is	[	] [1M]
3.	Interfacing of output device (A) Buffers (B) Latches (Control of the Control of t	<u>*</u>	•		][1M]
4.	Which part of the disk will creation of the file? (A) Boot sector (B) FAT (6)			, date ai	nd time of
5.	The lines BHE'=0 and A <sub>0</sub> =  (A) whole word  (C) Low byte to/from even a	(B) High byte to/	from odd address	[	][1M]
6.	Which pins are general purp (A) PA0 – PA7 (B) PB0-PF		*	82C55	? ][ <b>1M]</b>
7.	The interrupt vector table is (A) 1K (B) 256K (C) 51	•	area	of the n	nemory.
8.	The contents of the 16550 the type of parity used and	the data length are	and		1010, then bectively.
	(A) Even, 6 bits (B) Odd,		L1 L0 (D) Even, 8 bits	[	][2M]

9. If a 16- bit count is programmed into the 8254, which byte of the counfirst?	nt is pro	grammed					
(A) LSB (B) MSB (C) Both bytes at the same time (D) None	[	][1M]					
10. Where is the interrupt vector type number stored in 8259A? (A) ICW 1 (B) ICW 2 (C) ICW 3 (D) ICW 4	[	][1M]					
11. Where a slave INT pin is connected on the Master 8259A in cascade sys (A) IR input of the Master (B) INTR input of the processor (C) Cascade input of the master (D) INTA input of the processor		][ <b>1M</b> ]					
<ul><li>12. Which of the following technique is used to synchronize an I/O microprocessor?</li></ul>							
(A) Interfacing (B) Arbitration (C) Handshaking (D) Decoding	[	][1M]					
13. The 8237 DMA controller is channel device and each channel can transfer up to bytes with a single programming.							
(A) 3 and 1.6M (B) 3 and 64K (C) 4 and 1.6M (D) 4 and 64K	_	][2M]					
14. If the length of the bus signal increases, the system performance(A) remains same (B) increases (C) decreases (D) none of these.	[	 ][1M]					
15. PCI to ISA controller is a bridge between(A) Resident bus to Medium speed bus (B) Medium speed bus to Low s (C)Low speed bus to System bus (D) Resident local bus to System bus.							
16 transfer is/are also known as bus pipelini. (A) Burst (B) Bundle (C) Split (D) All of these.	ng. [	][1M]					
17. Which ISA bus works at a maximum speed of 8 MHz. (A) 8 bit (B) 16 bit (C) 32 bit (D) All of these.	[	][1 <b>M</b> ]					
18. If a daughter board wants to raise an interrupt, you can do it by asserting the							
Iine. (A) IRQ 0 (B) IRQ 1 (C) IRQ 8 (D) IRQ 9	[	][1M]					

## SET 'B'

### BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI **Hyderabad Campus, Second Semester 2014-2015** CS/ ECE /EEE/ INSTR F241 Microprocessor Programming & Interfacing

	24/04/15		Quiz-3 (Clos Day: Friday		)	Time:	12.00 –	12.30 PM
NAM.	Marks : 20				ID:			
Answ	er all the questions	•						
1.	If a 16- bit coun first?	t is program	nmed into the	8254, whi	ich byt	e of the cou	ınt is pr	ogrammed
	(A) LSB (B) M	SB (C) Both	h bytes at the	same time	;	(D) None	[	][1M]
2.	Where is the inte (A) ICW 1 (	-	type number s (C) ICW 3				[	][1M]
3.	Where a slave IN (A) IR input of th (C) Cascade input	ne Master	(B) II	NTR input	t of the	processor	stem?	][1 <b>M</b> ]
4.	Which of the microprocessor? (A) Interfacing (I	_	-	-		nize an I/O	device	with the
5.		th a single p	orogramming.				an trans	efer up to
6.	If the length of the (A) remains same	_		•			[	 ][1M]
7.	PCI to ISA contro (A) Resident bu (C)Low speed b	s to Medium	n speed bus (B					us ][ <b>1M]</b>
8.	(A)Burst (B) Bur	ndle (C) Spli			own as	bus pipelin	ing. [	][1M]
9.	Which ISA bus w (A)8 bit (B) 16 b		1		Z.		[	][1 <b>M</b> ]

10.		board wants to ine.	raise an	interrupt,	you can	do it by	y assert	ting the
			RQ 8	(D) IRQ 9			[	][1M]
11.	Which micropro (A) RESET and	cessor pins are use READY		est and ack	_	a DMA t	ransfer?	,
	(C) HOLD and I	HLDA	(D) No	one of these	<b>;</b>		[	] [1M]
12.		ess lines required to 16 lines (C) 18 l		-	of size 256	6 K is	[	] [1M]
13.	•	tput devices with Latches (C) Both	-				[	][1M]
14.	creation of the fi	ne disk will have the dinterpretable will have the disk will have the disk will have the					date and	time of
15.	(A) whole word	=0 and $A_0$ =1, will /from even address	(B) Hig	gh byte to/f selection	from odd a	address	[	][1M]
16.	1 -	general purpose I/O (B) PB0-PB7 (C)	1	_	1	n of the 8	2C55? [	][1M]
17.		ctor table is always 56K (C) 512K (I		n the first _		area of	f the me	emory. ][1 <b>M</b> ]
18.		the 16550 line co y used and the dat SB ST P	_			given as		
	(A) Even, 6 bits					3 bits	[	][2M]

# SET 'C'

### BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI Hyderabad Campus, Second Semester 2014-2015 CS/ ECE /EEE/ INSTR F241 Microprocessor Programming & Interfacing

Quiz-3 (Closed Book)

	24/04/15 Marks : 20	Day: Friday	Time: 12.00 –	12.30 PM
NAM			D:	
Answ	er all the questions.			
1.	(A)Burst (B) Bundle (C) Sp	transfer is/are also know plit (D) All of these.	vn as bus pipelining.	][1M]
2.	Which ISA bus works at a r (A)8 bit (B) 16 bit (C) 32 b		[	][1 <b>M</b> ]
3.	If a daughter board wan line.	its to raise an interrupt,	you can do it by ass	serting the
		(C) IRQ 8 (D) IRQ	9 [	][1M]
4.	· /	(B) READY and	WAIT	
	(C) HOLD and HLDA	(D) None of thes	e [	] [1M]
5.	The no. of address lines req (A)15 lines (B) 16 lines (		of size 256 K is	] [1M]
6.	Interfacing of output device (A)Buffers (B) Latches (			][1M]
7.	Which part of the disk will creation of the file? (A)Boot sector (B) FAT (6)			and time of
			i storage area.	][1141]
8.		(B) High byte to/	from odd address	][1 <b>M</b> ]
9.	Which pins are general purp (A)PA0 – PA7 (B) PB0-PI			5? ][ <b>1M</b> ]

10.	The interrupt vector table is always created in the first area of	f the me	mory.
	(A) 1K (B) 256K (C) 512K (D) 1M	[	][1M]
11.	The contents of the 16550 line control register shown below is given as the type of parity used and the data length are and		10, then ctively.
	(A) Even, 6 bits (B) Odd, 5 bits (C) Odd, 7 bits (D) Even, 8 bits	[	][2M]
12.	If a 16- bit count is programmed into the 8254, which byte of the count first?	is prog	rammed
	(A) LSB (B) MSB (C) Both bytes at the same time (D) None	[	][1M]
13.	Where is the interrupt vector type number stored in 8259A?		
	(A) ICW 1 (B) ICW 2 (C) ICW 3 (D) ICW 4	[	][1M]
14.	Where a slave INT pin is connected on the Master 8259A in cascade system (A) IR input of the Master (B) INTR input of the processor	m?	
	(C) Cascade input of the master (D) INTA input of the processor	[	][1M]
	Which of the following technique is used to synchronize an I/O d microprocessor?		
	(A) Interfacing (B) Arbitration (C) Handshaking (D) Decoding	[	][1M]
16.	The 8237 DMA controller is channel device and each channel can bytes with a single programming.		r up to
	(A) 3 and 1.6M (B) 3 and 64K (C) 4 and 1.6M (D) 4 and 64K	[	][2M]
17.	If the length of the bus signal increases, the system performance(A) remains same (B) increases (C) decreases (D) none of these.	[	 ][1M]
18.	PCI to ISA controller is a bridge between(A) Resident bus to Medium speed bus (B) Medium speed bus to Low speed	eed bus	
			][1M]