SET 'A'

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE, PILANI
Hyderabad Campus, Second Semester 2014-2015
CS/ ECE /EEE/ INSTR F241 Microprocessor Programming & Interfacing

Quiz-3 (Closed Book)

Date: 24/04/15 **Day: Friday** **Time : 12.00 – 12.30 PM**
Max Marks : 20

NAME: **ID:**

Answer all the questions**.**

1. Which microprocessor pins are used to request and acknowledge a DMA transfer?
   (A) RESET and READY (B) READY and WAIT
   (C) HOLD and HLDA (D) None of these [ ] **[1M]**

2. The no. of address lines required to address a memory of size 256 K is
   (A) 15 lines (B) 16 lines (C) 18 lines (D) 14 lines [ ] **[1M]**

3. Interfacing of output devices with microprocessor requires _____
   (A) Buffers (B) Latches (C) Both (A) & (B) (D) None. [ ]**[1M]**

4. Which part of the disk will have the information about the name, length, date and time of creation of the file?
   (A) Boot sector (B) FAT (C) Root directory (D) Data storage area. [ ]**[1M]**

5. The lines BHE'=0 and A_0 =1, will select_____
   (A) whole word (B) High byte to/from odd address
   (C) Low byte to/from even address (D) No selection [ ]**[1M]**

6. Which pins are general purpose I/O pins during mode-2 operation of the 82C55?
   (A) PA0 – PA7 (B) PB0-PB7 (C) PC0-PC3 (D) PC4-PC7 [ ]**[1M]**

7. The interrupt vector table is always created in the first _____ area of the memory.
   (A) 1K (B) 256K (C) 512K (D) 1M [ ]**[1M]**

8. The contents of the 16550 line control register shown below is given as 10001010, then the type of parity used and the data length are _____ and _____ respectively.

DL	SB	ST	P	PE	S	L1	L0

   (A) Even, 6 bits (B) Odd, 5 bits (C) Odd, 7 bits (D) Even, 8 bits [ ]**[2M]**

9. If a 16- bit count is programmed into the 8254, which byte of the count is programmed first?
   (A) LSB (B) MSB (C) Both bytes at the same time (D) None [ ]**[1M]**

10. Where is the interrupt vector type number stored in 8259A?
   (A) ICW 1 (B) ICW 2 (C) ICW 3 (D) ICW 4 [ ]**[1M]**

11. Where a slave INT pin is connected on the Master 8259A in cascade system?
   (A) IR input of the Master (B) INTR input of the processor
   (C) Cascade input of the master (D) INTA input of the processor [ ]**[1M]**

12. Which of the following technique is used to synchronize an I/O device with the microprocessor?
   (A) Interfacing (B) Arbitration (C) Handshaking (D) Decoding [ ]**[1M]**

13. The 8237 DMA controller is _____ channel device and each channel can transfer up to _____ bytes with a single programming.
   (A) 3 and 1.6M (B) 3 and 64K (C) 4 and 1.6M (D) 4 and 64K [ ]**[2M]**

14. If the length of the bus signal increases, the system performance _____.
   (A) remains same (B) increases (C) decreases (D) none of these. [ ]**[1M]**

15. PCI to ISA controller is a bridge between _____
   (A) Resident bus to Medium speed bus (B) Medium speed bus to Low speed bus
   (C) Low speed bus to System bus (D) Resident local bus to System bus. [ ]**[1M]**

16. _____ transfer is/are also known as bus pipelining.
   (A) Burst (B) Bundle (C) Split (D) All of these. [ ]**[1M]**

17. Which ISA bus works at a maximum speed of 8 MHz.
   (A) 8 bit (B) 16 bit (C) 32 bit (D) All of these. [ ]**[1M]**

18. If a daughter board wants to raise an interrupt, you can do it by asserting the _____ line.
   (A) IRQ 0 (B) IRQ 1 (C) IRQ 8 (D) IRQ 9 [ ]**[1M]**

SET 'B'

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Answer all the questions**.**

1. If a 16- bit count is programmed into the 8254, which byte of the count is programmed first?

   (A) LSB (B) MSB (C) Both bytes at the same time (D) None [ ]**[1M]**

2. Where is the interrupt vector type number stored in 8259A?
   (A) ICW 1 (B) ICW 2 (C) ICW 3 (D) ICW 4 [ ]**[1M]**

3. Where a slave INT pin is connected on the Master 8259A in cascade system?
   (A) IR input of the Master (B) INTR input of the processor
   (C) Cascade input of the master (D) INTA input of the processor [ ]**[1M]**

4. Which of the following technique is used to synchronize an I/O device with the microprocessor?
   (A) Interfacing (B) Arbitration (C) Handshaking (D) Decoding [ ]**[1M]**

5. The 8237 DMA controller is _____ channel device and each channel can transfer up to _____bytes with a single programming.
   (A) 3 and 1.6M (B) 3 and 64K (C) 4 and 1.6M (D) 4 and 64K [ ]**[2M]**

6. If the length of the bus signal increases, the system performance _____.
   (A) remains same (B) increases (C) decreases (D) none of these. [ ]**[1M]**

7. PCI to ISA controller is a bridge between _____
   (A) Resident bus to Medium speed bus (B) Medium speed bus to Low speed bus
   (C)Low speed bus to System bus (D) Resident local bus to System bus. [ ]**[1M]**

8. _____ transfer is/are also known as bus pipelining.
   (A)Burst (B) Bundle (C) Split (D) All of these. [ ]**[1M]**

9. Which ISA bus works at a maximum speed of 8 MHz.
   (A)8 bit (B) 16 bit (C) 32 bit (D) All of these. [ ]**[1M]**

10. If a daughter board wants to raise an interrupt, you can do it by asserting the _____ line.
(A)IRQ 0 (B) IRQ 1 (C) IRQ 8 (D) IRQ 9 [ ]**[1M]**

11. Which microprocessor pins are used to request and acknowledge a DMA transfer?
(A) RESET and READY (B) READY and WAIT
(C) HOLD and HLDA (D) None of these [ ] **[1M]**

12. The no. of address lines required to address a memory of size 256 K is
(A)15 lines (B) 16 lines (C) 18 lines (D) 14 lines [ ] **[1M]**

13. Interfacing of output devices with microprocessor requires _____
(A)Buffers (B) Latches (C) Both (A) & (B) (D) None. [ ]**[1M]**

14. Which part of the disk will have the information about the name, length, date and time of creation of the file?
(A)Boot sector (B) FAT (C) Root directory (D) Data storage area. [ ]**[1M]**

15. The lines BHE'=0 and A_0 =1, will select_____
(A) whole word (B) High byte to/from odd address
(C) Low byte to/from even address (D) No selection [ ]**[1M]**

16. Which pins are general purpose I/O pins during mode-2 operation of the 82C55?
(A)PA0 – PA7 (B) PB0-PB7 (C) PC0-PC3 (D) PC4-PC7 [ ]**[1M]**

17. The interrupt vector table is always created in the first _____ area of the memory.
(A) 1K (B) 256K (C) 512K (D) 1M [ ]**[1M]**

18. The contents of the 16550 line control register shown below is given as 10001010, then the type of parity used and the data length are _____ and _____ respectively.

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(A) Even, 6 bits (B) Odd, 5 bits (C) Odd, 7 bits (D) Even, 8 bits [ ]**[2M]**

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Answer all the questions**.**

1. _____ transfer is/are also known as bus pipelining.
   (A)Burst (B) Bundle (C) Split (D) All of these. [ ]**[1M]**

2. Which ISA bus works at a maximum speed of 8 MHz.
   (A)8 bit (B) 16 bit (C) 32 bit (D) All of these. [ ]**[1M]**

3. If a daughter board wants to raise an interrupt, you can do it by asserting the _____ line.
   (A)IRQ 0 (B) IRQ 1 (C) IRQ 8 (D) IRQ 9 [ ]**[1M]**

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   (A) RESET and READY (B) READY and WAIT
   (C) HOLD and HLDA (D) None of these [ ] **[1M]**

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   (A)15 lines (B) 16 lines (C) 18 lines (D) 14 lines [ ] **[1M]**

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   (A)Buffers (B) Latches (C) Both (A) & (B) (D) None. [ ]**[1M]**

7. Which part of the disk will have the information about the name, length, date and time of creation of the file?
   (A)Boot sector (B) FAT (C) Root directory (D) Data storage area. [ ]**[1M]**

8. The lines BHE'=0 and A_0 =1, will select_____
   (A) whole word (B) High byte to/from odd address
   (C) Low byte to/from even address (D) No selection [ ]**[1M]**

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   (A)PA0 – PA7 (B) PB0-PB7 (C) PC0-PC3 (D) PC4-PC7 [ ]**[1M]**

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