Birla Institute of Technology and Science Pilani, Hyderabad Campus

II Semester 2015-2016

CS/ECE/EEE/INSTR F241/ Microprocessor Programming and Interfacing

Comprehensive Examination

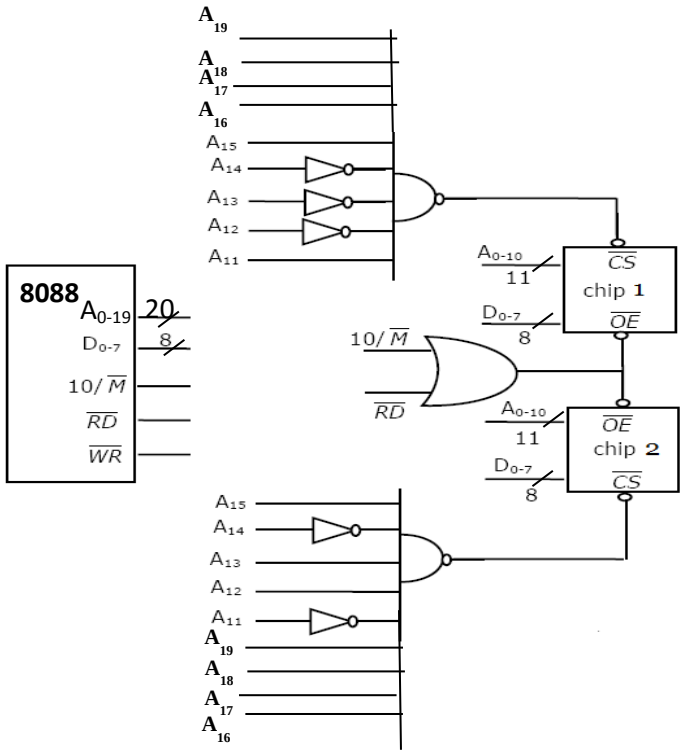
Part B (Open Book)

Time: 2Hrs **Date: 12/05/2016** **MM: 80**

1. Determine the instruction from the opcode, assuming the processor is working in 32-bit mode.
   (a) 67 8B 04 4B
   (b) 66 B9 00 00 00 12 [4M]

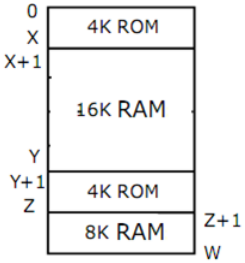
2. Write a program to convert a 16 bit binary number into its equivalent BCD number. [8M]

3. (a) What is the total size of each memory chip in the circuit given in Fig. 1?
   (b) What are the beginning and ending addresses of the memory in chip 1?
   (c) What are the beginning and ending addresses of the memory in chip 2?
   (d) Are the memory chips in the circuit ROM or RAM?
   (e) How will you replace the two NAND gates circuit with one 3 to 8 decoder without changing the memory size or the memory addresses? Assume that the decoder is 74LS138.Use absolute addressing (use extra logic gates if required) [2+2+2+1+5M]



4. A hypothetical CPU has a parallel address bus, a parallel data bus, a RD and WR active LOW signals. Two ROMs of size 4K words each and two RAMs of sizes 16K and 8K words, respectively, are to be connected to the CPU. The memories are to be so connected that they fill the address space of the CPU as per the memory map shown in the figure. Assuming the chip select signals are active LOW. [1+4+3M]

   a. What is the number of lines in the address bus of the CPU?
   b. Determine the values of address X, Y, Z and W in hexadecimal format.
   c. Using a 2 to 4 decoder and some additional gates, draw a circuit for the decoding logic.



5. Interface an 8255 with a 8086 to work as an I/O port. Initialize port A as output port, port B as an input port and port C as an output port. Port A address should be 0740H . Read the status of the switches SW_0 to SW_7. The sensed pattern is to be displayed on port A to which 8 LEDs are connected, while the port C lower displays the number of ON switches out of the total 8 switches. [10M]
(a) Write an ALP for this task.
(b) Draw the schematic showing the required hardware including the selection lines and address lines.

6. Design a programmable timer using 8254 and 8086 . Interface 8254 at an address 0040H for counter 0 and write the following ALPs.The 8086 and 8254 run at 6MHz and 1.5 MHz respectively. [14M]
(a) To generate a square wave of 1ms from counter 0.
(b) To interrupt the processor after 10 ms using counter 1.
(c) To derive a monoshot pulse with quasi stable state duration of 5 ms from counter 2.

7. Interface three IC s of 8259 PIC with 8086 system in such a way that one is master and the rest two are slaves connected at IR_3 and IR_6 interrupt request level of the master. The 8259s are having vector addresses 60H, 70H, and 80H .Initialize 8259 master in level triggered mode ,buffered , special fully nested mode. Write a program to initialize 8259 PIC so that IR_2 and IR_7 levels of master are masked. Initialize master in rotate in automatic EOI mode (set). [12M]

8. From the 8 byte 80386 descriptor given as FF **9F 93 00 50 45 FF FF.** [3M]
   (a) what will be the starting address and limit of the segment in memory
   (b) what is the size of the segment?
   (Descriptor is given in BIG ENDIAN FORMAT (i.e.) MSB onwards)

In 80286, if DS contains 0020H in protected mode, determine the descriptor table and descriptor number it refers. From the resulted 8 byte 80286 descriptor, find out the base address of the segment in memory and the size of the segment? Determine the physical address of the ending memory location? Also write the type of Segment , Protection Level (access byte information) etc . If we execute an instruction ADD BX, [000EH] for the same information given above then what will be the physical address of the memory location given in the instruction. **[9M]**

[The Descriptor tables are given below, Assume that the first table is GDT (where descriptor 0 address is 100000) and second table is LDT {the descriptor 0 (0^{th} descriptor) address is 010000}]

GDT

Address	Data							
100000	00	00	91	CD	00	00	1A	4E
100008	00	00	82	01	00	00	FF	FF
100010	00	00	82	20	00	00	FF	FF
100018	00	00	83	03	00	00	00	3F
100020	00	00	FC	0A	00	00	00	1F
100028	00	00	DF	B0	00	00	01	FF
100030	00	00	92	B1	00	00	0F	FF
100038	00	00	B2	7B	00	00	03	FF
100040	00	00	D2	7A	00	00	07	FF
100048	00	00	9F	A1	00	00	1F	FF

LDT

Address	Data							
010000	00	00	82	01	00	00	FF	FF
010008	00	00	82	20	00	00	FF	FF
010010	00	00	83	03	00	00	00	3F
010018	00	00	FC	0A	00	00	00	1F
010020	00	00	DF	B0	00	00	01	FF
010028	00	00	92	B1	00	00	0F	FF
010030	00	00	B2	7B	00	00	03	FF
010038	00	00	D2	7A	00	00	07	FF
010040	00	00	9F	A1	00	00	1F	FF
010048	00	00	B3	A3	00	00	3F	FF
010050	00	00	B3	B1	00	00	FF	FF
010058	00	00	82	50	00	00	1F	FF