Birla Institute of Technology and Science Pilani, Hyderabad Campus
II Semester 2014-2015
EEE/CS/INSTR F241/ Microprocessor Programming and Interfacing
Comprehensive Examination
Part B (Open Book)

Time: 2Hrs Date: 10/05/2015 MM: 60

Answer all parts of the question together

Q1. Suppose that DS=2345H , ESI=0000 5411H , EBX=0000437AH, EAX=00003000H For the instructions given below determine the machine code & addressing mode. Processor is working in 32-bit mode.

a) MOV [2344 $_H$], BH
b) MOV [SI+2156$_H$], ECX
c) MOV [EBX+2*ESI], DH
d) MOV DL , [EBX+4*ECX+4000$_H$] [**8]**

Q2. Write a program to scan the given word "HYDERABAD'' and replace the character 'D' by the character 'B'. **[7]**

Q3. Design an 8086 based system with the following memory requirements
a. 256K of ROM starting from 20000_H
b. 256K of RAM starting from 60000_H
c. 256K of ROM starting from $A0000_H$ **[15]**

Show the complete memory mapping and design the memory interfacing circuit using the chips mentioned in the table given below. All system bus signals (MEMR', MEMW', IOR', IOW', BHE', A_0- A_{19}, $D_0 - D_{15}$) are available. Use Absolute Addressing.

Use external logic gate(s), if required.

Chips Available	Nos.
64 K ROM	8
128 K RAM	2
LS138	2

Q4. a) The input frequency to the timer chip is 3.5 MHz. Generate a square wave of 12.5 KHz from counter 0, and use counter 2 to get an asymmetric output waveform. **Show the complete program including the control words and counts.**

b) A system is to be designed to measure the traffic rate on a road. A weight sensor is used to generate a pulse whenever a vehicle's wheel passes over it. Assume the roads are not crowded and there is sufficient gap between the arrivals of vehicle. **Design a system which detects and keeps the count of vehicles passed. Show the complete hardware diagram along with the program.** (Note: For each vehicle two pulses will be generated for front wheel and rear wheel and the pulses can be counted using 8254) **[5+8]**

Q5. The following data is present in memory of size 32 locations

Memory Address	Data	Memory Address	Data	Memory Address	Data	Memory Address	Data
00000	56	01000	53	10000	A5	11000	45
00001	65	01001	65	10001	C2	11001	46
00010	23	01010	A2	10010	48	11010	49
00011	11	01011	41	10011	27	11011	57
00100	26	01100	2C	10100	52	11100	5D
00101	57	01101	67	10101	94	11101	9C
00110	44	01110	B4	10110	F6	11110	36
00111	80	01111	F0	10111	5B	11111	6B

If the data is read by the processor in the following order from the addresses 00001, 00100, 01001, 01010, 11010, 11001. **[9]**

a) Show the contents of the cache step by step for direct-mapped; Eight line cache with each read operation.

b) Repeat the same for a four-way set associative, eight line cache after each read operation.

c) Indicate the type of miss for each read operation and compare the number of total miss in (a) and (b).Which method is better and why?

Q6. Processor – 80286, GDTR – 500000_H, Current CPL –01,

CALL 0021_H , [0700_H]

Find the DPL, type of segment descriptor and the physical address . **[8]**

GDT

Address	Data							
500008	00	00	82	01	00	20	FF	FF
500010	00	00	93	20	00	23	00	7F
500018	00	00	83	03	00	24	00	2F
500020	00	00	A8	0A	00	29	34	3F
500028	00	00	DF	B0	00	15	01	4F
500030	00	00	92	B1	00	67	0F	6F
500038	00	00	BF	82	16	24	3F	3F
500040	00	00	D2	13	00	22	07	1F
500048	00	00	9F	BC	00	12	1F	3F
500050	00	00	C4	1D	00	38	10	00
500058	00	00	85	13	00	20	00	00
500060	00	00	B3	50	00	11	1F	FF

LDT

Address	Data							
050000	00	00	82	01	00	00	FF	FF
050008	00	00	93	20	00	00	00	7F
050010	00	00	83	03	00	00	00	3F
050018	00	00	A1	0A	00	00	00	1F
050020	00	00	DF	B0	00	00	01	FF
050028	00	00	92	B1	00	00	0F	FF
050030	00	00	BF	7B	00	00	3F	FF
050038	00	00	D2	7A	00	00	07	FF
050040	00	00	9F	A1	00	00	1F	FF
050048	00	00	C4	02	00	38	10	00
050050	00	00	85	00	00	20	00	00
050058	00	00	B3	50	00	00	1F	FF