Birla Institute of Technology and Science Pilani, Hyderabad Campus
II Semester 2014-2015
EEE/ECE/CS/INSTR F241/ Microprocessor Programming and Interfacing
Comprehensive Examination- Part A (Open Book)

Time: 60 min. **D ate: 10-5-2015** **MM: 30**

(Note: Answer Part A on the Q-Paper itself and Part B on a separate answer sheet provided.)

ID No.:	**Name:**

Q1. If the input frequency to a timer is 1.5 MHz then what will be the count and control word to generate a waveform of 750 Hz with 50 % of duty cycle using counter 2? **[2]**

Q2. The memory location 2080H contains 16 bits of data. Write down the code to mask off the lower nibble of upper byte of the data. **[2]**

Q3. In a memory location 5000H a data is stored. Write the code to check the data whether it is positive or negative. If it is a positive number then store 00H in the location 5050H and if it is negative then store 01H in the location 5051H.

[**2]**

Q4. How to set an 80486 processor from the real mode to protected mode and again back to real mode from the protected mode? Which instruction is used to change a real mode to protected mode? **[2]**

Q5. What is Segments Relocatibility in 80286, 386 and 486? **[2]**

Q6. For an 80286 processor having the Access right byte 10111001, give the description of the nature of the segment. Write the privilege levels of the application that are allowed to access this segment. **[2]**

Q7. The initial contents of the registers are as shown below.

AX= 2345H , BX=1111H, DS=1000H, ES=2000H, SI=1000H DI= 1200H. Indicate the contents of registers after the execution of following lines of code. The contents of memory locations are as follows. **[4]**

Memory address	Data
10FFF	12
11000	34
11001	B1

Memory address	Data
211FF	24
21200	C2
21201	AB

ADD BX, AX
CLD
LODSW

Ans:

AX	
BX	
SI	
DI	

Q8. Determine the instructions from the opcodes given below. Assume the processor is working in 16-bit mode.

a) 66 89 90 00 02 **[2]**

b) 2E 8B 9D 00 20 **[2]**

Q9. Write the difference between write through and write back mechanisms of cache. Which one is used in 80486? **[2]**

Q10. What is burst transfer in 80486 processor and how many clock cycles are required to complete this process? Is it a slow process or fast process? **[2]**

Q11. Which method is used in 80386 and 80486 to avoid the wait state and how the process is done? **[2]**

Q12. What is LOCK'? Describe its function using an example? **[2]**

Q13. Contrast the operation of an instruction **JMP DI** with **JMP [DI]**. **[2]**