Birla Institute of Technology and Science, Pilani
II Semester 2014-2015
CS/ECEEEE/INSTR F241 Microprocessor Programming and Interfacing
Test-2 (Open Book)

Time: 1 Hr **Date: 22-03-2014** **MM: 40**

Q1. Design an 80286 based system that has the following memory requirements:

1 M of ROM from 000000_H
1 M of ROM from 800000_H
1 M of ROM from $F00000_H$
7 M of RAM from 100000_H
3 M of RAM from 900000_H

Chips available:

512K ROM chip	6 nos.
512K RAM chip	20 nos.
LS138	4 nos.

Show the complete memory mapping and design the memory decoding circuit ***using only the chips given***. All system bus signals (MEMR', MEMW', IOR', IOW' BHE', A_0- A_{23}, D_0 – D_{15}) are available. **Use absolute addressing. Show the complete memory interfacing circuit. [30]**

Q2. Using 8255 BSR generate a square waveform of frequency of 2 KHz on PC_0. 8255 base address is 00_H. Write the software segment for programming 8255 to generate the waveform. You can assume that there is a delay routine (delay250) available for generating a delay of 250μs. You need ***not*** show the hardware interfacing circuit. **[6]**

Q3. From the 8 byte 80386 descriptor given below (a) what will be the starting address of the segment in memory and (b) what is the size of the segment in bytes? (Descriptor is given in BIG ENDIAN FORMAT (i.e.) MSB onwards)

A2 5F B7 00 00 00 FF FF **[4]**