Maharashtra Institute of Technology, Aurangabad Department of Computer Science & Engineering

Class : SYCSE Subject: Digital Electronics & Microprocessor

Unit-I Number Systems & Codes

Questi	ons of 2 marks			
Q. No.	Question	BL level	Domain	
1	Perform the subtraction using 2's complement 11011 - 11001	BL-3	Apply	
2	Convert binary number 110100 into Gray code	BL-1,2	Remember, Understand	
3	Convert octal number (247.36)8 into equivalent hex number	BL-2	Understand	
4	Represent decimal numbers in 2's complement format a) -5 b) -9	BL-1	Remember	
5	Determine the binary numbers represented by decimal numbers a) 35 b) 15.65	BL-1,2	Remember, Understand	
6	Convert gray code 1101 into binary number	BL-1	Remember	
7	Classify the types of codes	BL-1	Remember	
8	Perform the addition using Excess-3 code (4)10+(3)10	BL-3	Apply	
9	Define Excess-3 & Gray code	BL-1	Remember	
10	Subtract 14 from 25 using 8-bit 1's complement arithmetic	BL-3	Apply	
Questi	ons of 4 Marks			
11	Give classification & explain types of codes	BL-2	Remember	
12	Write a short note on Exces-3 code & Gray code	BL-1	Remember	
13	Explain non-weighted codes & weighted codes	BL-1,2	Remember, Understand	
14	Describe ACSII & EBCDIC codes	BL-1	Remember	
15	Explain the types of codes			

2 Marks

- Q.No. 1) Perform binary addition i) $(1101)_2 + (1111)_2$ ii) $(1011)_2 + (1100)_2$ iii) $(0101)_2 + (1111)_2$ iv) $(101010.111)_2 + (10110.101)_2$
- Q No. 2) Perform subtraction using 1's & 2's complement i) 11011101- 1010 ii) 11110110 110111 iii) (25)10-(17)10 iv) (35)10-(48)10 v) (53)10-(37)10
- Q. No. 3) Define weighted & Non-weighted code
- Q. No. 4) Questions based on all number system conversions
- Q.No. 5) Questions based on Gray code to binary code conversions & vice-versa, addition using Excess-3 code.

Unit-2 Logic Gates & Boolean Algebra

Ques	stions of 2 Marks	9		
Q. No.	Question	BL level	Domain	
1	What are universal logic gates?	BL-1	Remember	
2	Describe the EX-OR & EX-NOR logic with truth table.	1,2	Remember, Understand	
3	Define with example Analog system & Digital system	1,2	Remember, Understand	
4	Define switching circuit & give its types	1,2	Remember, Understand	
5	What is logic design? Design logic for AND, OR & NOT and also write truth table	1,2	Remember, Understand	
6	Define truth table with example	1,2	Remember, Understand	
7	Give applications of logic gates	1	Remember	
8	Identify logic gates i) All low inputs produce high output ii) Output is low if and only if all inputs are high iii) Output is high if and only if all inputs are high iv) output is low if and only if all inputs are low v) output is high if and only if odd number of inputs are 1	1,2	Remember, Understand	
9	Which gate is inequality detector & why?	1,2	Remember, Understand	
10	Which gate is equality detector & why?			
11	What are the applications of EX-OR gates	1	Remember	
Ques	stions for 4 Marks			
11	State & Explain De-Morgan's Therom	1	Remember	
12	Simplify expression by applying De-Morgans Therom i) (A+(BC)')'	BL-3	Apply	
13	Simplify the logic expression by using boolean algebra i) ({AB)'(CD+E'F)((AB)'+(CD)')' ii) A(B+C'(AB+AC')')	BL-3	Apply	
14	Show that i) AB+AB'C+BC=AC+BC' ii) AB'C+B+BD'+ABD'+A'C=B+C	BL-3	Apply	
15	Realize AND,OR & NOT gate using universal gates	BT-2	Understanding	
16	Draw a logic circuit for the expression i) (AB)'(CD)(C+D+(EF)'+G')' ii) A'BC'+AD+AC'D iii) (A+C)(A'+B') iv) ABC+A'D' v) (A+B)(A'+B')	BT-4	Analyze	
Ques	stions of 8 Marks			
1	Evaluate the boolean expression using boolean algebra & implement it by using logic gates i) f(W,X,Y,Z)= (W+WX'+YZ)' ii) f(A,B,C,D)=((A+BC')'+(AB'C+ABCD')'+A'D)' iii) f=A[B+C'(AB+AC')'] iv) f=AB'+ABD+ABD'+A'C'D'+A'BC' IV) BD+BCD'+AB'C'D' V) F=X'Y'+XY+X'Y VI) (A+(BC)')'((AB)'+(ABC)') VII)AB+ABC+AB(E+F) Reduce the following expression & implement reduced expression using logic gates i) XY'Z+X'YZ+XYZ ii) (A'B+A'+AB)' iii) AB+A'C+AB'C(AB+C) iv) WX'+	BT-5	Evaluate	
2	(W+Y)+WY(W+X') iv) Reduce the following expressions & Implement by using	рт	Apply Applyac	
2	Reduce the following expressions & Implement by using	BT-	Apply, Analyze	

	NAND gate or NOR gate only i) AB+(AC)'+AB'C+ (AB+C) ii) (A+BC+AC'+B'C)' iii) (A+BC+AC'+BC)' iv) Y=(AB+BC)C v) Y=((AB)'+(A+B)')AB'	3,4	
3	Prove the following i) A'BC+AB'C+ABC'+ABC=AB+BC+AC ii) (W[X+Y(Z+W')])'=W'+(XY)'+(XZ)' iii) AB+A'C+BC=AB+A'C iv) A+A'B+AB'=A+B	BT-3	Apply
4	Study the logic circuit above i) What should be the input to make output X high ii) justify the answer by giving output of each gate	BT-4	Analyze

Unit-3 Combinational & Sequential Logic Circuit (CO2)

Questions of 2 Marks					
Q. No.	Question	BL- Level	Domain		
1	Define & give example of standard SOP form.	BL-1	Remember		
2	What is Combinational Logic Circuit?	BL-1	Remember		
3	Define & give example of Canonical SOP & POS form.	BL-1,2	Remember, Understand		
4	Define minterm & maxterm with example	BL-1	Remember		
5	Convert the expression AB+ABC+A to canonical SOP form	BL-2	Understand		
6	State the Sequential logic circuit with example.	BL-1	Remember		
7	Differentiate Combinational & Sequential logic circuits	BL-4	Analyze		
8	Enlist the types of Combinational Circuits	BL-1	Remember		
9	Enlist the Types of Sequential Logic Circuits	BL-1	Remember		
10	Draw a logic circuit of 2:1 & 4:1 MUX	BL-2 Understand			
11	Enlist the types of Flip-Flops	BL-1	Remember		
12	Draw a logic circuit of i) R-S & ii) J-K Flip-Flop	BL-2	Understand		
13	Convert the following expression to POS Y=AB+ (ABC)'+A'BC ii) Y=AB'+A'C'++B'C	BL-2	Understand		
14	Convert the expression to SOP i) Y=(A+B)(A'+B'+C')	Bl-2	Understand		
Questi	ons of 4 & 8 Marks	•			
1	Minimize the following logic function using K-map & realize using logic gates $ \begin{array}{ccc} \text{i)} & F(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14,15) \\ \text{ii)} & F(A,B,C,D) = \prod M(0,1,2,3,8,9,10,11,14,15) \\ \text{iii)} & F(A,B,C,D) = \prod M(1,3,5,7,8,9,14,15) \\ \text{iv)} & F(A,B,C,D) = \prod M(0,2,4,6,8,10).d(1,3,57) \\ \text{v)} \end{array} $	BL-3	Apply		
2	Represent the expression using K-map i) $Y=A'B'C'+ABC+AB'C+A'BC$ ii) $A'BC'D+A'B'C'D'+ABC'D'+A'B'CD+AB$ CD' iii) $Y=\sum m(0,1,5,7,11,13,14)$	BL-4	Analyze		

3 Minimize the following expression using K-map i) F(A,B,C,D)=∑m(1,3,5,10,11,12,13,14,15) ii) F(A,B,C,D)=∑m(1,3,5,8,9,11,15)+d(2,13) BL-3 Apply 4 Realize the full adder using i) NAND gate only ii) NOR gate only BL-3 Apply 5 Realize the Half Adder & Full Adder logic circuits BL-3 Apply 6 Realize the Half Subtractor & Full Subtractor logic circuits BL-3 Apply 7 Realize the Half & Full Subtractor using i) NAND gate only ii) NOR gate only ii) NOR gate only ii) NOR gate only ii) NOR gate only iii) All MUX iii) 4:1 MUX iii) 1:2 DEMUX using logic gates i) 1:2 DEMUX iii) 1:3 DEMUX iii) 1:4 DEMUX iii) 1:4 DEMUX iii) 1:4 DEMUX iii) 1:5 DEMUX iii) 1:8 DEMUX BL-3 Apply 10 Implement the following functions by using 8:1 MUX iii) 1:8 DEMUX iii) 1:8 DEMUX BL-4 Analyze 11 Implement Full Adder using 8:1 MUX iii F=[M(1,2,3,4) BL-4 Analyze 12 Implement the following function using 8:1 MUX iii F=[M(1,3,5,7,9,14,15) BL-4 Analyze 15 Distinguish the Combinational & Sequential logic circuits BL-2 Understand circuits 16 Design & verify the truth table of different flip-flops BL-3 Apply 17 Explain the S-R & J-K flip-flop working in detail <t< th=""><th></th><th></th><th></th><th></th></t<>				
gate only 5 Realize the Half Adder & Full Adder logic circuits 6 Realize the Half Subtractor & Full Subtractor logic circuits 7 Realize the Half & Full Subtractor using i) NAND gate only ii) NOR gate only 8 Design the following MUX using logic gates i) 2:1 MUX ii) 4:1 MUX iii) 4:1 MUX iii) 8:1 MUX 9 Design the following DEMUX using logic gates i) 1:2 DEMUX ii) 1:3 DEMUX iii) 1:8 DEMUX 10 Implement the following functions by using 8:1 Multiplexer i) F=∑m(0,2,4,6) ii) F=∏M(1,2,3,4) 11 Implement Full Adder using 8:1 MUX 12 Implement Full Subtractor using 8:1 MUX 13 Implement the following function using 8:1 MUX 14 Implement the following function using 4:1 MUX ii) F=∑m(1,3,5,7,9,14,15) 14 Implement the following function using 4:1 MUX i) F=∑m(1,3,7)+d(2,5) 15 Distinguish the Combinational & Sequential logic circuits 16 Design & verify the truth table of different flip-flops 17 Explain the S-R & J-K flip-flop working in detail 18 Minimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates i) F(A,B,C,D)=∑m(1,3,7,8,9,11,15) iii) F(A,B,C,D)=∑m(1,3,7,8,9,11,15)	3	i) $F(A,B,C,D)=\sum m(1,3,5,10,11,12,13,14,15)$ ii) $F(A,B,C,D)=\prod M(2,7,8,9,10,12)$	BL-3	Apply
6 Realize the Half Subtractor & Full Subtractor logic circuits 7 Realize the Half & Full Subtractor using i) NAND gate only ii) NOR gate only 8 Design the following MUX using logic gates i) 2:1 MUX ii) 4:1 MUX iii) 8:1 MUX 9 Design the following DEMUX using logic gates i) 1:2 DEMUX iii) 1:3 DEMUX iii) 1:4 DEMUX iii) 1:8 DEMUX 10 Implement the following functions by using 8:1 Multiplexer i) F=∑m(0,2,4,6) ii) F=∏M(1,2,3,4) 11 Implement Full Adder using 8:1 MUX 12 Implement Full Subtractor using 8:1 MUX 13 Implement the following function using 8:1 MUX 14 Implement the following function using 8:1 MUX 15 Implement the following function using 8:1 MUX 16 Implement the following function using 8:1 MUX 17 Explain the Combinational & Sequential logic circuits 18 Design & verify the truth table of different flip-flops 19 Explain the S-R & J-K flip-flop working in detail 10 Design & verify the truth table of different flip-flops 11 Explain the S-R & J-K flip-flop working in detail 12 Dintimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates i) F(A,B,C,D)=∑m(1,3,7,8,9,11,15) iii) F(A,B,C,D)=∑m(1,3,7,8,9,11,15) iii) F(A,B,C,D)=∑m(1,3,5,8,9,11,15) iii) F(A,B,C,D)=∑m(0,2,4,6,8,9,12,15) iii) F(A,B,C,D)=∑m(1,3,5,8,9,11,15) iii) F(A,B,C,D)=∑m(1,3,5,10,12,13,14,15)	4		BL-3	Apply
circuits 7 Realize the Half & Full Subtractor using i) NAND gate only ii) NOR gate only 8 Design the following MUX using logic gates i) 2:1 MUX ii) 4:1 MUX iii) 8:1 MUX 9 Design the following DEMUX using logic gates i) 1:2 DEMUX ii) 1:3 DEMUX iii) 1:4 DEMUX iii) 1:8 DEMUX 10 Implement the following functions by using 8:1 Multiplexer i) $F = \sum m(0, 2, 4, 6)$ ii) $F = \prod M(1, 2, 3, 4)$ 11 Implement Full Adder using 8:1 MUX 12 Implement Full Subtractor using 8:1 MUX 13 Implement the following function using 8:1 MUX 14 Implement the following function using 8:1 MUX 15 Implement the following function using 8:1 MUX 16 Implement the following function using 8:1 MUX 17 Explain the Combinational & Sequential logic circuits 18 Design & verify the truth table of different flip-flops 19 Explain the S-R & J-K flip-flop working in detail 10 Design & verify the truth table of different flip-flops 11 Explain the S-R & J-K flip-flop working in detail 12 Minimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates i) $F(A,B,C,D) = \sum m(1,3,7,8,9,11,15)$ iii) $F(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$ iii) $F(A,B,C,D) = \sum m(0,2,4,6,8,9,12,15)$	5	Realize the Half Adder & Full Adder logic circuits	BL-3	Apply
only ii) NOR gate only 8 Design the following MUX using logic gates i) 2:1 MUX ii) 4:1 MUX iii) 8:1 MUX 9 Design the following DEMUX using logic gates i) 1:2 DEMUX ii) 1:4 DEMUX iii) 1:4 DEMUX iii) 1:8 DEMUX 10 Implement the following functions by using 8:1 MUX 11 Implement Full Adder using 8:1 MUX 12 Implement Full Subtractor using 8:1 MUX 13 Implement the following function using 8:1 MUX 14 Implement the following function using 8:1 MUX 15 Implement the following function using 8:1 MUX 16 Implement the following function using 8:1 MUX 17 Implement the following function using 4:1 MUX 18 Implement the following function using 4:1 MUX 19 F(A,B,C)= \sum m(1,3,7)+d(2,5) 19 Distinguish the Combinational & Sequential logic circuits 10 Design & verify the truth table of different flip-flops 11 Explain the S-R & J-K flip-flop working in detail 12 Minimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates i) F(A,B,C,D)= \sum m(0,1,3,7,8,9,11,15) ii) F(A,B,C,D)= \sum m(0,1,3,5,8,9,11,15) iii) F(A,B,C,D)= \sum m(0,2,4,6,8,9,12,15) iv) F(A,B,C,D)= \sum m(0,2,4,6,8,9,12,15) iv) F(A,B,C,D)= \sum m(1,3,5,10,12,13,14,15)	6		BL-3	Apply
i) 2:1 MUX ii) 4:1 MUX iii) 4:1 MUX iii) 8:1 MUX 9 Design the following DEMUX using logic gates i) 1:2 DEMUX ii) 1:4 DEMUX iii) 1:8 DEMUX 10 Implement the following functions by using 8:1 Multiplexer i) F=∑m(0,2,4,6) ii) F=∏M(1,2,3,4) 11 Implement Full Adder using 8:1 MUX 12 Implement Full Subtractor using 8:1 MUX 13 Implement the following function using 8:1 MUX i) F=∑m(1,3,5,7,9,14,15) 14 Implement the following function using 4:1 MUX i) F(A,B,C)=∑m(1,3,7)+d(2,5) 15 Distinguish the Combinational & Sequential logic circuits 16 Design & verify the truth table of different flip-flops 17 Explain the S-R & J-K flip-flop working in detail 18 Minimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates i) F(A,B,C,D)=∑m(0,1,3,7,8,9,11,15) ii) F(A,B,C,D)=∑m(0,1,3,7,8,9,11,15) iii) F(A,B,C,D)=∑m(0,2,4,6,8,9,12,15) iv) F(A,B,C,D)=∑m(0,2,4,6,8,9,12,15) iv) F(A,B,C,D)=∑m(0,2,4,6,8,9,12,15) iv) F(A,B,C,D)=∑m(1,3,5,10,12,13,14,15)	7		BL-3	Apply
i) 1:2 DEMUX ii) 1:4 DEMUX iii) 1:8 DEMUX 10 Implement the following functions by using 8:1 Multiplexer i) $F=\sum m(0,2,4,6)$ ii) $F=\prod M(1,2,3,4)$ 11 Implement Full Adder using 8:1 MUX 12 Implement Full Subtractor using 8:1 MUX 13 Implement the following function using 8:1 MUX 14 Implement the following function using 4:1 MUX 15 i) $F=\sum m(1,3,5,7,9,14,15)$ 16 Distinguish the Combinational & Sequential logic circuits 17 Circuits 18 Minimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates 19 i) $F(A,B,C,D)=\sum m(0,1,3,7,8,9,11,15)$ 10 ii) $F(A,B,C,D)=\sum m(0,1,3,5,8,9,11,15)$ 11 iii) $F(A,B,C,D)=\sum m(0,2,4,6,8,9,12,15)$ 12 iv) $F(A,B,C,D)=\sum m(0,2,4,6,8,9,12,15)$ 13 iv) $F(A,B,C,D)=\sum m(0,2,4,6,8,9,12,15)$ 14 iv) $F(A,B,C,D)=\sum m(0,2,4,6,8,9,12,15)$	8	i) 2:1 MUX ii) 4:1 MUX	BL-3	Apply
Multiplexer i) $F=\sum m(0,2,4,6)$ ii) $F=\prod M(1,2,3,4)$ 11 Implement Full Adder using 8:1 MUX 12 Implement Full Subtractor using 8:1 MUX 13 Implement the following function using 8:1 MUX 14 Implement the following function using 4:1 MUX 15 i) $F(A,B,C)=\sum m(1,3,7)+d(2,5)$ 16 Design & verify the truth table of different flip-flops 17 Explain the S-R & J-K flip-flop working in detail 18 Minimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates 19 i) $F(A,B,C,D)=\sum m(0,1,3,7,8,9,11,15)$ 10 iii) $F(A,B,C,D)=\sum m(0,2,4,6,8,9,12,15)$ 11 iv) $F(A,B,C,D)=\sum m(0,2,4,6,8,9,12,15)$ 12 iv) $F(A,B,C,D)=\sum m(1,3,5,10,12,13,14,15)$	9	i) 1:2 DEMUX ii) 1:4 DEMUX	BL-3	Apply
Implement Full Subtractor using 8:1 MUX Implement the following function using 8:1 MUX i) $F=\sum m(1,3,5,7,9,14,15)$ BL-4 Analyze i) $F(A,B,C)=\sum m(1,3,7)+d(2,5)$ BL-4 Analyze i) $F(A,B,C)=\sum m(1,3,7)+d(2,5)$ Distinguish the Combinational & Sequential logic circuits BL-2 Understand Circuits Design & verify the truth table of different flip-flops Explain the S-R & J-K flip-flop working in detail Minimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates i) $F(A,B,C,D)=\sum m(0,1,3,7,8,9,11,15)$ ii) $F(A,B,C,D)=\sum m(0,2,4,6,8,9,12,15)$ iv) $F(A,B,C,D)=\sum m(0,2,4,6,8,9,12,15)$ iv) $F(A,B,C,D)=\sum m(1,3,5,10,12,13,14,15)$	10		BL-4	Analyze
Implement the following function using 8:1 MUX i) $F = \sum m(1,3,5,7,9,14,15)$ BL-4 Analyze 14 Implement the following function using 4:1 MUX i) $F(A,B,C) = \sum m(1,3,7) + d(2,5)$ BL-2 Understand 15 Distinguish the Combinational & Sequential logic circuits BL-2 Understand 16 Design & verify the truth table of different flip-flops 17 Explain the S-R & J-K flip-flop working in detail 18 Minimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates i) $F(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$ ii) $F(A,B,C,D) = \sum m(1,3,5,8,9,11,15)$ iii) $F(A,B,C,D) = \sum m(0,2,4,6,8,9,12,15)$ iv) $F(A,B,C,D) = \sum m(1,3,5,10,12,13,14,15)$	11	Implement Full Adder using 8:1 MUX	BL-4	Analyze
i) $F=\sum m(1,3,5,7,9,14,15)$ 14 Implement the following function using 4:1 MUX i) $F(A,B,C)=\sum m(1,3,7)+d(2,5)$ 15 Distinguish the Combinational & Sequential logic circuits 16 Design & verify the truth table of different flip-flops 17 Explain the S-R & J-K flip-flop working in detail 18 Minimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates i) $F(A,B,C,D)=\sum m(0,1,3,7,8,9,11,15)$ ii) $F(A,B,C,D)=\sum m(1,3,5,8,9,11,15)$ iii) $F(A,B,C,D)=\sum m(0,2,4,6,8,9,12,15)$ iv) $F(A,B,C,D)=\sum m(1,3,5,10,12,13,14,15)$	12	Implement Full Subtractor using 8:1 MUX		
i) $F(A,B,C)=\sum m(1,3,7)+d(2,5)$ 15 Distinguish the Combinational & Sequential logic circuits 16 Design & verify the truth table of different flip-flops 17 Explain the S-R & J-K flip-flop working in detail 18 Minimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates i) $F(A,B,C,D)=\sum m(0,1,3,7,8,9,11,15)$ ii) $F(A,B,C,D)=\sum m(1,3,5,8,9,11,15)$ iii) $F(A,B,C,D)=\sum m(0,2,4,6,8,9,12,15)$ iv) $F(A,B,C,D)=\sum m(1,3,5,10,12,13,14,15)$	13	, ,	BL-4	Analyze
circuits 16 Design & verify the truth table of different flip-flops 17 Explain the S-R & J-K flip-flop working in detail 18 Minimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates i) $F(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$ ii) $F(A,B,C,D) = \sum m(1,3,5,8,9,11,15)$ iii) $F(A,B,C,D) = \sum m(0,2,4,6,8,9,12,15)$ iv) $F(A,B,C,D) = \sum m(1,3,5,10,12,13,14,15)$	14		BL-4	Analyze
17 Explain the S-R & J-K flip-flop working in detail BL-3 Apply 18 Minimize the following expression using Quine Mc- Cluskey method & Implement it using logic gates i) $F(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$ ii) $F(A,B,C,D) = \sum m(1,3,5,8,9,11,15)$ iii) $F(A,B,C,D) = \sum m(0,2,4,6,8,9,12,15)$ iv) $F(A,B,C,D) = \sum m(1,3,5,10,12,13,14,15)$	15	1 9	BL-2	Understand
18 Minimize the following expression using Quine Mc-Cluskey method & Implement it using logic gates i) $F(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$ ii) $F(A,B,C,D) = \sum m(1,3,5,8,9,11,15)$ iii) $F(A,B,C,D) = \sum m(0,2,4,6,8,9,12,15)$ iv) $F(A,B,C,D) = \sum m(1,3,5,10,12,13,14,15)$	16	Design & verify the truth table of different flip-flops	BL-3	Apply
Cluskey method & Implement it using logic gates i) $F(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$ ii) $F(A,B,C,D) = \sum m(1,3,5,8,9,11,15)$ iii) $F(A,B,C,D) = \sum m(0,2,4,6,8,9,12,15)$ iv) $F(A,B,C,D) = \sum m(1,3,5,10,12,13,14,15)$	17	Explain the S-R & J-K flip-flop working in detail	BL-3	Apply
Explain the working of different flip-flops	18	Cluskey method & Implement it using logic gates i) $F(A,B,C,D) = \sum m(0,1,3,7,8,9,11,15)$ ii) $F(A,B,C,D) = \sum m(1,3,5,8,9,11,15)$ iii) $F(A,B,C,D) = \sum m(0,2,4,6,8,9,12,15)$		
	19	Explain the working of different flip-flops		

Unit-4 Microprocessor (CO3,4)

Questions of 2 Marks					
Q. No	o. Question			Domain	
1	Define Microprocessor & Draw a block diagram		BL Level BL-1	Remember	
2	What is Microprocessor? Give the power supply & clock		BL-1	Remember	
	frequency of 8085				
3	What are the functions of an accumulator in 8085 & 808	36?	BL-1	Remember	
4	List the 16 – bit registers of 8085 microprocessor		BL-1	Remember	
5	List the allowed register pairs of 8085		BL-1	Remember	
6	Give features of 8086 Microprocessor		BL-1	Remember	
7	What is the role of instruction queue in 8086?		BL-2	Understand	
8	What is the purpose of segment registers in 8086?		BL-2	Understand	
9	Enlist the flag registers of 8086 microprocessor		BL-1	Remember	
10	List the various types of addressing modes		BL-1	Remember	
11	State the significance of LOCK signal in 8086		BL-2	Understand	
12	What is pipelining in 8086?		BL-2	Understand	
13	List any two type of address transfer instructions		BL-4	Analyze	
14	What is bus? Enlist the types of buses		BL-1	Remember	
15	What is the role of different types of buses in		BL-2	Understand	
	microprocessor?				
Ques	tions of 8 Marks				
Q.	Questions			Domain	
No.		Level			
1	Draw & Explain the internal architecture of 8085	BL-1,2	Remem	ber,Understand	
2	Draw a pin diagram & give signal description of 8085				
	microprocessor				
3	Draw & Explain the internal architecture of 8086	BL-1,2		Remember, Understand	
4	Discuss the evolution of microprocessor family	BL-1,2		Remember, Understand	
5	Draw a pin diagram of 8086 microprocessor & Write the	BL-1,2	Remem	Remember, Understand	
	functions of each pin				
6	Describe the addressing modes of 8086 microprocessor	BL-1,2	_	ber,Understand	
7	Describe the Instruction set of 8086 microprocessor			ber,Understand	
8	Write an assembly language program for 8-bit addition & 16-bit addition in 8086 microprocessor	BL-5	Create	Create	
9	Write an assembly language program for sorting an array in ascending order in 8086	BL-5	Create	Create	
10	Write an assembly language program to print Hello World message in 8086	BL-5	Create	Create	
11	9		Create		
11	smallest number from an array		Create		
12	Write an assembly language program to find whether	BL-5	Create		
	given string is palindrome or not		Greate		
13	Write an assembly language program to reverse the	BL-5	Create		
	string				
14			 e		
	offset address is 4510H				
15	Compare 8085 & 8086 microprocessor	BL-6	Evaluate	Evaluate	
16	Demonstrate the functions of EU in 8086	BL-2		Understand	
17	How is the memory segment accessed by 8086				
	microprocessor identified?				
18	Discuss the functions of BIU & EU of 8086	BL-2	Understand		

	microprocessor		
19	Describe the interrupts of 8086	BL-2	Understand
20	Describe Maskable & No-Maskable interrupts in 8086	BL-2	Understand

UNIT-5 Peripherals & their Interfacing with 8086/8088 Microprocessor (CO-5) Questions of 2 Marks

- **1.** Define interfacing
- **2.** What are the modes of operations used in 8253
- **3.** What are the basic modes of operation of 8255?
- **4.** Write the features of mode 0 in 8255?
- **5.** What are the different types of write operations used in 8253?
- **6.** What are the modes of operations used in 8253?
- **7.** What is purpose of 8255?
- **8.** What is the role of 8253 Programmable timer interval.?
- **9.** What is the function of DMA?
- **10.** List the operation modes of 8255
- **11.** What is a control word? What is use of control word register?
- **12.** What is the size of ports in 8255?
- **13.** What is an USART?
- **14.** What are the functions performed by USART?
- **15.** What is the use of 8251 chip?
- **16.** What is memory interfacing? Give the role of 8251USART.

Questions of 8 Marks

- 1. With a neat block diagram, explain in detail the internal architecture of 8255 and its registers
- 2. Explain the block diagram and the functions of each block of the 8251 USART
- 3. Draw & Explain the block diagram of PIO 8255
- **4.** Describe the modes of operations of 8255 in detail
- **5.** With neat block diagram, explain in detail architecture of 8253.
- **6.** Write a short note on i) Memory Interfacing ii) modes of operation of 8255
- 7. Draw & Explain the architecture of DMA Controller in detail.

UNIT – 6 Micro-controller (CO-6)

Questions of 2 Marks

- **1.** What is mean by microcontroller?
- **2.** State the function of RS1 and RS0 bits in the flag register of intel 8051 microcontroller?
- **3.** Name the special functions registers available in 8051.
- **4.** Give the differences of Microprocessor and Microcontroller
- **5.** List the features of 8051 microcontroller.
- **6.** Name any four additional hardware features available in microcontrollers when compared to microprocessor
- 7. Give examples of devices in which 8051 family microcontrollers are used
- **8.** What is the need of 8051 microcontroller
- **9.** Identify & Give the applications of 8051 microcontrollers
- **10.** What are PORT 0 & PORT 1 in 8051

Questions of 8 Marks

- 1. Describe the architecture of 8051 with neat diagram.
- 2. Draw & Explain the Block diagram of 8051 Microcontroller in detail
- 3. Explain the functional pin diagram of 8051 Microcontroller.
- 4. Give the PIN detail of an 8051 microcontroller and explain
- 5. Describe the basic components of 8051 Microcontroller
- 6. Compare Microprocessor and Microcontroller
- 7. Compare the 8051 microcontroller family