ARCHITECTURE OF 80386 MICROPROCESSOR

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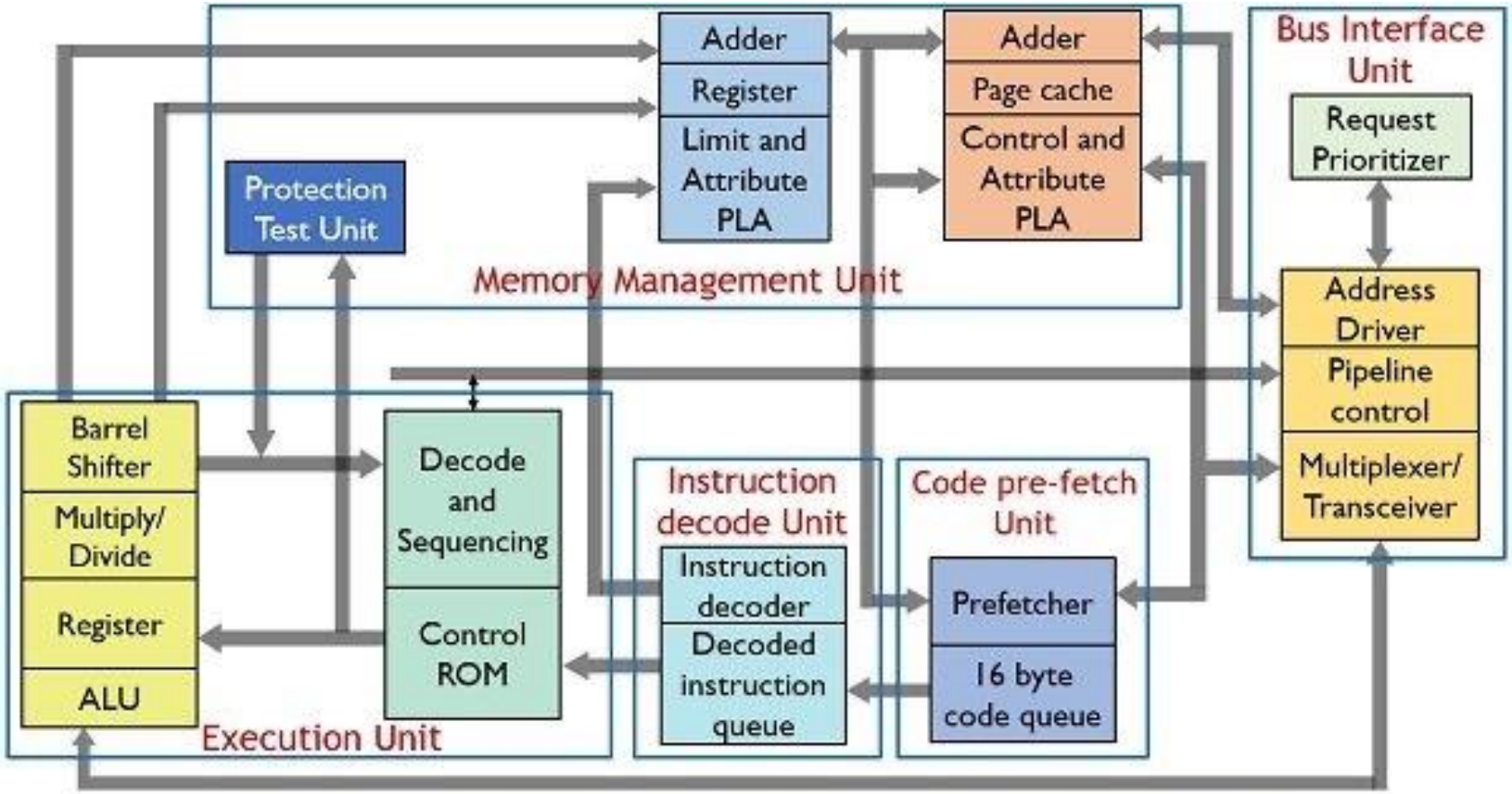
Features of 80386 microprocessor

i. As it is a 32-bit microprocessor. Thus has a 32-bit ALU.
ii. 80386 has a data bus of 32-bit.
iii. It holds an address bus of 32 bit.
iv. It supports physical memory addressability of 4 GB and virtual memory addressability of 64 TB.
v. 80386 supports a variety of operating clock frequencies, which are 16 MHz, 20 MHz, 25 MHz, and 33 MHz.
vi. It offers 3 stage pipeline: fetch, decode and execute. As it supports simultaneous fetching, decoding, and execution inside the system.



Architecture of 80386 Microprocessor

Electronics Desk

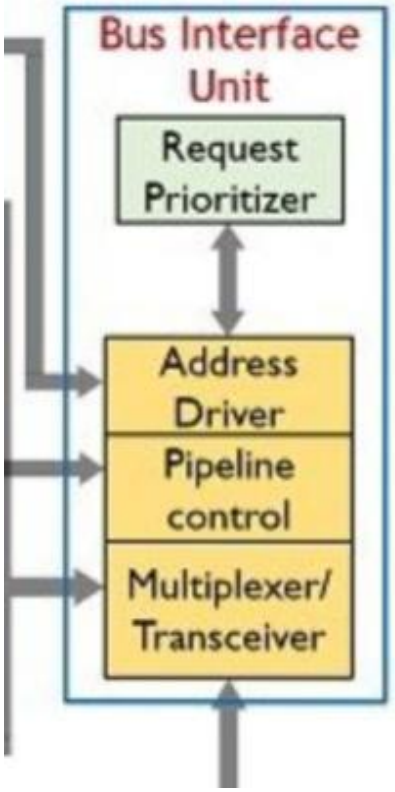
Blocks of 80386 microprocessor

Basically, it has 5 functional units which are as follows:

1. Bus Interface Unit
2. Code Fetch Unit
3. Instruction Decode Unit
4. Execution Unit
5. Memory Management Unit

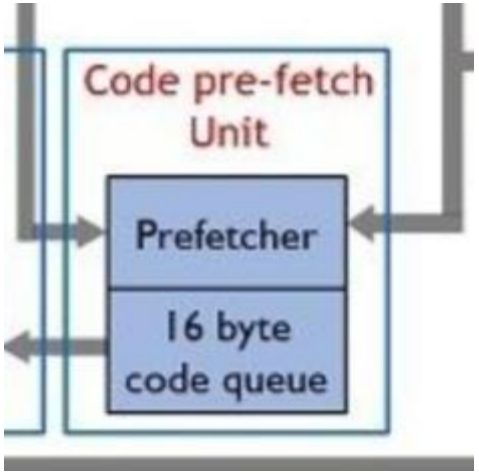
Bus Interface Unit

- The bus interface unit or BIU holds a 32-bit bidirectional data bus as well as a 32-bit address bus. Whenever a need for instruction or a data fetch is generated by the system then the BIU generates signals (according to the priority) for activating the data and address bus in order to fetch the data from the desired addresses.



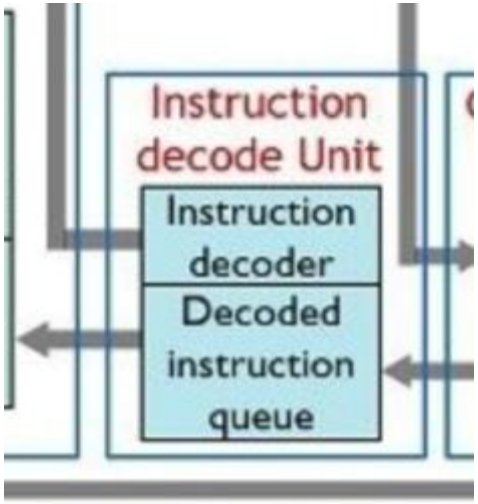
Code Prefetch Unit

- This unit fetches the instructions stored in the memory by making use of system buses. Whenever the system generates a need for instruction then the code prefetch unit fetches that instruction from the memory and stores it in a 16-byte pre-fetch queue.



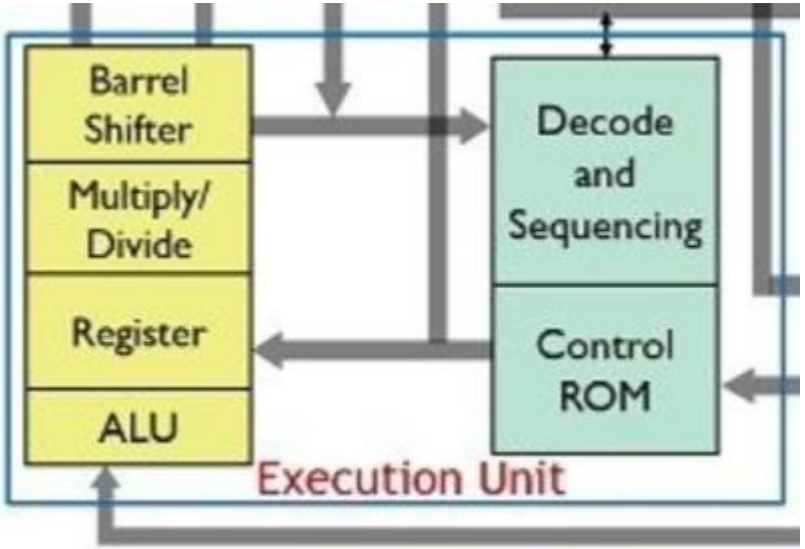
Instruction Decode Unit

- We know that instructions in the memory are stored in the form of bits. So, this unit decodes the instructions stored in the prefetch queue. Basically the decoder changes the machine language code into assembly language and transfers it to the processor for further execution.



Execution Unit

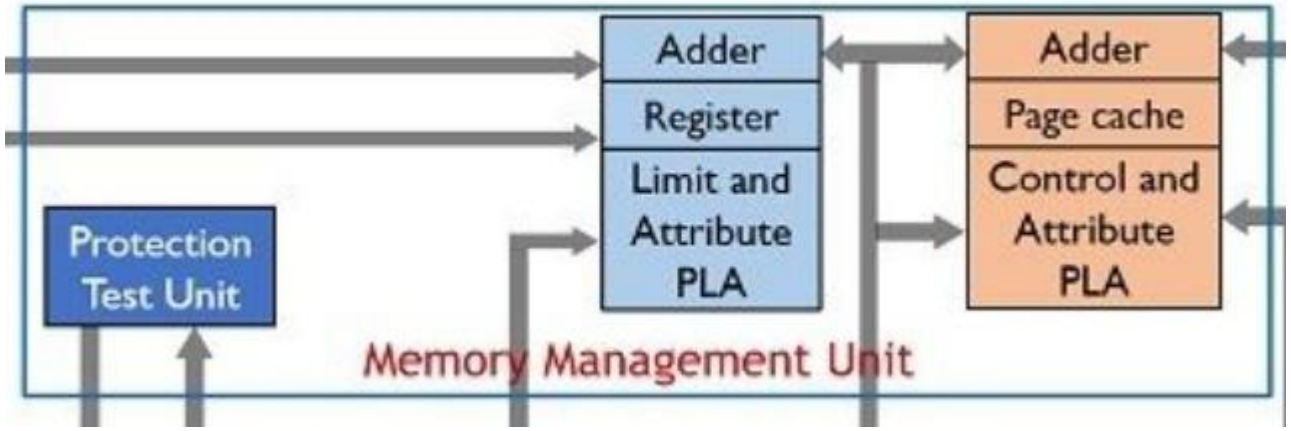
- The execution unit controls the execution of the decoded instructions. This unit has a 32-bit ALU, that performs the operation over 32-bit data in one cycle. Also, it consists of 8 general purpose as well as 8 special purpose registers. These are used for data handling and calculation of offset address.



Memory Management Unit

This unit has two separate units within it. These are:

1. Segmentation Unit
2. Paging Unit



Segmentation unit:

It offers a protection mechanism in order to protect the code or data present in the memory from application programs. It gives 4 level protection to the data or code present in the memory. Every information in the memory is assigned a privilege level from PL0 to PL3. Here, PL0 holds the highest priority and PL3 holds the lowest priority.

Data Memory	
Byte 7	PL0
Byte 6	PL0
Byte 5	PL0
Byte 4	PL1
Byte 3	PL3
Byte 2	PL1
Byte 1	PL2

Paging Unit

- The paging unit operates only in protected mode.
- It changes the linear address into a physical address.
- The segmentation unit controls the action of the paging unit, as the segmentation unit has the ability to convert the logical address into the linear address at the time of executing an instruction.
- Basically, it changes the overall task map into pages and each page has a size of 4K.
- It supports multi-tasking.

Thank you.