Register organization of 80286

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Register organization of 80286

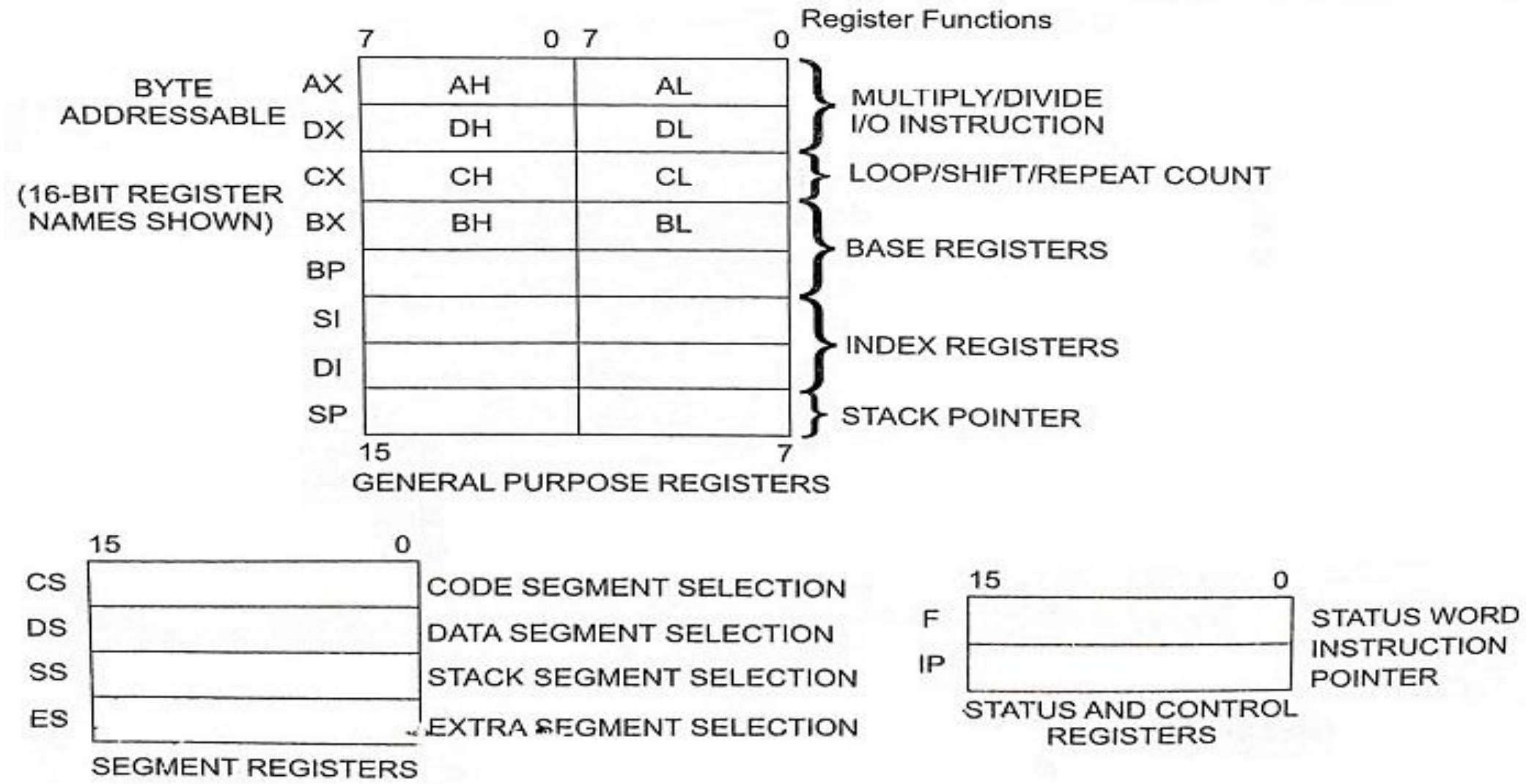

Fig. 11.16 *Register set of 80286*

Register organization of 80286

The 80286 CPU contains almost the same set of registers, as in 8086, namely

1. Eight 16-bit general purpose registers

2. Four 16-bit segment registers

3. Base and Index Registers

4. Status and Control Registers

Register organization of 80286

1. General-Purpose Registers:

Eight 16-bit general-purpose registers are used to store arithmetic and logical operands.

Four of these (AX, BX, CX, and DX) can be used either as 16-bit words or split into pairs of separate 8-bit registers.

- **AX Register (16-Bits)**

It holds operands and results during multiplication and division operations. All IO data

transfers using IN and OUT instructions use A reg (AL/AH or AX).

It functions as accumulator during string operations.

- **BX Register (16-Bits)**

Holds the memory address (offset address), in Indirect Addressing modes.i.e functions as base register during indirect addressing modes.

Indirect addressing mode.

- **indirect addressing mode** is a method of addressing memory where the address of the operand is not specified directly in the instruction. Instead, the address is provided indirectly through one of the general-purpose registers or memory locations. This allows for more flexible and dynamic memory access patterns.

General purpose register

- **CX Register (16-Bits)**

Holds count for instructions like: Loop, Rotate, Shift and String Operations.

- **DX Register (16-Bits)**

It is used with AX to hold 32 bit values during Multiplication and Division.

It is used to hold the address of the IO Port in indirect IO addressing mode.

indirect I/O addressing mode involves specifying an I/O port indirectly using a register.

Register organization of 80286

2.Segment Registers :

Four 16-bit special-purpose registers are used to select the segments of memory that are immediately addressable for code, stack, and data.(holds the base address of each segment)

- Memory segmentation:

1. Data segment(DS register)
2. Code segment(CS register)
3. Stack segment(SS register)
4. Extra segment(ES register)

Segment register in more detail

- **CS Register:**

CS holds the base (Segment) address for the Code Segment. All programs are stored in the Code Segment.

It is multiplied by 10H (16d), to give the 20-bit physical address of the Code Segment.

- **DS Register :**

DS holds the base (Segment) address for the Data Segment.

It is multiplied by 10H (16d), to give the 20-bit physical address of the Data Segment.

Segment register in more detail

- **SS Register :**

SS holds the base (Segment) address for the Stack Segment.

It is multiplied by 10H (16d), to give the 20-bit physical address of the Stack Segment.

- **ES Register:**

ES holds the base (Segment) address for the Extra Segment.

It is multiplied by 10H (16d), to give the 20-bit physical address of the Extra Segment.

Register organization of 80286

3.Base and Index Registers:

Four of the general-purpose registers can also be used to determine offset addresses of operands in memory.

Usually, these registers hold base addresses or indexes to particular locations within a segment.

Any specified addressing mode determines the specific registers used for operand address calculations.

They are:

- **Code Segment :**

This segment is used to hold the program to be executed. Instruction are fetched from the Code Segment.

CS register holds the 16-bit base address for this segment.

IP register (Instruction Pointer) holds the 16-bit offset address

Base and Index Registers:

- **Data Segment :**

This segment is used to hold general data.

This segment also holds the source operands during string operations.

DS register holds the 16-bit base address for this segment.

BX register is used to hold the 16-bit offset address for this segment.

SI register (Source Index) holds the 16-bit offset address during String Operations.

Base and Index Registers:

- **Stack Segment:**

This segment holds the Stack memory, which operates in LIFO manner.

SS holds its Base address.

SP (Stack Pointer) holds the 16-bit offset address of the Top of the Stack.

BP (Base Pointer) holds the 16-bit offset address during Random Access.

Base and Index Registers:

- **Extra Segment:**

This segment is used to hold general data

Additionally, this segment is used as the destination during String Operations.

ES holds the Base Address.

DI holds the offset address during string operations.

Register organization of 80286

4.Status and Control Registers:

The three 16-bit special-purpose registers are used of record and control of the 80286 processor. The instruction pointer contains the offset address of the next sequential instruction to be executed.

- **Status registers** are used to indicate the current status or state of a device or system. They typically contain flags or bits that reflect various operational conditions. These flags can signal things like error conditions, readiness, or completion of operations.
- **Control registers** are used to configure or control the behavior of hardware components. They allow software to enable or disable features, set modes of operation, or control specific hardware functions.

Flag registers

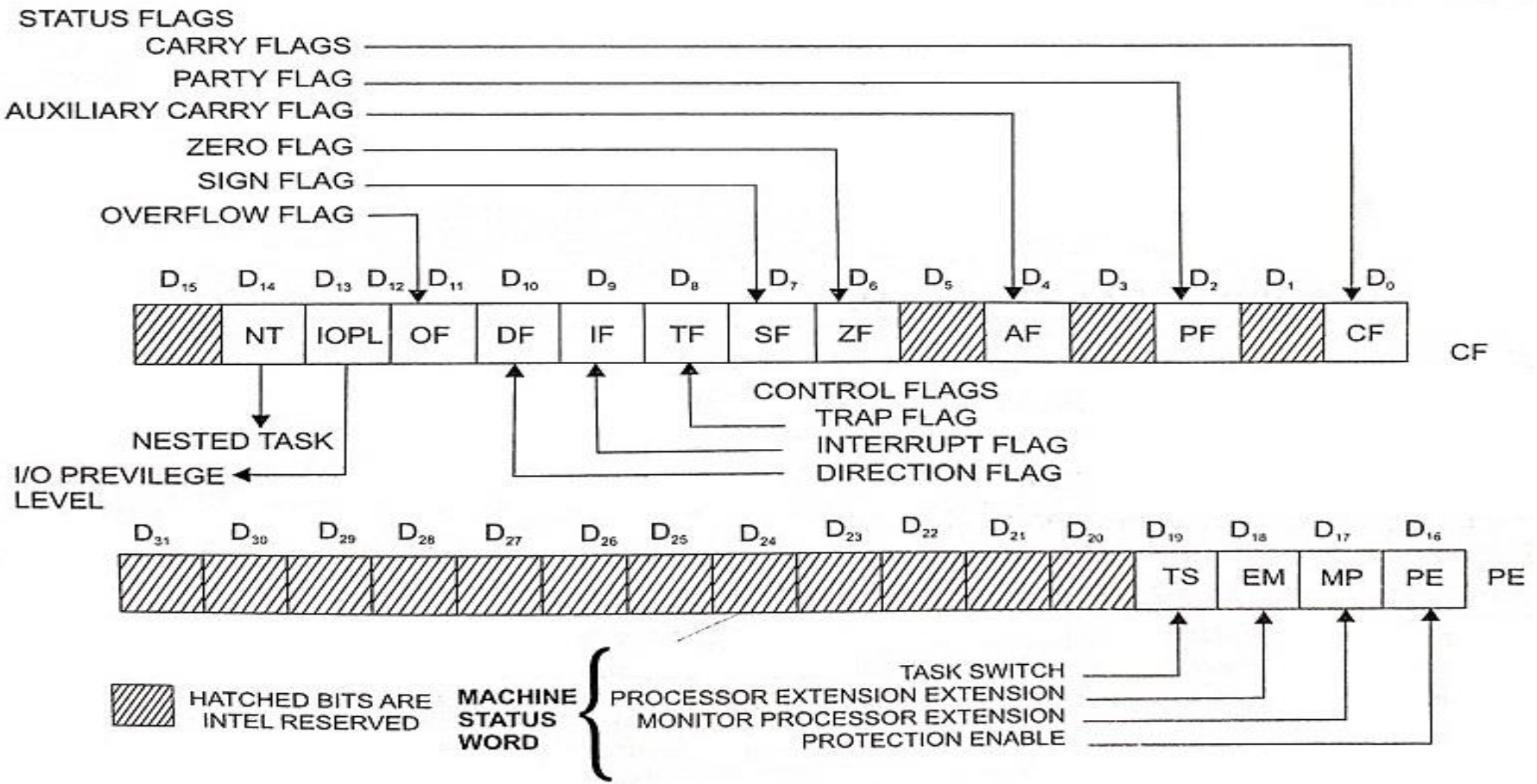

Fig. 11.17 *80286 flag registers*

Flag registers in 80286

- **Status flag bits:**

D0,D2, D4, D6, D7 and D11 are called as status flag bits.

- **Control flags:**

The bits D8 (TF) ,D9 (IF) and D10 (DF) are used for controlling machine operation and thus they are called control flags.

Status flags in 80286

- **(CF)Carry Flag (bit D0):**

Set on high-order bit carry or borrow; cleared otherwise.

- **(PF) Parity Flag (bit D2) :**

Set if low-order 8 bits of result contain an even number of 1 bit; cleared otherwise.

- **(AF) Auxiliary carry flag(bit D4):**

Set on carry from or borrow to the lower order four bits of AL; cleared otherwise.

Status flags in 80286

- **(ZF) Zero Flag (bit D6):**

Set if result is zero: cleared otherwise,

- **(SF) Sign Flag (bit D7):**

Set equal to high-order bit of result (0 if positive, 1 if negative).

- **(OF) Overflow Flag (bit D11):**

Set if result is a too-large positive number or a too-small negative number (excluding sign-bit) to fit in destination operand: cleared otherwise.

Control flags in 80286

- **(TF) Single Step Flag (bit D8):**

Once set, a single-step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.

- **(IF)Interrupt–enable Flag (bit D9):**

When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location.

- **(DF) Direction Flag (bit D10) :**

Causes string instructions to auto-decrement the appropriate index registers when set. Clearing DF causes auto increment.

Flag registers in 80286

The additional fields available in 80286 flag registers are:

1. IOPL - I/O Privilege Field (bits D12 and D13):

Bits D12 and D13 specify the I/O privilege level.

2. NT - Nested Task flag (bit D14):

Bit D14 indicates whether the CPU is executing a nested task.

3. PE - Protection Enable (bit D16):

Bit D16 enables or disables protection**.**

Protection Enable flag places the 80286 in protected mode, if set.

This can only be cleared by resetting the CPU.

Flag registers in 80286

4. MP - Monitor Processor Extension (bit D17):

Bit D17 allows or disallows the WAIT instruction to generate a processor extension not present exception .

If the Monitor Processor Extension flag is set, allows WAIT instruction to generate a processor extension not present exception.

5. EM - Processor Extension Emulator (bit D18):

Bit D18 causes a processor extension absent exception and permits emulation of processor extensions by the CPU, if set.

Flag registers in 80286

6.TS – Task Switch (bit D19)

Task Switch flag if set, indicates the next instruction using extension will generate exception 7, permitting the CPU to test whether the current processor extension is for the current task.

Machine Status Word (MSW)

Machine Status Word (MSW):

The machine status word consists of four flags – PE, MO, EM and TS of the four lower order bits D19 to D16 of the upper word of the flag register.

LMSW and SMSW :

The LMSW and SMSW instructions are available in the instruction set of 80286 to write and read the MSW in real address mode.