Unit – 7

ADVANCED MICROPROCESSORS

What is microprocessor?

- The microprocessor is a multipurpose, programmable device that accepts digital data as input, processes it according to instructions stored in it's memory and provide results as output.
  It is an example of digital logic and it uses binary and hexadecimal numerical systems

80286 Microprocessor

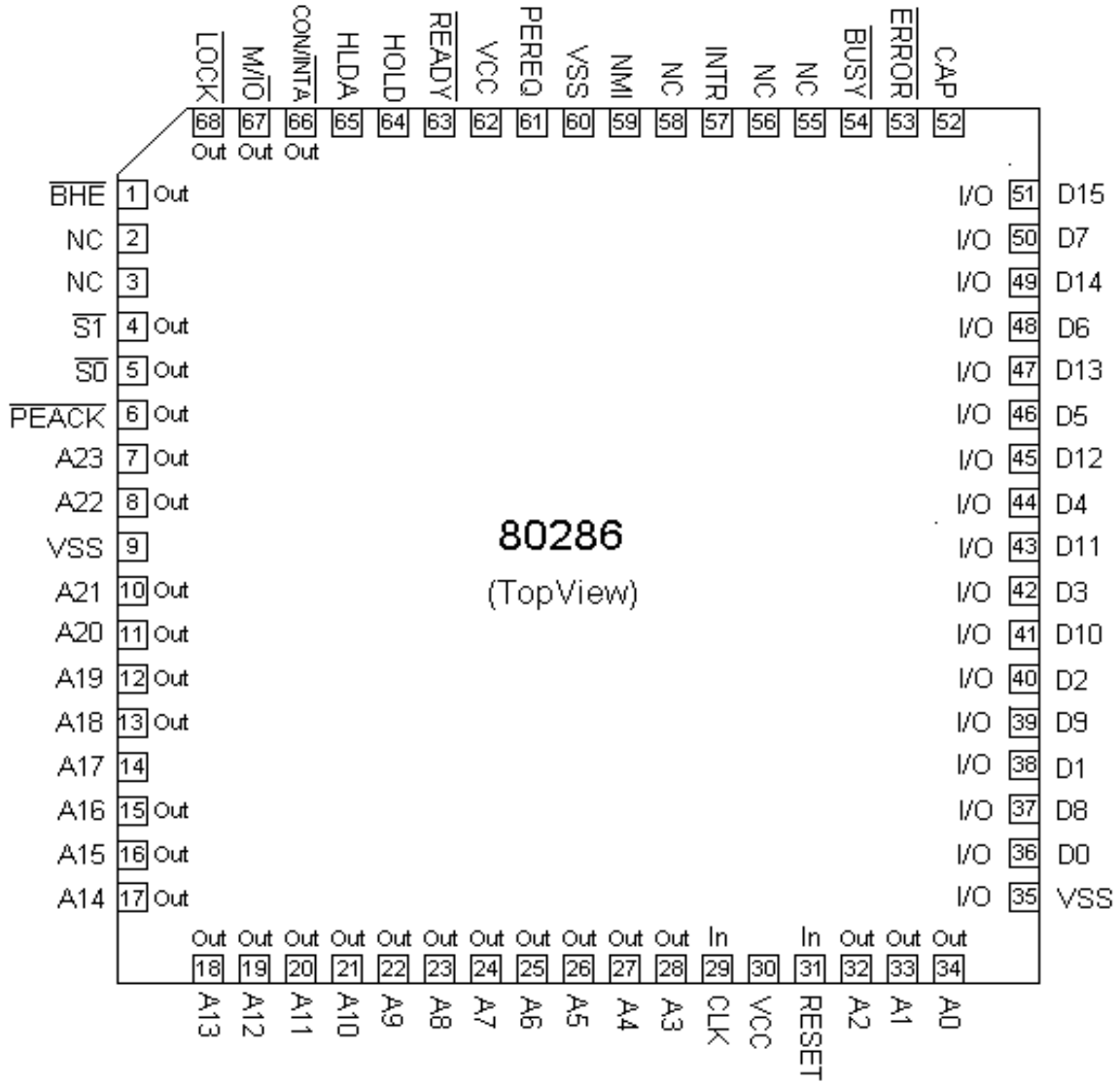
About…

- introduced on 1 February 1982
- maximal clock rate of 4, 6 or 8 MHz and later releases for 12.5 MHz
- 16-bit microprocessor having 24 address lines and 16 data lines.
- first 8086 based CPU with separate, non-multiplexed address and data buses
- approximately 134,000 transistors in its original nMOS.
- upwardly compatible with 8086 in terms of instruction set.

Cntd.,

- Advanced Memory management
- It is available in variety of pin packages such as 68-pin PLCC (Plastic Leaded Chip Carrier),
- Ceramic LCC (Leadless Chip Carrier), and PGA(Pin Grid Array).
- Specially designed for Multiuser & Multitasking systems.
- 4-level memory protection & support for virtual memory & operating system.
- Better Pipelining method
- 4 independent functional unit in internal architecture
- The 6 MHz, 10 MHz and 12 MHz models were reportedly measured to operate at 0.9 MIPS, 1.5 MIPS and 2.66 MIPS respectively.

80286 pin diagram



80286 Salient features

Feature 1: Operating Modes

Two modes of operation

- 1. Real address mode.
- 2. Protected Virtual address mode.

Real Address Mode :

- 80286 just act as a faster version of 8086
- And program for 8086 can be executed without modification in 80286
- can address up to 1MB of Physical Memory.

Protected Virtual Address Mode:

- 80286 supports multitasking
- Able to run several program at the same time
- Able to protect memory space for another program
- memory management unit can manage upto 1GB of virtual memory.

Feature 2: More Addressable Memory

- In protected mode 80286 can address 16 megabytes of physical memory.
- Where 8086 can address only 1 megabyte

Feature 3: Virtual Memory in Protected Mode

- 80286 can treat external storage as it were physical memory.
- Execute programs that are too large to be contained in physical memory.
- Program can be upto 2^30 bytes.

INTERNAL ARCHITECTURE OF 80286

Register organization of 80286

- The 80286 CPU contains almost the same set of registers, as in 8086.
    1. Eight 16-bit general purpose registers.
    2. Four 16 bit segment registers.
    3. Status and control register.
    4. Instruction register.

The register set of 80286 is shown in Fig. 9.1.

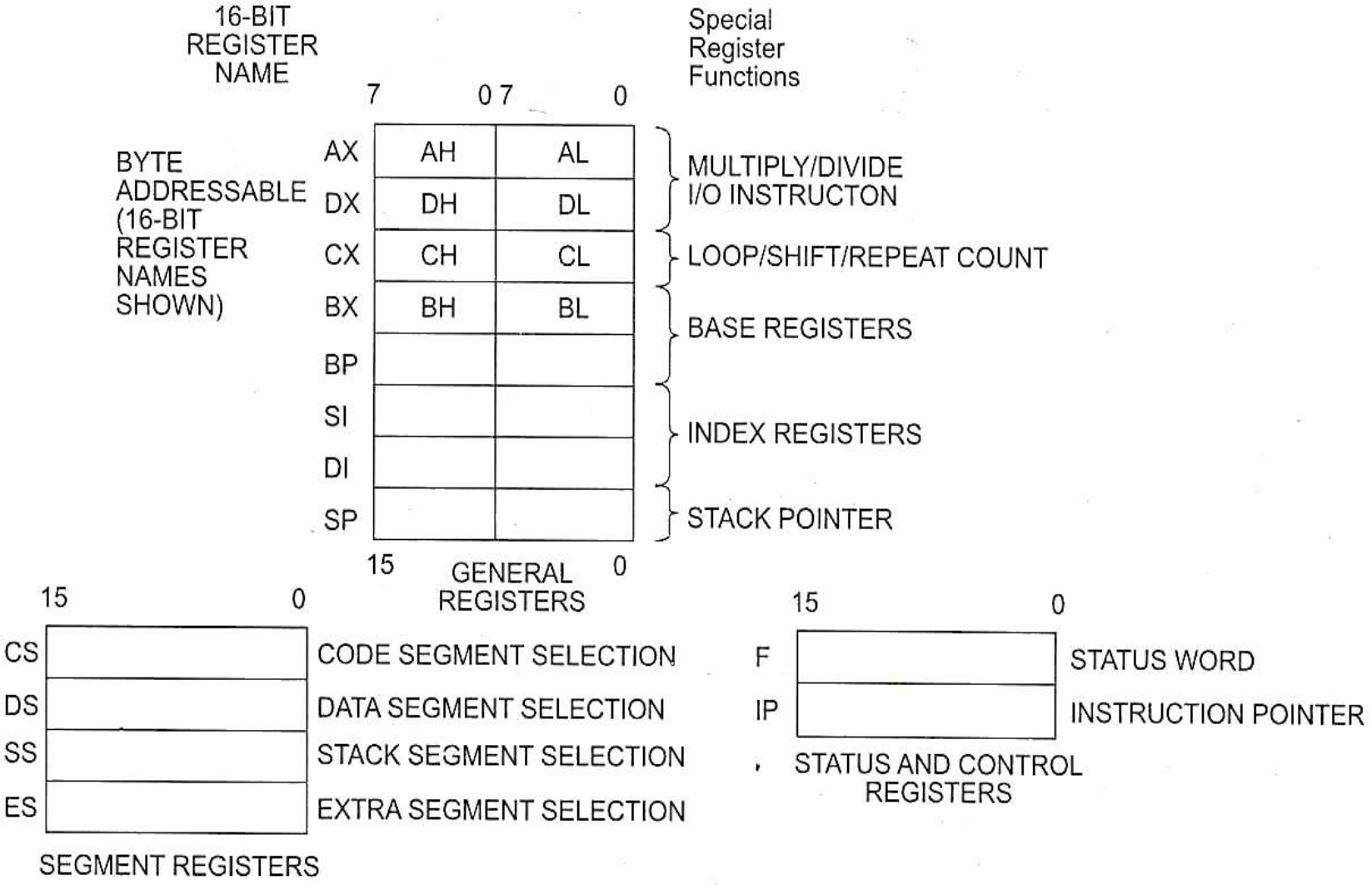


Fig. 9.1 *Register Set of 80286 (Intel Corp.)*

Flag Registers

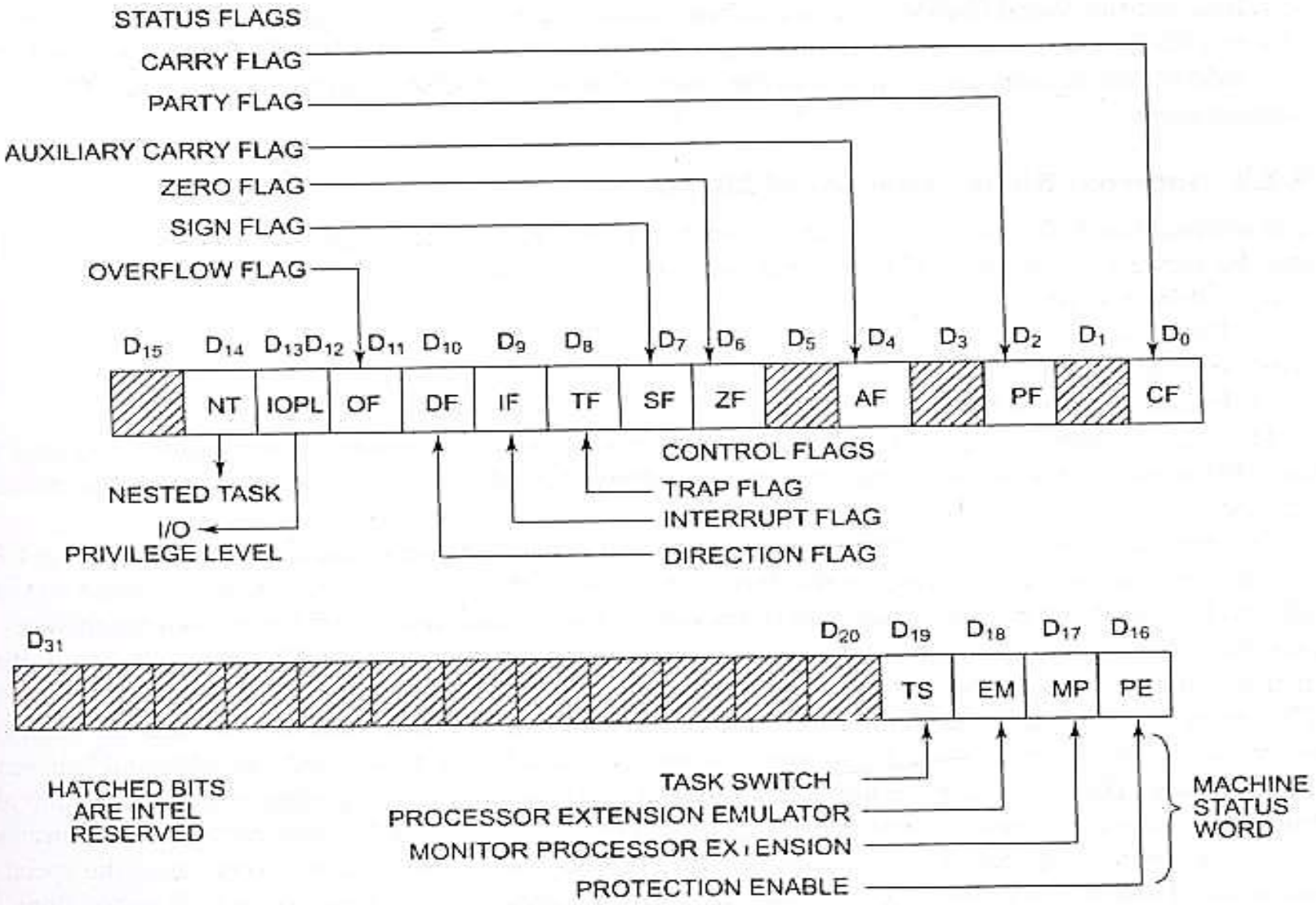


Fig. 9.2 *80286 Flag Register (Intel Corp.)*

- The flag register bits **D0, D2, D4, D6, D7 and D11** are modified according to the result of the execution of logical and arithmetic instructions. These are called status flag bits.

PE - Protection enable

- Protection enable flag places the 80286 in protected mode, if set. This can only be cleared by resetting the CPU.

MP – Monitor processor extension

- flag allows WAIT instruction to generate a processor extension.

EM – Emulate processor extension flag

- if set, causes a processor extension absent exception and permits the emulation of processor extension by CPU.

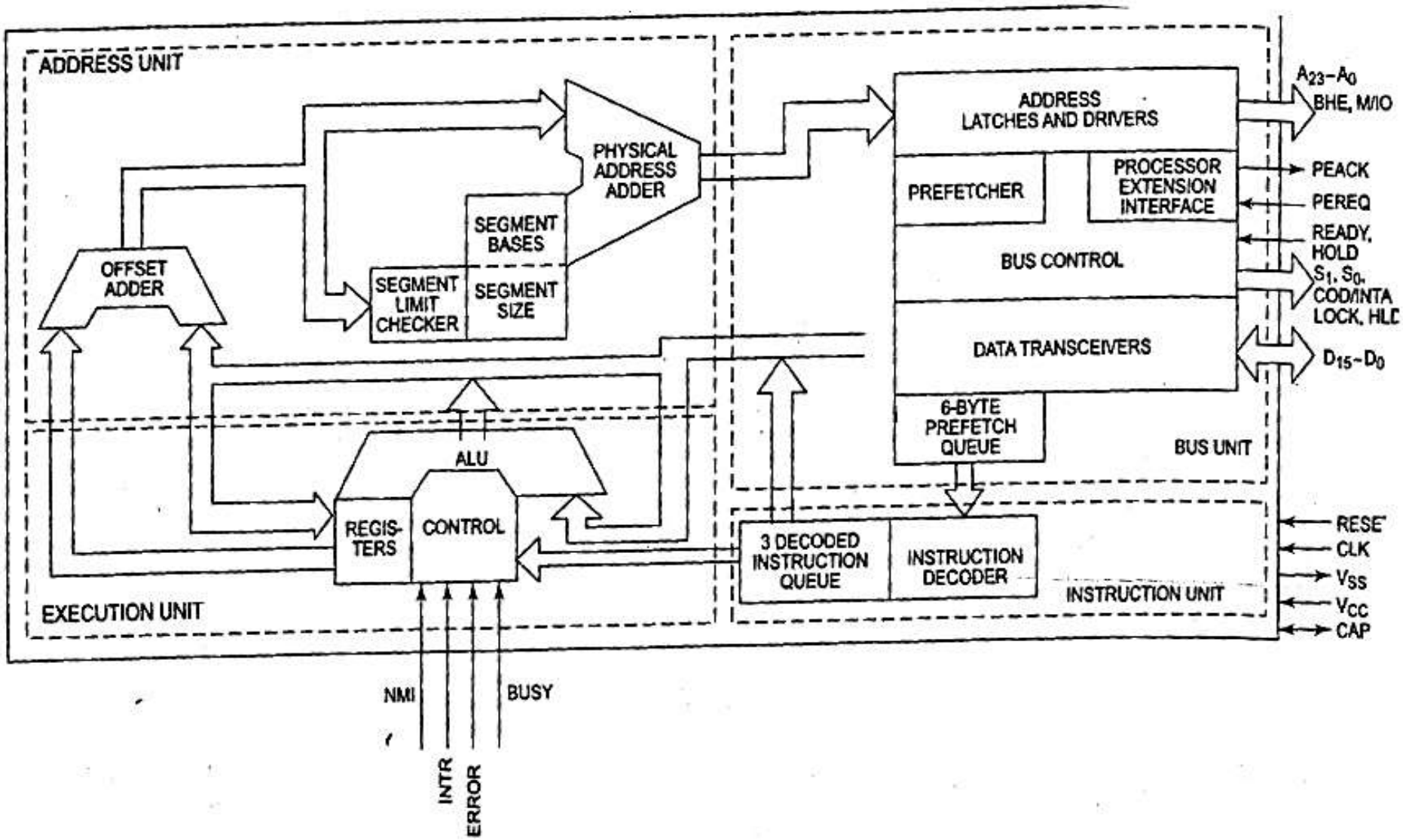
TS – Task switch

- if set this flag indicates the next instruction using extension will generate exception, permitting the CPU to test whether the current processor extension is for current task.

Machine Status Flag (MSW) :

- The machine status word consists of four flags. These are **–PE,MP,EM, and TS** of the four lower order bits D19 to D16 of the upper word of the flag register.
- The **LMSW** and **SMSW** instructions are available in the instruction set of 80286 to write and read the MSW in real address mode.

Internal Block Diagram of 80286



- The CPU may be viewed to contain four functional parts, viz.
    (a) **Address Unit** (AU)
    (b) **Bus Unit** (BU)
    (c) **Instruction Set** (IU)
    (d) **Execution Unit** (EU)
- The **Address Unit** (AU) is responsible for calculating the physical address of instructions and data that CPU wants to access.
- This physical address computed by the address unit is handed over to the **Bus Unit** (BU) of the CPU.
- The address latches and drivers in the bus unit transmit the physical address thus formed over the address bus A0-A23.
- One of the major function of the bus unit is to fetch instruction bytes from the memory.

- The **Instruction Unit** (IU) accepts instructions from the prefetch queue and an instruction decoder decodes them one by one.
- The output from the decoding circuit drives a control circuit in the **Execution Unit** (EU) is responsible for instructions received from the decoded instruction queue, which sends the data part of the instruction over the data bus.

80386

Salient Features of 80386X

- It supports 8/16/32 bit data operands
- It has 132 pins.
- It has 32-bit internal registers
- It supports 32-bit data bus and 32-bit non-multiplexed address bus
- It supports

  Physical Address of 4GB

  Maximum Segment size of 4GB

  Virtual Address of 64TB(4GB seg. * 16, 384 segments)

3 Types of 80386

1. 80386DX(floating point capability.)
2. 80386SX(16-bit data bus)
3. 80386SL(several power management options)

It operates in 3 different modes

- Real
- Protected
- Virtual .

- MMU provides virtual memory, paging and 4 levels of protection
- Low cost & low power consumption.
- Clock Frequency : 20, 25 and 33MHz


intel
NG80386SX-16
C STEP
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U2
U26
U42
R607
R608
C612
C613
R610
C602
R594
C56
R5
U10
R56

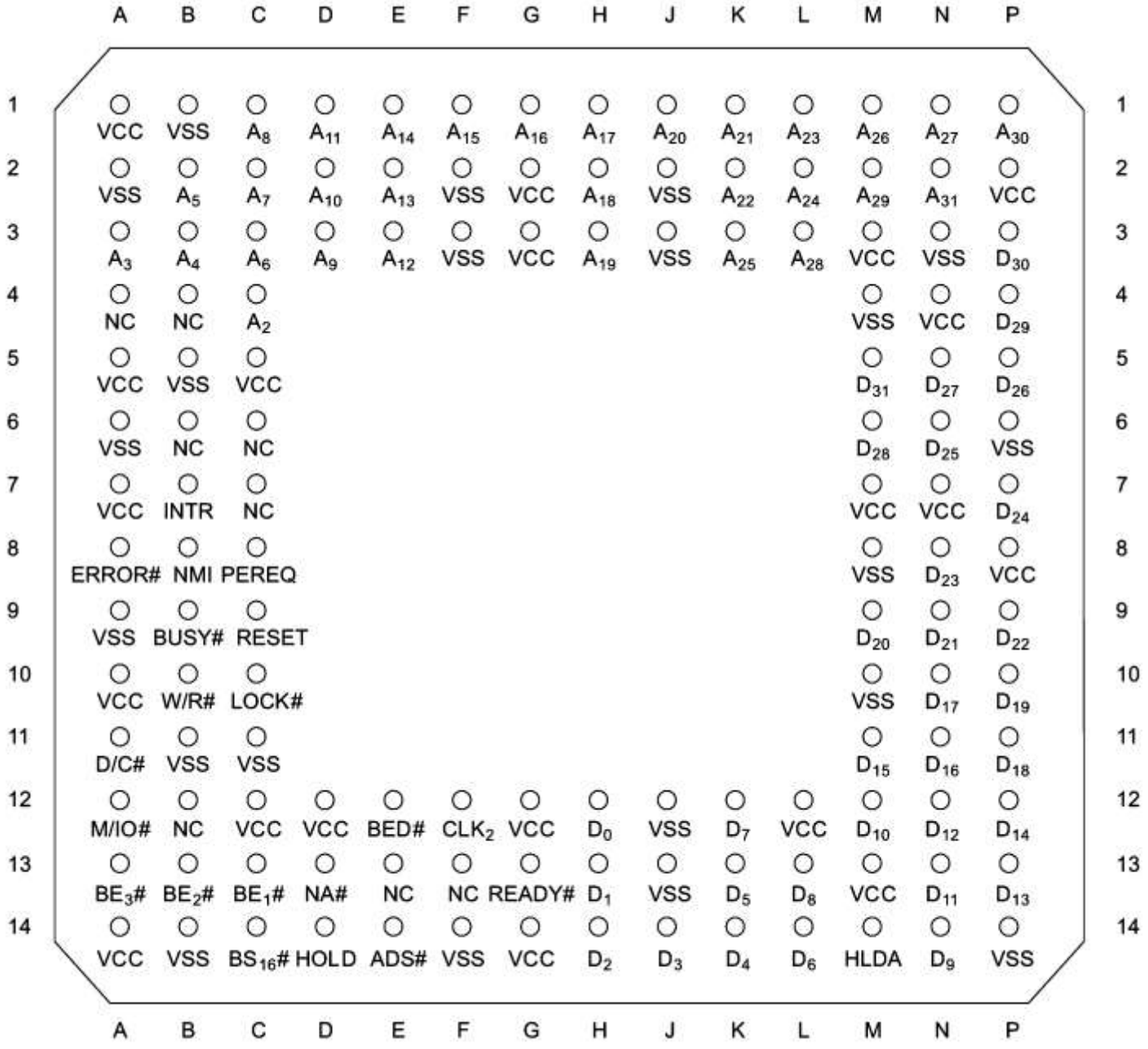
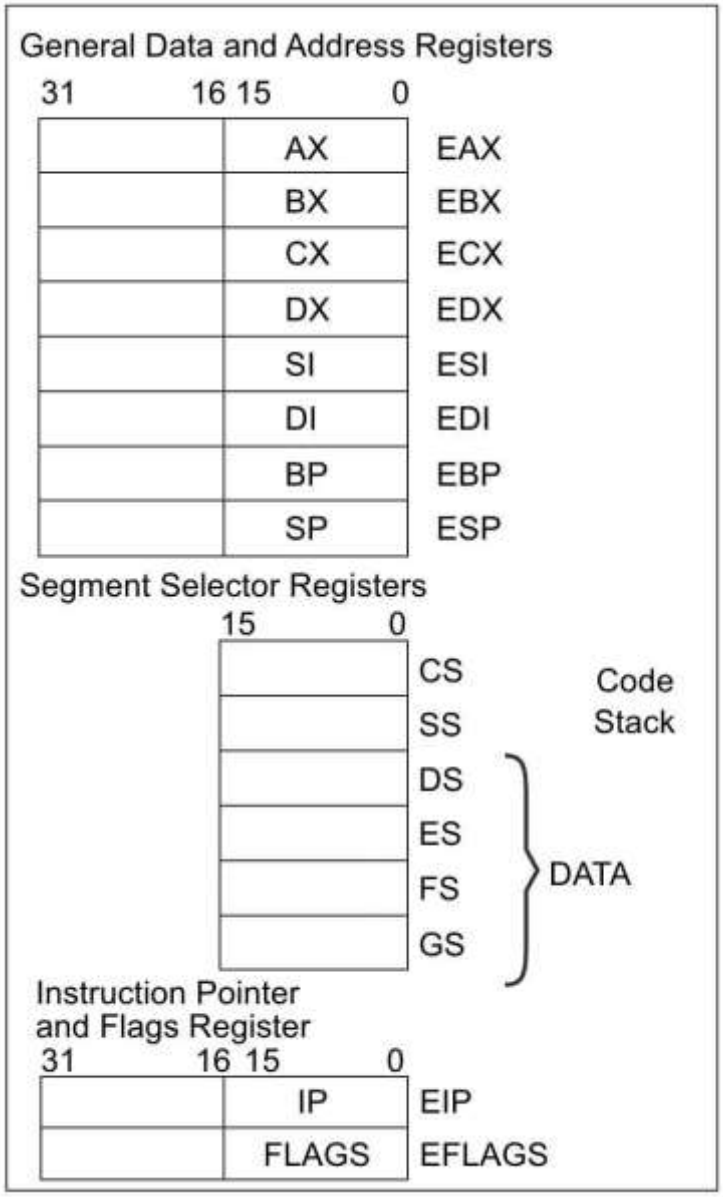
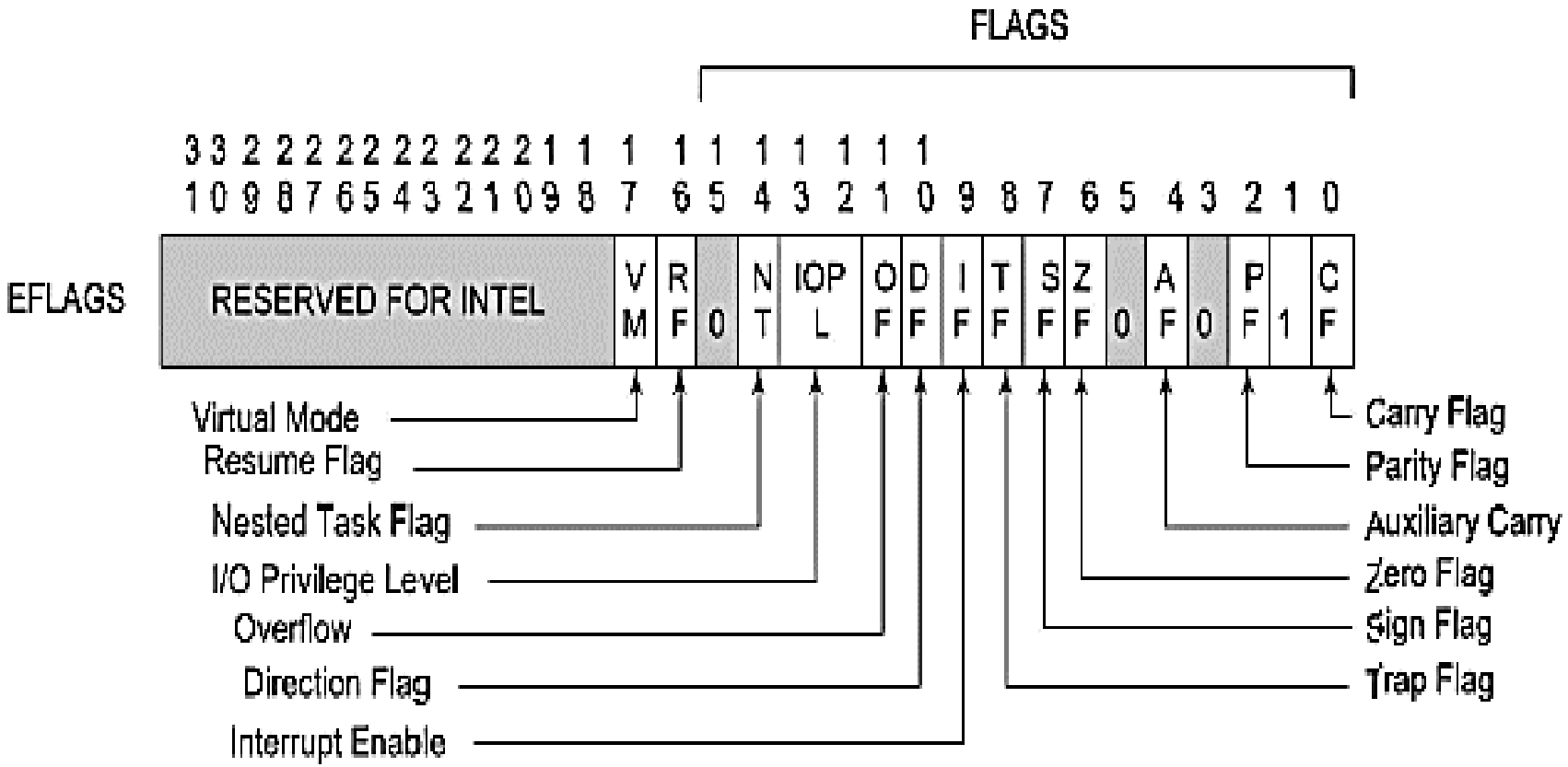


Fig. 10.1(b) *Pin Diagram of 80386 (Intel Corp.)*

Register Bank of 80386





Note: 0 indicates Intel reserved

Fig. 10.2(b) *Flag Register of 80386 (Intel Corp.)*

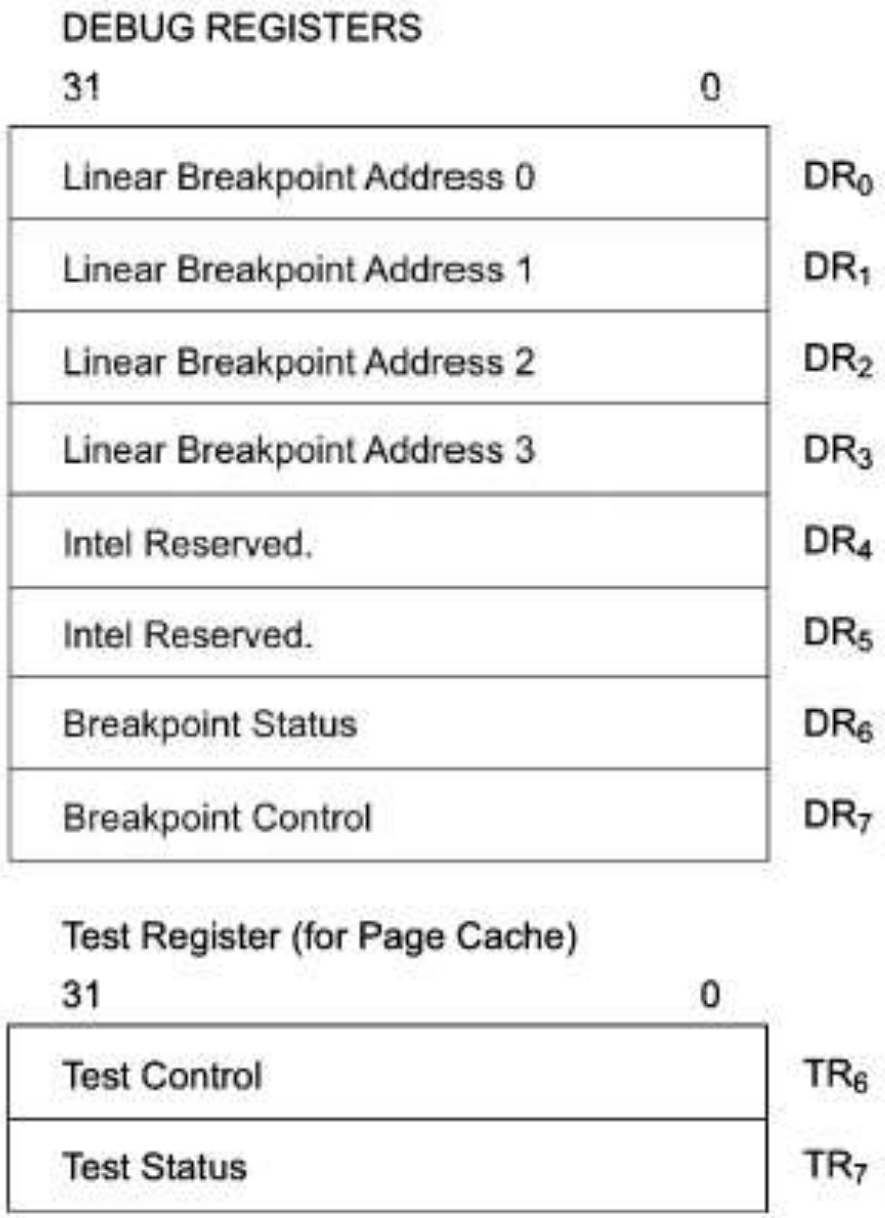
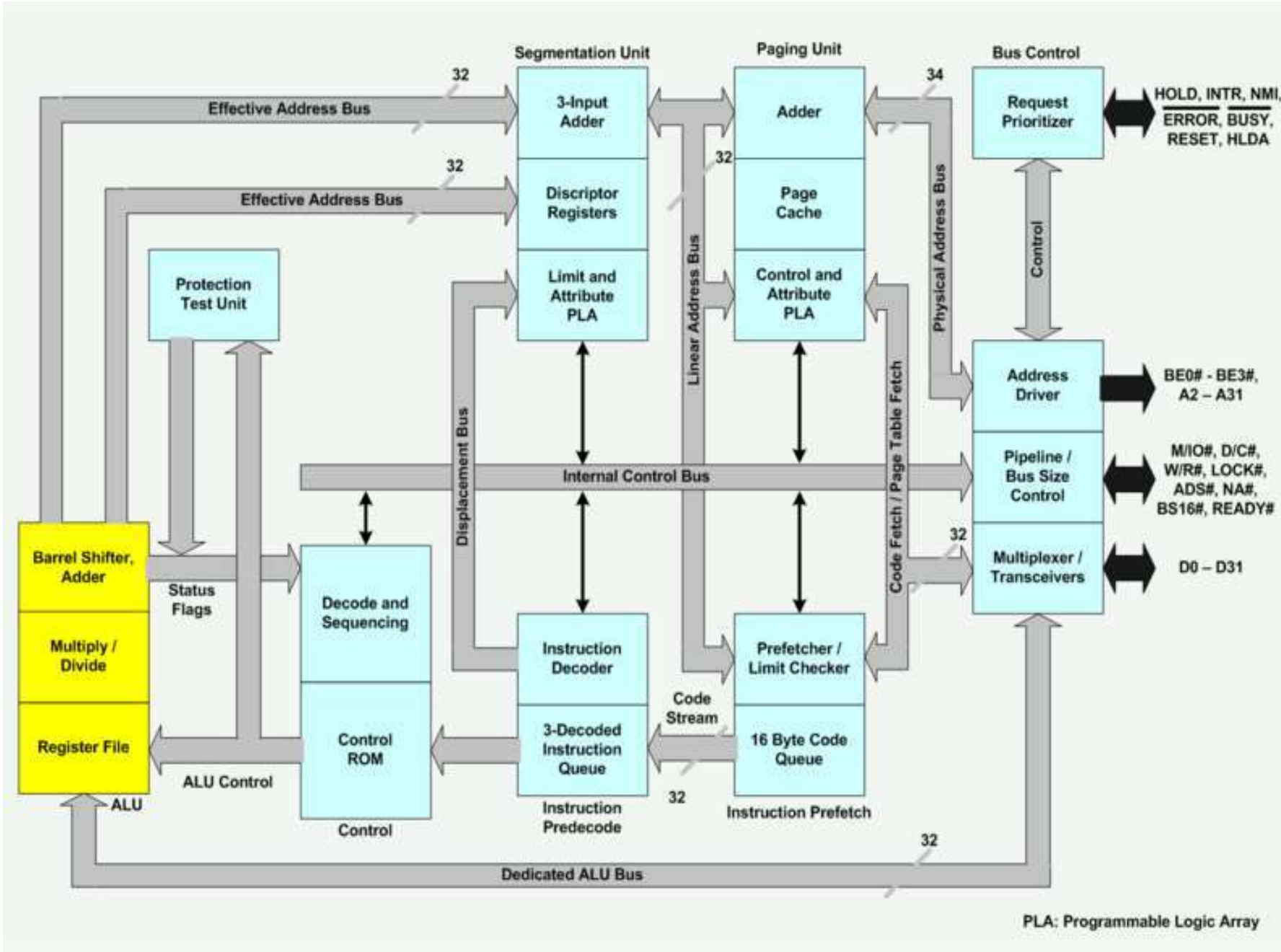


Fig. 10.3 ***Debug and Test Registers of 80386 (Intel Corp.)***

Architecture of 80386



- **Central Processing Unit**
- **Memory Management Unit**
- **Bus Control Unit**

Central Processing Unit :

- The CPU is further divided into:
  - Execution Unit
  - Instruction Unit

Execution Unit:

- Execution unit has 8 General and Special purpose registers, which are either used for handling data or calculating offset addresses.
- The 64-bit barrel shifter increases the speed of all shift, rotate.
- Multiply/divide logic implements the bit-shift rotate algorithms to complete the operation in minimum time.

Instruction Unit:

- It decodes the opcode bytes received from the 16-byte instruction code queue and arrange them into a 3-decoded instruction queue.
- After decoding it is passed to control section for deriving necessary control signals

Memory Management Unit

- MMU consists of a segmentation unit and paging unit.
- **Segmentation Unit:**
- Uses of two address components - segment and offset – for reliability and sharing of data.
- It allows a maximum segment size of 4GB.

- **Paging Unit**
- It organizes physical memory in terms of pages of 4KB size.
- It works under the control of segmentation unit i.e. each segment is divided into pages.
- It converts linear addresses into physical addresses.
- The control and attribute PLA checks privileges at page level.

Bus Control Unit

- It has a prioritizer to resolve the priority of various bus requests. This controls the access of the bus.
- The address driver drives the bus enable and address signals A2 – A31.

Real Address Mode of 80386

- After reset, the 80386 starts from memory location FFFFFFF0H under the real address mode. In the real mode, 80386 works as a fast 8086 with 32-bit registers and data types.
- In real mode, the default operand size is 16 bit but 32- bit operands and addressing modes may be used with the help of override prefixes.
- The segment size in real mode is 64k, hence the 32-bit effective addressing must be less than 0000FFFFH. The real mode initializes the 80386 and prepares it for protected mode.

10.6.1 Memory Addressing in Real Mode

In the real mode, the 80386 can address at the most 1Mbytes of physical memory using address lines A_0–A_{19}. Paging unit is disabled in the real address mode, and hence the real addresses are the same as the physical addresses. To form a physical memory address, appropriate segment register contents (16-bits) are shifted left by four positions and then added to the 16-bit offset address formed using one of the addressing modes, in the same way as in the 80386 real address mode. The segments in 80386 real mode can be read, written or executed, i.e. no protection is available. Any fetch or access past the end of the segment limit generate exception 13 in real address mode. The segments in 80386 real mode may be overlapped or non-overlapped. The interrupt vector table of 80386 has been allocated 1Kbyte space starting from 00000H to 003FFH. Figure 10.4 shows the physical address formation in real mode of 80386.

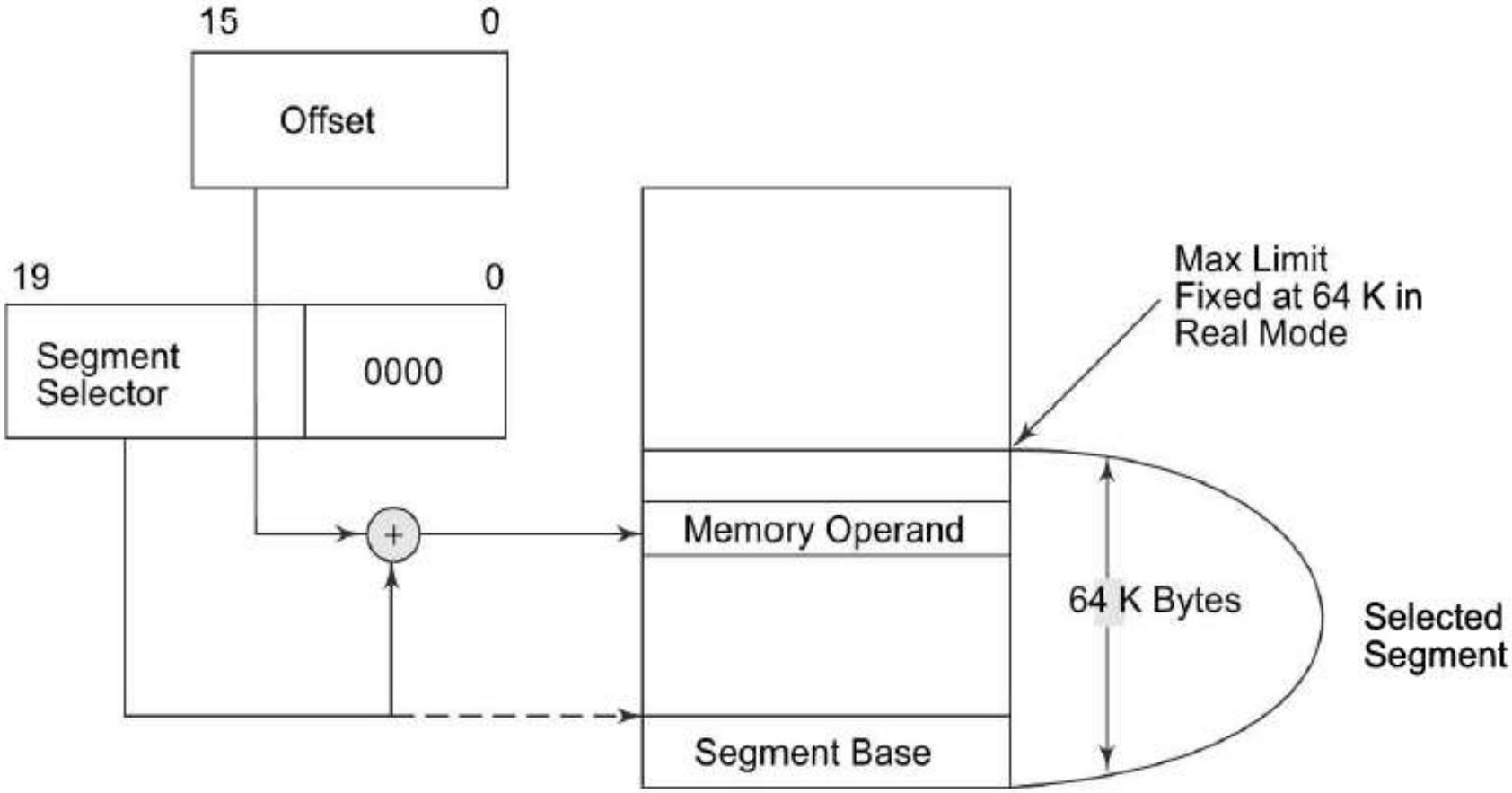


Fig.10.4 *Physical Address Formation in Real Mode of 80386 (Intel Corp.)*

Protected Mode of 80386:

- All the capabilities of 80386 are available for utilization in its protected mode of operation.
- The 80386 in protected mode support all the software written for 80286 and 8086 to be executed under the control of memory management and protection abilities of 80386.
- The protected mode allows the use of additional instruction, addressing modes and capabilities of 80386.

10.7.1 Addressing in Protected Mode

In this mode, the contents of segment registers are used as selectors to address descriptors which contain the segment limit, base address and access rights byte of the segment. The effective address (offset) is added with segment base address to calculate linear address. This linear address is further used as physical address, if the paging unit is disabled. Otherwise, the paging unit converts the linear address into physical address.

The paging unit is a memory management unit enabled only in the protected mode. The paging mechanism allows handling of large segments of memory in terms of pages of 4 Kbyte size. The paging unit operates under the control of segmentation unit. The paging unit if enabled converts linear addresses into physical addresses, in protected mode. Figures 10.5(a) and (b) show addressing in protected mode without and with paging unit enabled respectively.

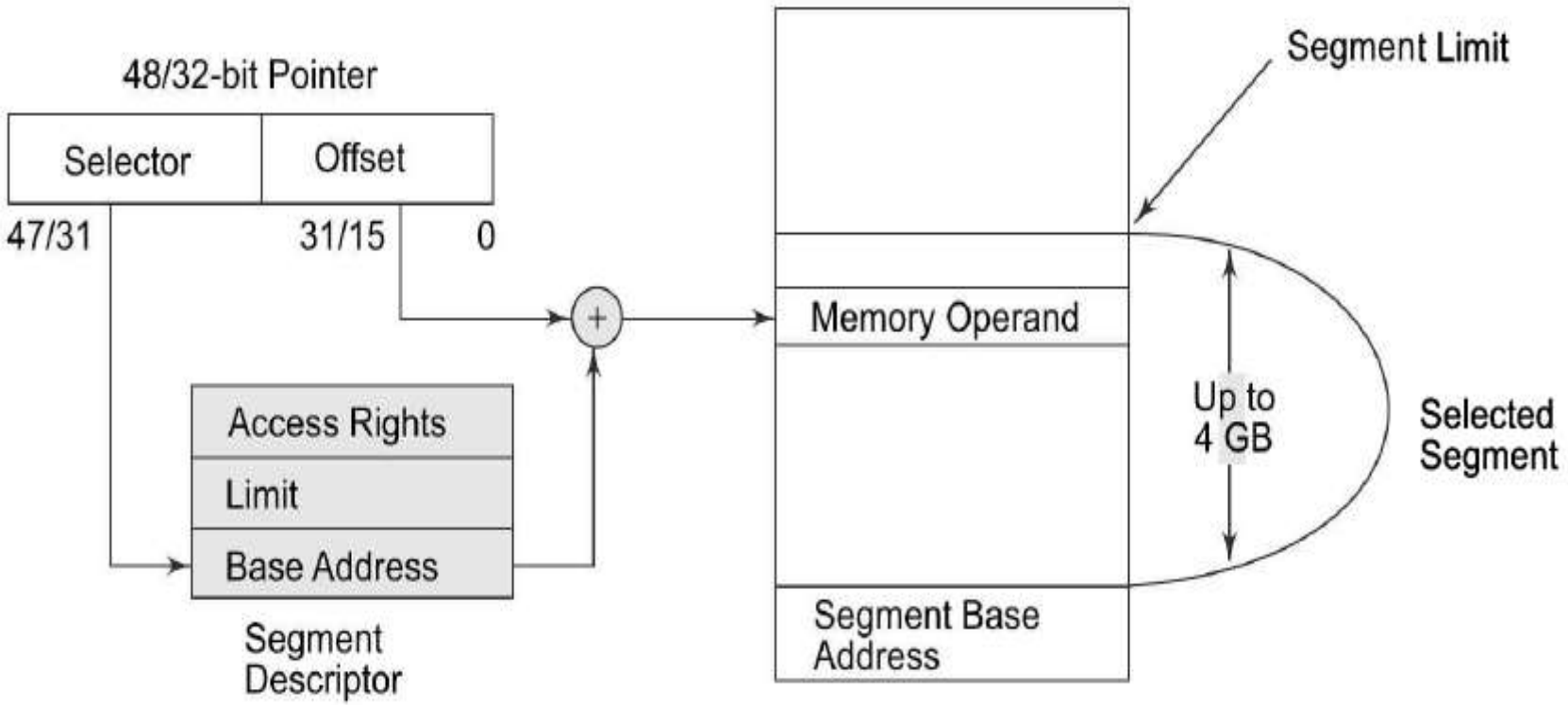


Fig. 10.5(a) *Protected Mode Addressing without Paging Unit (Intel Crop.)*

Segmentation:

- ***Descriptor tables*:** These descriptor tables and registers are manipulated by the operating system to ensure the correct operation of the processor, and hence the correct execution of the program.
- Three types of the 80386 descriptor tables are listed as follows:
  - GLOBAL DESCRIPTOR TABLE (GDT)
  - LOCAL DESCRIPTOR TABLE (LDT)
  - INTERRUPT DESCRIPTOR TABLE (IDT)

- ***Descriptors*:** The 80386 descriptors have a 20-bit segment limit and 32-bit segment address. The descriptor of 80386 are 8-byte quantities access right or attribute bits along with the base and limit of the segments.
- ***Descriptor Attribute Bits*:** The A (accessed) attributed bit indicates whether the segment has been accessed by the CPU or not.
- The TYPE field decides the descriptor type and hence the segment type.
- The S bit decides whether it is a system descriptor (S=0) or code; data segment descriptor (S=1).
- The DPL field specifies the descriptor privilege level.

- The D bit specifies the code segment operation size. If D=1, the segment is a 32-bit operand segment, else, it is a 16-bit operand segment.
- The P bit (present) signifies whether the segment is present in the physical memory or not. If P=1, the segment is present in the physical memory.
- The G (granularity) bit indicates whether the segment is page addressable. The zero bit must remain zero for compatibility with future process.
- The AVL (available) field specifies whether the descriptor is for user or for operating system.

PAGING:

***Paging Unit*:** The paging unit of 80386 uses a two level table mechanism to convert a linear address provided by segmentation unit into physical addresses.

The paging unit converts the complete map of a task into pages, each of size 4K. The task is further handled in terms of its page, rather than segments.

The paging unit handles every task in terms of three components namely page directory, page tables and page itself.

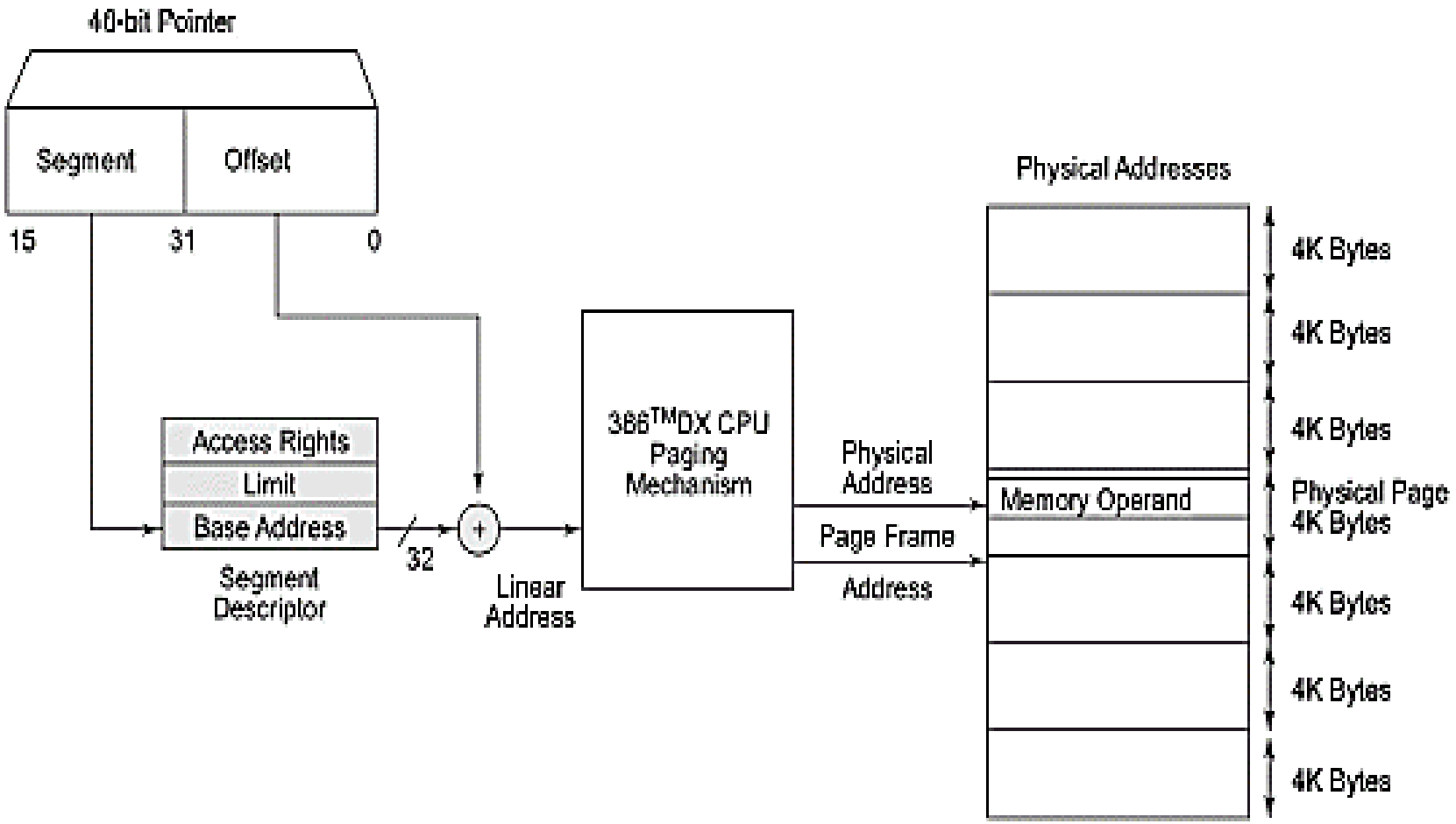


Fig. 10.5(b) *Paging Unit Enabled in Protected Mode Addressing (Intel Corp.)*

- ***Page Directory*** : This is at the most 4Kbytes in size. Each directory entry is of 4 bytes, thus a total of 1024 entries are allowed in a directory. The upper 10 bits of the linear address are used as an index to the corresponding page directory entry. The page directory entries point to page tables.
- ***Page Tables*****:** Each page table is of 4Kbytes in size and many contain a maximum of 1024 entries. The page table entries contain the starting address of the page and the statistical information about the page.
- The upper 20 bit page frame address is combined with the lower 12 bit of the linear address. The address bits A12 - A21 are used to select the 1024 page table entries. The page table can be shared between the tasks.

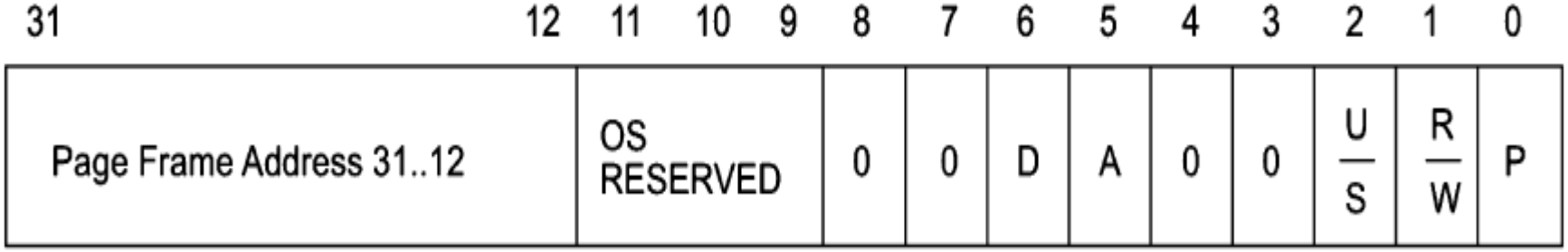


Fig. 10.7(a) *Page Directory Entry (Intel Corp.)*

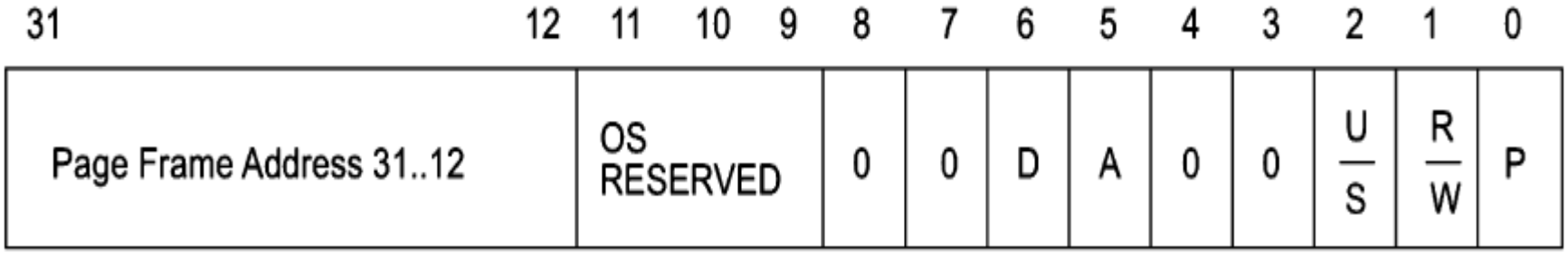


Fig. 10.7(b) *Page Table Entry (Intel Corp.)*

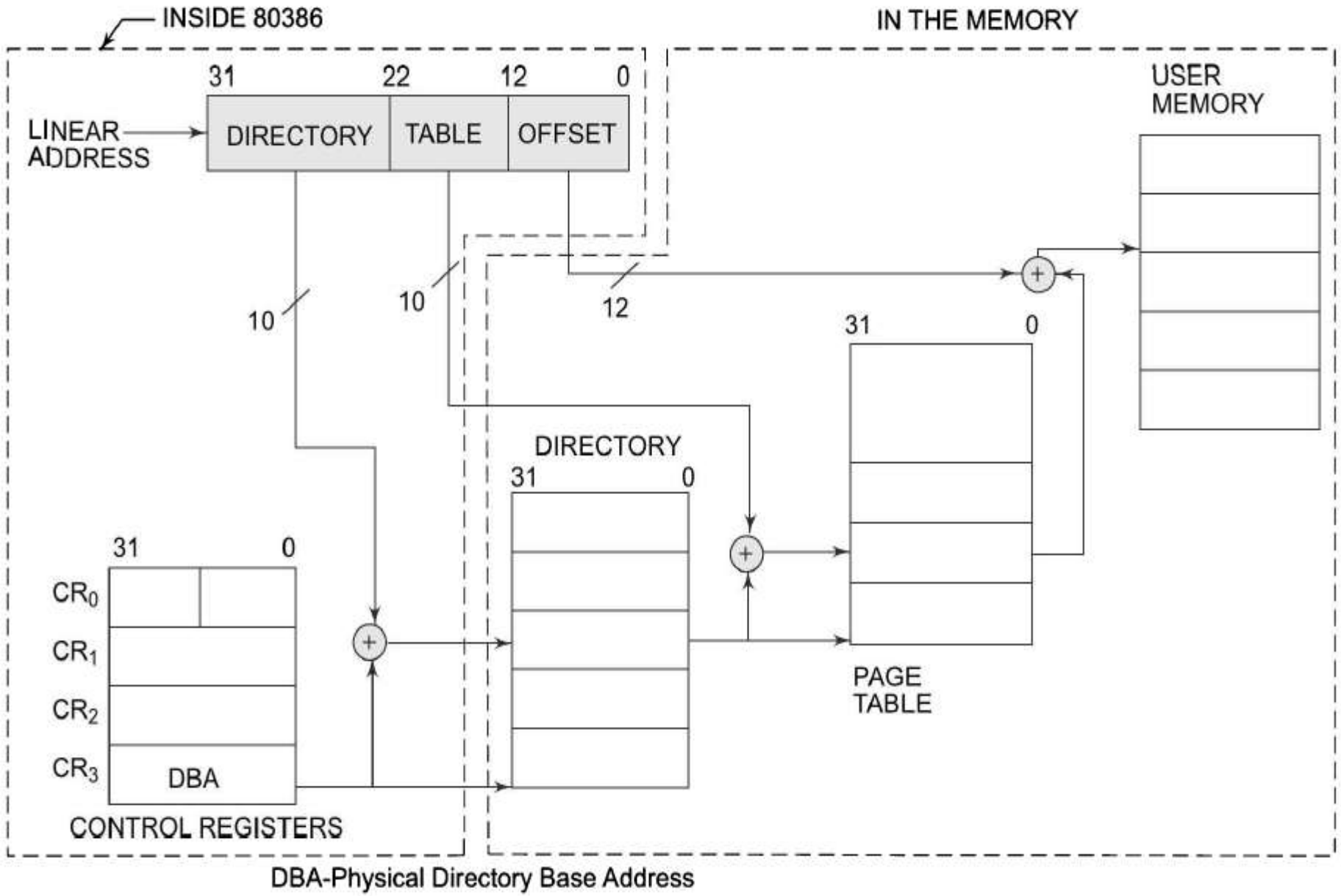


Fig. 10.8 *Paging Mechanism of 80386 (Intel Corp.)*

Intel Pentium

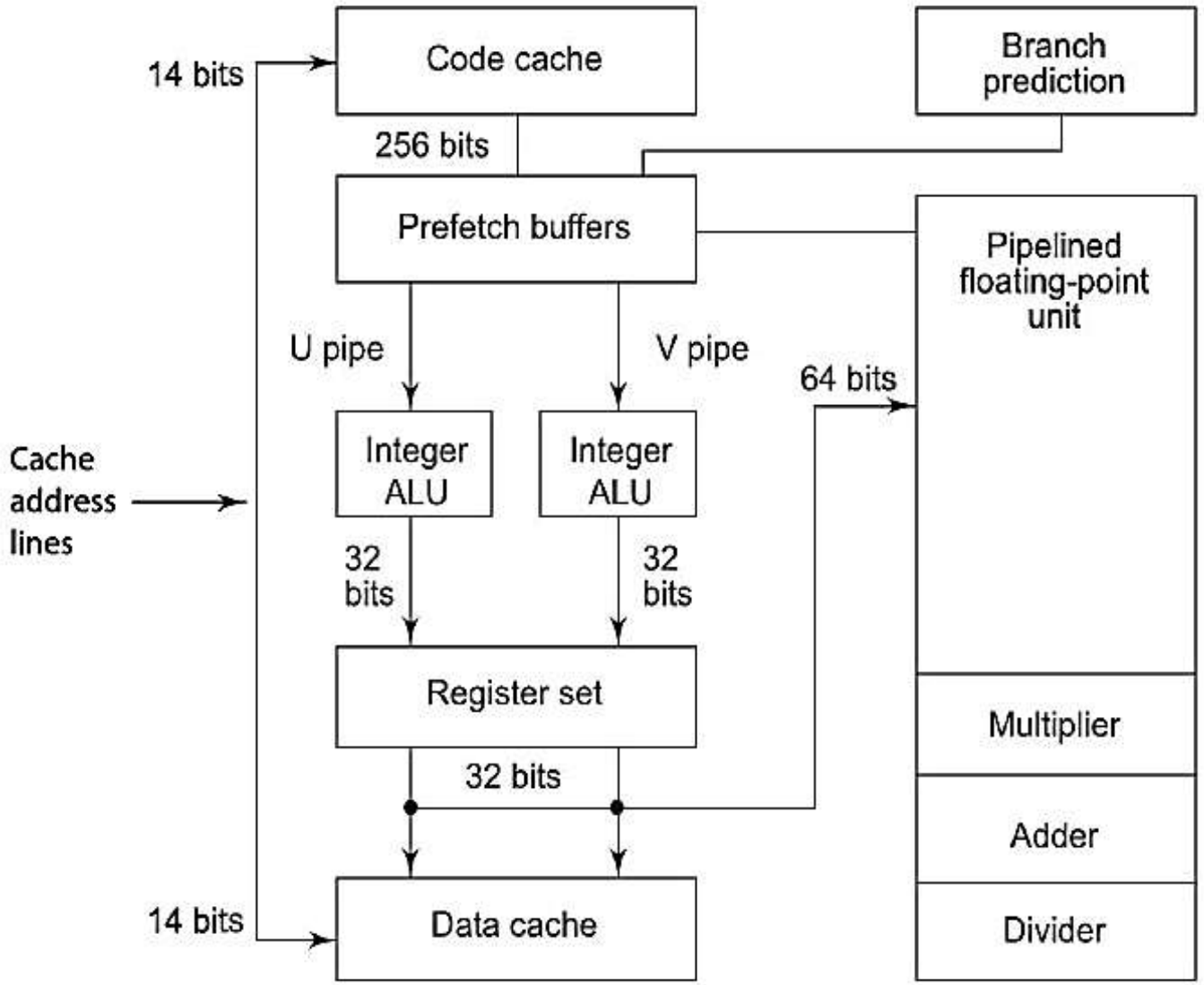


Fig. 11.1 *Pentium CPU Architecture*

11.3.1 Superscalar Execution

A salient feature of Pentium is that it supports superscalar architecture which has been explained in the previous section. For execution of multiple instructions concurrently, Pentium microprocessor issues two instructions in parallel to the two independent integer pipelines known as U and V pipelines. Each of these two pipelines has 5 stages, as shown in Fig. 11.2. These pipeline stages are similar to the one in 80486 CPU.

Functions of these pipelines have been presented in brief:

1. In the prefetch stage of the pipeline, the CPU fetches the instructions from the instruction cache, which stores the instructions to be executed. In this stage, the CPU also aligns the codes appropriately. This is required since the instructions are of variable length and the initial opcode bytes of each instruction should be appropriately aligned. After the prefetch stage, there are two decode stages D_1 and D_2.
2. In the D_1 stage, the CPU decodes the instruction and generates a control word. For simple RISC like instructions involving register data transfer or arithmetic and logical operations, only a single control word might be sufficient enough for starting the execution. However, as we know X86 architecture supports complex CISC instructions and require microcoded control sequencing.

3. Thus a second decode stage D_2 is required where the control word from D_1 stage is again decoded for final execution. Also the CPU generates addresses for data memory references in this stage.
4. In the execution stage, known as E stage, the CPU either accesses the data cache for data operands or executes the arithmetic/logic computations or floating-point operations in the execution unit.
5. In the final stage of the five-stage pipeline, which is the WB (writeback) stage, the CPU updates the registers' contents or the status in the flag register depending upon the execution result.

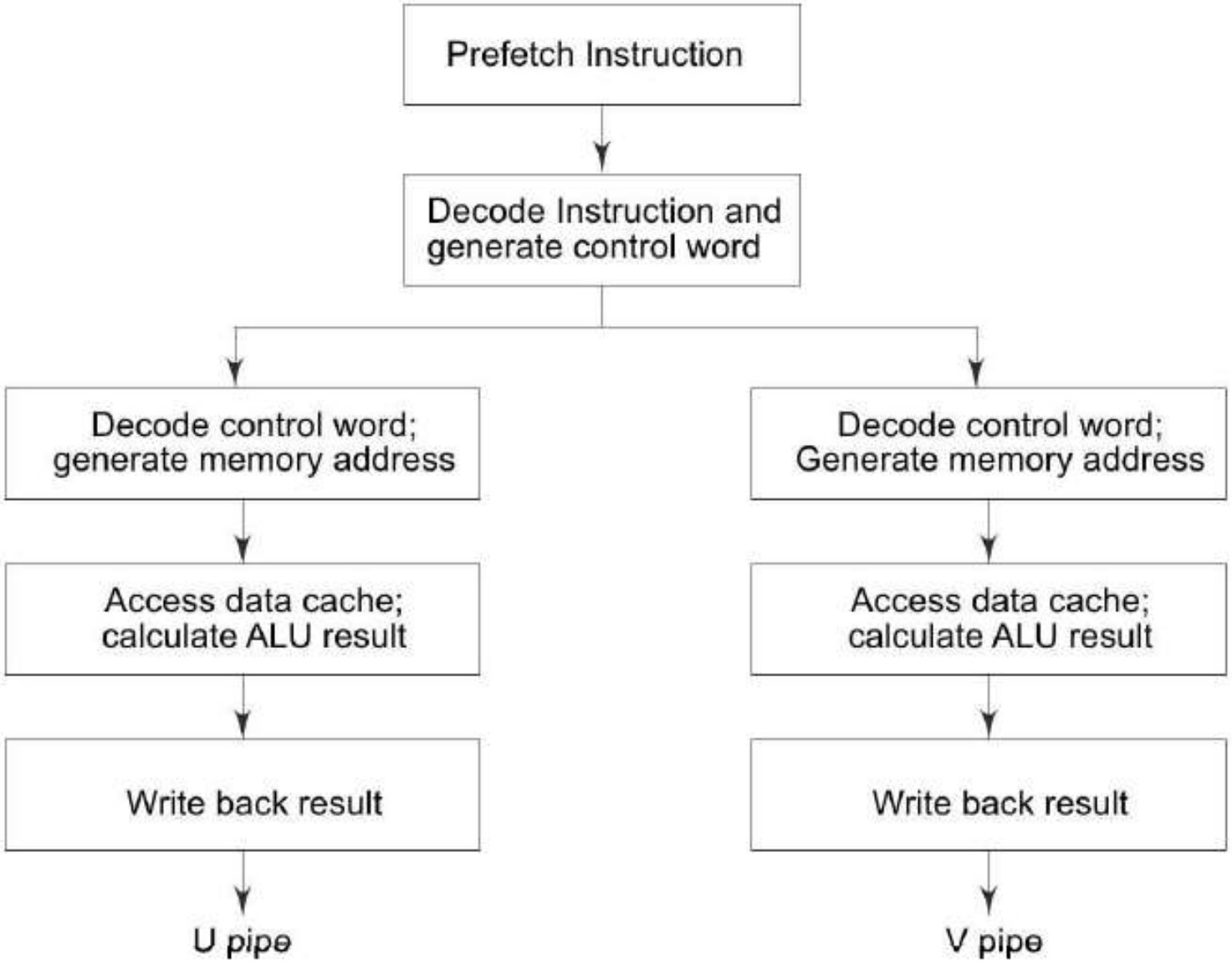
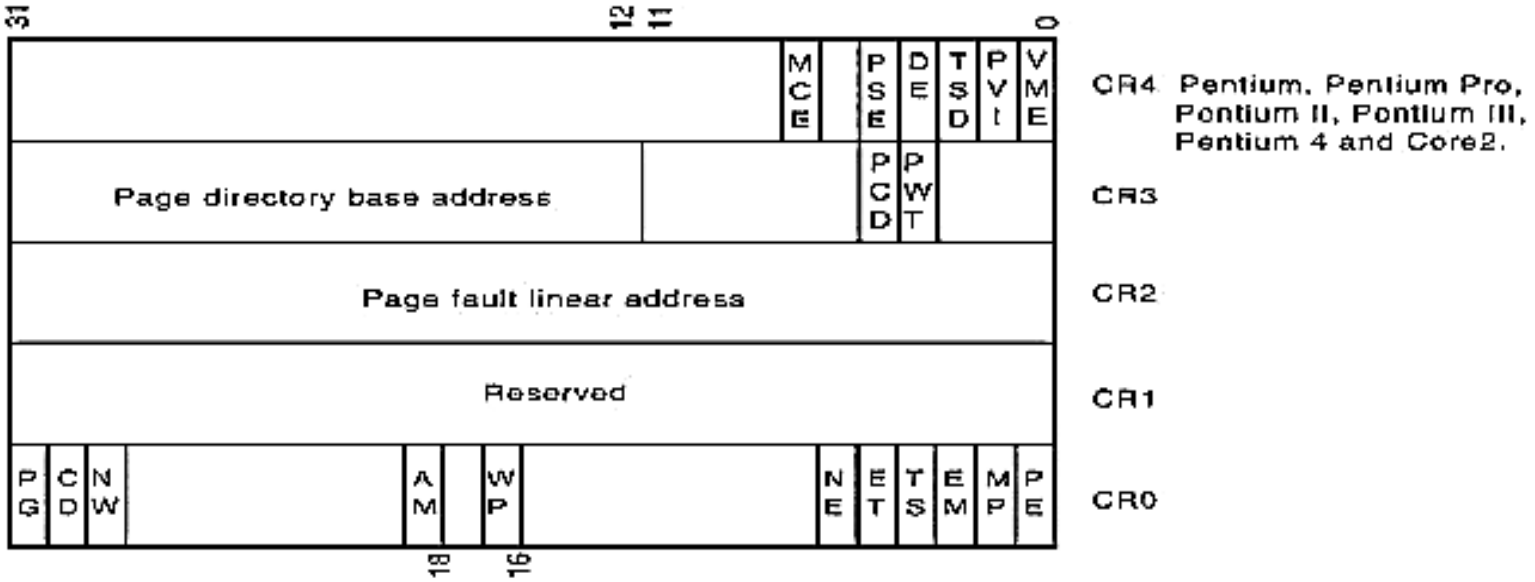


Fig. 11.2 ***Superscalar Organisation***

Control Registers



Bit	Name	Function
0	Virtual-8086 mode Extensions (VME)	Logic 1 enables support for a virtual interrupt flag in virtual-8086 mode.
1	Protected mode Virtual Interrupts (PVI)	Logic 1 enables support for a virtual interrupt flag in protected mode.
2	Time-date stamp Disable (TSD)	Logic 1 makes the read from time stamp counter (RDTSC) instruction a privileged instruction.
3	Debugging Extensions (DE)	Logic 1 enables I/O breakpoints.
4	Page size Extensions (PSE)	Logic 1 enables 4M-byte page size.
6	Machine check enable (MCE)	Logic 1 enables the machine-check exceptions.

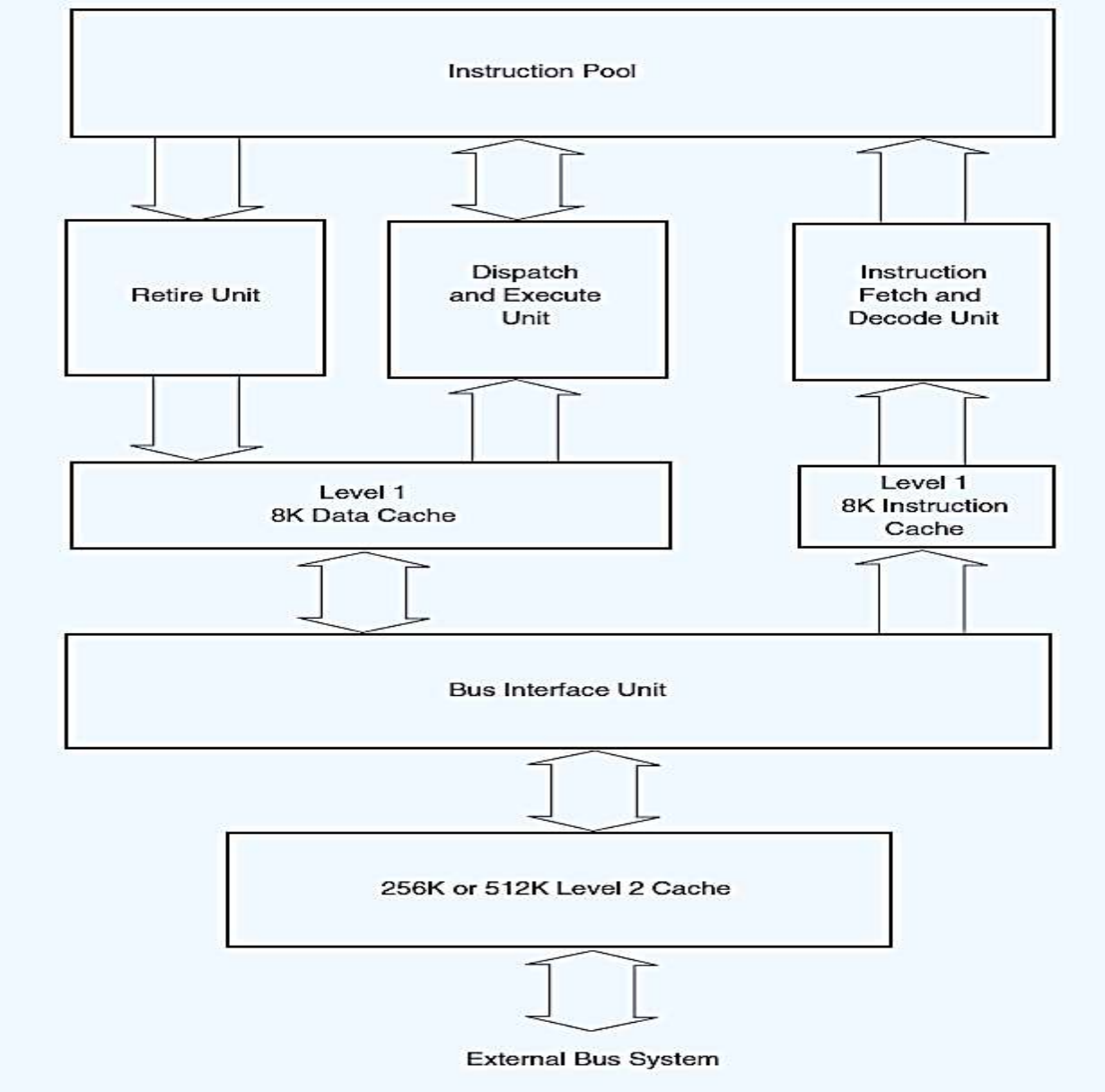
- **CD** cache disable controls the internal cache. If CD=1 , the cache will not fill with new data . If CD=0 misses will cause the cache to fill with new data
- **NW** Not write through selects the mode of operation for the data cache. If NW=1, the data cache is inhibited from cache write though
- **AM** Alignment mask enables alignment checking when set, it only occurs for protected mode
- **WP** write protect protects user level pages against supervisor level write operations. When WP=1, the supervisor can write to user level segments
- **NE** numeric error enables standard numeric coprocessor error detection.

Intel Pentium Pro

Introduction

- Pipeline is divided in 3 sections. Fetch and decode unit, dispatch and execution unit and retire unit.
- Intel Pentium Pro microprocessor takes CISC instructions and converts them into RISC micro-operations.

Internal Structure Of Pentium Pro



Internal Structure Of Pentium Pro

- The system bus connects to L2 cache.
- BIU controls system bus access via L2 cache.
- L2 cache is integrated in Intel Pentium Pro.
- BIU generates control signals and memory address.
- BIU fetches or passes data or instruction via L1 cache.
- The IFDU can decode three instructions simultaneously, and passes it to instruction pool.
- The IFDU has branch prediction logic.
- The DEU then executes the instructions.

- DEU contains three execution units. Two for processing integer instruction and one for processing floating point instruction simultaneously.
- Lastly RU checks the instruction pool and removes decoded instructions that have been executed.
- RU can remove three decoded instructions per clock pulse.

Drawbacks of Intel Pentium Pro Microprocessor

- As Intel Pentium Pro uses RISC approach the first drawback is converting instructions from CISC to RISC. It takes time to do so.
- So Pentium pro inevitably takes performance hit when processing instructions.
- Second is that out of order design can be particularly affected by 16 bit code resulting in eventual stop of process.
- ECC scheme causes additional cost of SDRAM that is 72 bits wide.

Differences Between Intel Pentium and Intel Pentium Pro

- Level-2 cache is integrated in Intel Pentium Pro and not in Pentium microprocessor. This speeds up processing and reduces number of components.
- In Pentium unified cache holds both instructions and data, but in Pentium Pro separate cache is used for instruction and data which speeds up performance.
- Pentium microprocessor doesn't have jump execution unit or address generation unit as Pentium Pro has. It's one of the major changes.