Unit 7 : - ADVANCE MICROPROCESSORS

Syllabus

- 80286 Microprocessor Architecture

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Features Of 80286 Microprocessor

The Intel 80286, often referred to as the 286, is a **16-bit microprocessor** that was introduced by Intel in 1982. It was the first processor in the x86 family to support protected mode, allowing for more advanced memory management and multitasking capabilities. Here's an overview of the 80286 microprocessor, including its address, data, and control buses, as well as the number of bits it uses:

Address Bus

- Size: **24 bits**
- Function: The address bus is used to specify the memory addresses that the CPU wants to access (either for reading or writing data). With 24 bits, the 80286 can address up to 16 MB (2^24 bytes) of physical memory.

Features Of 80286 Microprocessor

Data Bus

- Size: **16 bits**
- Function: The data bus is used for the transfer of actual data between the CPU and memory or I/O devices. Since the 80286 has a 16-bit data bus, it can read or write 16 bits (2 bytes) of data in a single operation.

Control Bus

- Function: The control bus is composed of various control signals that are used to manage and coordinate the operations of the CPU, memory, and I/O devices. These signals control the direction of data flow, memory access, interrupt handling, and more. Key control signals in the 80286 include:
- **RD(Read):** Indicates that the CPU is reading data from memory or an I/O device.
- **WR(Write):** Indicates that the CPU is writing data to memory or an I/O device.
- **ALE(Address Latch Enable**): Used to indicate that the address bus contains a valid address.
- **M/IO**: Distinguishes between memory and I/O operations.
- **INTA(Interrupt Acknowledge)**: Used to acknowledge an interrupt request.

Features Of 80286 Microprocessor

- 80286 is composed of nearly around **125K transistors** and the pin configuration has a total of **68 pins**.
- Two Modes Of Operation. They are:-

1.Real Address Mode

2.Protected Address Mode

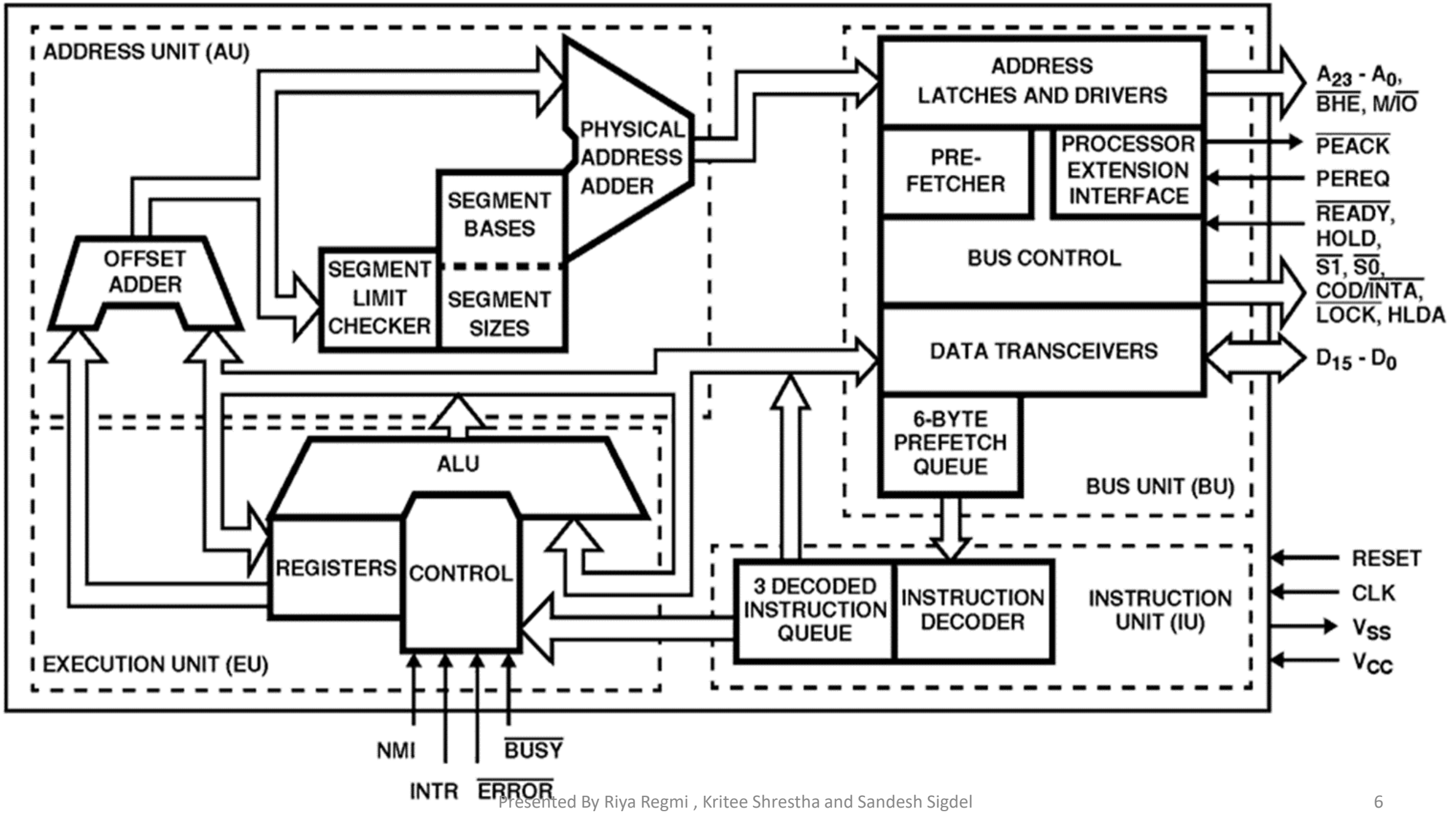
- 8 General Purpose Registers (**AX,BX,CX,DX,SI,DI,BP and SP**)
- 4 Segment Registers (**CS,DS,ES And SS**)

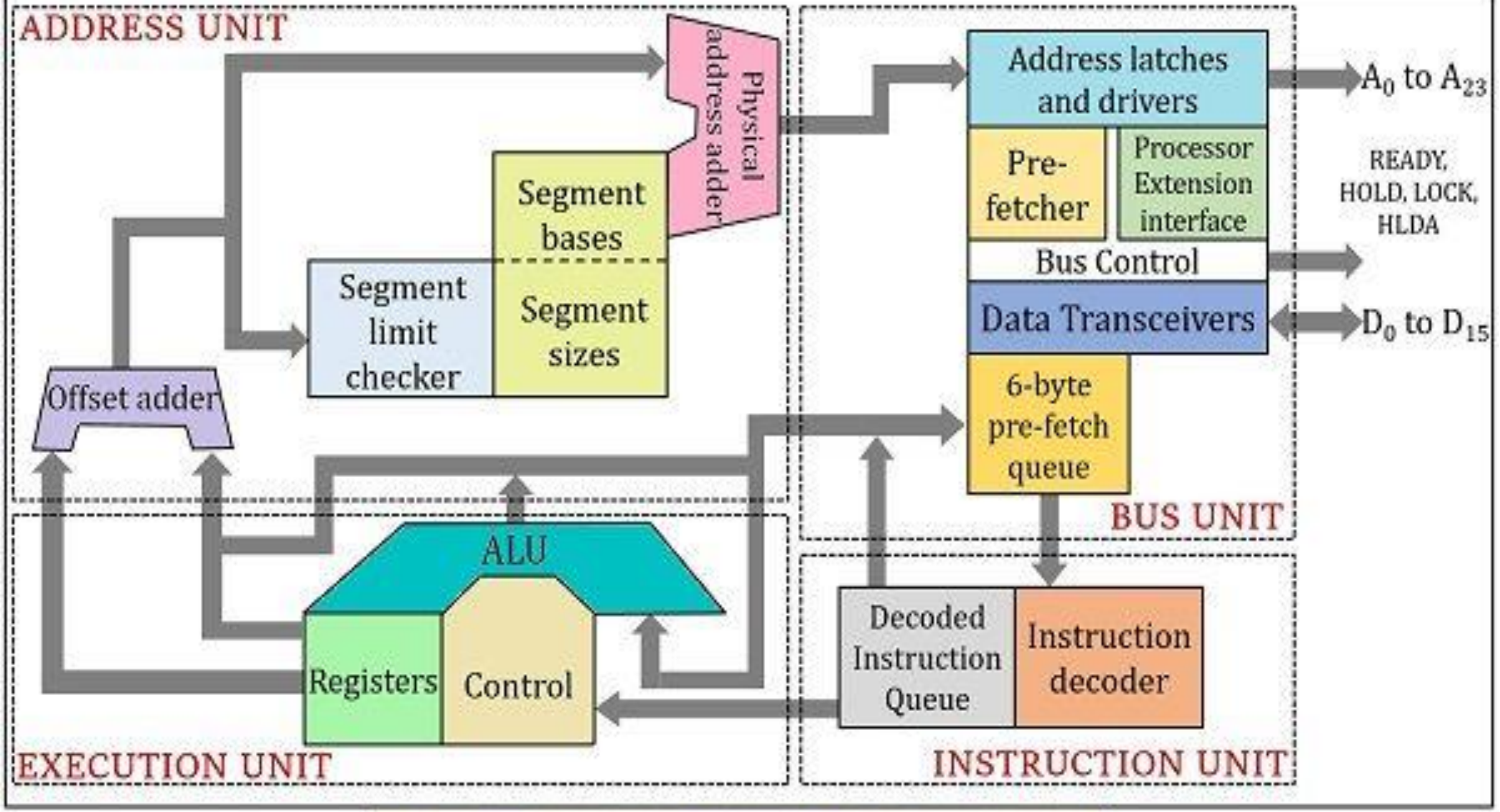
Logical Block Diagram/Internal Architecture of 80286 Microprocessor

The Architecture Of 80286 Microprocessor is composed of 4 Functional Units. They are :

- **Address Unit (AU)**
- **Bus Unit(BU)**
- **Instruction Unit (IU)**
- **Execution Unit (EU)**

- The figure below shows the block diagram of architectural representation of 80286 Microprocessor:


ADDRESS UNIT (AU)
PHYSICAL ADDRESS ADDER
SEGMENT BASES
SEGMENT LIMIT CHECKER
SEGMENT SIZES
OFFSET ADDER
ADDRESS LATCHES AND DRIVERS
PRE-FETCHER
PROCESSOR EXTENSION INTERFACE
BUS CONTROL
DATA TRANSCEIVERS
6-BYTE PREFETCH QUEUE
BUS UNIT (BU)
A23 - A0, BHE, M/IO
PEACK
PEREQ
READY, HOLD, S1, S0, COD/INTA, LOCK, HLDA
D15 - D0
ALU
REGISTERS
CONTROL
3 DECODED INSTRUCTION QUEUE
INSTRUCTION DECODER
INSTRUCTION UNIT (IU)
EXECUTION UNIT (EU)
RESET
CLK
VSS
VCC
NMI
BUSY
INTR
ERROR



Block Diagram of 80286 Microprocessor

Address Unit (AU)

- The address unit (AU) is used to determine the physical addresses of instructions and operands which are stored in memory.
- The AU computes the 20-bit physical address based on the contents of the segment register and 16-bit offset just like 8086.
- The address lines derived by AU can be used to address different peripheral devices such as memory and I/O devices. This physical address computed by the address unit is sent to the Bus Unit (BU) of the CPU

Bus Unit(BU)

- The bus unit interfaces the 80286 with memory and I/O devices.
- This processor has a 16-bit data bus, a 24-bit address bus, and a control bus.
- The bus unit is responsible for performing all external bus operations.
- This unit consists of latches and drivers for the address bus, which transmit the physical address A19 A0. The A19-A0 facilitates all memory and I/O devices for read and write operations.
- The bus unit is used to fetch instruction bytes from the memory. Generally, the instructions are fetched in advance and stored in a queue for faster execution of the instructions. This concept is known as instruction pipelining.
- Hence, to fetch instruction, the CPU will not wait till the completion of execution of the previous instruction. While one instruction is being executed, the subsequent instruction is to be prefetched, decoded and kept ready for execution. The prefetcher module in the bus unit performs this task of prefetching. The bus unit has a bus control module which controls the prefetcher module. The fetched instructions are arranged in a 6-byte prefetch queue. In this way, the CPU prefetches the instructions, to enhance the speed of execution.

Instruction Unit(IU)

- The 6-byte prefetch queue forwards the instructions sequentially to the Instruction Unit (IU).
- The instruction unit receives instructions from the prefetch queue and an instruction decoder decodes them one by one. The decoded instructions are latched onto a decoded instruction queue.
- The IU decodes maximum 3 prefetched instructions and loads them into decoded instruction queue for execution by execution unit.

Execution Unit(EU)

- The output of the decoded instruction queue is fed to a control circuit of the execution unit.
- This unit is responsible for executing the instructions received from the decoded instruction queue.
- The execution unit consists of the **Register bank**, **Arithmetic and logic unit (ALU)** and **Control block**.
- The **register bank** is used for storing the data as a scratch pad. The register bank can also be used as special-purpose registers.
- The **ALU** is the core of the EU and perform all the arithmetic and logical operations and sends the results either over the data bus or back to the register bank.
- The **control block** controls the overall operation of the execution unit.