WEL COME

TO OUR PRESENTATION

REGISTER ORGANIZATTION OF 80386 MICROPROCESSOR

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INTRODUCTION TO 80386 MICROPROCESSOR

- 80386 microprocessor was launched by intel in 1985.
- Landmark in the history of computing for various different reasons
- It used 32 bit processing to the architecture which significantly enhanced computing capabilities and performance
- The processor played a crucial role in the development of the modern personal computers , servers and work stations.
- Introduction of the advanced features like multitasking and virtual memory management over its predecessors 8085,8086,80286.

KEY FEATURES OF 80386 MICROPROCESSOR

- 32 Bit Data Bus

  Allowed For handling 32 bit of data types and improved efficiency and the speed of data processing

- 32 Bit Address Bus

  Enabled access to a larger memory space up to 4 GB (2^32)

- Multitasking Support

  Allowing multiple application to run simultaneously improving efficiency and speed.

- Virtual memory Management

  Provided mechanism for paging and segmentation allowing use of memory and protection of application data.

- Backward compatibility

  Ensuring the software designed for earlier 16-bit processor would run in 80386.

Registers of 80386 Microprocessor

- The 80386 processor has significantly extended the 8086 register set.
- All the registers of 80286 are exist in the 80386 processor and some new registers have been added in 80386.
- Generally, the registers of 80386 microprocessor are of 32 bits and they can be used as 8-bit and 16-bit registers.

- General Purpose Register
- Segment Register
- Control Register
- Debug Register
- Test Register
- Flag Register
- Special Register

Registers of 80386 Microprocessor

The registers of 80386 are divided as general-purpose registers and special registers.

General-purpose registers:

- 32-bit EAX, EBX, ECX, EDX, ESI, SDI, EBP and ESP.

Special registers:

- Segment (selector) registers 16-bit CS, DS, ES, SS, FS, and GS
- 32-BIT EIP
- EFLAGs

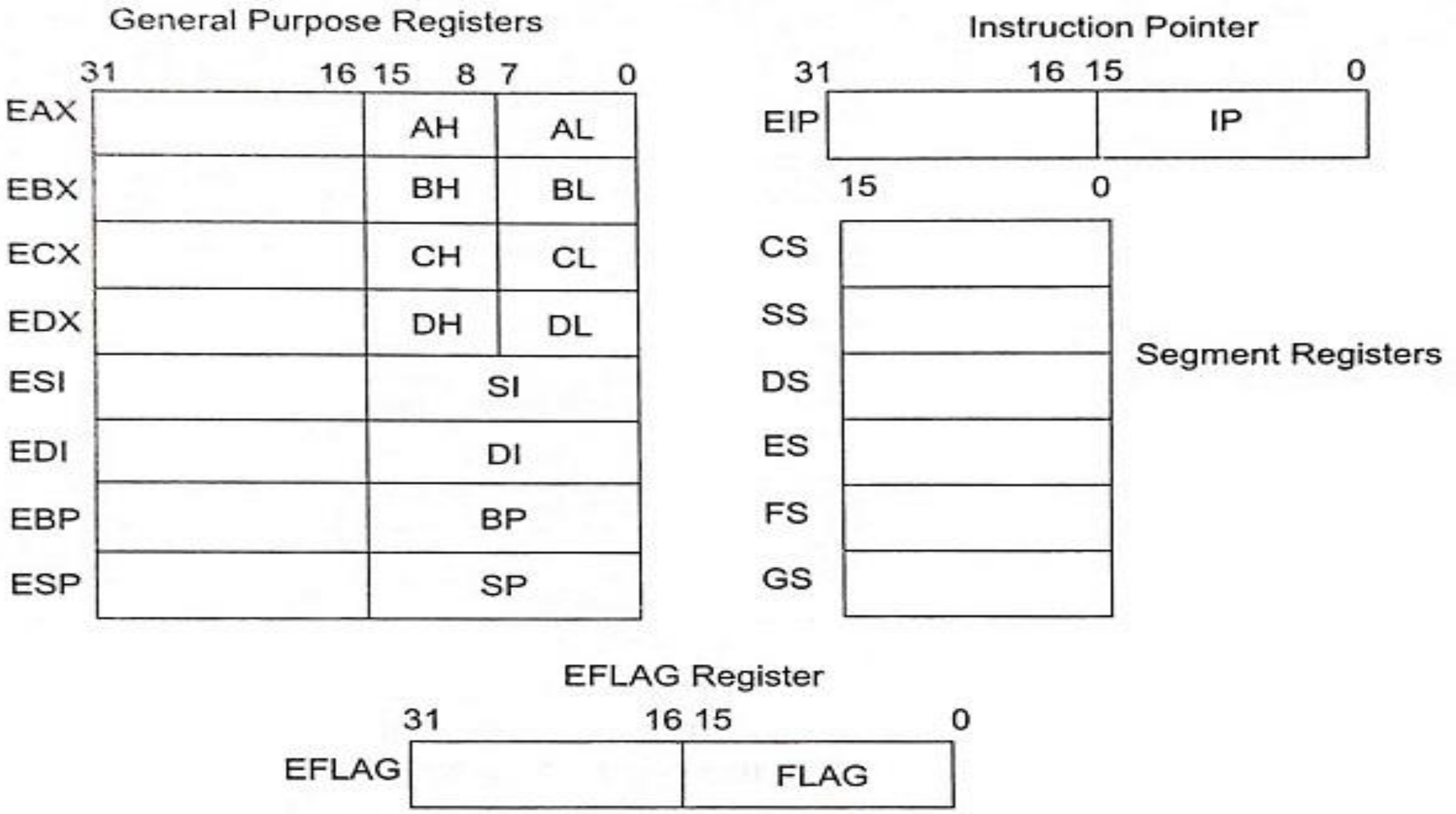

Fig. 11.33 *Registers of 80386*

General-Purpose Registers

- The general-purpose registers is able to hold 8-bit, 16-bit, or 32-bit data.
- The 8086 microprocessor has byte and word-sized registers, but the 80386 contains double-word sized or extended registers.
- The 8- and 16-bit registers can be addressed just like the 8086 processor.
- The AX, BX, CX, DX, SI, DI, BP, SP, FLAGS and IP registers are 16-bit registers and they have been extended to 32 bits.
- A 32-bit register is called an extended register and it is represented by the register name with prefix E. For example, a 32-bit register corresponding to AX is represented by EAX.
- Similarly, all 32-bit general-purpose registers are represented by EAX, EBX, ECX, EDX, ESI, EDI.
- The other 32-bit registers are EBP, ESP, EFLAGS, and EIP.

Segment Registers

- In 80386 MP, there are 6(16-bits) segment register in which 4 of them are same as the 8086 MP and 2 new additional registers FS and GS registers.
- They are:
  - CS(code segment):
    - Holds the base address of the code segment.
    - It is the memory area in which all the instructions that the MP executes is written at
  - DS(data segment):
    - Points to the base address of the data segment where most data variables are stored.

- SS(stack segment):

  -Points to the stack segment, which holds the stack for managing function calls, local variables, and return addresses.

- ES(extra segment):

  -Acts as an additional data segment that can be used for string operations and other data manipulations.

- FS and GS:
  - They are the additional segment registers which are used for increasing the efficiency of the CPU.
  - FS and GS can be used to quickly access frequently used data structures. By setting these segment registers to point to specific areas of memory, the processor can efficiently access the data without recalculating addresses through this register.
  - FS and GS segment registers are often used to point to the base of the thread-local storage area. This makes it easy for threads to quickly access their own data without complex address calculations or conflicts with other threads.

Control Register

- They are 32-bits register.
- They are used to control different modes of operation of CPU, memory management and the task switching process indicate in the microprocessor.
- There are 4 control registers each of 32-bits in 80386mp from CR0 to CR3.
  - CR0:

    -it enables/disables the features, protected mode and the paging.

    -it indicates if the task switching has occurred.
  - CR1:

    -They are the reserved and not used.
  - CR2:

    -Holds the address that caused a page fault in memory.

    -Tells the OS where a memory error happened.

- CR3:
  -Points to a table used for translating virtual memory addresses to physical memory addresses.

Debugging Registers

- They are 32-bits register.
- They are used for the debugging purposes during the execution of the program.
- They are used for diagnosing and debugging the errors executed in the program.
- There are 8 debugging registers in 80386 MP from DR0-DR7.
    - DR0 to DR3:

      -These 4 registers DR0,DR1,DR2 and DR3 are used to store 4 breakpoint address.

      -We can setup the 4 breakpoints on our own in the debugger in its address.

      -Here the breakpoint means the pausing of the execution of the programming and the control is transferred to the debugger for debugging purpose.

      -If the breakpoint is hit then the debugging exception trigger.
    - DR4 and DR5:

      -They are reserved which means that it cannot be used for the debugging purpose.

- DR6 and DR7:

  -They are used for storing the status of the breakpoint and control of the breakpoints triggering.

  DR6(status of breakpoint):

  -it indicates which of the breakpoint was hit.

  -it consists of flags like:

  *b0 to b3 correspond to the breakpoint 0 to 3 (DR0 to DR3).

  *BD indicates if there is failure in handling error.

  *BT indicates if the task switching has occurred.

  DR7(debug control register):

  -Controls how the breakpoints are triggered.

  -Sets condition to enable/disable the breakpoint.

Test Registers

- Two test registers TR6 and TR7 exist in the 80386 processor for page caching as shown in above figure.
- TR6 is known as test control and TR7 is called a test status register.

FLAG Register

- The flag register of the 80386 is a 32-bit register as shown in below figure.
- Among these 32 bits, D31 to D18, D15, D5 and D3 are reserved by Intel and D_1 is always 1.
- The lower fifteen bits of flag register of 80386 are same as 80286. Only two flags are newly added to the 80286 flag register to get the flag register of 80386.
- The two new flags are VM and RF flag.

RF (Resume Flag)

- This is the first bit in the extended EFLAGS register. It is used with the debug register breakpoints.
- At the starting of each instruction cycle, the status of RF is always checked.
- If RF = 1, any debug fault will be ignored while executing any instruction.
- This flag is automatically reset after execution of instructions except IRET and POPF.

VM (Virtual Mode Flag)

- When this flag is set, the 80386 enters in the virtual 8086 mode within the protected mode.
- If VF is set, 80386 operates in protected mode.

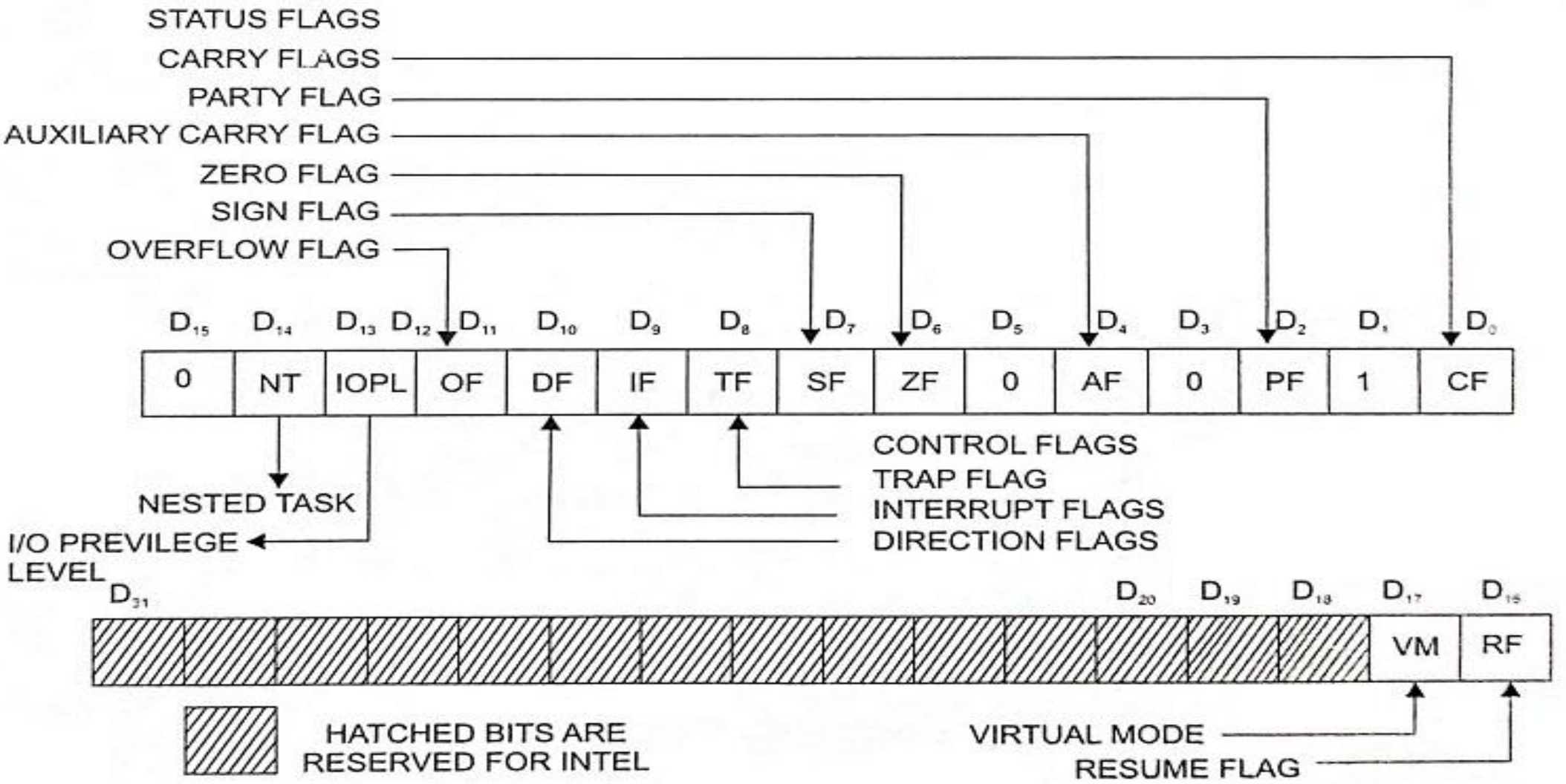

Fig. 11.35 *FLAG register of the 80386*