Architecture(Block)diagram of 80286 Microprocessor

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Architecture of 80286 Microprocessor

·The Architecture of 80286 Microprocessor is an advanced, high performance microprocessor with specially optimized capabilities for multi-user and multitasking systems.

·The 80286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy. The 80286 is compatible with 8086 and 8088 operating software.

The Architecture of 80286 Microprocessor has two operating modes:

a. **real address mode** : uses a 20-bit address bus, allowing it to address up to 1 MB (2^20 bytes) of physical memory.

b. **protected virtual address mode**: uses a 24-bit address bus, allowing it to address up to 16 MB (2^24 bytes) of physical memory

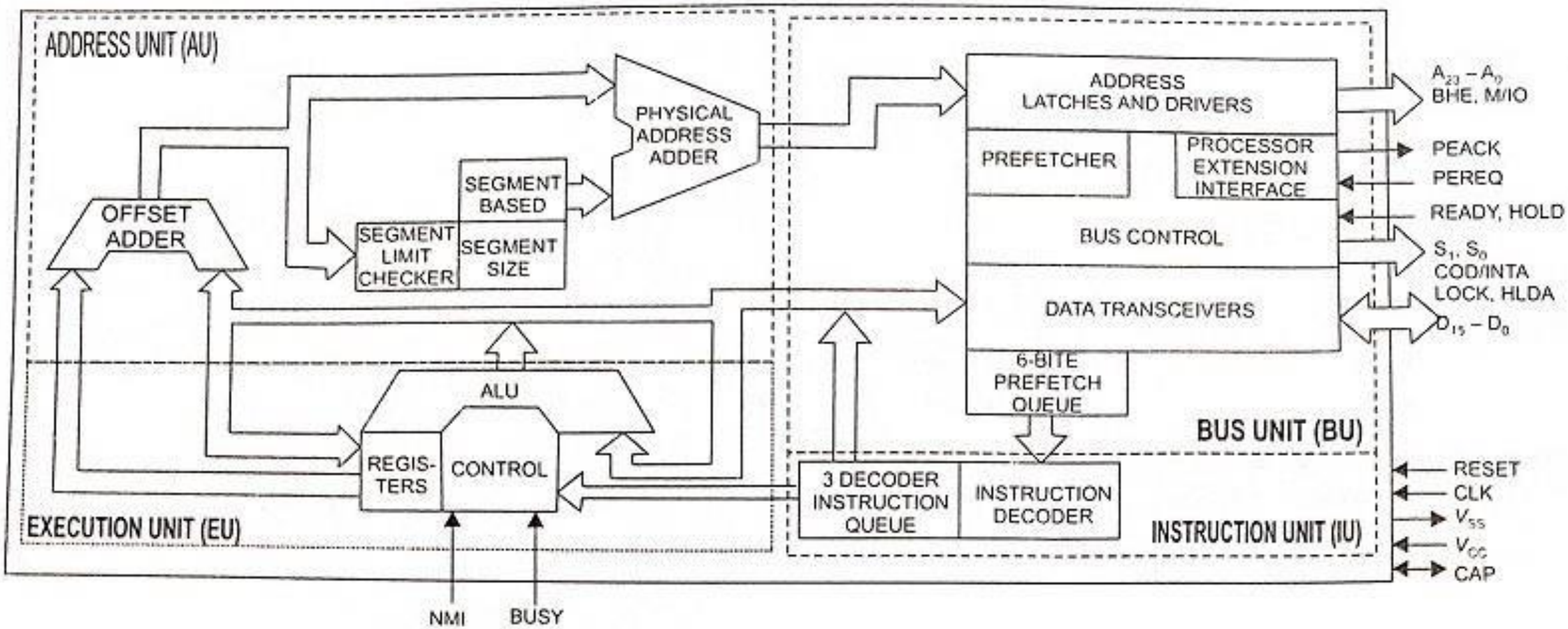

Fig. 11.15 *Internal block diagram of the 80286 processor*

The CPU of the 80286 processor consists of four functional units such as

1.Address Unit (AU)

2.Bus Unit (BU)

3.Instruction Unit (IU)

4.Execution Unit (EU)

Address Unit

- The address unit (AU) is used to determine the physical addresses of instructions and operands which are stored in memory.
- The AU computes the 20-bit physical address based on the contents of the segment register and 16-bit offset just like 8086.
- The address lines derived by AU can be used to address different peripheral devices such as memory and I/O devices.
- This physical address computed by the address unit is sent to the Bus Unit (BU) of the CPU.

Bus Unit

·The bus unit interfaces the 80286 with memory and I/O devices. This processor has a 16-bit data bus, a 24-bit address bus, and a control bus. ·The bus unit is responsible for performing all external bus operations.

·This unit consists of latches and drivers for the address bus, which transmit the physical address A_{19}-A_0. The A_{19}-A_0 facilitates all memory and I/O devices for read and write operations.

Instruction Unit

- The 6-byte prefetch queue forwards the instructions sequentially to the Instruction Unit (IU).
- The instruction unit receives instructions from the prefetch queue and an instruction decoder decodes them one by one.
- The decoded instructions are latched onto a decoded instruction queue.
- The IU decodes maximum 3 prefetched instructions and loads them into decoded instruction queue for execution by execution unit

Execution Unit

- The output of the decoded instruction queue is fed to a control circuit of the execution unit.
- This unit is responsible for executing the instructions received from the decoded instruction queue.
- The execution unit consists of the register bank, arithmetic and logic unit (ALU) and control block.
- The register bank is used for storing the data as a scratch pad. The register hank can also be used as special purpose registers