Texas International collage
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80386 Microprocessor Architecture

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Characteristics of 80386 microprocessor

- 80386 microprocessor is a 32 bit processor that holds the ability to carry out 32-bit operations in one cycle. It has a data and address bus of 32-bit each. Thus has the ability to address 4 GB (or 2^{32}) of physical memory.
- 80386 supports a variety of operating clock frequencies, which are 16 MHz, and 33MHz.
- It offers 3 stage pipeline: fetch, decode, and execute. As it supports simultaneous fetching, decoding, and execution inside the system.

Block Diagram of 80386 Microprocessor

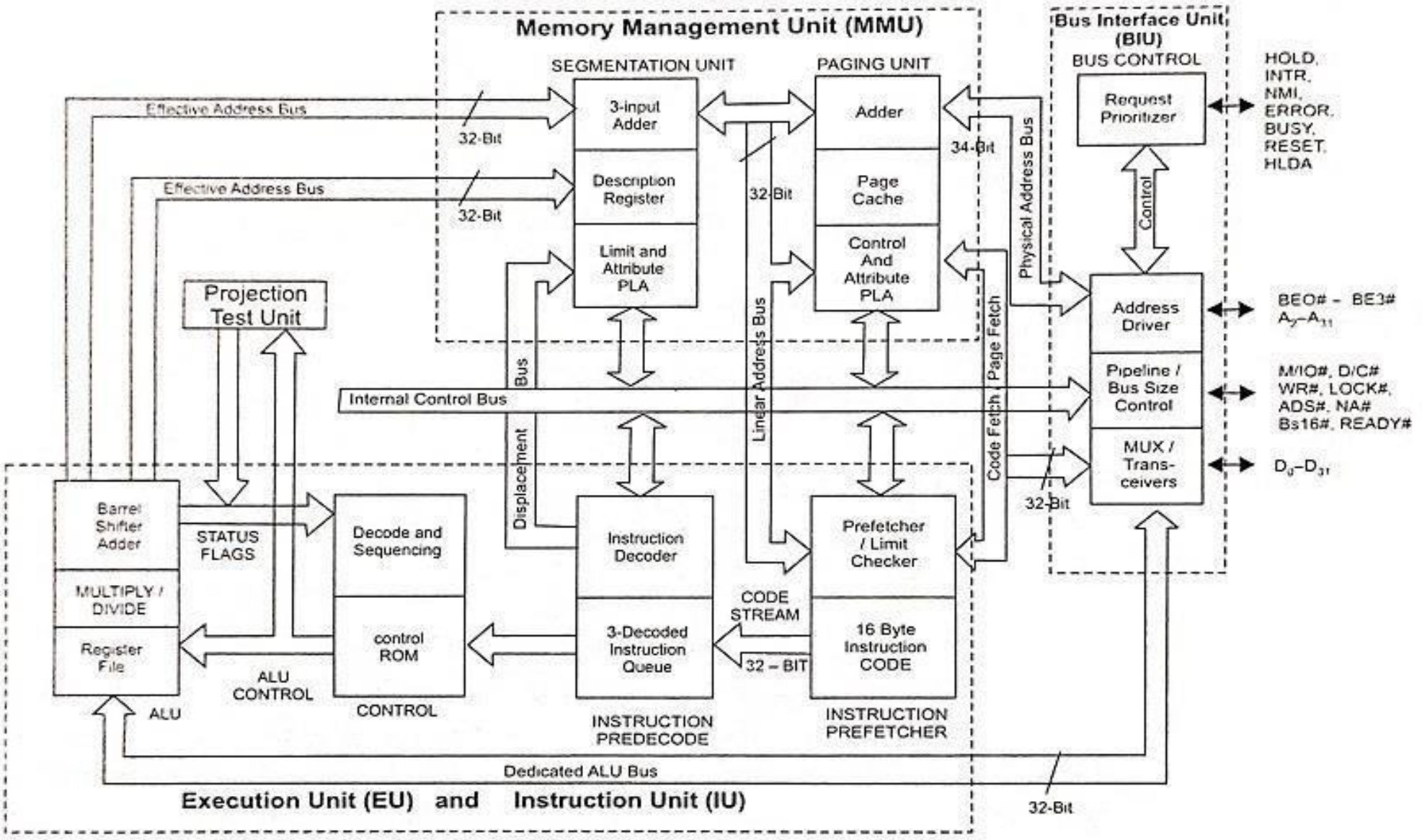
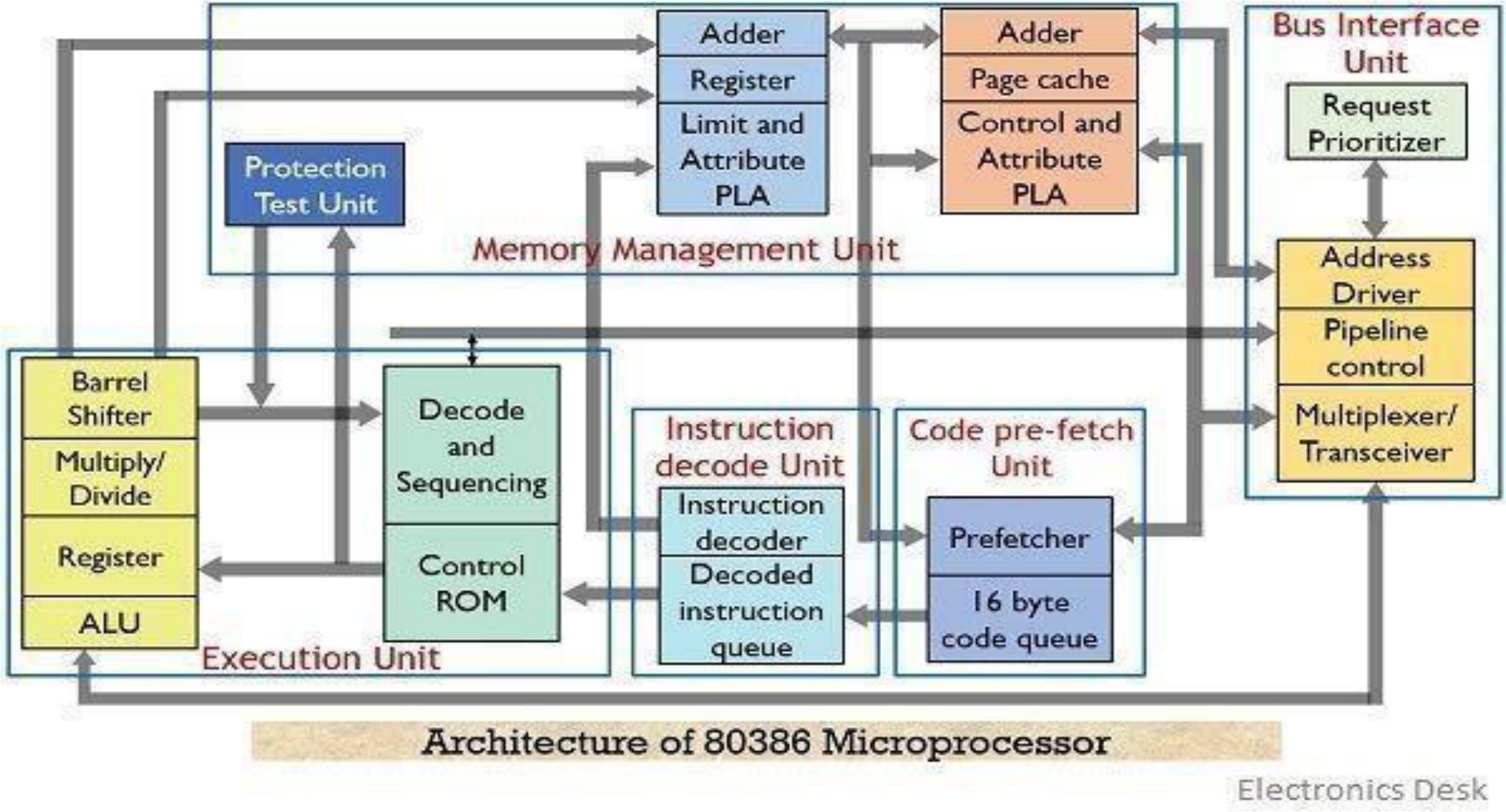


Fig. 11.32 *The detailed internal architecture of 80386 processor*

Architecture of 80386



Basically, from above diagram of architecture of 80386 microprocessor, It has 6 functional units which are as follows:

1. Bus interface unit
2. Code fetch unit
3. Instruction decode unit
4. Execution unit
5. Segmentation unit
6. Paging unit

As 80386 possesses the ability of 3 stages fetching, decoding, and execution simultaneously along with memory management and bus accessing. Thus all unit operate parallelly. Thus pipelining leads to a reduction in overall processing time thereby increasing the performance of the overall system.

1. Bus interface unit

- BIU has a 32-bit bidirectional data bus and a 32-bit address bus.
- Generates signals to activate data and address buses for fetching instructions or data.
- Connects peripheral devices through the memory unit.
- Controls interfacing of external buses with microprocessors.

2. Code fetch unit

- Fetches instructions from memory using system buses.
- Stores fetched instructions in a 16-byte prefetch queue.
- Fetches instructions in advance to speed up operations.
- Instruction sequence in queue matches memory order.
- Releases control of buses when data transfer is needed.

3.instruction decode unit

- Instruction in the memory are stored in the form of bytes. So, this unit decodes the instructions stored in the prefetch queue.

- Basically, the decoder changes the machine language code into assembly language and transfer it to the processor for the further execution.

4. Execution unit

- Decoded instructions stored in a decoded instruction queue.
- Execution unit uses this queue to execute instructions.
- Execution unit controls instruction execution.
- Has a 32-bit ALU for 32-bit operations in one cycle.
- Includes 8 general-purpose and 8 special-purpose registers.
- Registers used for data handling and offset address calculation.

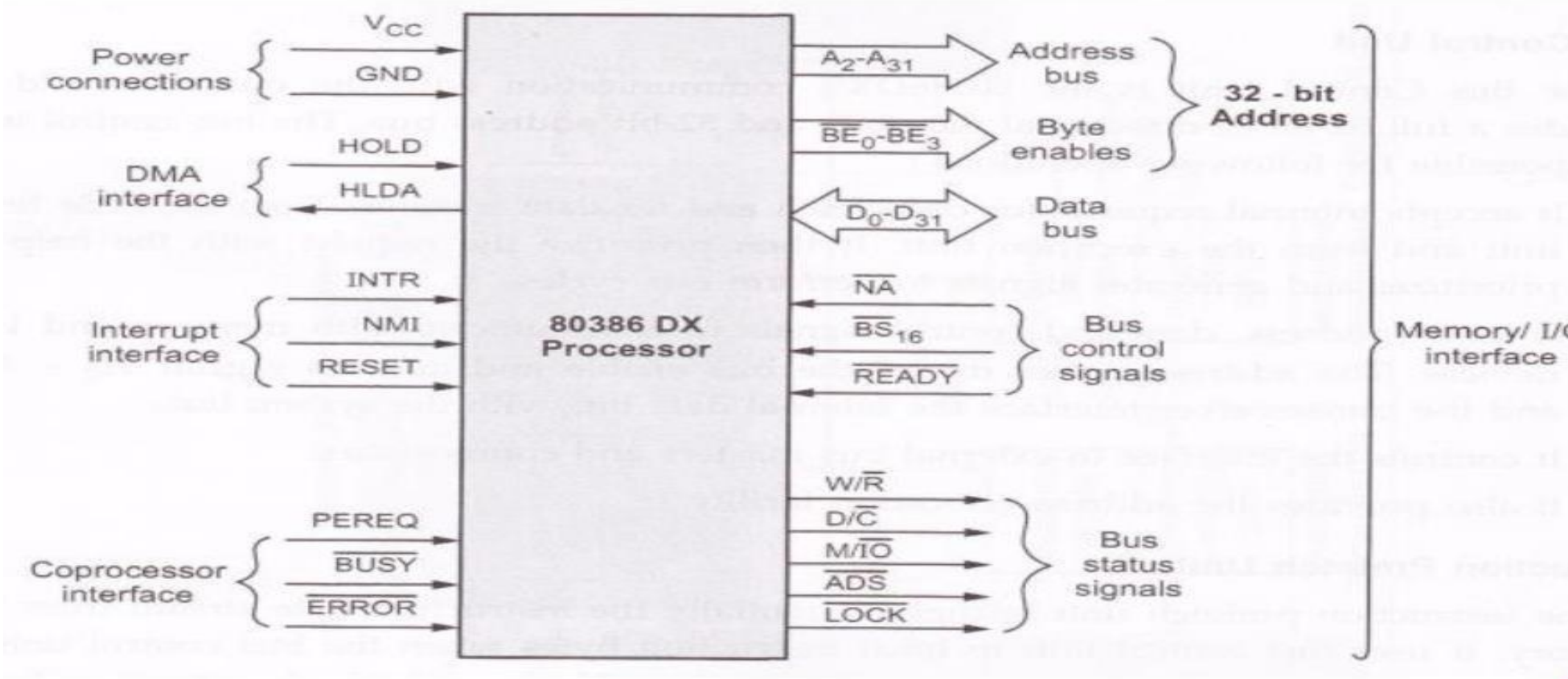
5. Segmentation unit

- Provides a protection mechanism for memory.
- Offers 4 levels of protection (PL0 to PL3).
- PL0 has the highest priority, PL3 the lowest.
- Main OS parts stored in PL0, user programs in PL3.
- First microprocessor to introduce this protection feature.

6. Paging unit

- Paging unit operates only in protected mode.
- It converts linear addresses into physical addresses.
- Programmers provide virtual addresses, not physical addresses.
- Segmentation unit controls the paging unit's actions.
- Segmentation unit converts logical addresses to linear addresses during instruction execution.
- Paging unit maps tasks into pages, each 4KB in size.
- This allows handling tasks as pages instead of segments.
- Supports multitasking.
- Only stores currently needed segment parts in memory.

Pin diagram of 80386 microprocessor



Brief information of pins of 80386 MP

1. **AD0-AD31 (Address/Data Bus)**: These are the time-multiplexed address and data lines. During the address phase, these lines carry the address, and during the data phase, they carry the data.
2. **A0-A31 (Address Bus)**: These pins provide the higher order address bits.
3. **BE0#-BE3# (Bus Enable)**: These pins are used to indicate the valid bytes of data on the data bus. They are active low.
4. **ADS# (Address Status)**: This pin is asserted by the processor to indicate that a valid bus cycle is in progress. It is active low.
5. **READY**: This pin is used to indicate that the addressed memory or I/O device is ready for data transfer.
6. **NA# (Next Address)**: This pin is used to allow pipelining of bus cycles. It signals that the next address is ready.

7. **M/IO# (Memory/Input-Output)**: This pin indicates whether the current bus cycle is a memory operation or an I/O operation. It is active low for I/O operations.
8. **D/C# (Data/Control)**: This pin indicates whether the current bus cycle is data or control. It is active low for control operations.
9. **W/R# (Write/Read)**: This pin indicates whether the current bus cycle is a write or a read. It is active low for read operations.
10. **LOCK#**: This pin is used to lock the system bus during certain critical operations to ensure exclusive use.
11. **HOLD**: This pin is used by external devices to gain control of the bus.
12. **HLDA (Hold Acknowledge)**: This pin is used by the processor to acknowledge the hold request.
13. **INTA# (Interrupt Acknowledge)**: This pin is used to acknowledge interrupt requests.

14. **NMI (Non-Maskable Interrupt)**: This pin is used for non-maskable interrupts that cannot be disabled, which are high-priority interrupts that cannot be ignored by the processor.
15. **INTR (Interrupt Request)**: This pin is used for maskable interrupts, which can be enabled or disabled by the processor.
16. **RESET**: This pin is used to reset the processor.
17. **VCC**: These pins provide the power supply to the processor.
18. **GND**: These pins are the ground reference for the processor.
19. **CLK2**: This pin provides the clock signal for the processor.
20. **PEREQ (Processor Extension Request)**: This pin is used to indicate a request from a microprocessor.
21. **PEREQACK (Processor Extension Request Acknowledge)**: This pin is used by the processor to acknowledge a request from a microprocessor.
22. **BUSY#**: This pin is used by the microprocessor to indicate that it is busy.

23. **ERROR#**: This pin is used by the microprocessor to indicate an error.