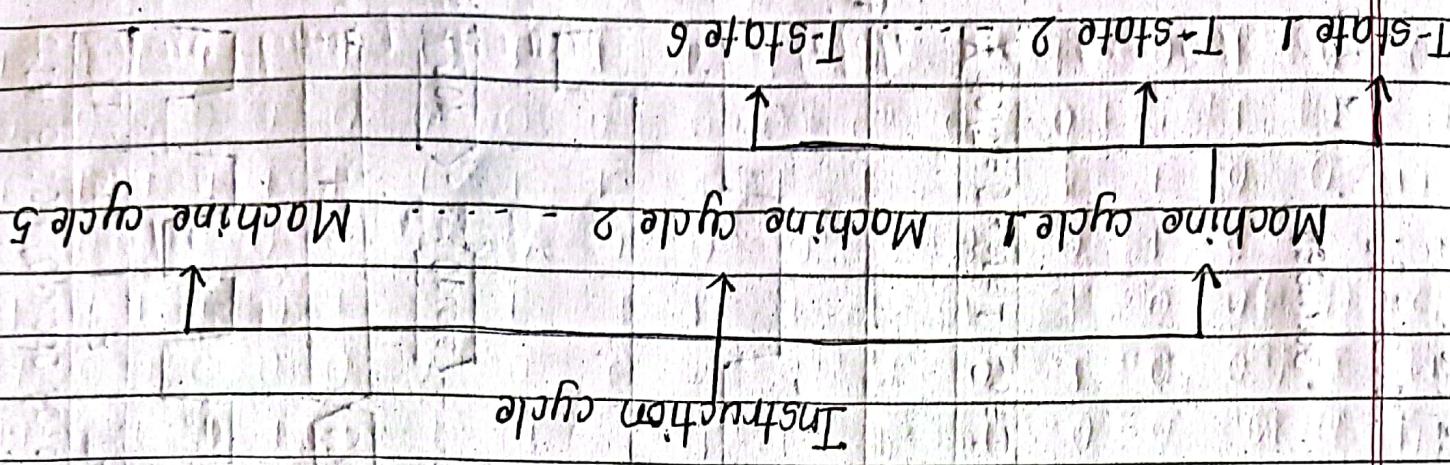


Fig. Relationship between Instruction cycle, Machine cycle & T-states



The total number of machine cycles required to execute a complete instruction is called instruction cycle.

The number of T-states required for performing a read and write operation either from memory or I/O devices is called machine cycle. It may consists of three to six T-states.

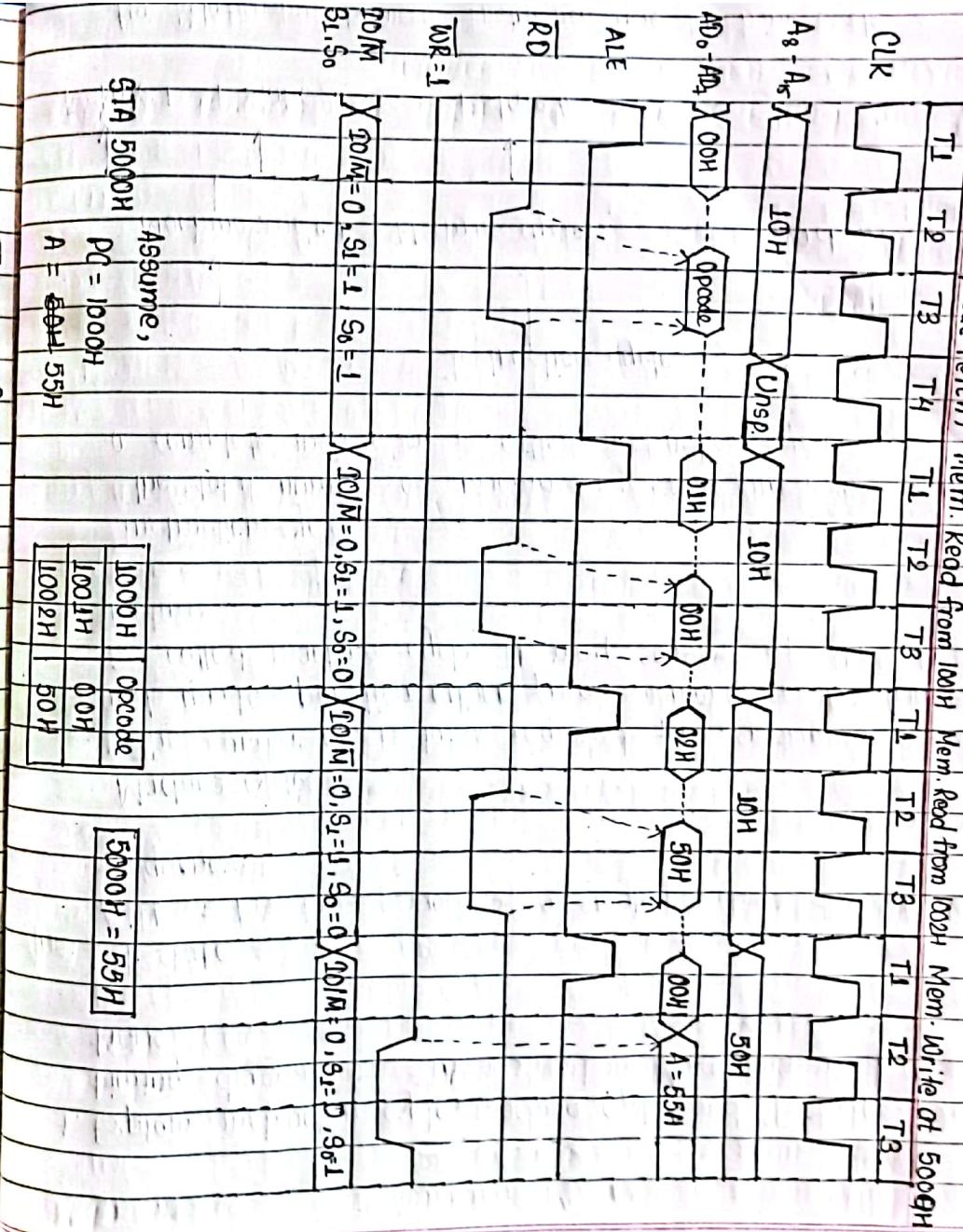
If it is the time period of a single cycle of the clock frequency

T-state

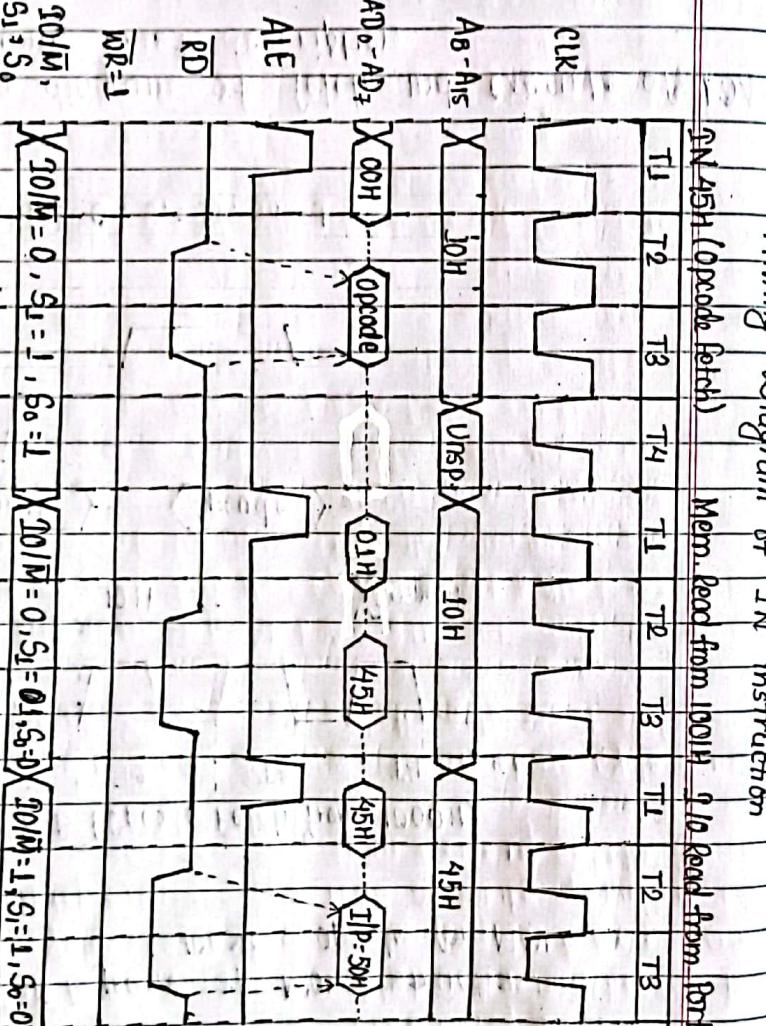
1 Explain instruction cycle, machine cycle and T-states. (Raw timing diagram of STA instruction. Make necessary assumption.)

Assignment - 4

### Timing Diagram of STA Instruction.



Timing Diagram of TN instruction  
IN 45H (Opcode Fetch) Mem. Read from 100H I/O Read from Port address 545H



Assume,  
PC = 1000H  
A = 50H

1000H = Opcode  
45H = 50H

2. Draw timing diagram of IN instruction with brief description

4. Draw timing diagram of fetch and execute of LDI instruction with brief description

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Ans: Instruction cycle is the total number of machine cycle required to execute a complete instruction.

3. What is instruction cycle? Draw timing diagram of M01

5. Differentiate between instruction cycle and machine cycle.  
Draw timing diagram of MVI A, 32H.

Ans: The difference between instruction cycle and machine cycle are:-

	Instruction cycle	Machine cycle
i.	It is the total number of machine cycles required to execute a complete instruction.	i. It is the number of T-states required for performing read or write operation either from memory or I/O devices.
ii.	One instruction cycle consists of several machine cycle.	ii. One machine cycle consists of three to six T-states.

### Timing Diagram of MVI A, 32H

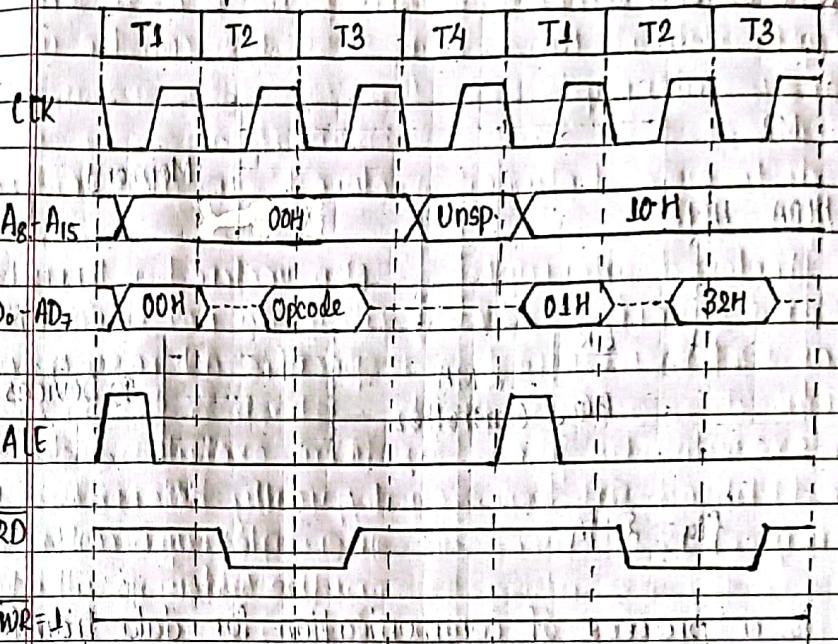
MVI A, 32H

1000H = Opcode of MVI A

Assume PC = 1000H

1001H = 32H

MVI A, 32H (Op. Fetch from 1000H) \ Mem. Read from 1001H



6. What do you mean by Isolated I/O? Explain basic DMA operation in brief.

Ans: Isolated I/O is one of the methods to perform input/output operations between the CPU and peripheral devices in the computer. It uses two separate address spaces for memory locations and for I/O devices. There are two separate address spaces for control lines for both memory

and I/O transfer.

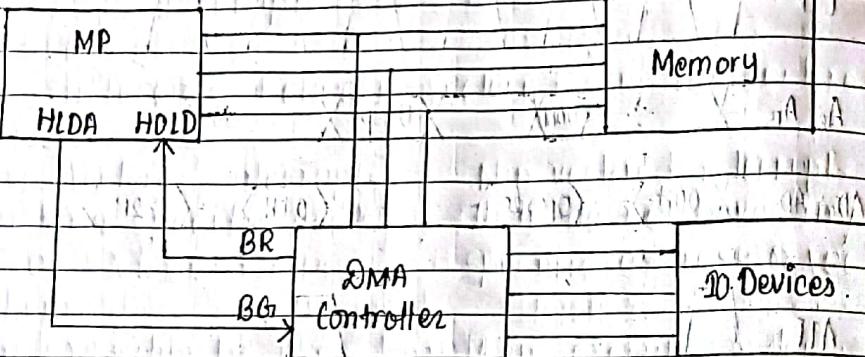


fig: DMA

DMA is a process of communication for data transfer between memory and input /output, controlled by an external circuit called DMA controller, without involvement of CPU. 8085 MP has two pins HOLD and HDLDA which are used for DMA operation. First, DMA controller sends a request by making Bus Request (BR) control line high. When MP receives high signal to HOLD pin, it first completes the execution of current machine cycle, it takes few clocks and sends HDLDA signal to the DMA controller. After receiving HDLDA through Bus Grant (BG) pin of DMA controller, the DMA controller takes control over system bus and transfer data directly between memory and I/O without involvement of CPU. During DMA operation, the processor is free to perform next job which does not need system bus. At the end of data transfer, the DMA

controller terminates the request by sending low signal to HOLD pin and MP regains control of system bus by making HDLDA low.

7. Differentiate between interrupt based I/O and DMA based I/O.

Ans. The difference between interrupt based I/O and DMA based I/O are :-

- | DMA based I/O   | Interrupt based I/O   |
|---|---|
| i) In DMA based I/O, a specialized DMA controller takes over control of the system bus and handles the data transfer independently. | i) In interrupt-driven I/O, the CPU remains in control and handles interrupt processing.              |
| ii) DMA offloads data transfer tasks from the CPU entirely.   | ii) Interrupt-based I/O requires CPU involvement for initiating and handling data transfer.           |
| iii) DMA is more suitable for large, continuous data transfers.   | iii) It is suitable for small, occasional data transfers or devices that require immediate attention. |

8. Differentiate between vectored and non-vectored interrupts. Where and how 8259 PIC can be used to handle interrupts?

Ans: The difference between vectored and non-vectored interrupts are:

Vectored interrupts

Non-vectored interrupts.

i) They have specific address or vectors assigned to them.

ii) They do not have any specific address or vectors assigned to them.

Their execution is pre-defined based on their priority. Their execution order is typically determined by the interrupt controller based on the order in which they occur.

The vectored interrupt.

iii) When a non-vectored interrupt is received, it jumps into the program counter to carry out in software.

iv) Its handling time is faster and more efficient in handling due to iteration.

v) It requires complex hardware and software mechanisms.

Ans: An interrupt which can be disabled by software that means we can disable the interrupt by sending an appropriate instruction is called a maskable interrupt. Interrupt masking is important for controlling the timing and order of the interrupt requests in microprocessor.

9. What is the significance of interrupt masking?

Ans: An interrupt which can be disabled by software that means we can disable the interrupt by sending an appropriate instruction is called a maskable interrupt. Interrupt masking is important for controlling the timing and order of the interrupt requests in microprocessor.

10. Write short note on:

a) DMA

DMA is a process of communication for data transfer between memory and input/output, controlled by an external circuit, called DMA controller, without involvement of CPU. It is a hardware controlled I/O Transfer technique. It is mainly used for high

speed data transfer between I/O and Memory. A device known as the DMA controller (DMAc) is responsible for the DMA transfer. They are used in different areas like cinemas, theatres, hotels, railway stations, museums and many more.

by Interrupts.

Interrupt is a signal send by an external device informing the processor that it is ready for communication and requests attention to perform a particular task. It is useful to interface I/O device that provide or require data. When the microprocessor receives an interrupt signal, it suspends the currently executing program and jumps to an Interrupt Service Routine (ISR) to respond to the incoming interrupt. Each interrupt has its own ISR. In 8085 up, there are 5 interrupts such as TRAP, RST 5.5, RST 6.5, RST 7.5, INT.

c) Interrupt Masking.

An interrupt which can be disabled by software that means we can disable the interrupt by sending appropriate instruction is called a maskable interrupt. The maskable interrupt is processed immediately if the interrupt occurred has higher priority than currently executing instruction. Else the interrupt is processed after completing the current execution. RST 7.5, RST 6.5 and RST 5.5 are the examples of Maskable interrupt.