# [EEC-204] B.Tech. Degree Examination

# ECE & EEE IV SEMESTER

#### LINEAR INTEGRATED CIRCUITS

(Effective from the admitted batch 2015–16 onwards)

Ti	me:	3 Hours	Max.Marks:	Max.Marks: 60		
Instructions:			Each Unit carries 12 marks.  Answer all units choosing one question from each unit.  All parts of the unit must be answered in one place only.  Figures in the right hand margin indicate marks allotted.			
			MODULE-I			
1.	a) b)	with th	n the effect of output offset voltage on operational Amplifier e expression n all the DC-characteristics of an Op-Amp briefly	6 6		
			OR			
2.	a) b)	Slew ra	Slew rate and explain how it affects sine waves ate of an Op-Amp is 0.9V/µsec. At what maximum acy the undistorted sinusoidal output voltage is 10V peak	6		
			MODULE-II			
3.	a) b)	of peak	a Positive peak detector circuit and explain the operation detector in the Trans resistance amplifier in detail	6		
			OR			
4.	a)	Explair sketch	n the operation of Instrumentation Amplifier with neat	6		

b)	For the given Non inverting Op-Amp let R1=5k $\Omega$ , Rf=20 k $\Omega$ and Vi=1V.A. load Resistance R <sub>L</sub> =5k $\Omega$ is connected at the output. Calculate (i) Output Voltage (Vo) (ii) Closed loop gain (Acl) (iii) Load Current (I <sub>L</sub> )	6
Ţ	Vi O+	
	MODULE-III	
a)	Describe the functional diagram of 555 timer in detail	6

### 5. b) Explain the astable operation of 555 6 OR a) Explain about fixed voltage regulators 6 b) What is Duty Cycle? Calculate duty cycle for RA= $6.8k\Omega$ , $RB=3.3k\Omega$ 6 **MODULE-IV** 7. a) Sketch the circuit of second order active high pass filter and explain its working 6 b) Explain the operation of Wide band pass filter with a neat diagram 6 OR 8. a) Design a wide band reject filter having $f_h=400$ Hz and $f_l=2$ KHz having pass band gain as 2 6 b) Write short notes on switched capacitor filter 6

## **MODULE-V**

9.	a)	Explain ADC/DAC specifications in detail	6	
	b)	Sketch the diagram and explain the operation of Successive		
		approximation type ADC	6	
		OR		
10.	a)	Explain the operation of parallel comparator	6	
	b)	Design R-2R ladder Digital to Analog converter. Explain its		
		operation	6	

[4,5/IV S/118]