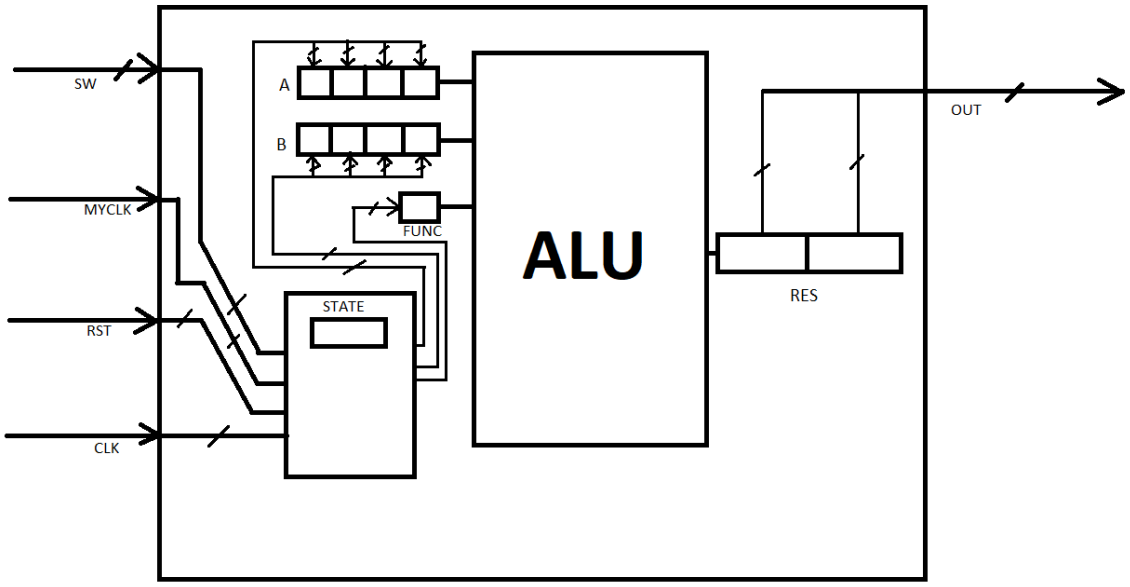
VERILOG ASSIGNMENT 7 – PROBLEM 1

SEMESTER 5

GROUP 47

ANIT MANGAL, OMAIR ALAM

TOP LEVEL



INPUT

SW: 8-bit bus, nibble input for function selection, bytewise input for 32-bit instruction

RST: flag wire, resets process to take new instruction

CLK: standard clock

MYCLK: flag wire, signals when input byte applies to a separate part of the 32-bit instruction

OUTPUT

OUT: 16-bit bus, displays the answer double as two words that are printed one at a time

REGISTERS AND WIRES

A: 32-bit register, stores the first four input bytes as first operand of the ALU

B: 32-bit register, stores the last four input bytes as second operand of the ALU

FUNC: 4-bit register, stores the first nibble as function for operation of ALU

STATE: 5-bit register, keeps track of state machine for taking inputs in parts

COUNTER: 26-bit register, used as a helper register to implement CLKSLOW

CLKSLOW: wire, acts as slow clock (2^26 clock cycles are one CLKSLOW cycle)

RES: 32-bit bus, acts as output port for ALU

ZERO: wire, acts as output port for ALU

SIGN: wire, acts as output port for ALU

CARRY: wire, acts as output port for ALU

OPERATION

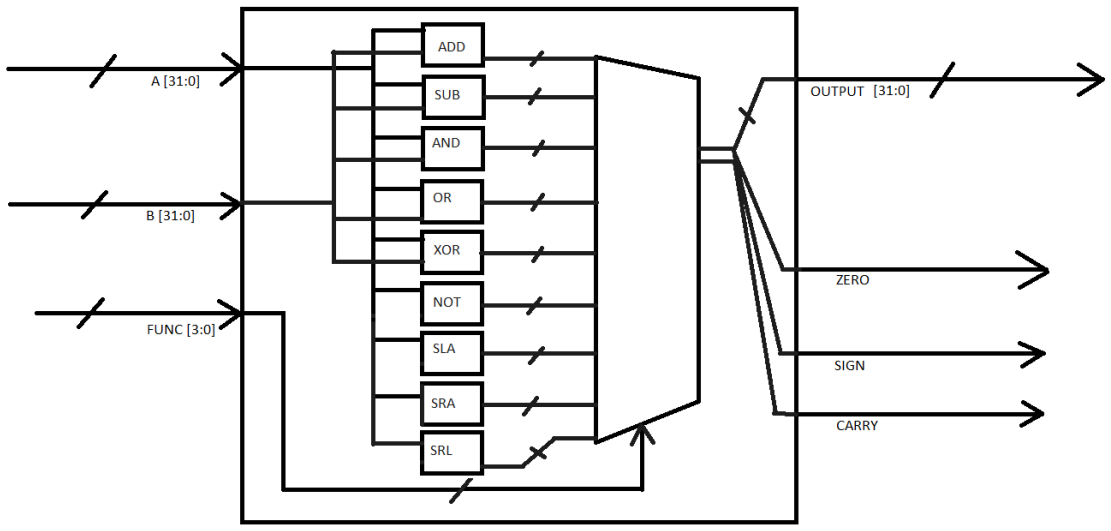
The module initially sets A, B, FUNC, COUNTER to 0, STATE to -1, OUT to 1.

COUNTER in incremented clock cycle. CLKSLOW is assigned to most significant bit of COUNTER to only give a posedge signal every 2^26 standard cycles. CLKSLOW acts as clock for all output and monitoring of operations.

While MYCLK is enabled, STATE increments every CLKSLOW cycle and accepts input from the switches. These inputs in parts are concatenated to form the operands. While MYCLK is disabled, the state machine pauses at the present state.

Once FUNC has a value and the operands are passed, the ALU returns a value to OUT which is displayed in parts.

ALU



INPUT

A: 32-bit bus, operand

B: 32-bit bus, operand

FUNC: 4-bit bus, function selector for MUX

OUTPUT

OUTPUT: 32 but bus, final result

ZERO: flag wire, set when result is 0

SIGN: flag wire, set when result is negative

(CARRY) OVER: flag wire, set when addition/subtraction results in overflow

Operation

A and B are passed in parallel to the different arithmetic and logical operation units, and the respective results are passed to a MUX. FUNC acts as the select line and chooses which of the different outputs to pass forward