Computer Organization and Architecture Laboratory

Assignment - 7

Problem 2 - Control Unit and Data Path Specifications

Group 47

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INSTRUCTIONS

R TYPE

OPCODE	rs	rt	rd	Don't care	function
4 bits	5 bits	5 bits	5 bits	8 bits	5 bits

instruction	opcode	function
ADD	0000	00000
SUB	0000	00001
AND	0000	00010
OR	0000	00011
XOR	0000	00100
NOT	0000	00101
SLA	0000	00110
SRA	0000	00111
SRL	0000	01000
MOVE	1101	xxxxxx
PUSH	1001	xxxxxx
POP	1010	xxxxxx

I TYPE - ALU

opcode	rs	immediate	func
4 bits	5 bits	18 bits	5 bits

instruction	opcode	function
ADDI	0000	01001
SUBI	0000	01010
ANDI	0000	01011
ORI	0000	01100
XORI	0000	01101
NOTI	0000	01110
SLAI	0000	01111
SRAI	0000	10000
SRLI	0000	10001

I TYPE – 18

opcode	rs	immediate	rd
4 bits	5 bits	18 bits	5 bits

instruction	opcode	function
BMI	0110	xxxxx
BPL	0111	xxxxx
BZ	1000	xxxxx
LD	0001	xxxxx
ST	0010	xxxxx
LDSP	0011	xxxxx
STSP	0100	xxxxx

J TYPE

opcode	immediate
4 bits	28 bits

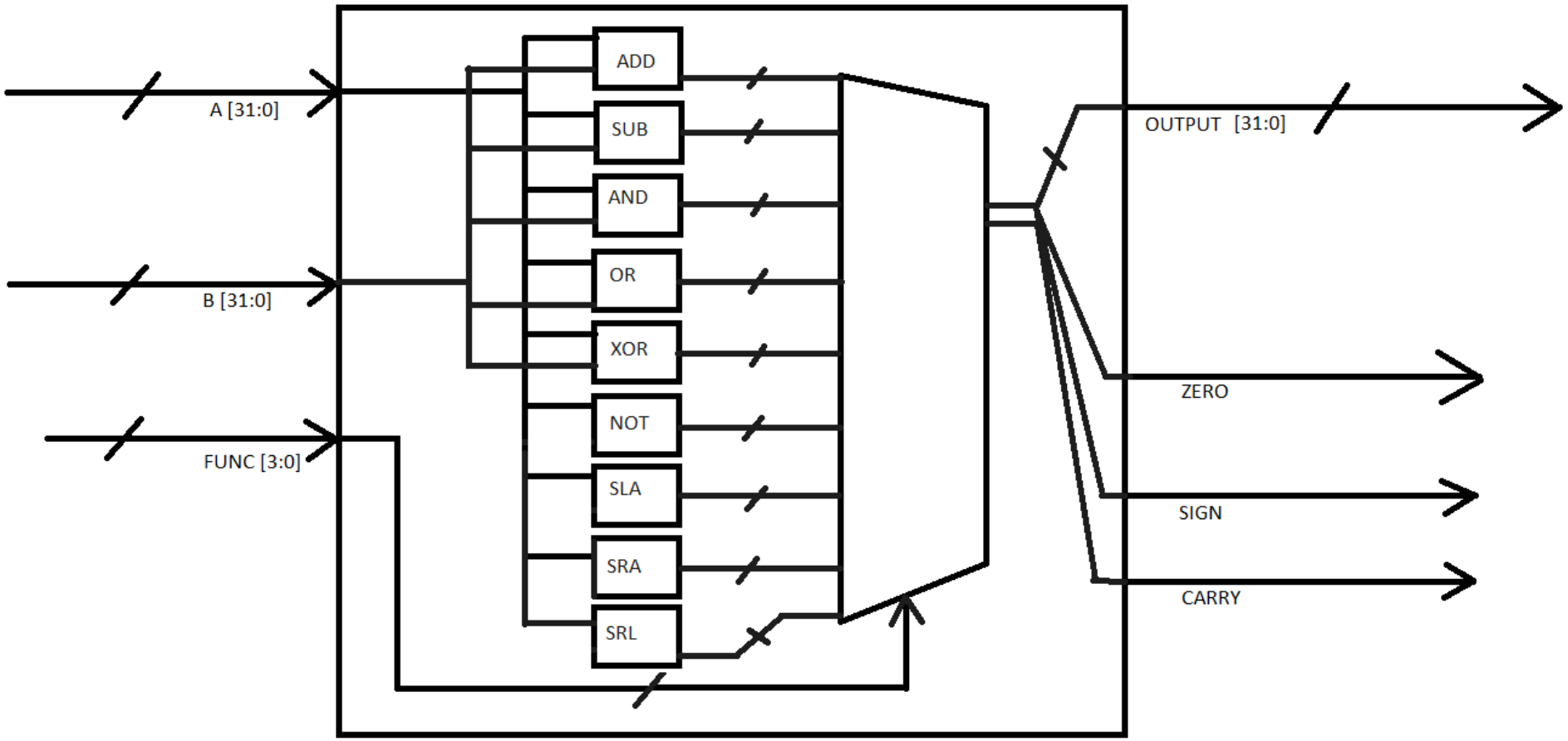
instruction	opcode	function
BR	101	xxxxx
CALL	1011	xxxxx

NO-FIELD TYPE

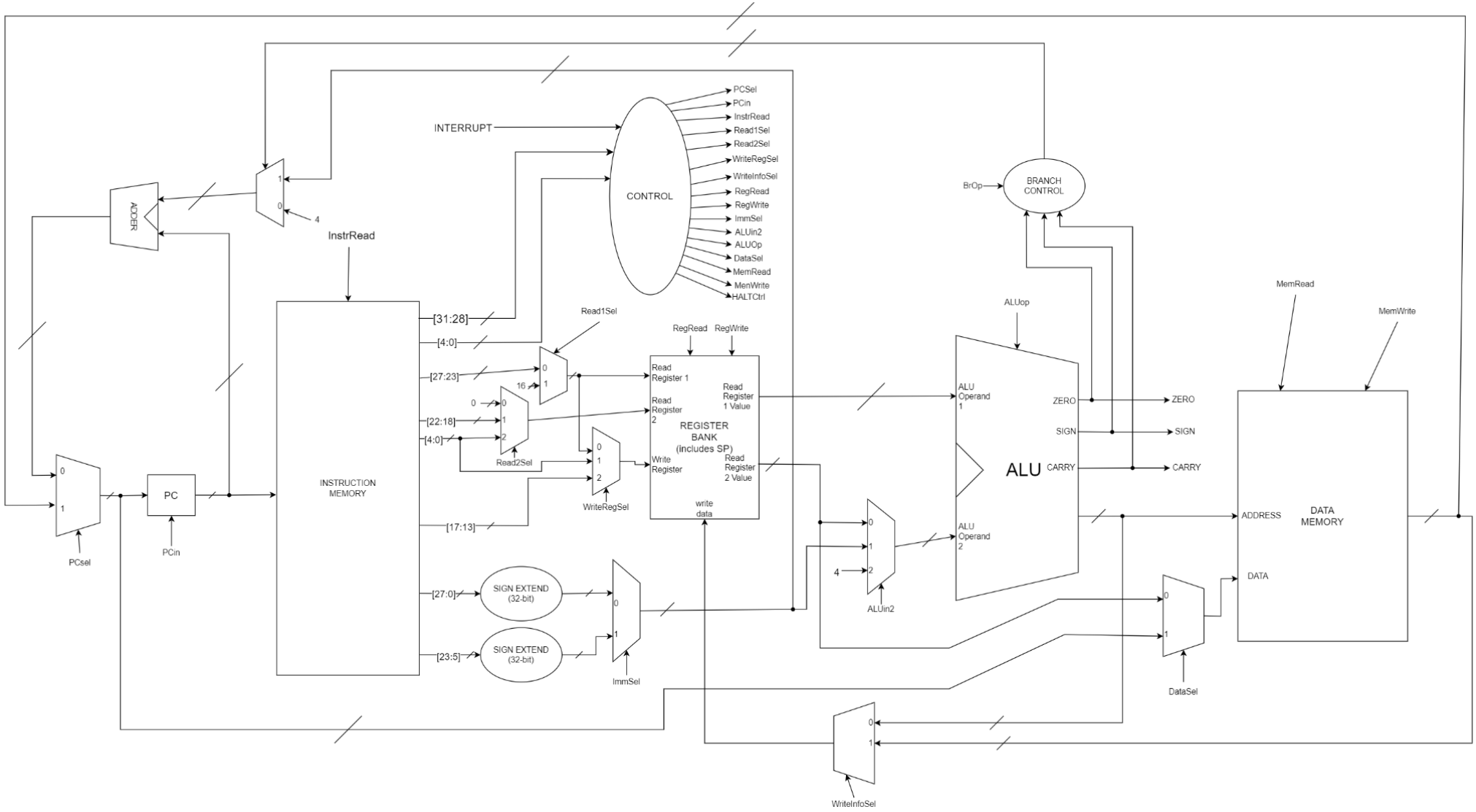
opcode	Don’t care
4 bits	28 bits

instruction	opcode	function
RET	1100	xxxxx
HALT	1110	xxxxx
NOP	1111	xxxxx

ALU


A [31:0]
B [31:0]
FUNC [3:0]
ADD
SUB
AND
OR
XOR
NOT
SLA
SRA
SRL
OUTPUT [31:0]
ZERO
SIGN
CARRY

DATA DESIGN


INTERRUPT
CONTROL
PCSel
PCin
InstrRead
Read1Sel
Read2Sel
WriteRegSel
WriteInfoSel
RegRead
RegWrite
ImmSel
ALUin2
ALUOp
DataSel
MemRead
MemWrite
HALTCtrl
ADDER
1
0
4
InstrRead
BrOp
BRANCH CONTROL
ALUop
MemRead
MemWrite
[31:28]
[4:0]
[27:23]
[22:18]
[4:0]
[17:13]
Read1Sel
RegRead
RegWrite
Read Register 1
Read Register 2
Write Register
write data
Read Register 1 Value
Read Register 2 Value
REGISTER BANK (includes SP)
16
0
Read2Sel
WriteRegSel
INSTRUCTION MEMORY
PC
PCsel
PCin
[27:0]
[23:5]
SIGN EXTEND (32-bit)
SIGN EXTEND (32-bit)
ImmSel
4
ALUin2
ALU Operand 1
ALU Operand 2
ALU
ZERO
SIGN
CARRY
ZERO
SIGN
CARRY
ADDRESS
DATA
DATA MEMORY
DataSel
WriteInfoSel

CONTROLS

SNO	opcode	function	ACTION	PC Sel	PCin	Instr Read	Read 1Sel	Read2 Sel	WriteRegSel	WriteInfoSel	Reg Read	Reg Write	Imm Sel	ALUin 2	ALUOp	BrOp	Data Sel	Mem Read	Mem Write	HALT Ctrl
1	0000	00000	ADD	0	1	1	0	1	2	0	1	1	x	0	00000	0	x	x	x	x
2	0000	00001	SUB	0	1	1	0	1	2	0	1	1	x	0	00001	0	x	x	x	x
3	0000	00010	AND	0	1	1	0	1	2	0	1	1	x	0	00010	0	x	x	x	x
4	0000	00011	OR	0	1	1	0	1	2	0	1	1	x	0	00011	0	x	x	x	x
5	0000	00100	XOR	0	1	1	0	1	2	0	1	1	x	0	00100	0	x	x	x	x
6	0000	00101	NOT	0	1	1	0	1	2	0	1	1	x	0	00101	0	x	x	x	x
7	0000	00110	SLA	0	1	1	0	1	2	0	1	1	x	0	00110	0	x	x	x	x
8	0000	00111	SRA	0	1	1	0	1	2	0	1	1	x	0	00111	0	x	x	x	x
9	0000	01000	SRL	0	1	1	0	1	2	0	1	1	x	0	01000	0	x	x	x	x
10	0000	01001	ADDI	0	1	1	0	x	1	0	1	1	1	1	00000	0	x	x	x	x
11	0000	01010	SUBI	0	1	1	0	x	1	0	1	1	1	1	00001	0	x	x	x	x
12	0000	01011	ANDI	0	1	1	0	x	1	0	1	1	1	1	00010	0	x	x	x	x
13	0000	01100	ORI	0	1	1	0	x	1	0	1	1	1	1	00011	0	x	x	x	x
14	0000	01101	XORI	0	1	1	0	x	1	0	1	1	1	1	00100	0	x	x	x	x
15	0000	01110	NOTI	0	1	1	0	x	1	0	1	1	1	1	00101	0	x	x	x	x
16	0000	01111	SLAI	0	1	1	0	x	1	0	1	1	1	1	00110	0	x	x	x	x
17	0000	10000	SRAI	0	1	1	0	x	1	0	1	1	1	1	00111	0	x	x	x	x
18	0000	10001	SRLI	0	1	1	0	x	1	0	1	1	1	1	01000	0	x	x	x	x
19	0001	XXXXX	LD	0	1	1	0	x	1	1	1	1	1	1	00000	0	x	1	0	x
20	0010	XXXXX	ST	0	1	1	0	2	x	x	1	0	1	1	00000	0	0	0	1	x
21	0011	XXXXX	LDSP	0	1	1	0	x	1	1	1	1	1	1	00000	0	x	1	0	x
22	0100	XXXXX	STSP	0	1	1	1	2	x	x	1	0	1	1	00000	0	0	0	1	x
23	0101	XXXXX	BR	0	1	1	x	x	x	x	0	0	0	x	11111	1	x	0	0	x
24	0110	XXXXX	BMI	0	1	1	0	0	x	x	1	0	1	0	00001	1	x	0	0	x
25	0111	XXXXX	BPL	0	1	1	0	0	x	x	1	0	1	0	00000	1	x	0	0	x
26	1000	XXXXX	BZ	0	1	1	0	0	x	x	1	0	1	0	00100	1	x	0	0	x
27	1001	XXXXX	PUSH	0	1	1	1	1	x	x	1	0	x	2	00001	0	0	0	1	x
28	1010	XXXXX	POP	0	1	1	1	0	2	1	1	1	x	0/2	00000	0	x	1	0	x
29	1011	XXXXX	CALL	0	0/1	1	1	x	0	0	1	2	0	2	00000	0/1	1	0	1	x
30	1100	XXXXX	RET	1/0	1	1	1	0	0	0	1	1	x	0/2	00000	x	x	1	0	x

31	1101	XXXXX	MOVE	0	1	1	0	0	2	0	1	1	x	0	00000	0	x	x	x	x
32	1110	XXXXX	HALT	x	0	1	x	x	x	x	0	0	x	x	xxxxx	x	x	0	0	1
33	1111	XXXXX	NOP	0	1	1	x	x	x	x	0	0	x	x	xxxxx	0	x	0	0	x

PCSel - Controls whether value to be passed as PC is taken from {0}incrementing/decrementing current PC value or {1}a value from memory

PCin- Controls whether adjusted PC value is {1}passed to PC register or {0}not (disabled during steps in CALL)

InstrRead - Controls whether {1}pointed instruction is read or {0}not

Read1Sel - Controls Read Register 1, can either be {0}0-15 from first register operand, or {1}16 (for SP)

Read2Sel - Controls Read Register 2, can either be {0}constant 0, or 0-15 from second register operand {1}in bits [22:18] or {2}in bits [4:0]

WriteRegSel - Controls Write Register, can either be {0}a copy of Read Register 1, {1}1-15 from second register operand, or {2}1-15 from third register operand

WriteInfoSel - Controls Write Register's value, chooses between {0}ALU operation result or {1}data read from memory

RegRead - Controls whether to {1}allow Reading of Registers or {0}not

RegWrite - Controls whether to {1}allow Writing of Registers or {0}not

ImmSel - Controls which immediate value is selected ({0}28-bit or {1}18-bit)

ALUin2 - Controls whether ALU Operand 2 is {1}Read Register 2's value, {1}immediate value, or {2}constant 4

ALUOp - Chooses among different ALU operations ({0000}Addition, {00001}Subtraction, {00010}AND, {00011}OR, {00100}XOR, {00101}NOT, {00110}Left Arithmetic Shift, {00111}Right Arithmetic Shift, {01000}Right Logical Shift or {11111}Nothing in order)

BrOp - Chooses between reading flags to {1}set PC Adder Operand 2 as a controlled value, or to {0}set PC Adder Operand 2 as a constant 4

DataSel - Chooses between {0}Read Register 2's value, or {1}adjusted PC value

MemRead - Controls whether to {1}allow Reading of Data Memory or {0}not

MemWrite - Controls whether to {1}allow Writing to Data Memory or {0}not

HALTCtrl - Controls whether to {1}halt execution or {0}let it resume

ASSUMPTION

Instruction Memory is defined as separate from Data Memory

Instruction Memory module output is a register which can pass sliced outputs to different modules and the control unit

SP is included in the register bank as register number 16 (b10000)

Jump Control acts as a separate control unit for PC increment/decrement to choose whether to increment PC normally or to increment/decrement on the basis of an instruction

ALU output is a register within the ALU toplevel

ALUop = b11111 signifies no ALU operation

SLOW-CLOCK MODULE generates slowclock from system clock

HALT results in slowclock getting paused, slowclock can be resumed with INTERRUPT