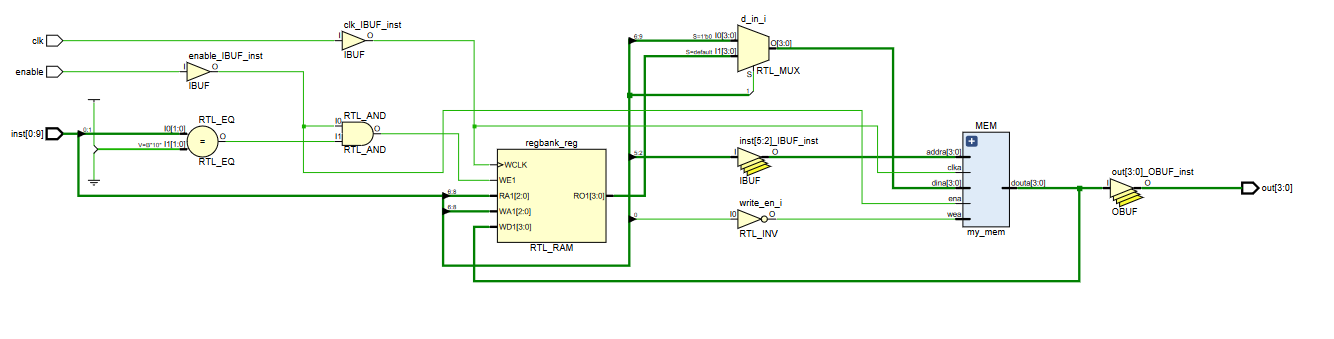
**Verilog Assignment - 6**

Group – 47

Anit Mangal

Omair Alam



**TOP LEVEL MODULE**

    /\*

    10-bit instruction: 2-bit opcode, 4-bit memory location, 4-bit data/3-bit register address. Leftover bits are don’t care bits

    00  \_ \_ \_ \_   \_ \_ \_ \_ (mem <- data)

    01  \_ \_ \_ \_   \_ \_ \_ (mem <- reg)

    10  \_ \_ \_ \_   \_ \_ \_ (mem -> reg)

    11  \_ \_ \_ \_ (display mem)

    \*/