# #50DAYS CHALLENGE

**DAY 7**

## A)MUX 4:1

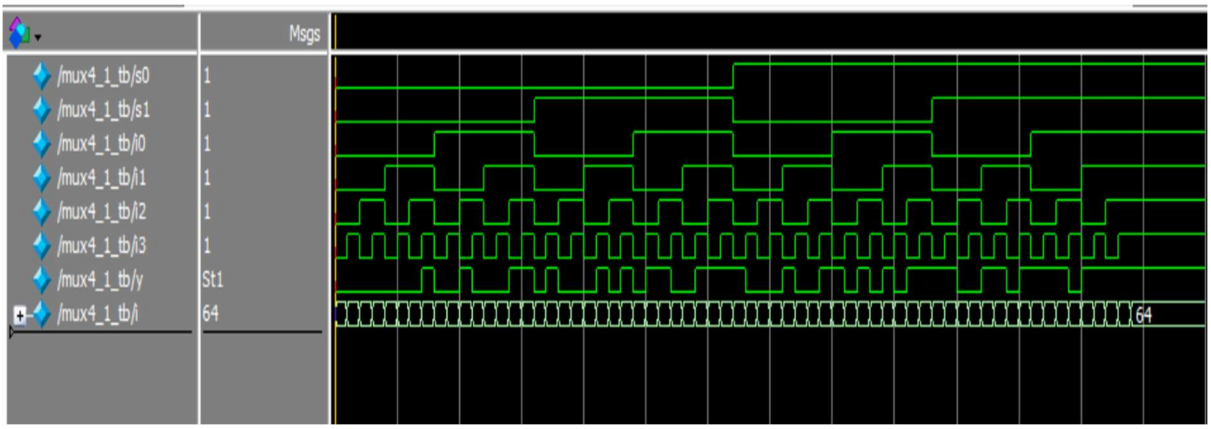
a)Design Code

```
module mux4_1(i0,i1,i2,i3,s0,s1,y);
input i0,i1,i2,i3,s0,s1;
output reg y;

always@(*)
begin
if(~s0&~s1)
y=i0;
else if(~s0&s1)
y=i1;
else if(s0&~s1)
y=i2;
else
y=i3;
end
endmodule
```

b)Testbench

```
module mux4_1_tb();
reg s0,s1,i0,i1,i2,i3;
wire y;
integer i;
mux4_1 dut(s0,s1,i0,i1,i2,i3,y);
initial
begin
{s0,s1}=2'b00;
{i0,i1,i2,i3}=4'b0000;
end
initial
begin
for(i=0;i<64;i=i+1)
begin
{s0,s1,i0,i1,i2,i3}=i;
#10;
end
end
initial
$monitor("input s0=%b s1=%b i0=%b i1=%b i2=%b i3=%b and output y=%b",s0,s1,i0,i1,i2,i3,y);
initial
#700 $finish();
endmodule
```

c)Waveform




d)Console Output

```
# input s0=0 s1=0 i0=0 i1=0 i2=0 i3=0 and output y=0
# input s0=0 s1=0 i0=0 i1=0 i2=0 i3=1 and output y=0
# input s0=0 s1=0 i0=0 i1=0 i2=1 i3=0 and output y=0
# input s0=0 s1=0 i0=0 i1=0 i2=1 i3=1 and output y=0
# input s0=0 s1=0 i0=0 i1=1 i2=0 i3=0 and output y=0
# input s0=0 s1=0 i0=0 i1=1 i2=0 i3=1 and output y=0
# input s0=0 s1=0 i0=0 i1=1 i2=1 i3=0 and output y=0
# input s0=0 s1=0 i0=0 i1=1 i2=1 i3=1 and output y=1
# input s0=0 s1=0 i0=1 i1=0 i2=0 i3=0 and output y=0
# input s0=0 s1=0 i0=1 i1=0 i2=0 i3=1 and output y=0
# input s0=0 s1=0 i0=1 i1=0 i2=1 i3=0 and output y=1
# input s0=0 s1=0 i0=1 i1=0 i2=1 i3=1 and output y=0
# input s0=0 s1=0 i0=1 i1=1 i2=0 i3=0 and output y=0
# input s0=0 s1=0 i0=1 i1=1 i2=0 i3=1 and output y=0
# input s0=0 s1=0 i0=1 i1=1 i2=1 i3=0 and output y=1
# input s0=0 s1=0 i0=1 i1=1 i2=1 i3=1 and output y=1
# input s0=0 s1=1 i0=0 i1=0 i2=0 i3=0 and output y=0
# input s0=0 s1=1 i0=0 i1=0 i2=0 i3=1 and output y=1
# input s0=0 s1=1 i0=0 i1=0 i2=1 i3=0 and output y=0
# input s0=0 s1=1 i0=0 i1=0 i2=1 i3=1 and output y=0
# input s0=0 s1=1 i0=0 i1=1 i2=0 i3=0 and output y=0
# input s0=0 s1=1 i0=0 i1=1 i2=0 i3=1 and output y=1
# input s0=0 s1=1 i0=0 i1=1 i2=1 i3=0 and output y=0
# input s0=0 s1=1 i0=0 i1=1 i2=1 i3=1 and output y=1
# input s0=0 s1=1 i0=1 i1=0 i2=0 i3=0 and output y=0
# input s0=0 s1=1 i0=1 i1=0 i2=0 i3=1 and output y=1
# input s0=0 s1=1 i0=1 i1=0 i2=1 i3=0 and output y=1
# input s0=0 s1=1 i0=1 i1=0 i2=1 i3=1 and output y=0
# input s0=0 s1=1 i0=1 i1=1 i2=0 i3=0 and output y=0
# input s0=0 s1=1 i0=1 i1=1 i2=0 i3=1 and output y=1
# input s0=0 s1=1 i0=1 i1=1 i2=1 i3=0 and output y=1
# input s0=0 s1=1 i0=1 i1=1 i2=1 i3=1 and output y=1
# input s0=1 s1=0 i0=0 i1=0 i2=0 i3=0 and output y=0
# input s0=1 s1=0 i0=0 i1=0 i2=0 i3=1 and output y=0
# input s0=1 s1=0 i0=0 i1=0 i2=1 i3=0 and output y=0
# input s0=1 s1=0 i0=0 i1=0 i2=1 i3=1 and output y=0
# input s0=1 s1=0 i0=0 i1=1 i2=0 i3=0 and output y=0
# input s0=1 s1=0 i0=0 i1=1 i2=0 i3=1 and output y=1
# input s0=1 s1=0 i0=0 i1=1 i2=1 i3=0 and output y=0
# input s0=1 s1=0 i0=0 i1=1 i2=1 i3=1 and output y=0
# input s0=1 s1=0 i0=1 i1=0 i2=0 i3=0 and output y=0
# input s0=1 s1=0 i0=1 i1=0 i2=0 i3=1 and output y=0
# input s0=1 s1=0 i0=1 i1=0 i2=1 i3=0 and output y=0
# input s0=1 s1=0 i0=1 i1=0 i2=1 i3=1 and output y=0
# input s0=1 s1=0 i0=1 i1=1 i2=0 i3=0 and output y=0
# input s0=1 s1=0 i0=1 i1=1 i2=0 i3=1 and output y=0
# input s0=1 s1=0 i0=1 i1=1 i2=1 i3=0 and output y=0
# input s0=1 s1=0 i0=1 i1=1 i2=1 i3=1 and output y=0
# input s0=1 s1=1 i0=0 i1=0 i2=0 i3=0 and output y=0
# input s0=1 s1=1 i0=0 i1=0 i2=0 i3=1 and output y=0
# input s0=1 s1=1 i0=0 i1=0 i2=1 i3=0 and output y=0
# input s0=1 s1=1 i0=0 i1=0 i2=1 i3=1 and output y=0
# input s0=1 s1=1 i0=0 i1=1 i2=0 i3=0 and output y=0
# input s0=1 s1=1 i0=0 i1=1 i2=0 i3=1 and output y=0
# input s0=1 s1=1 i0=0 i1=1 i2=1 i3=0 and output y=0
# input s0=1 s1=1 i0=0 i1=1 i2=1 i3=1 and output y=0
# input s0=1 s1=1 i0=1 i1=0 i2=0 i3=0 and output y=0
# input s0=1 s1=1 i0=1 i1=0 i2=0 i3=1 and output y=0
# input s0=1 s1=1 i0=1 i1=0 i2=1 i3=0 and output y=0
# input s0=1 s1=1 i0=1 i1=0 i2=1 i3=1 and output y=0
# input s0=1 s1=1 i0=1 i1=1 i2=0 i3=0 and output y=0
# input s0=1 s1=1 i0=1 i1=1 i2=0 i3=1 and output y=0
# input s0=1 s1=1 i0=1 i1=1 i2=1 i3=0 and output y=0
# input s0=1 s1=1 i0=1 i1=1 i2=1 i3=1 and output y=0
```

## B)MUX8_1

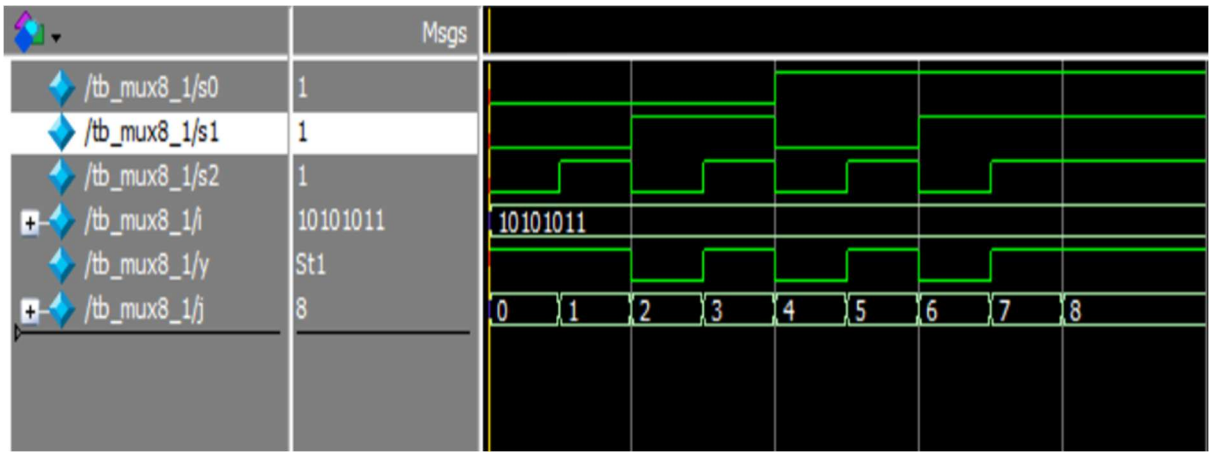
a)Design Code

```
module mux8_1(s0,s1,s2,i, y);
input  [7:0]i;
input  s0,s1,s2;
output reg y;

always@(*)
begin
case({s0,s1,s2})
3'b000:y=i[0];
3'b001:y=i[1];
3'b010:y=i[2];
3'b011:y=i[3];
3'b100:y=i[4];
3'b101:y=i[5];
3'b110:y=i[6];
3'b111:y=i[7];
default: y = 1'b0;
endcase
end
endmodule
```

b)Testbench

```
module tb_mux8_1();
reg s0,s1,s2;
reg [7:0]i;
wire y;
integer j;

mux8_1 dut(.s0(s0),.s1(s1),.s2(s2),.i(i),.y(y));

initial
begin
i=8'b010101011;

for(j=0;j<8;j=j+1)
begin
{s0,s1,s2}=j;
#10;
end

end

initial begin
        $monitor("Time=%0t | s0=%b s1=%b s3=%b | y=%b",
                  $time, s0, s1, s2, y);
#100;
$finish;
    end

endmodule
```

c)Waveform




d)Console Output

```
# Time=0  | s0=0 s1=0 s3=0 | y=1
# Time=10 | s0=0 s1=0 s3=1 | y=1
# Time=20 | s0=0 s1=1 s3=0 | y=0
# Time=30 | s0=0 s1=1 s3=1 | y=1
# Time=40 | s0=1 s1=0 s3=0 | y=0
# Time=50 | s0=1 s1=0 s3=1 | y=1
# Time=60 | s0=1 s1=1 s3=0 | y=0
# Time=70 | s0=1 s1=1 s3=1 | y=1
```

## RECONFIGURABLE MUX

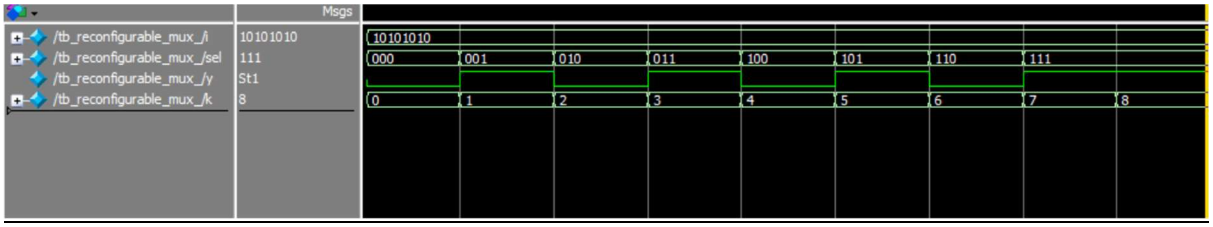
a)Design Code

```
module reconfigurable_mux #(parameter N = 8 ) (
          input [N-1:0] i,
          input [$clog2(N)-1:0] sel,
          output reg y);

always @(*) begin
     y = i[sel];
end
endmodule
```

b)Testbench

```
`timescale 1ns/1ps
module tb_reconfigurable_mux_();
    parameter N = 8;
        reg [N-1:0] i;
    reg [$clog2(N)-1:0] sel;
    wire y;
    reconfigurable_mux_ #(N) dut (
        .i(i),
        .sel(sel),
        .y(y)
    );
    integer k;
initial begin
    i = 8'b10101010;
    sel = 0;
    for (k = 0; k < N; k = k + 1) begin
        sel = k;
        #10;
    end

    #10;
    $finish;
end
    initial begin
        $monitor("Time=%0t | sel=%0d | y=%b", $time, sel, y);
    end
endmodule
```

c)Waveform




d)Console Output

```
# Time=0 | sel=0 | y=0
# Time=10000 | sel=1 | y=1
# Time=20000 | sel=2 | y=0
# Time=30000 | sel=3 | y=1
# Time=40000 | sel=4 | y=0
# Time=50000 | sel=5 | y=1
# Time=60000 | sel=6 | y=0
# Time=70000 | sel=7 | y=1
```