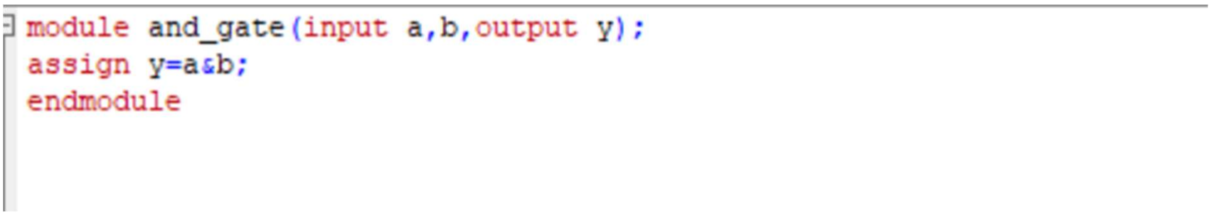
#50DAYS CHALLENGE

DAY 1

AND GATE

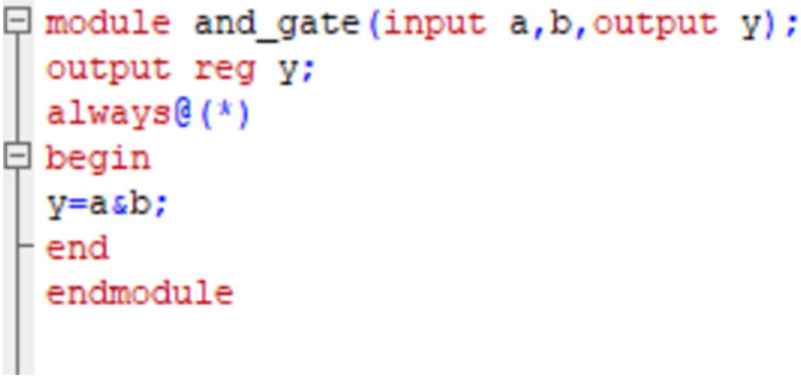
a) Design Code

Data Flow Modelling



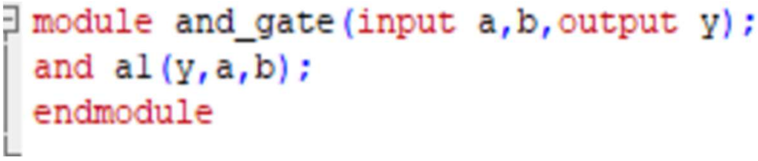
```
module and_gate(input a,b,output y);
assign y=a&b;
endmodule
```

Behavioral Modelling



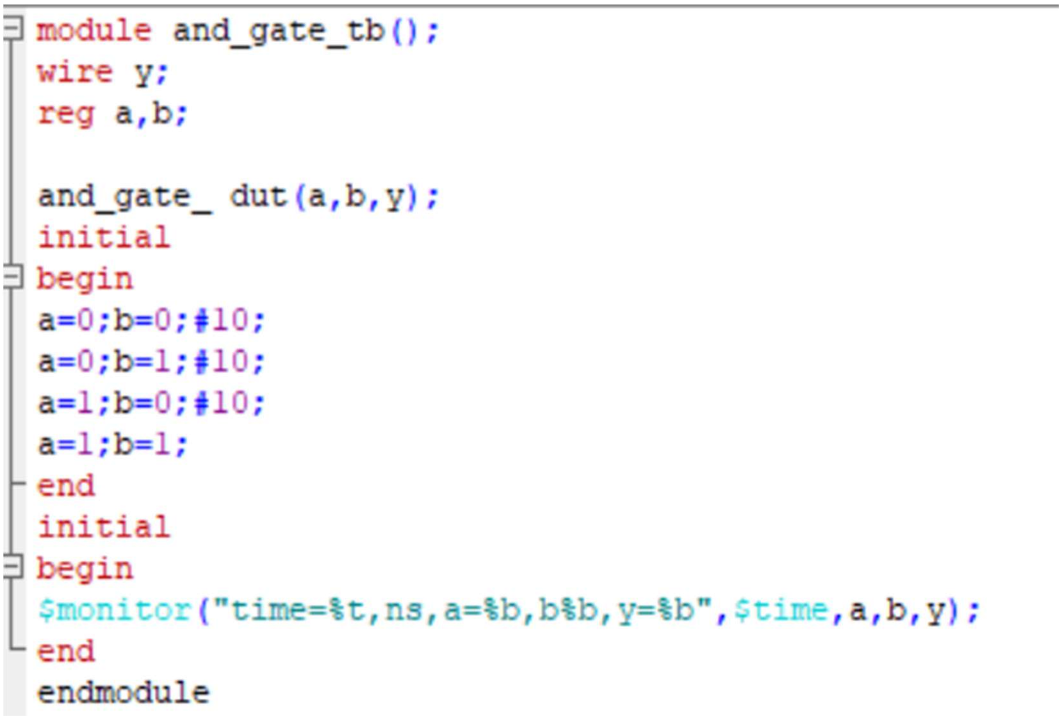
```
module and_gate(input a,b,output y);
output reg y;
always@(*)
begin
y=a&b;
end
endmodule
```

Gate Level Modelling



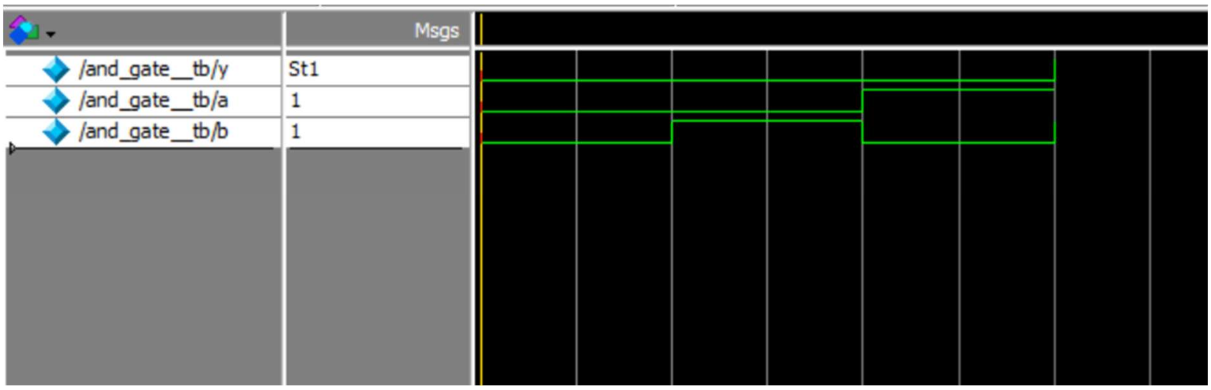
```
module and_gate(input a,b,output y);
and a1(y,a,b);
endmodule
```

b)Testbench Code

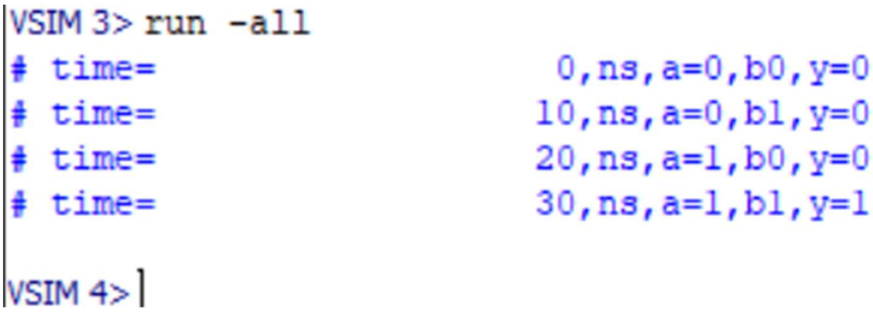


```
module and_gate_tb();
wire y;
reg a,b;

and_gate_ dut(a,b,y);
initial
begin
a=0;b=0;#10;
a=0;b=1;#10;
a=1;b=0;#10;
a=1;b=1;
end
initial
begin
$monitor("time=%t,ns,a=%b,b%b,y=%b",$time,a,b,y);
end
endmodule
```

c)Waveform



d)Console Output

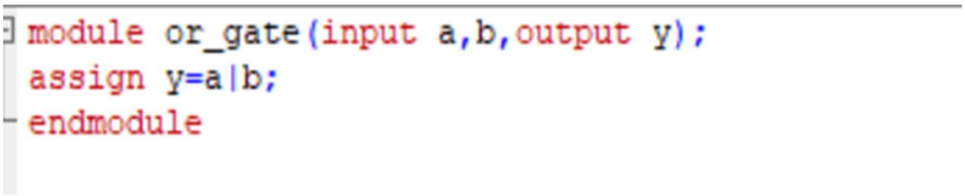


```
VSIM 3> run -all
# time=                    0,ns,a=0,b0,y=0
# time=                   10,ns,a=0,b1,y=0
# time=                   20,ns,a=1,b0,y=0
# time=                   30,ns,a=1,b1,y=1

VSIM 4>
```

OR GATE

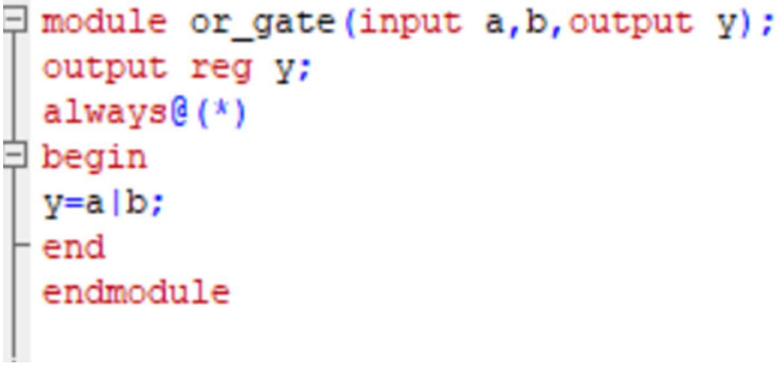
a)Design Code

Data Flow Modelling



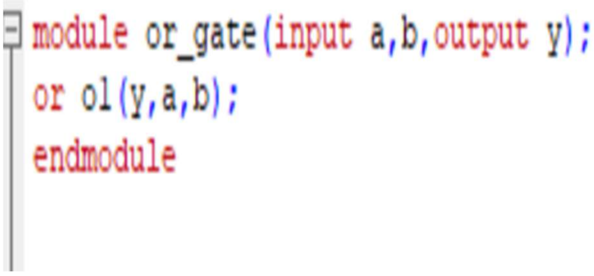
```
module or_gate(input a,b,output y);
assign y=a|b;
endmodule
```

Behavioral Modelling



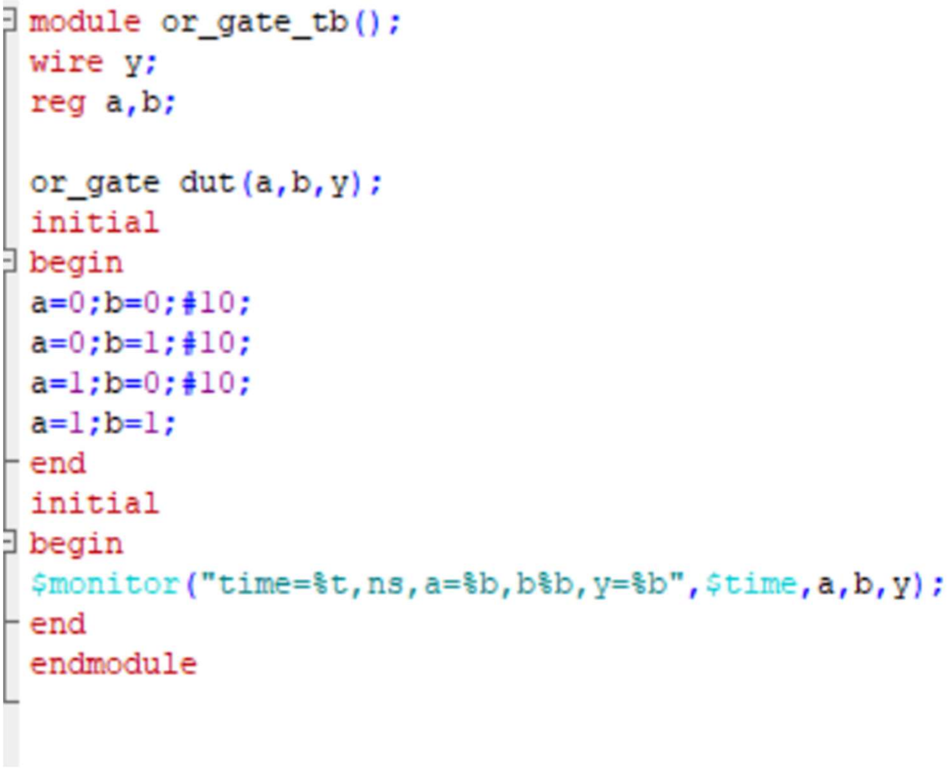
```
module or_gate(input a,b,output y);
output reg y;
always@(*)
begin
y=a|b;
end
endmodule
```

Gate Level Modelling



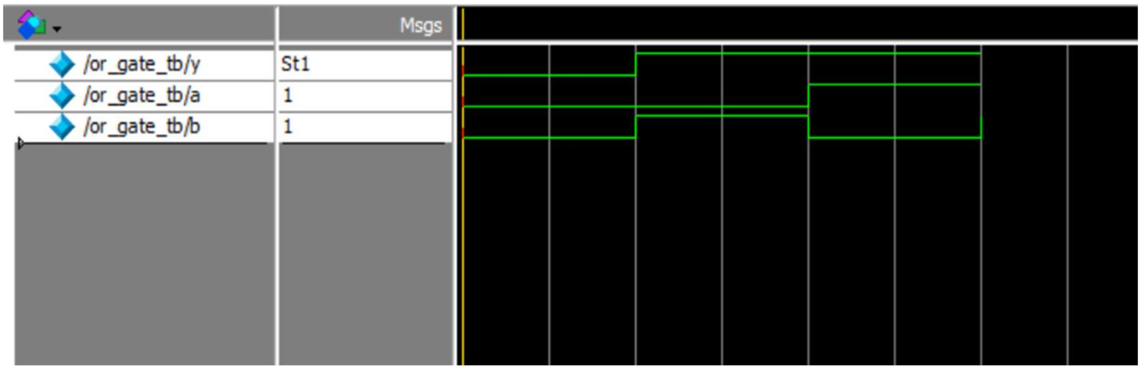
```
module or_gate(input a,b,output y);
or o1(y,a,b);
endmodule
```

b) Testbench

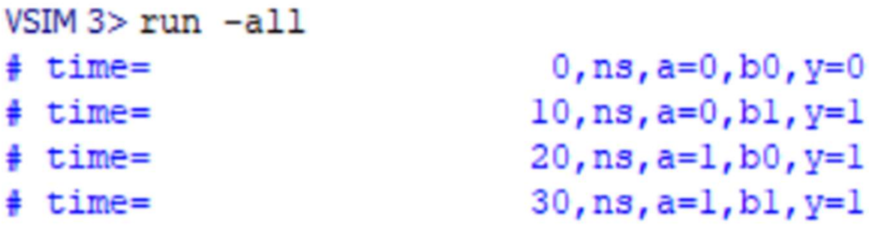


```
module or_gate_tb();
wire y;
reg a,b;

or_gate dut(a,b,y);
initial
begin
a=0;b=0;#10;
a=0;b=1;#10;
a=1;b=0;#10;
a=1;b=1;
end
initial
begin
$monitor("time=%t,ns,a=%b,b%b,y=%b",$time,a,b,y);
end
endmodule
```

c) Waveform



d)Console Output

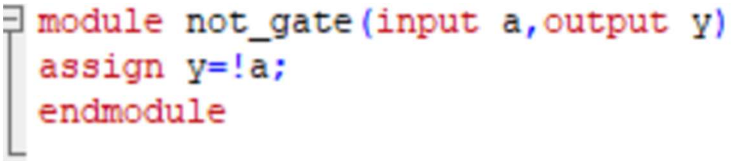


```
VSIM 3> run -all
# time=                    0,ns,a=0,b0,y=0
# time=                   10,ns,a=0,b1,y=1
# time=                   20,ns,a=1,b0,y=1
# time=                   30,ns,a=1,b1,y=1
```

NOT GATE

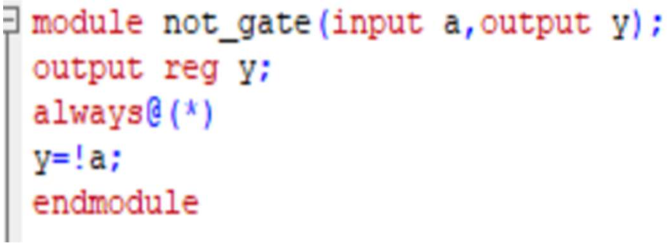
a)Design Code

Data Flow Modelling



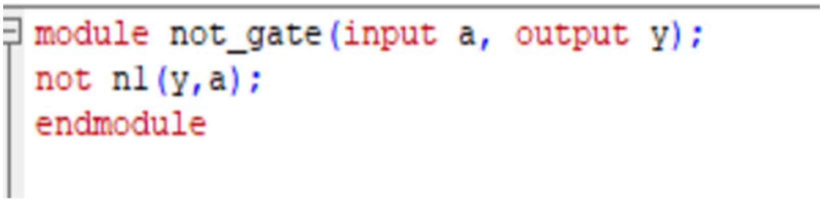
```
module not_gate(input a,output y)
assign y=!a;
endmodule
```

Behavioral Modelling



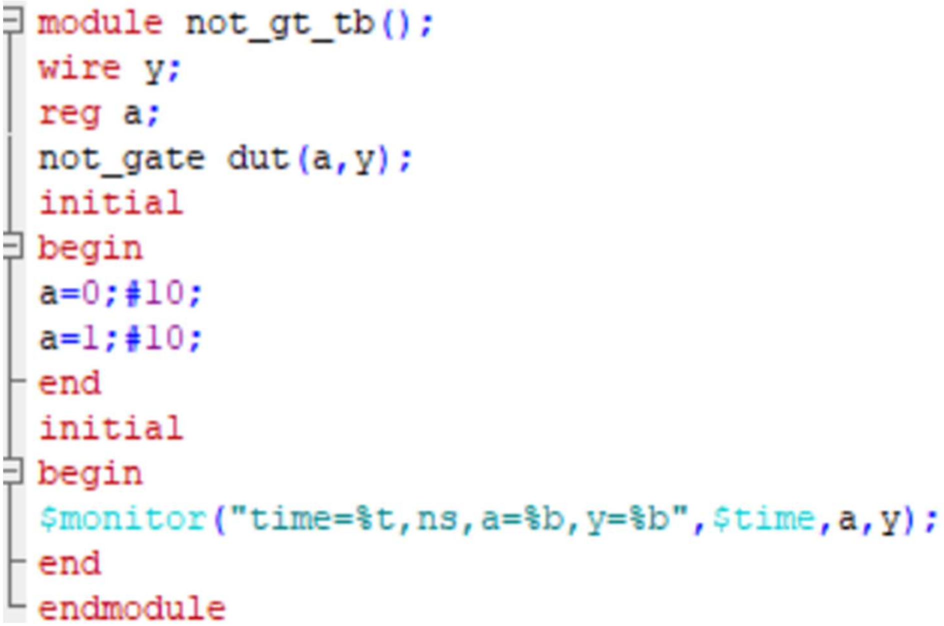
```
module not_gate(input a,output y);
output reg y;
always@(*)
y=!a;
endmodule
```

Gate Level Modelling



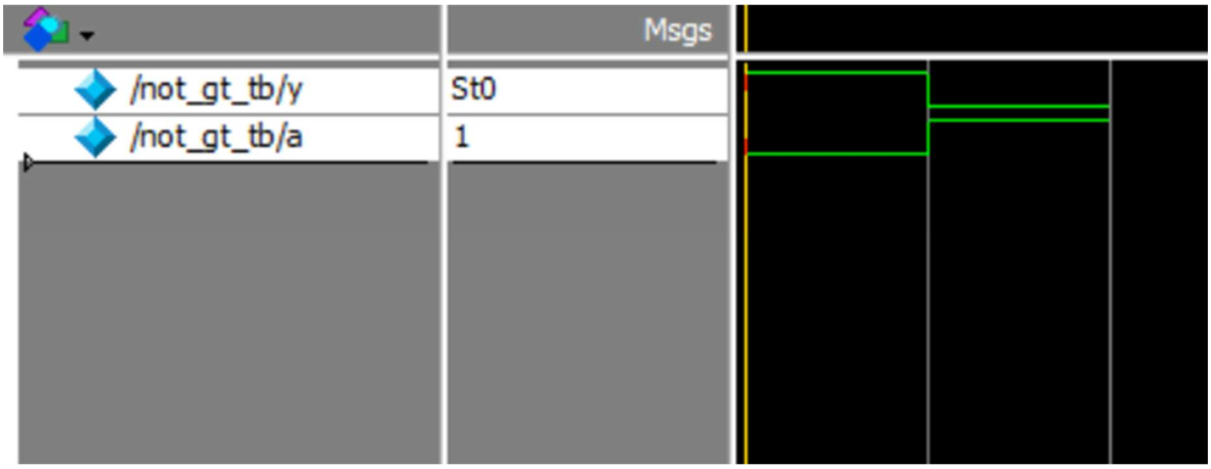
```
module not_gate(input a, output y);
not nl(y,a);
endmodule
```

b)Testbench

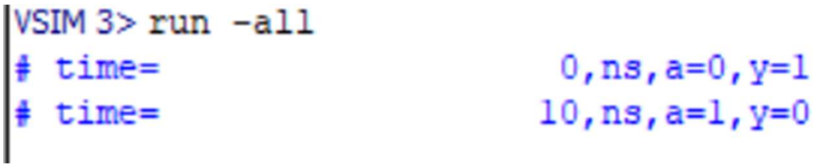


```
module not_gt_tb();
wire y;
reg a;
not_gate dut(a,y);
initial
begin
a=0;#10;
a=1;#10;
end
initial
begin
$monitor("time=%t,ns,a=%b,y=%b",$time,a,y);
end
endmodule
```

c)Waveform



d)Console Output

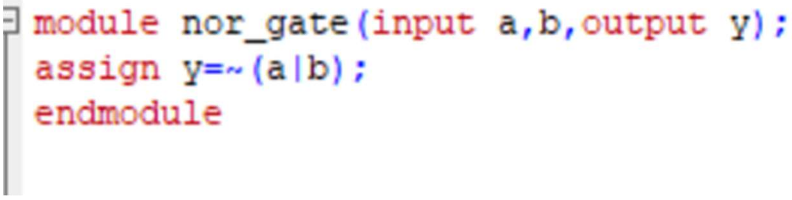


```
VSIM 3> run -all
# time=                   0,ns,a=0,y=1
# time=                  10,ns,a=1,y=0
```

NOR GATE

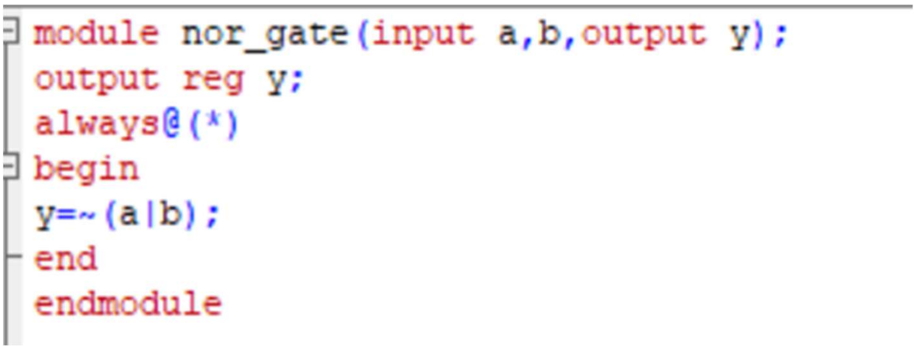
a)Design Code

Data Flow Modelling



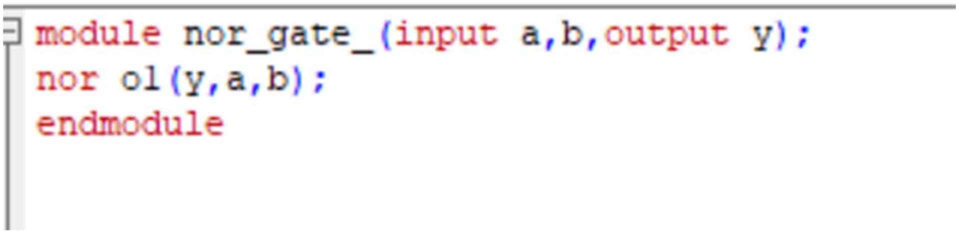
```
module nor_gate(input a,b,output y);
assign y=~(a|b);
endmodule
```

Behavioral Modelling



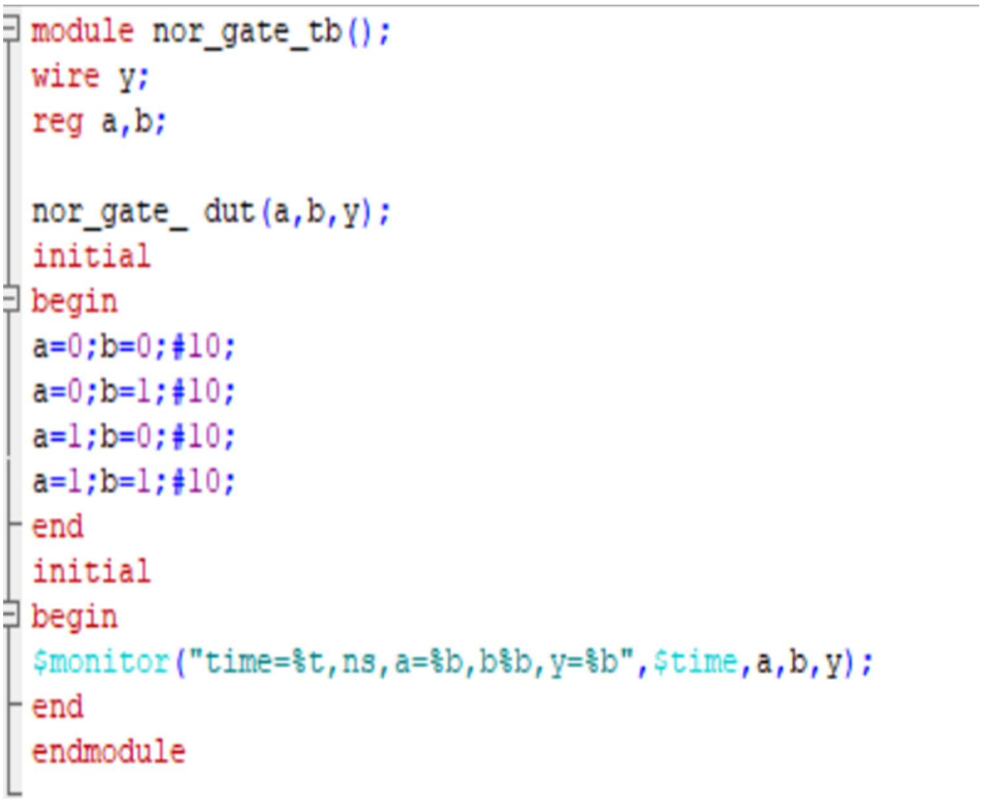
```
module nor_gate(input a,b,output y);
output reg y;
always@(*)
begin
y=~(a|b);
end
endmodule
```

Gate Level Modelling



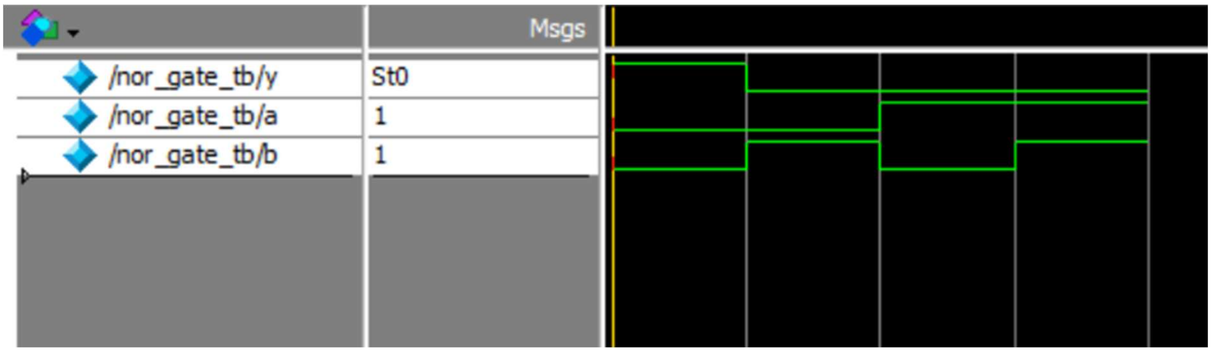
```
module nor_gate_(input a,b,output y);
nor ol(y,a,b);
endmodule
```

b)Testbench



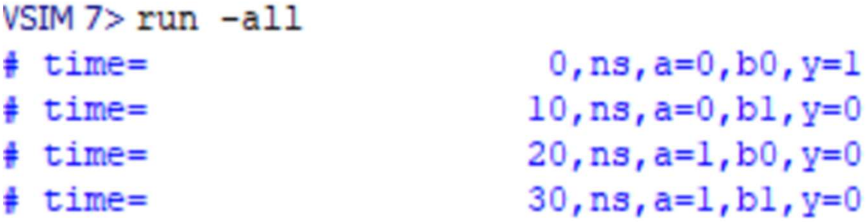
```
module nor_gate_tb();
wire y;
reg a,b;

nor_gate_ dut(a,b,y);
initial
begin
a=0;b=0;#10;
a=0;b=1;#10;
a=1;b=0;#10;
a=1;b=1;#10;
end
initial
begin
$monitor("time=%t,ns,a=%b,b%b,y=%b",$time,a,b,y);
end
endmodule
```

c)Waveform



	Msgs
/nor_gate_tb/y	St0
/nor_gate_tb/a	1
/nor_gate_tb/b	1

d)Console Output

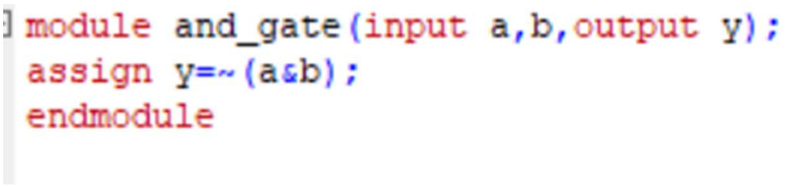


```
VSIM 7> run -all
# time=                    0,ns,a=0,b0,y=1
# time=                   10,ns,a=0,b1,y=0
# time=                   20,ns,a=1,b0,y=0
# time=                   30,ns,a=1,b1,y=0
```

NAND GATE

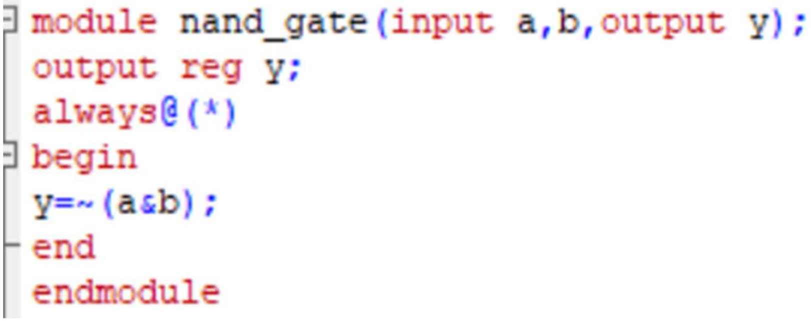
a)DesignCode

Data Flow Modelling



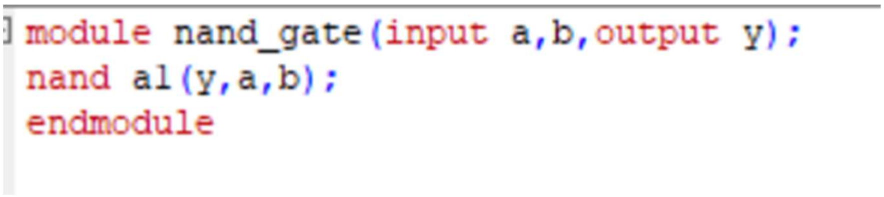
```
module and_gate(input a,b,output y);
assign y=~(a&b);
endmodule
```

Behavioral Modelling



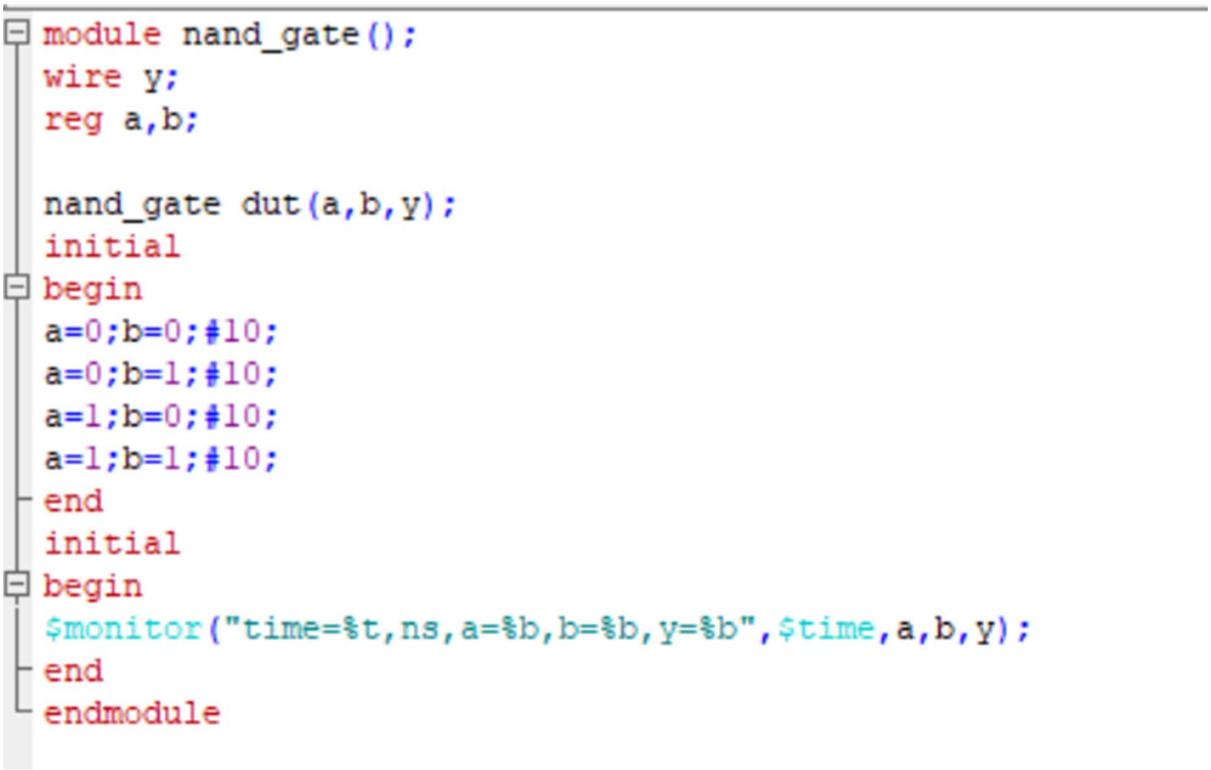
```
module nand_gate(input a,b,output y);
output reg y;
always@(*)
begin
y=~(a&b);
end
endmodule
```

Gate Level Modelling



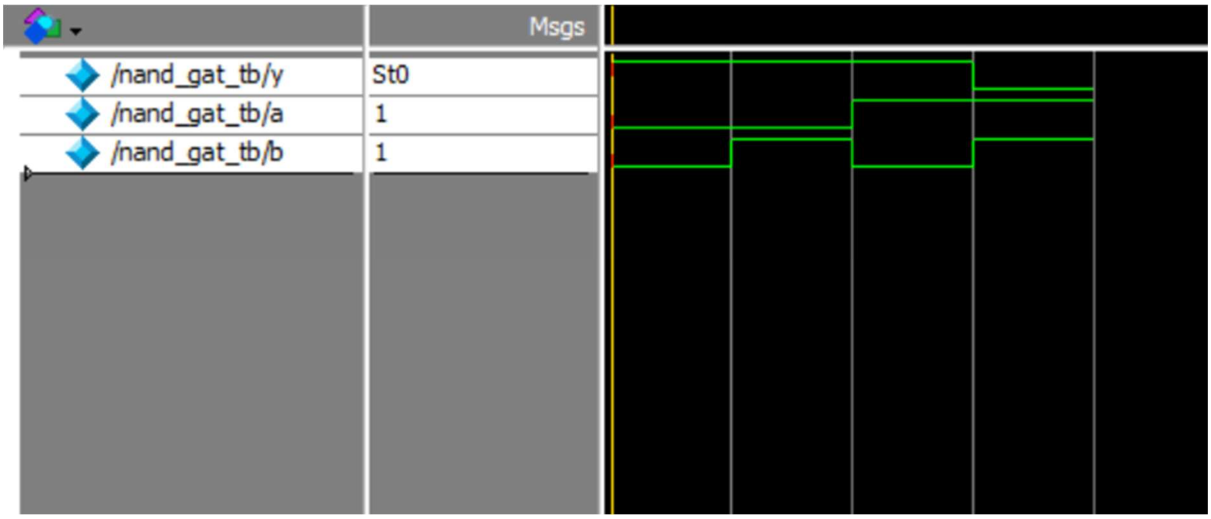
```
module nand_gate(input a,b,output y);
nand a1(y,a,b);
endmodule
```

b)Testbench

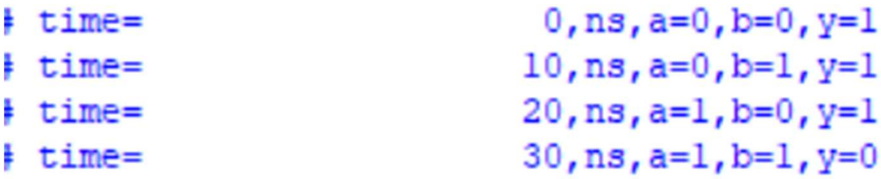


```
module nand_gate();
wire y;
reg a,b;

nand_gate dut(a,b,y);
initial
begin
a=0;b=0;#10;
a=0;b=1;#10;
a=1;b=0;#10;
a=1;b=1;#10;
end
initial
begin
$monitor("time=%t,ns,a=%b,b=%b,y=%b",$time,a,b,y);
end
endmodule
```

c)Waveform



d)Console Output

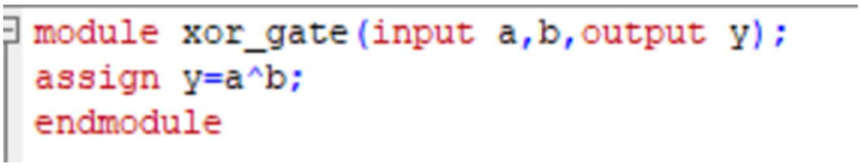


```
# time=                    0,ns,a=0,b=0,y=1
# time=                   10,ns,a=0,b=1,y=1
# time=                   20,ns,a=1,b=0,y=1
# time=                   30,ns,a=1,b=1,y=0
```

XOR GATE

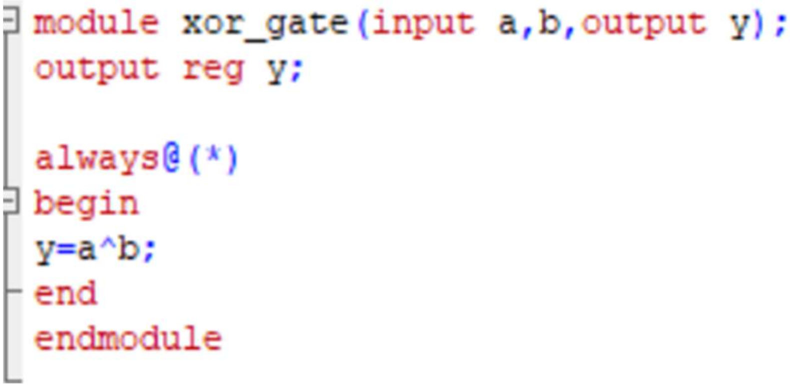
a)Design Code

Data Flow Modelling



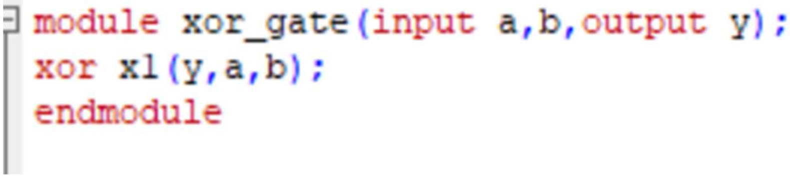
```
module xor_gate(input a,b,output y);
assign y=a^b;
endmodule
```

Behavioral Modelling



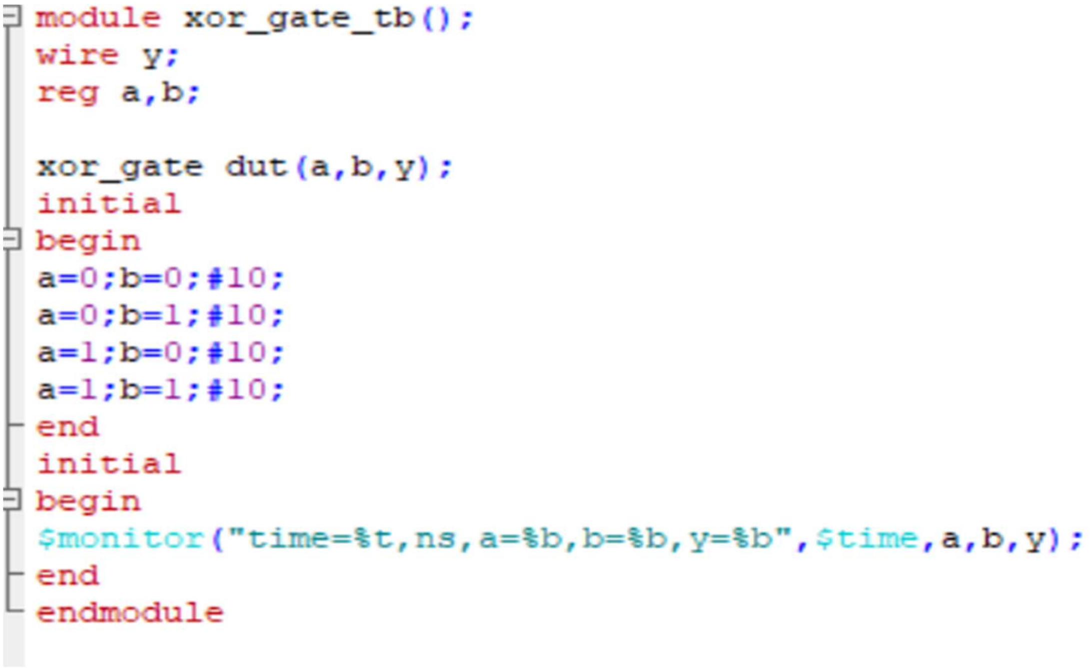
```
module xor_gate(input a,b,output y);
output reg y;

always@(*)
begin
y=a^b;
end
endmodule
```

Gate Level Modelling



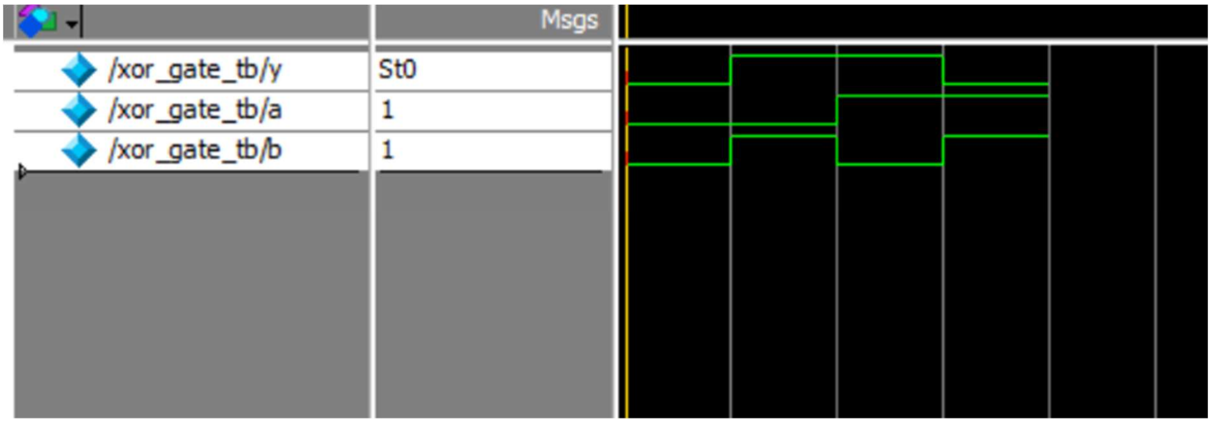
```
module xor_gate(input a,b,output y);
xor x1(y,a,b);
endmodule
```

b)Testbench



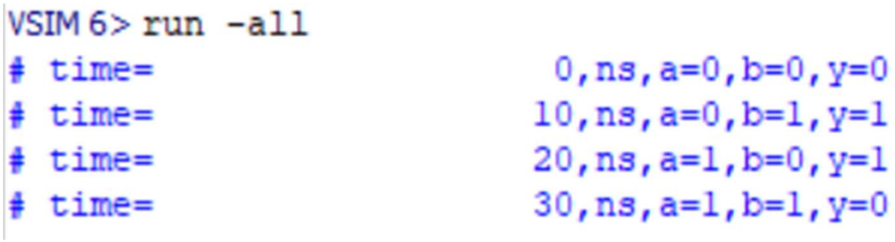
```
module xor_gate_tb();
wire y;
reg a,b;

xor_gate dut(a,b,y);
initial
begin
a=0;b=0;#10;
a=0;b=1;#10;
a=1;b=0;#10;
a=1;b=1;#10;
end
initial
begin
$monitor("time=%t,ns,a=%b,b=%b,y=%b",$time,a,b,y);
end
endmodule
```

c)Waveform



```
                 Msgs
/xor_gate_tb/y   St0
/xor_gate_tb/a   1
/xor_gate_tb/b   1
```

d)Console Output

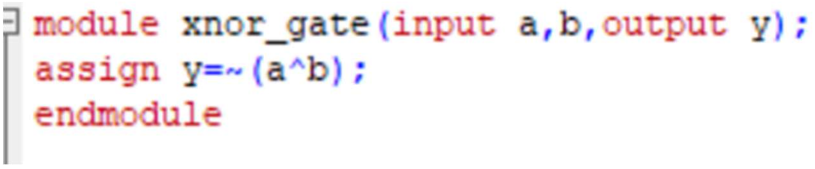


```
VSIM 6> run -all
# time=                    0,ns,a=0,b=0,y=0
# time=                   10,ns,a=0,b=1,y=1
# time=                   20,ns,a=1,b=0,y=1
# time=                   30,ns,a=1,b=1,y=0
```

XNOR GATE

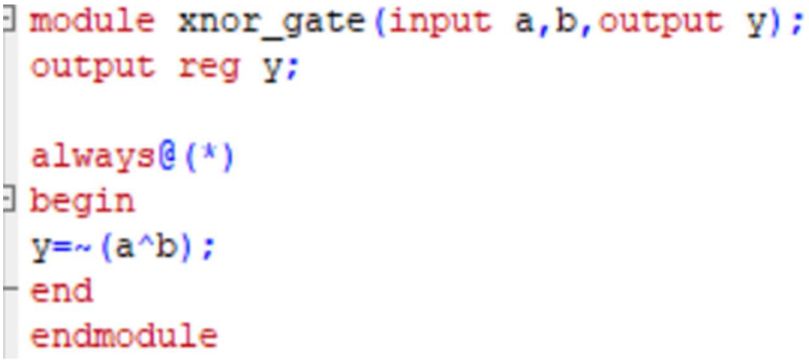
a)Design Code

Data Flow Modelling



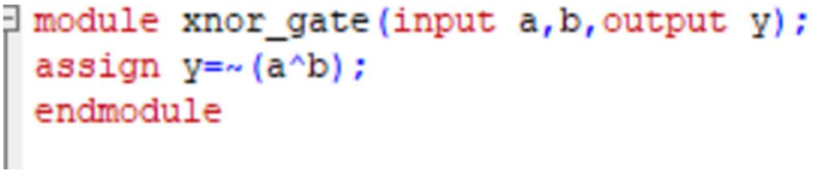
```
module xnor_gate(input a,b,output y);
assign y=~(a^b);
endmodule
```

Behavioral Modelling



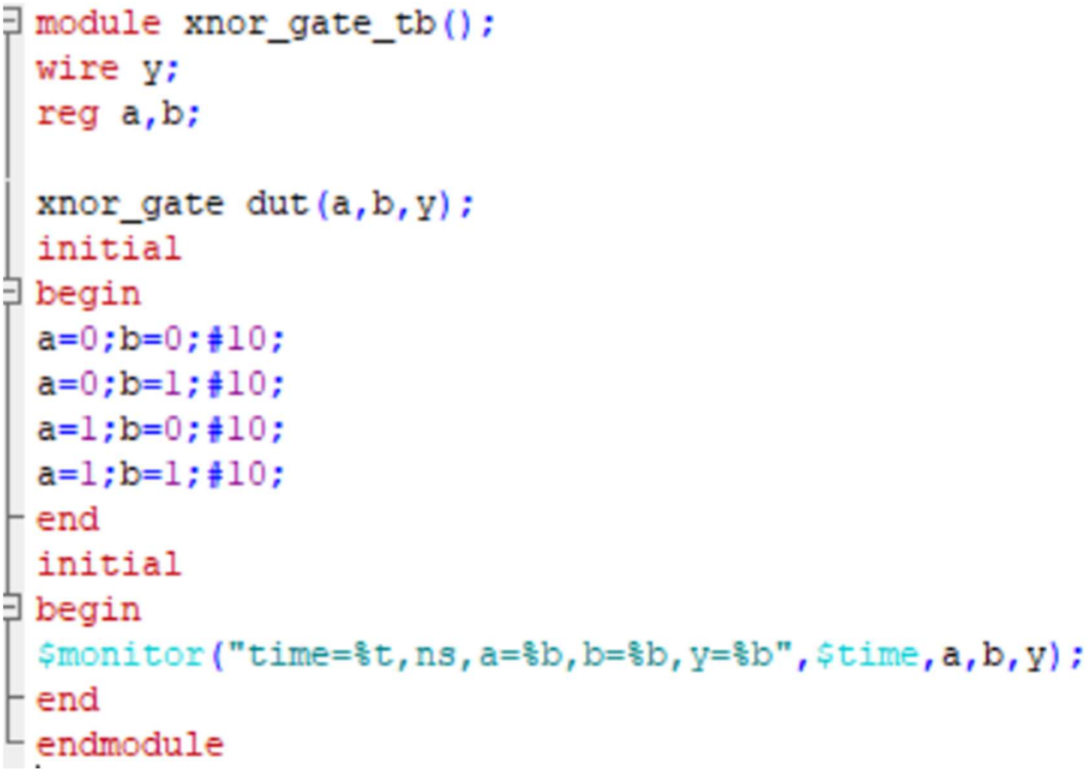
```
module xnor_gate(input a,b,output y);
output reg y;

always@(*)
begin
y=~(a^b);
end
endmodule
```

Gate Level Modelling



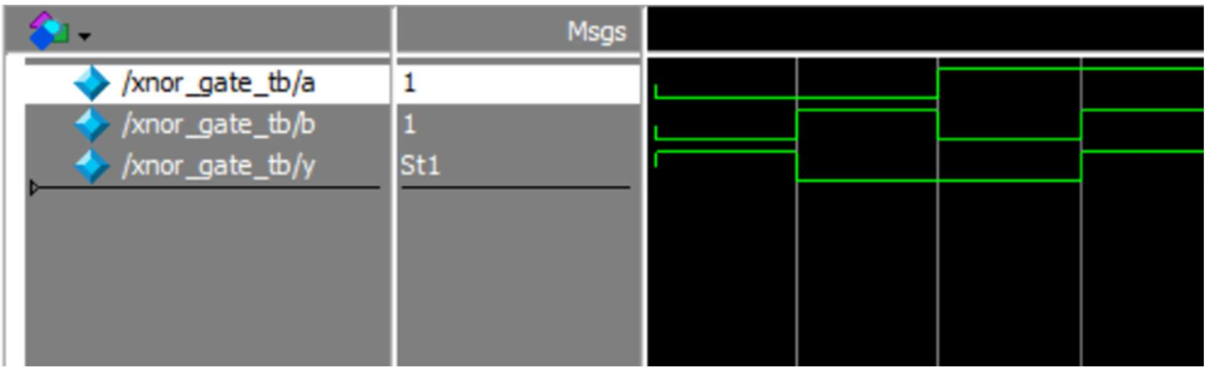
```
module xnor_gate(input a,b,output y);
assign y=~(a^b);
endmodule
```

b)Testbench

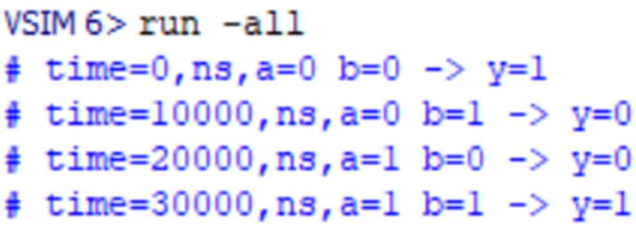


```
module xnor_gate_tb();
wire y;
reg a,b;

xnor_gate dut(a,b,y);
initial
begin
a=0;b=0;#10;
a=0;b=1;#10;
a=1;b=0;#10;
a=1;b=1;#10;
end
initial
begin
$monitor("time=%t,ns,a=%b,b=%b,y=%b",$time,a,b,y);
end
endmodule
```

c)Waveform



d)Console Output



```
VSIM 6> run -all
# time=0,ns,a=0 b=0 -> y=1
# time=10000,ns,a=0 b=1 -> y=0
# time=20000,ns,a=1 b=0 -> y=0
# time=30000,ns,a=1 b=1 -> y=1
```