#50DAYS CHALLENGE

DAY 3

FULL ADDER

a)Design Code

Data Flow Modelling

```
module full_adder(input a,b,cin,output sum,carry);
assign sum=a^b^cin;
assign carry=(asb)|(bscin)|(ascin);
endmodule
```

Behavioral Modelling

```
module full_adder(a,b,cin,sum,carry);
input a,b,cin;
output reg sum,carry;
always@(*)
begin
{carry,sum}=a+b+cin;
end
endmodule
```

Gate Level Modelling

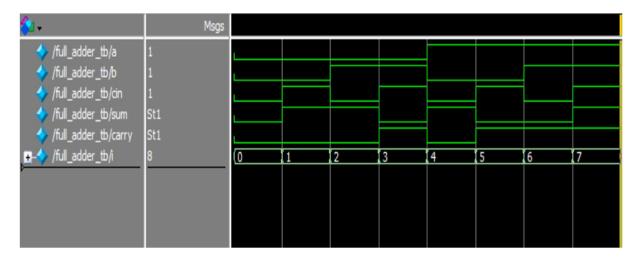
```
module full_adder(input a,b,cin,output sum,carry);
wire wl,w2,w3;
xor xl(wl,a,b);
xor x2(sum,wl,cin);
and al(w2,a,b);
and a2(w3,wl,cin);
or ol(carry,w2,w3);
endmodule
```

b)Testbench

```
module full_adder_tb();
reg a,b,cin;
wire sum,carry;
integer i;

full_adder dut(.a(a),.b(b),.cin(cin),.sum(sum),.carry(carry));
initial
begin
for(i=0;i<8;i=i+1)
begin
{a,b,cin}=i;
$10;
$display("Time:%t | a=%b b=%b cin=%b |sum=%b |carry=%b |",$time,a,b,cin,sum,carry);
end
$finish();
end
endmodule</pre>
```

c)Waveform



d)Console Output

```
# Time:
                         10 | a=0 b=0 cin=0 |sum=0 |carry=0
# Time:
                         20 | a=0 b=0 cin=1 |sum=1 |carry=0
                         30 | a=0 b=1 cin=0
# Time:
                                            |sum=1 |carrv=0
                         40 | a=0 b=1 cin=1
# Time:
                                            |sum=0 |carry=1
# Time:
                         50 | a=1 b=0 cin=0
                                            |sum=1 |carry=0
# Time:
                         60 | a=1 b=0 cin=1
                                            |sum=0 |carry=1
# Time:
                         70 | a=1 b=1 cin=0
                                            |sum=0 |carry=1
# Time:
                        80 | a=1 b=1 cin=1
                                            |sum=1 |carry=1
```

FULL ADDER USING HALF ADDER

a)Design Code

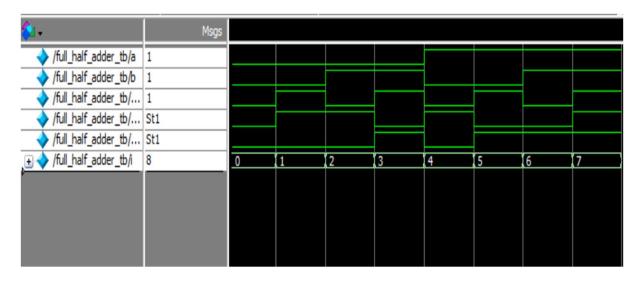
```
module half_adder(input a,b,output sum,carry);
assign sum=a^b;
assign carry=asb;
endmodule

module full_half_adder(input a,b,cin,output sum,carry);
wire wl,w2,w3;
half_adder hl(a,b,wl,w3);
half_adder h2(cin,wl,sum,w2);
assign carry= w3|w2;
endmodule
```

b)Testbench

```
module full half adder tb();
 reg a,b,cin;
 wire sum, carry;
integer i;
 full_half_adder dut(.a(a),.b(b),.cin(cin),.sum(sum),.carry(carry));
 initial
begin
 for (i=0;i<8;i=i+1)
begin
 {a,b,cin}=i;
 #10;
 $display("Time: %t | a= %b b= %b cin= %b | sum= %b | carry= %b | ", $time, a, b, cin, sum, carry);
- end
 $finish();
end
endmodule
```

c)Waveform



d)Console Output

ŧ	Time:	10	I	a=0	b=0	cin=0	sum=0	carry=0	1
ŧ	Time:	20	I	a=0	b=0	cin=1	sum=1	carry=0	1
ŧ	Time:	30	I	a=0	b=1	cin=0	sum=1	carry=0	1
ŧ	Time:	40	I	a=0	b=1	cin=1	sum=0	carry=1	1
ŧ	Time:	50	I	a=1	b=0	cin=0	sum=1	carry=0	1
ŧ	Time:	60	I	a=1	b=0	cin=1	sum=0	carry=1	1
ŧ	Time:	70	ı	a=1	b=1	cin=0	sum=0	carry=1	1
ŧ	Time:	80	I	a=1	b=1	cin=1	sum=1	carry=1	1