#50DAYS CHALLENGE

T FLIPFLOP USING D FLIPFLOP

a)Design Code

```verilog
module t_ff_using_d_ff(clk,t,rst,q,qbar);
input clk,t,rst;
output reg q;
output qbar;
wire d;

always@(posedge clk)
begin
if(rst)
q<=1'b0;
else
q<=d;
end

assign d=t^q;
assign qbar=~q;
endmodule
```

b)Testbench

```verilog
module tb_t_ff_using_d_ff();
reg clk,rst,t;
wire q,qbar;

t_ff_using_d_ff dut(.clk(clk),.rst(rst),.t(t),.q(q),.qbar(qbar));

initial
begin
clk=1'b0;
#10;
forever #5 clk=~clk;
end

task rst_dut();
begin
rst=1'b1;
@(negedge clk);
rst=1'b0;
end
endtask
```

```
task t_inputs(input i);
begin
 @(negedge clk);
 t=i;
end
endtask

initial
begin
    t = 0;
    rst_dut();
    t_inputs(1);
    t_inputs(0);
    t_inputs(1);
    t_inputs(0);
    t_inputs(1);
    rst_dut();
    t_inputs(1);

    #20;
    $finish;
end

initial
begin
$monitor("Time=%t | clk=%b | rst=%b |t=%b  |q=%b  |qbar=%b ",$time,clk,rst,t,q,qbar);
end
endmodule
```
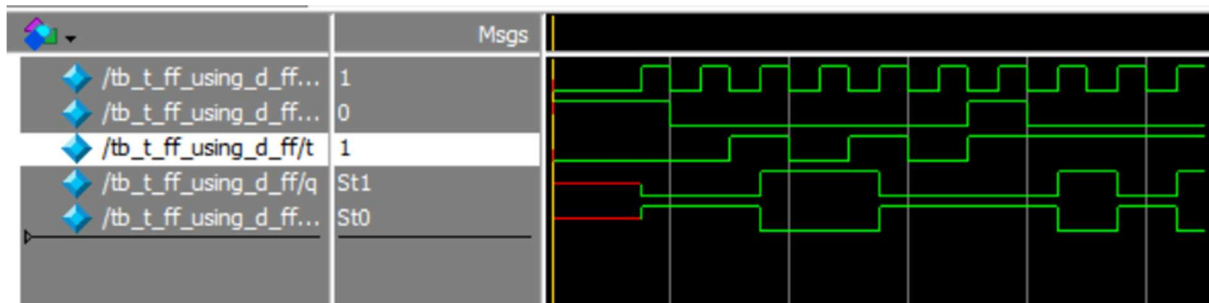
c)Waveform

d)Transcript

```
# Time=              0 | clk=0 | rst=1 |t=0   |q=x  |qbar=x
# Time=             15 | clk=1 | rst=1 |t=0   |q=0  |qbar=1
# Time=             20 | clk=0 | rst=0 |t=0   |q=0  |qbar=1
# Time=             25 | clk=1 | rst=0 |t=0   |q=0  |qbar=1
# Time=             30 | clk=0 | rst=0 |t=1   |q=0  |qbar=1
# Time=             35 | clk=1 | rst=0 |t=1   |q=1  |qbar=0
# Time=             40 | clk=0 | rst=0 |t=0   |q=1  |qbar=0
# Time=             45 | clk=1 | rst=0 |t=0   |q=1  |qbar=0
# Time=             50 | clk=0 | rst=0 |t=1   |q=1  |qbar=0
# Time=             55 | clk=1 | rst=0 |t=1   |q=0  |qbar=1
# Time=             60 | clk=0 | rst=0 |t=0   |q=0  |qbar=1
# Time=             65 | clk=1 | rst=0 |t=0   |q=0  |qbar=1
# Time=             70 | clk=0 | rst=1 |t=1   |q=0  |qbar=1
# Time=             75 | clk=1 | rst=1 |t=1   |q=0  |qbar=1
# Time=             80 | clk=0 | rst=0 |t=1   |q=0  |qbar=1
# Time=             85 | clk=1 | rst=0 |t=1   |q=1  |qbar=0
# Time=             90 | clk=0 | rst=0 |t=1   |q=1  |qbar=0
# Time=             95 | clk=1 | rst=0 |t=1   |q=0  |qbar=1
# Time=            100 | clk=0 | rst=0 |t=1   |q=0  |qbar=1
# Time=            105 | clk=1 | rst=0 |t=1   |q=1  |qbar=0
```