#50DAYS CHALLENGE

DAY 2

HALF ADDER

a)Design Code

Data Flow Modelling

```
module half_adder(input a,b,output s,c);
assign s=a^b;
assign c=a&b;
endmodule
```

Behavioral Modelling

```
module half_adder(a,b,s,c);
input a,b;
output reg s,c;
always @(*)
begin
s=a^b;
c=a&b;
end
endmodule
```

Gate Level Modelling

```
module half_adder(input a,b,output s,c);
xor xl(s,a,b);
and al(c,a,b);
endmodule
```

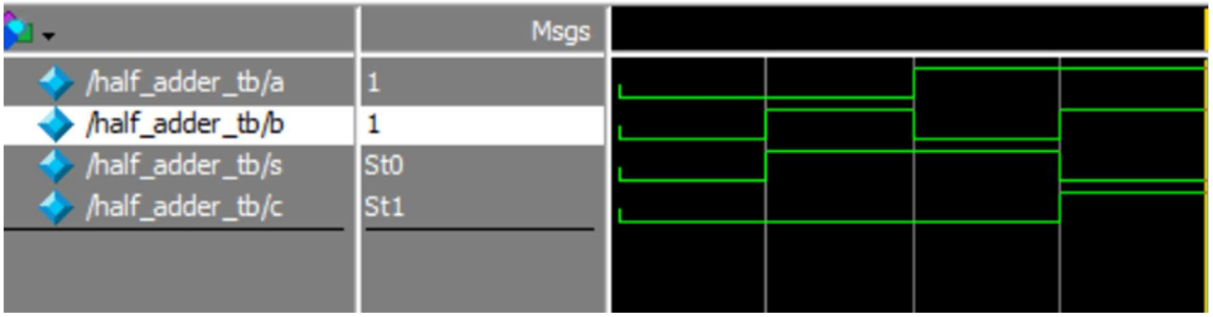
b)Testbench

```
module half_adder_tb();
reg a,b;

half_adder dut(a,b,s,c);

initial
begin
a=0;b=0;#10;
a=0;b=1;#10;
a=1;b=0;#10;
a=1;b=1;#10;
end
initial
begin
$monitor("time=%tns|a=%b|b=%b|s=%b|c=%b",$time,a,b,s,c);
end
endmodule
```

c)Waveform



d)Console Output

```
VSIM 8> run -all
# time=                    0ns|a=0|b=0|s=0|c=0
# time=                   10ns|a=0|b=1|s=1|c=0
# time=                   20ns|a=1|b=0|s=1|c=0
# time=                   30ns|a=1|b=1|s=0|c=1
```