

Day 3

cd to runs and ls

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/placement$ cd ../../..
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ ls -ltr
total 4
drwxr-xr-x 6 vsduser vsduser 4096 Jul 17 09:11 16-07_04-55
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$
```

cd to latest run and ls

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd 16-07_04-55/results/floorplan
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/floorplan$ ls
merged_unpadded.lef  picorv32a.floorplan.def  picorv32a.floorplan.def.png
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/floorplan$
```

Run magic

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/floorplan$ magic -T ~/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.floorplan.def &
```

See that pins are equidistant in magic



cd to configuration and open README.md

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/floorplan$ cd ../../..
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/configuration$ less README.md
```

```

| `VERILOG_INCLUDE_DIRS` | Specifies the verilog includes directories. <br> optional. |
| `SYNTH_FLAT_TOP` | Specifies whether or not the top level should be flattened during elaboration. 1 = True, 0= False <br> Default: `0` |
| `IO_PCT` | Specifies the percentage of the clock period used in the input/output delays. Ranges from 0 to 1.0. <br> (Default: `0.2`) |

### Floorplanning

| Variable | Description | |
|---|---|---|
| `FP_CORE_UTIL` | The core utilization percentage. <br> (Default: `50` percent) |
| `FP_ASPECT_RATIO` | The core's aspect ratio (height / width). <br> (Default: `1`)| |
| `FP_SIZING` | Whether to use relative sizing by making use of `FP_CORE_UTIL` or absolute one using `DIE_AREA`. <br> (Default: `relative` - accepts "absolute" as well)|
| `DIE_AREA` | Specific die area to be used in floorplanning. Specified as a 4-corner rectangle. Units in mm <br> (Default: unset)|
| `FP_IO_HMETAL` | The metal layer on which to place the io pins horizontally (top and bottom of the die). <br>(Default: `4`)| |
| `FP_IO_VMETAL` | The metal layer on which to place the io pins vertically (sides of the die) <br> (Default: `3`)| |
| `FP_IO_MODE` | Decides the mode of the random IO placement option. 0=matching mode, 1=random equidistant mode <br> (Default: `1`)| |
| `FP_WELLTAP_CELL` | The name of the welltap cell during welltap insertion. |
| `FP_ENDCAP_CELL` | The name of the endcap cell during endcap insertion. |
| `FP_PDN_VOFFSET` | The offset of the vertical power stripes on the metal layer 4 in the power distribution network <br> (Default: `16.32`)| |
| `FP_PDN_VPITCH` | The pitch of the vertical power stripes on the metal layer 4 in the power distribution network <br> (Default: `153.6`)| |
| `FP_PDN_HOFFSET` | The offset of the horizontal power stripes on the metal layer 5 in the power distribution network <br> (Default: `16.65`)| |
| `FP_PDN_HPITCH` | The pitch of the horizontal power stripes on the metal layer 5 in the power distribution network <br> (Default: `153.18`)| |
| `FP_PDN_AUTO_ADJUST` | Decides whether or not the flow should attempt to re-adjust the power grid, in order for it to fit inside the constraints. |

```

Open floorplan.tcl

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/configuration$ less floorplan.tcl
```

Mode is set to equidistant

```

set ::env(FP_PDN_AUTO_ADJUST) 1

set ::env(FP_PDN_CORE_RING) 0
set ::env(FP_PDN_ENABLE_RAILS) 1

set ::env(FP_PDN_CHECK_NODES) 1

set ::env(FP_IO_MODE) 1; # 0 matching mode - 1 random equidistant mode
set ::env(FP_IO_HLENGTH) 4
set ::env(FP_IO_VLENGTH) 4
set ::env(FP_IO_VEXTEND) -1
set ::env(FP_IO_HEXTEND) -1
set ::env(FP_IO_VTHICKNESS_MULT) 2
set ::env(FP_IO_HTHICKNESS_MULT) 2

```

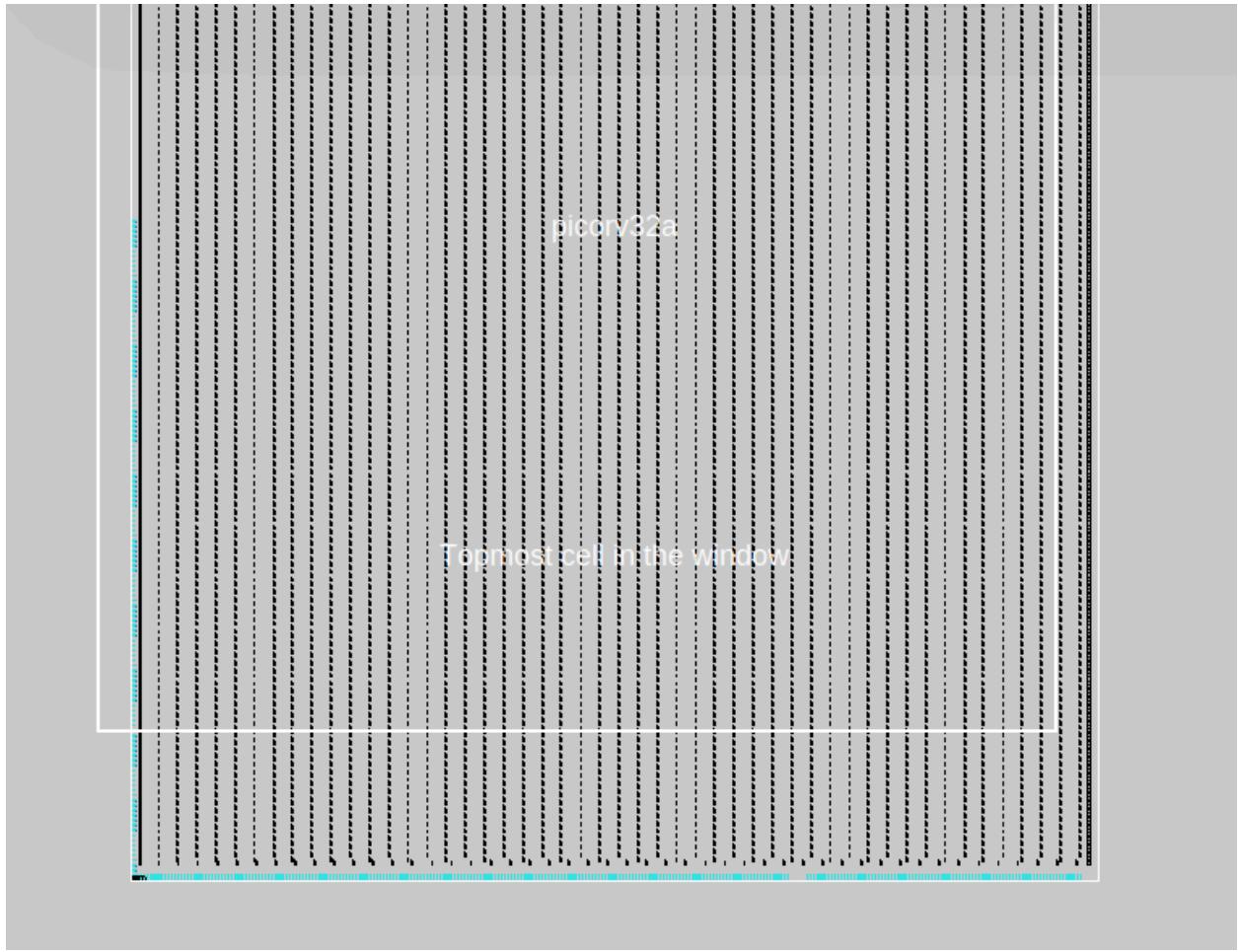
Set it to 2 and run floorplan

```
% set ::env(FP_IO_MODE) 2
2
% run_floorplan
```

Is to see that it's been updated and run magic again

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/floorplan$ ls -ltr
total 2640
lrwxrwxrwx 1 vsduser vsduser 29 Jul 16 10:25 merged_unpadded.lef -> ../../tmp/merged_unpadded.lef
-rw-r--r-- 1 vsduser vsduser 2436314 Jul 18 07:37 picorv32a.floorplan.def
-rw-r--r-- 1 vsduser vsduser 265080 Jul 18 07:37 picorv32a.floorplan.def.png
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/floorplan$ magic -T ~/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.floorplan.def &
```

Pins are not equidistant anymore



pwd in openlane directory

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ pwd  
/home/vsduser/Desktop/work/tools/openlane_working_dir/openlane
```

Clone git repo and see folder in openlane directory

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ git clone https://github.com/nickson-jose/vsdstdcelldesign.git  
Cloning into 'vsdstdcelldesign'...  
remote: Enumerating objects: 492, done.  
remote: Counting objects: 100% (18/18), done.  
remote: Compressing objects: 100% (18/18), done.  
remote: Total 492 (delta 7), reused 0 (delta 0), pack-reused 474 (from 1)  
Receiving objects: 100% (492/492), 24.08 MiB | 1.67 MiB/s, done.  
Resolving deltas: 100% (210/210), done.  
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ ls -ltr  
total 140  
drwxr-xr-x 15 vsduser docker 4096 Jun 29 2021 scripts  
-rw-r--r-- 1 vsduser docker 20787 Jun 29 2021 run_designs.py  
-rw-r--r-- 1 vsduser docker 7898 Jun 29 2021 report_generation_wrapper.py  
drwxr-xr-x 3 vsduser docker 4096 Jun 29 2021 regression_results  
-rw-r--r-- 1 vsduser docker 25509 Jun 29 2021 README.md  
-rw-r--r-- 1 vsduser docker 7273 Jun 29 2021 Makefile  
-rw-r--r-- 1 vsduser docker 11350 Jun 29 2021 LICENSE  
-rwxr-xr-x 1 vsduser docker 6519 Jun 29 2021 flow.tcl  
drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docs  
drwxr-xr-x 5 vsduser docker 4096 Jun 29 2021 docker_build  
drwxr-xr-x 44 vsduser docker 4096 Jun 29 2021 designs  
-rw-r--r-- 1 vsduser docker 1285 Jun 29 2021 CONTRIBUTING.md  
-rw-r--r-- 1 vsduser docker 5514 Jun 29 2021 conf.py  
drwxr-xr-x 2 vsduser docker 4096 Jun 29 2021 configuration  
-rwxr-xr-x 1 vsduser docker 966 Jun 29 2021 clean_runs.tcl  
-rw-r--r-- 1 vsduser docker 709 Jun 29 2021 AUTHORS.md  
-rw-r--r-- 1 vsduser vsduser 963 May 20 2023 default.cvcrc  
drwxrwxr-x 6 vsduser vsduser 4096 Jul 18 08:12 vsdstdcelldesign  
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$
```

cd and ls in vsdstdcelldesign

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd vsdstdcelldesign/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 44
-rw-rw-r-- 1 vsduser vsduser 13525 Jul 18 08:12 README.md
-rw-rw-r-- 1 vsduser vsduser 11357 Jul 18 08:12 LICENSE
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 Images
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 extras
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 libs
-rw-rw-r-- 1 vsduser vsduser 2716 Jul 18 08:12 sky130_inv.mag
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

pwd to see location

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ pwd
/home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
```

cd and ls in magic directory

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cd ../../pdks/sky130A/libs.tech/magic
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic$ ls
bump_bond_generator generate_fill.py sky130A-BindKeys sky130A.magicrc sky130A.tech
check_density.py seal_ring_generator sky130A-GDS.tech sky130A.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic$ ls -ltr
total 408
drwxr-xr-x 2 vsduser docker 4096 Jun 28 2021 seal_ring_generator
drwxr-xr-x 2 vsduser docker 4096 Jun 28 2021 bump_bond_generator
-rwxr-xr-x 1 vsduser docker 136710 Jun 28 2021 sky130A.tech
-rwxr-xr-x 1 vsduser docker 203669 Jun 28 2021 sky130A.tcl
-rwxr-xr-x 1 vsduser docker 3013 Jun 28 2021 sky130A.magicrc
-rwxr-xr-x 1 vsduser docker 11471 Jun 28 2021 sky130A-GDS.tech
-rwxr-xr-x 1 vsduser docker 5098 Jun 28 2021 sky130A-BindKeys
-rwxr-xr-x 1 vsduser docker 15144 Jun 28 2021 generate_fill.py
-rwxr-xr-x 1 vsduser docker 21168 Jun 28 2021 check_density.py
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic$
```

Copy to vsdstdcelldesign

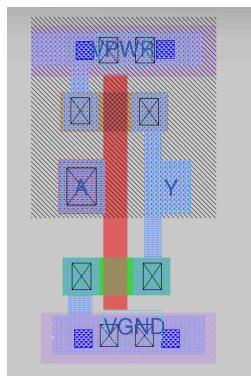
```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic$ cp sky130A.tech /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
```

Check that it has copied successfully

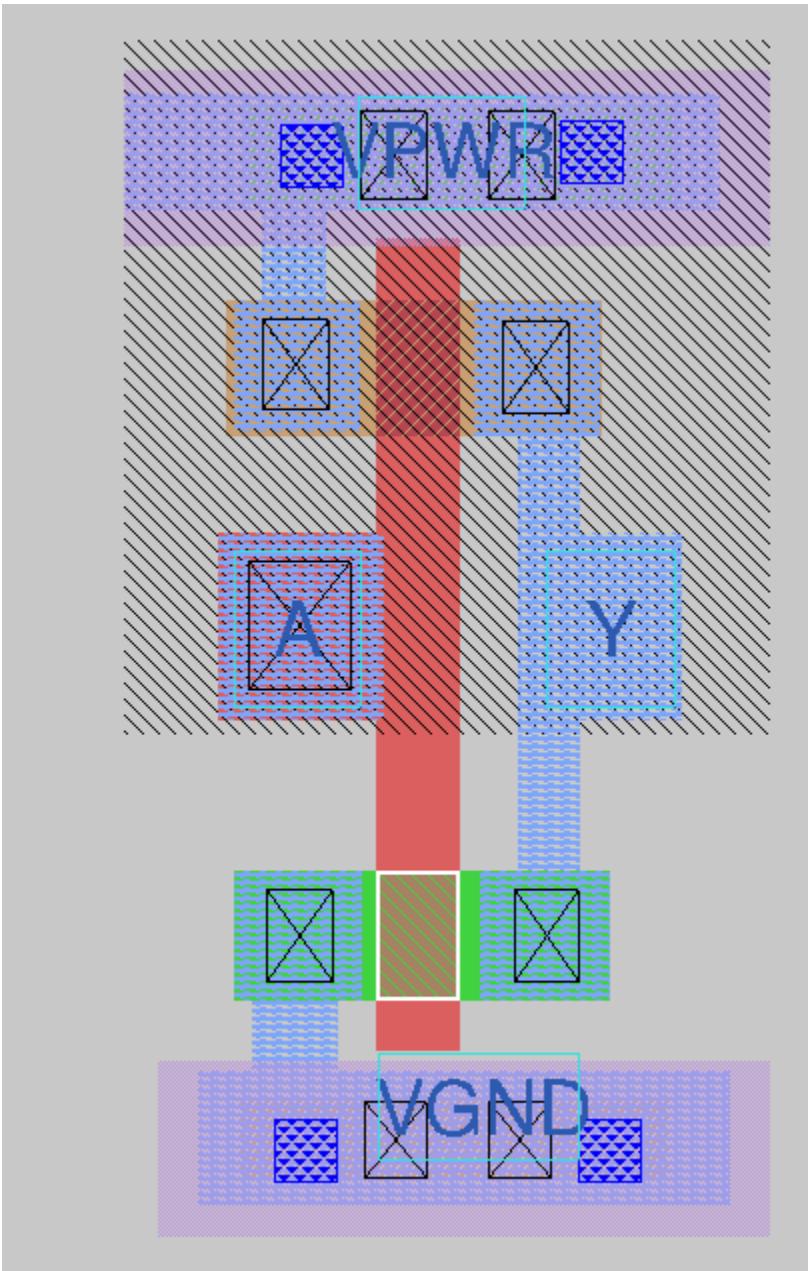
```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 180
-rw-rw-r-- 1 vsduser vsduser 13525 Jul 18 08:12 README.md
-rw-rw-r-- 1 vsduser vsduser 11357 Jul 18 08:12 LICENSE
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 Images
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 extras
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 libs
-rw-rw-r-- 1 vsduser vsduser 2716 Jul 18 08:12 sky130_inv.mag
-rwxr-xr-x 1 vsduser vsduser 136710 Jul 18 08:44 sky130A.tech
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

Run magic to display CMOS inverter

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ magic -T sky130A.tech sky130_inv.mag &
```



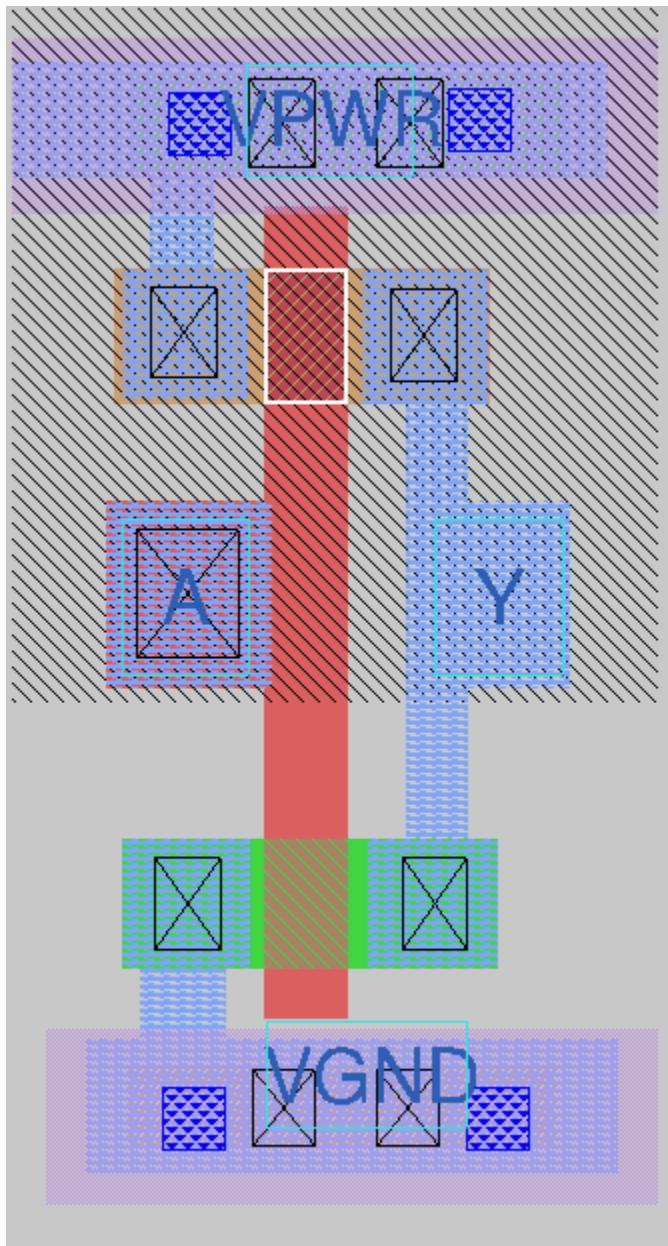
Press S while hovering over ndiffusion and polysilicon to select



Use what to see what selected part is

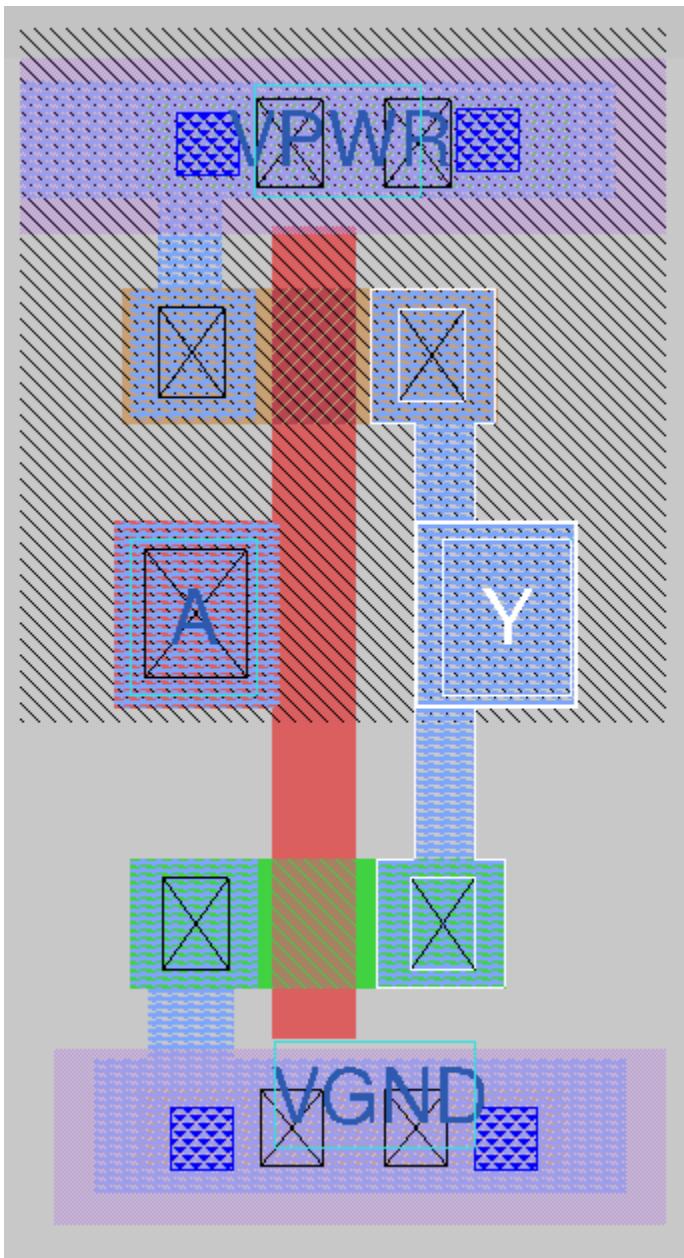
```
% what
Selected mask layers:
  nmos      ( Topmost cell in the window )
%
```

Do the same for pmos

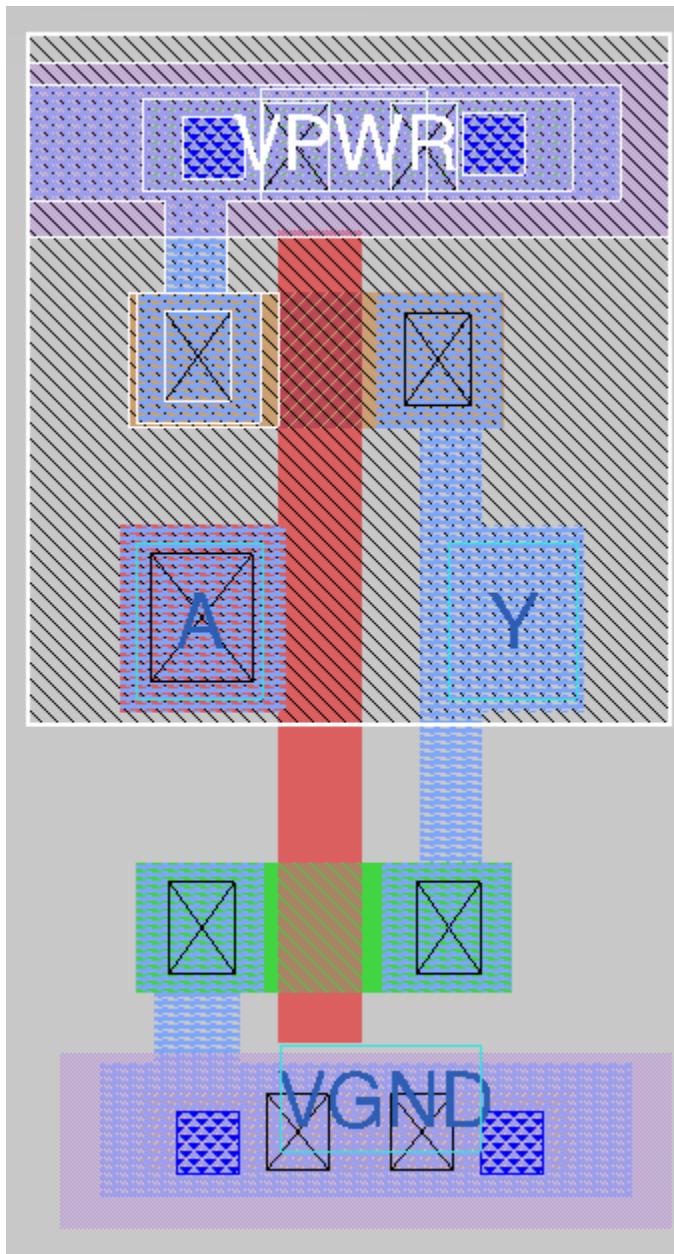


```
% what
Selected mask layers:
    pmos      ( Topmost cell in the window )
%
```

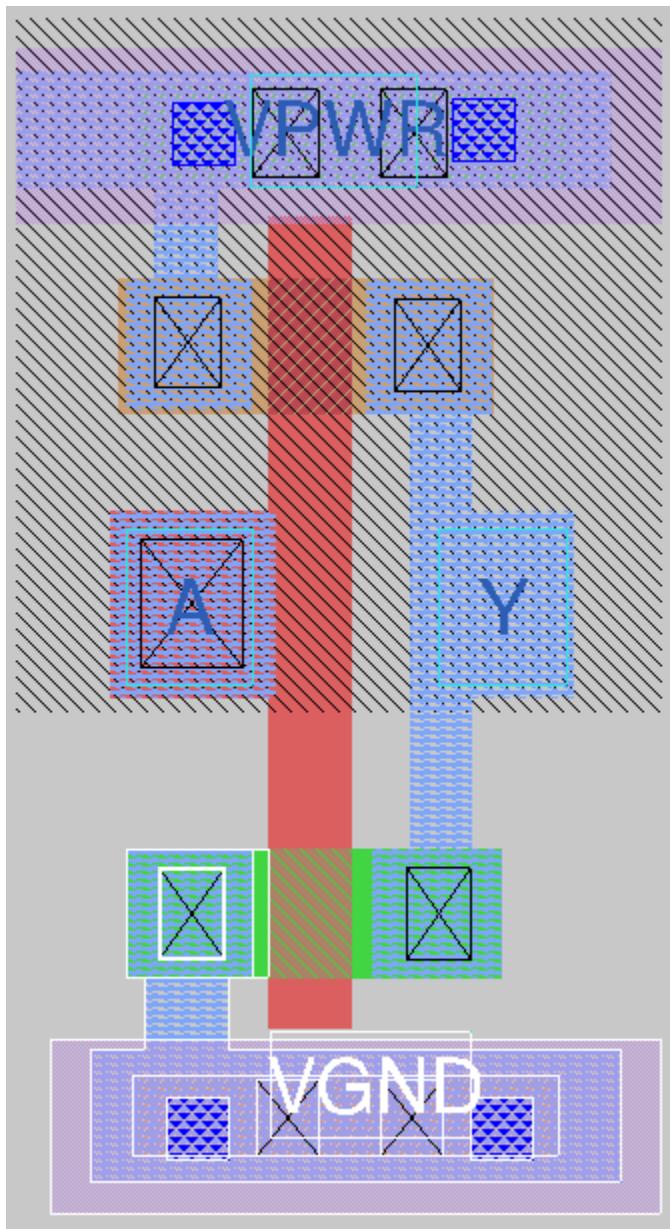
Pressing s twice shows you what the selected part is connected to



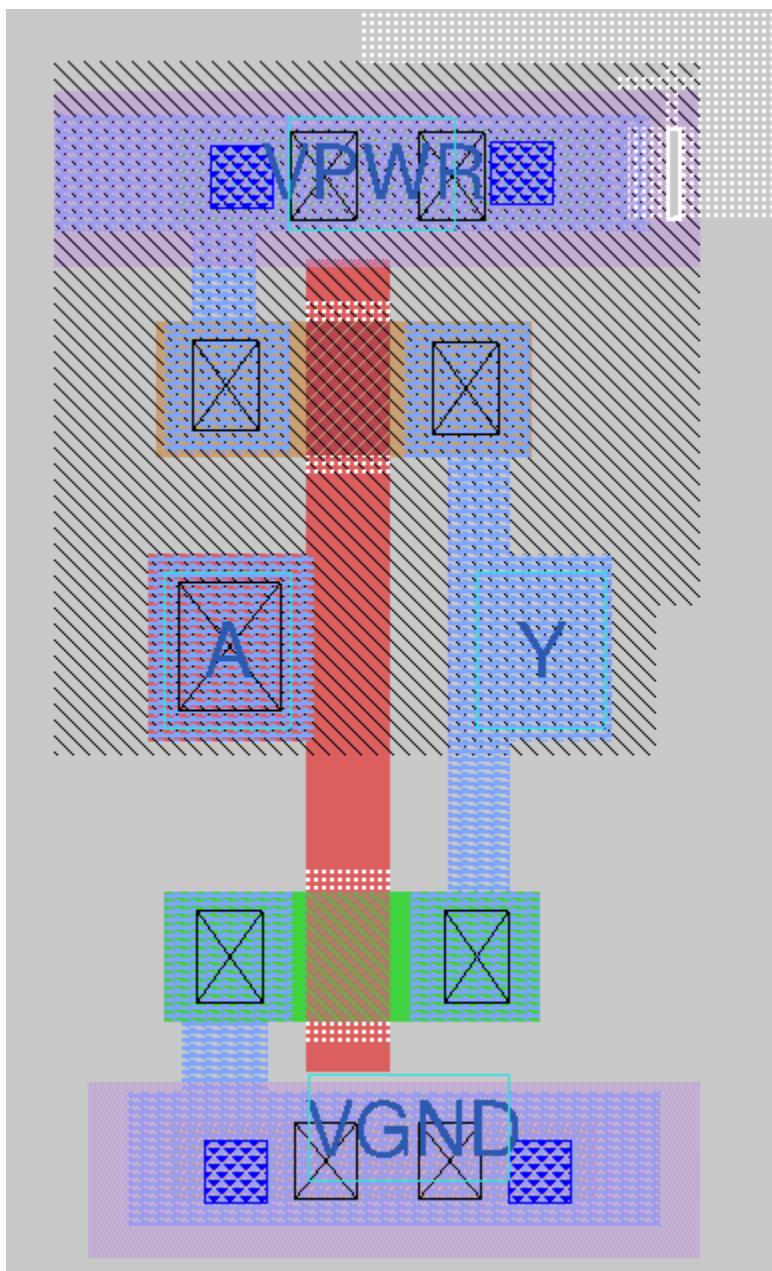
Press s a few times while hovering over the interconnect to see what it is connected to



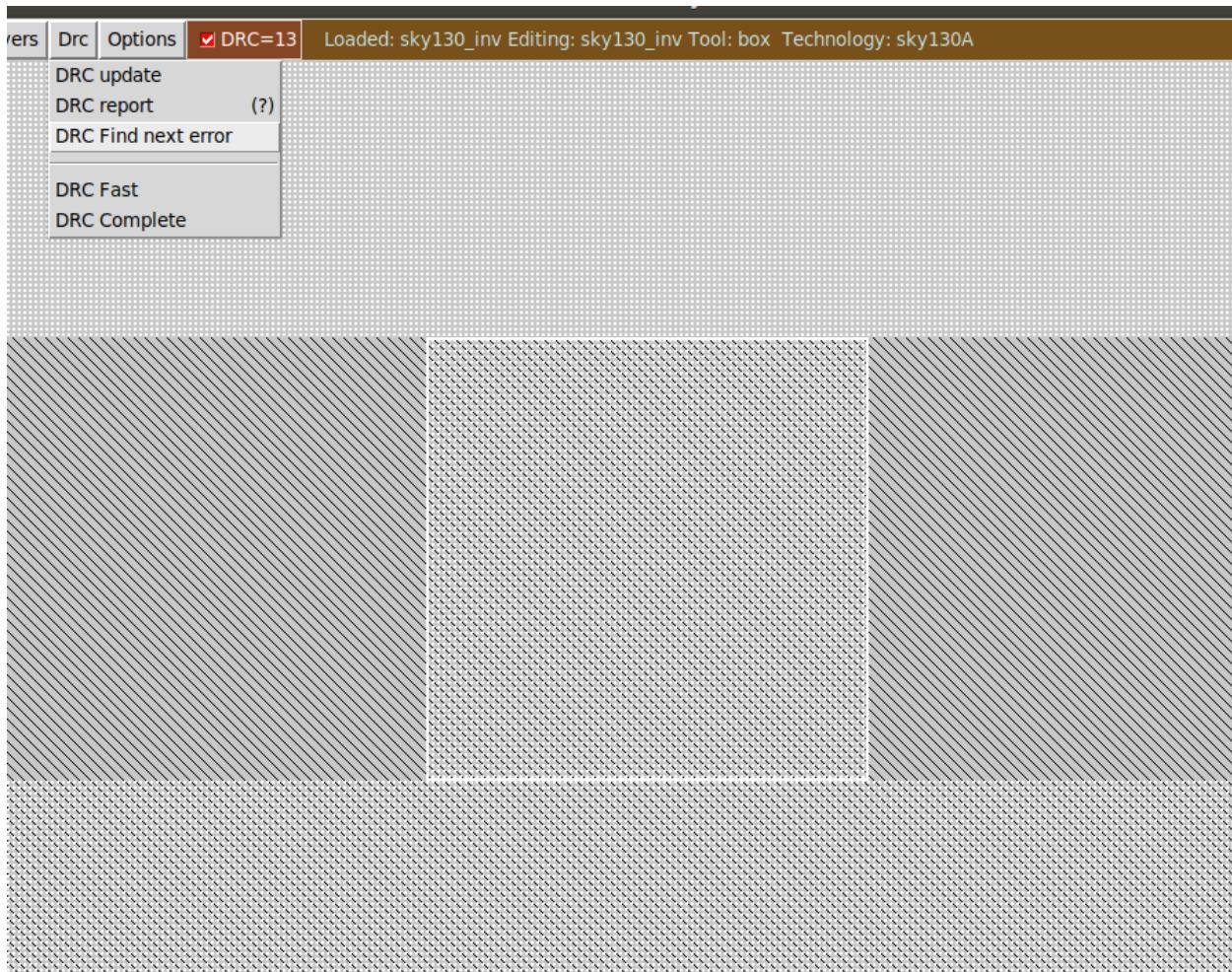
Repeat for the nmos



Erase parts of the nwell to cause DRC errors. Draw a box around the area then click in empty space with the middle mouse button to erase.



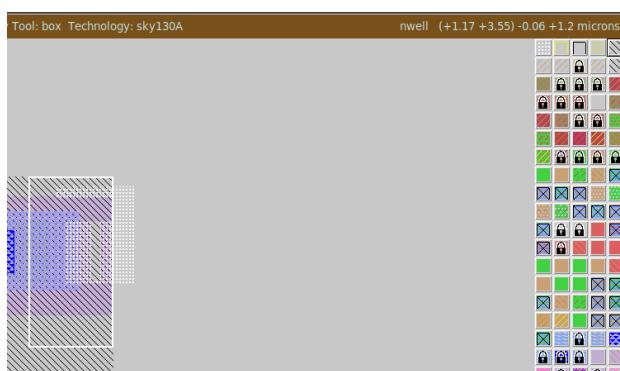
Go to DRC>DRC find next error to see the DRC errors



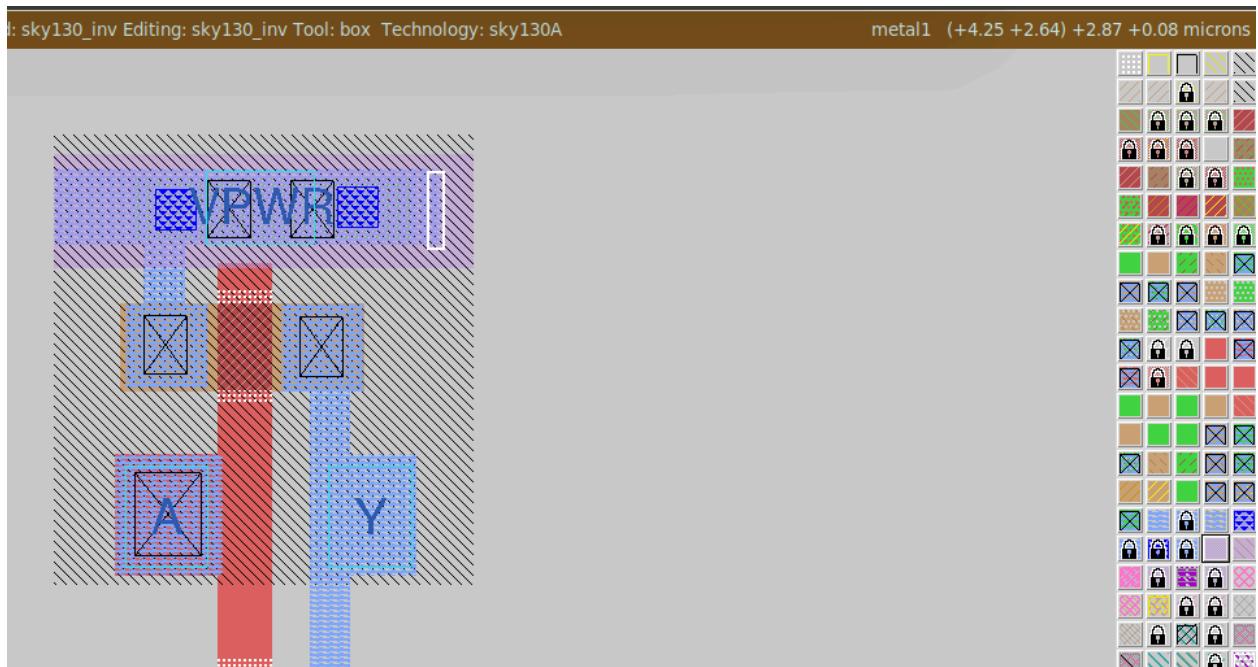
Error will be explained in the terminal

```
Error area #2:  
N-well spacing < 1.27um (nwell.2a)  
%
```

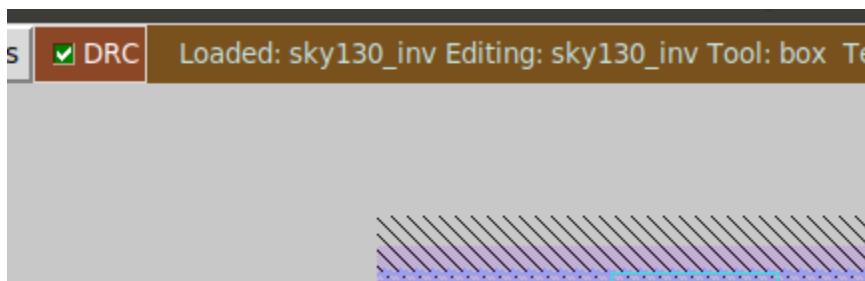
Select area with errors and click with middle mouse button on the nwell layer on the right side to fix some of the DRC errors



Then do the same thing but with the metal1 layer



No more DRC errors



Print working directory in openlane

```
% pwd
/home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
```

Extract the design

```
% extract all
Extracting sky130_inv into sky130_inv.ext
```

ls in vsdstdcelldesign to check that it has extracted successfully

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 184
-rw-rw-r-- 1 vsduser vsduser 13525 Jul 18 08:12 README.md
-rw-rw-r-- 1 vsduser vsduser 11357 Jul 18 08:12 LICENSE
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 Images
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 extras
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 libs
-rw-rw-r-- 1 vsduser vsduser 2716 Jul 18 08:12 sky130_inv.mag
-rwxr-xr-x 1 vsduser vsduser 136710 Jul 18 08:44 sky130A.tech
-rw-rw-r-- 1 vsduser vsduser 1365 Jul 21 04:34 sky130_inv.ext
```

Extract the parasitics

```
% ext2spice cthresh 0 rthresh 0
```

Extract the ext file to spice

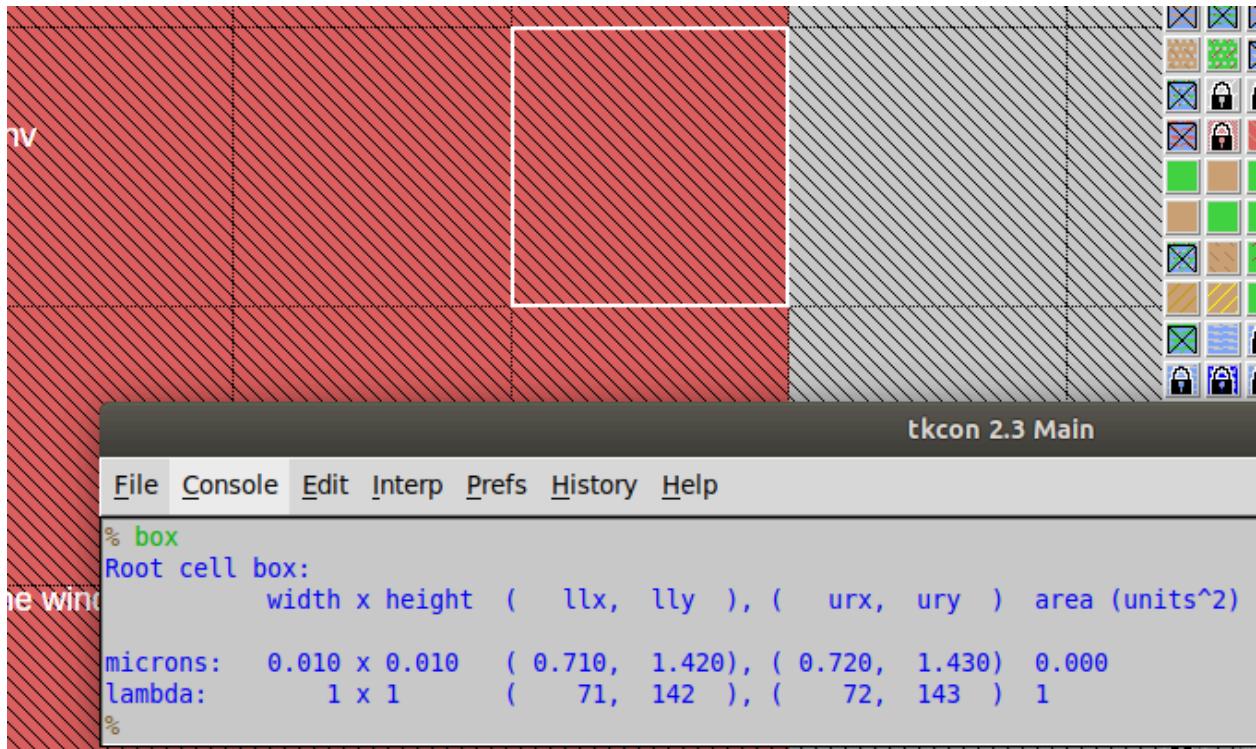
```
% ext2spice  
exttospice finished.
```

Check that spice file has been created

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openLane/vsdstdcelldesign$ ls -ltr
total 188
-rw-rw-r-- 1 vsduser vsduser 13525 Jul 18 08:12 README.md
-rw-rw-r-- 1 vsduser vsduser 11357 Jul 18 08:12 LICENSE
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 Images
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 extras
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 libs
-rw-rw-r-- 1 vsduser vsduser 2716 Jul 18 08:12 sky130_inv.mag
-rwxr-xr-x 1 vsduser vsduser 136710 Jul 18 08:44 sky130A.tech
-rw-rw-r-- 1 vsduser vsduser 1365 Jul 21 04:34 sky130_inv.ext
-rw-rw-r-- 1 vsduser vsduser 404 Jul 21 04:42 sky130_inv.spice
```

Open spice file

Select 1 box and check its dimensions



Edit the scale to 0.01 microns

```
.option scale=0.01u
```

Include PMOS and NMOS lib files; comment out .ends; define VDD, VSS, Va; do analysis

```
* SPICE3 file created from sky130_inv.ext - technology: sky130A

.option scale=0.01u
.include ./libs/pshort.lib
.include ./libs/nshort.lib

.subckt sky130_inv A Y VPWR VGND
X0 Y A VGND VGND sky130_fd_pr_nfet_01v8 ad=1.44n pd=0.152m as=1.37n ps=0.148m w=35 l=23
X1 Y A VPWR VPWR sky130_fd_pr_pfet_01v8 ad=1.44n pd=0.152m as=1.52n ps=0.156m w=37 l=23
VDD VPWR 0 3.3V
VSS VGND 0 0V
Va A VGND PULSE(0V 3.3V 0 0.1ns 0.1ns 2ns 4ns)
C0 VPWR Y 0.117f
C1 A Y 0.0754f
C2 A VPWR 0.0774f
C3 Y VGND 0.279f
C4 A VGND 0.45f
C5 VPWR VGND 0.781f
//.ends
.tran 1n 20n

.control
run
.endc
.end
```

Exit vim

```
:wq! [
```

to exit and save

cd to libs and view pshort.lib

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cd libs/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign/libs$ less pshort.lib
```

```
* Copyright 2020 The SkyWater PDK Authors
*
* Licensed under the Apache License, Version 2.0 (the "License");
* you may not use this file except in compliance with the License.
* You may obtain a copy of the License at
*
*     https://www.apache.org/licenses/LICENSE-2.0
*
* Unless required by applicable law or agreed to in writing, software
* distributed under the License is distributed on an "AS IS" BASIS,
* WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
* See the License for the specific language governing permissions and
* limitations under the License.
*
* SPDX-License-Identifier: Apache-2.0
*Auto-converted ..spectremodels/pshort.pm3 by model_spectre_mismatchmaker.rb
// converted from amsmodels_88x/pshort.pm3
/*simulator lang=spectre
// BSIMTran Version 0.1.24, Created on 4-26-2002
// Username: hal
// Command Line: /home/hai/config/cydir/bin/lnx86/bsimtran pmos_bsim4.rf pmos -p -npshort pshort_modelnamechanged.pm3 pshort-overlap.pm
// DIV1.PMD pdcv1.pm pshort_bsimtranoutput.pm3
// Working Directory: /home/hai/models/s8/s8tee/models.3.1/pshort/combined
// Time: Sun Jun 10 17:40:56 2007
// Rule File: pmos_bsim4.rf
// Output File: pshort_bsimtranoutput.pm3
// Input Files:
// (1) pshort_modelnamechanged.pm3
// (2) pshort-overlap.pm
// (3) DIV1.PMD
// (4) pdcv1.pm
// BSIM3.V3 PMOS Model
// spectre mismatch params here
//parameters pshort_lint_slope_spectre = 0.0
//parameters pshort_wint_slope_spectre = 0.0
pshort.lib]
```

Actual file starts here

```
.model pshort_model.0 pmos (
```

Open the spice file with vim again and make some edits

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ vim sky130_inv.spice
X0 Y A VGND VGND nshort_model.0 sky130_fd_pr_nfet_01v8 ad=1.44n pd=0.152m as=1.37n ps=0.148m w=35 l=23
X1 Y A VPWR VPWR pshort_model.0 sky130_fd_pr_pfet_01v8 ad=1.44n pd=0.152m as=1.52n ps=0.156m w=37 l=23
```

Exit vim

```
:wq! [
```

Open spice

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ngspice sky130_inv.spice
*****
** ngspice-27 : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Tue Dec 26 17:10:20 UTC 2017
****

Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a

Scale set
ngspice 1 -> [
```

Plot output and time

```
ngspice 1 -> plot y vs time a
```

```

vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ngspice sky130_inv.spice
*****
** ngspice-27 : Circuit level simulation program
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Please get your ngspice manual from http://ngspice.sourceforge.net/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Tue Dec 26 17:10:20 UTC 2017
*****


Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a

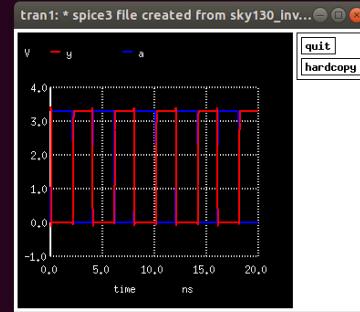
Scale set
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000

Warning: va: no DC value, transient time 0 value used

Initial Transient Solution
-----
Node          Voltage
-----
y            3.3
a            0
vgnd         0
vpwr         3.3
va#branch    0
vss#branch   3.32336e-12
vdd#branch   -3.32337e-12

No. of Data Rows : 147
ngspice 1 -> plot y vs time a
ngspice 1 -> []

```



Open the spice file again and change C3 to 2fF

```

* SPICE3 file created from sky130_inv.ext - technology: sky130A

.option scale=0.01u
.include ./libs/pshort.lib
.include ./libs/nshort.lib

//.subckt sky130_inv A Y VPWR VGND
M1001 Y A VGND VGND nshort_model.0 ad=1.44n pd=0.152m as=1.37n ps=0.148m w=35 l=23
M1000 Y A VPWR VPWR pshort_model.0 ad=1.44n pd=0.152m as=1.52n ps=0.156m w=37 l=23
VDD VPWR 0 3.3V
VSS VGND 0 0V
Va A VGND PULSE(0V 3.3V 0 0.1ns 0.1ns 2ns 4ns)
C0 VPWR Y 0.117f
C1 A Y 0.0754f
C2 A VPWR 0.0774f
C3 Y VGND 2fF
C4 A VGND 0.45f
C5 VPWR VGND 0.781f
//.ends
.tran 1n 20n

.control
run
.endc
.end
"sky130_inv.spice" 25L, 565C

```

Plot it again

```
Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a
```

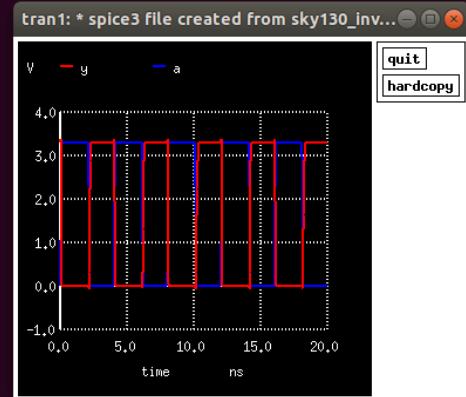
```
Scale set
```

```
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
```

```
Warning: va: no DC value, transient time 0 value used
```

```
Initial Transient Solution
```

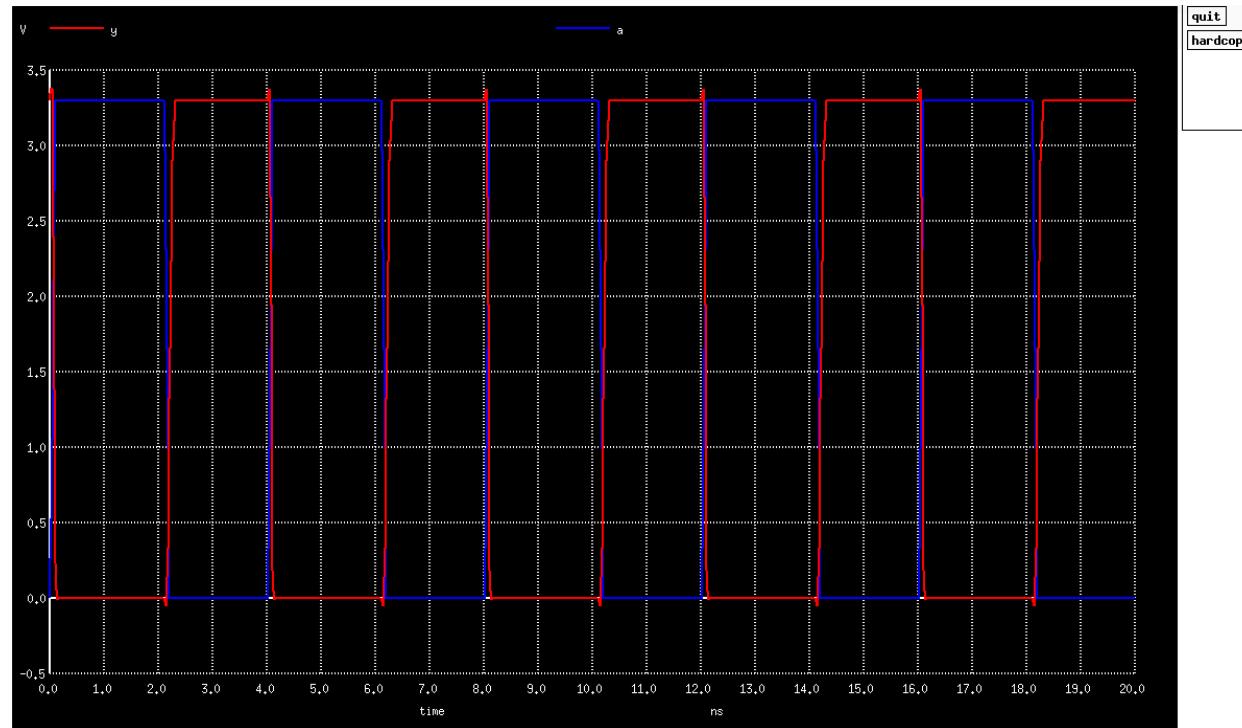
Node	Voltage
y	3.3
a	0
vgnd	0
vpower	3.3
va#branch	0
vss#branch	3.32336e-12
vdd#branch	-3.32337e-12



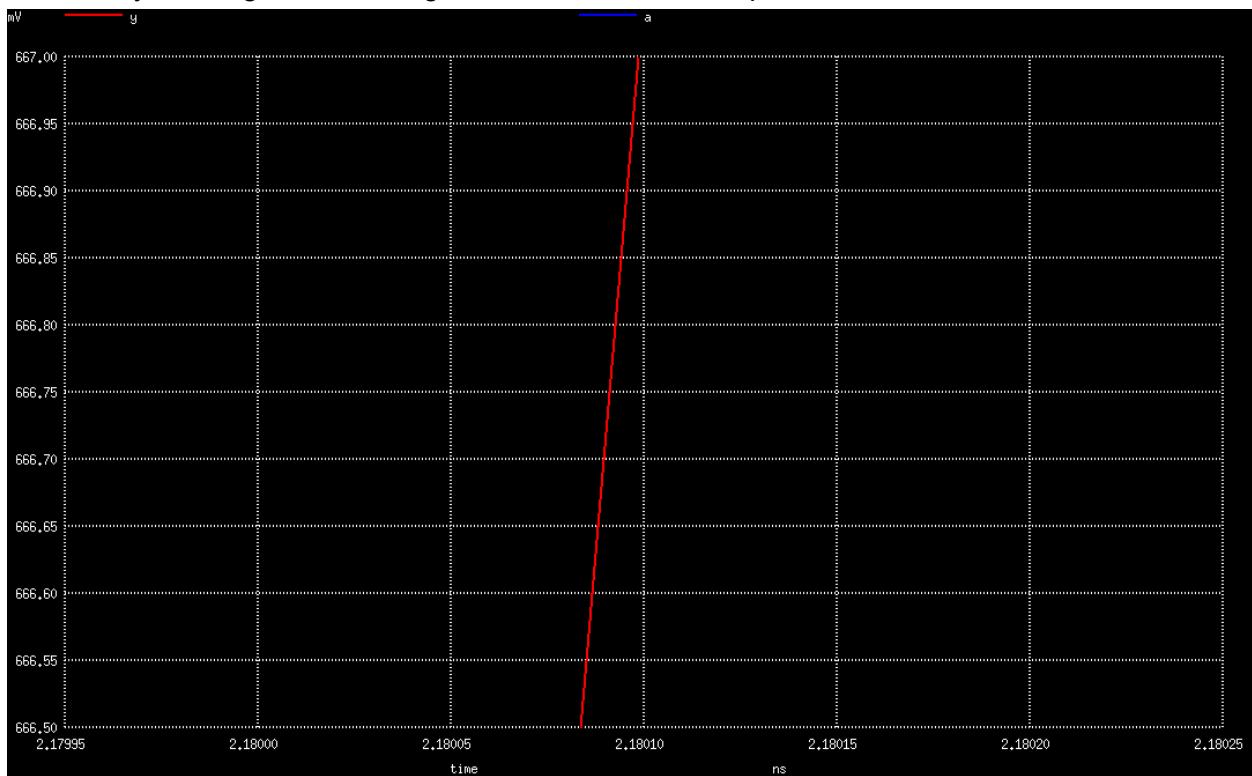
```
No. of Data Rows : 160
```

```
ngspice 1 -> plot y vs time a
```

```
ngspice 1 -> 
```



Zoom in by drawing a box with right click and click on the point where it is 0.666



See the coordinates in the terminal and calculate rise time from difference in x-value of these 2 points

$x_0 = 2.18009e-09, y_0 = 0.6666$

$x_0 = 2.23949e-09, y_0 = 2.6399$

Difference between these two points is propagation delay

$x_0 = 2.20678e-09, y_0 = 1.65$

$x_0 = 2.14983e-09, y_0 = 1.65008$

Sky130 Tech File Labs

Download the files

```
vsduser@vsdsquadron:~$ wget http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
--2025-07-21 09:05:15-- http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz
Resolving opencircuitdesign.com (opencircuitdesign.com)... 69.251.37.208
Connecting to opencircuitdesign.com (opencircuitdesign.com)|69.251.37.208|:80... connected.
HTTP request sent, awaiting response... 200 OK
Length: 41651 (41K) [application/x-gzip]
Saving to: 'drc_tests.tgz'

drc_tests.tgz          100%[=====] 40.67K   236KB/s    in 0.2s

2025-07-21 09:05:21 (236 KB/s) - 'drc_tests.tgz' saved [41651/41651]
```

```
vsduser@vsdsquadron:~$ tar xfz drc_tests.tgz
```

cd to drc_tests and ls

```
vsduser@vsdsquadron:~$ cd drc_tests
vsduser@vsdsquadron:~/drc_tests$ ls -al
total 276
drwxrwxr-x  2 vsduser vsduser  4096 Sep 16 2020 .
drwxr-xr-x 20 vsduser vsduser  4096 Jul 21 09:07 ..
-rw-rw-r--  1 vsduser vsduser  3178 Sep 15 2020 capm.mag
-rw-rw-r--  1 vsduser vsduser 3610 Sep 16 2020 difftap.mag
-rw-rw-r--  1 vsduser vsduser 1535 Sep 16 2020 dnwell.mag
-rw-rw-r--  1 vsduser vsduser 1684 Sep 15 2020 hvtp.mag
-rw-rw-r--  1 vsduser vsduser  897 Sep 15 2020 hvtr.mag
-rw-rw-r--  1 vsduser vsduser 11586 Sep 15 2020 licon.mag
-rw-rw-r--  1 vsduser vsduser 1480 Sep 15 2020 li.mag
-rw-rw-r--  1 vsduser vsduser 4648 Sep 15 2020 lvtn.mag
-rw-rw-r--  1 vsduser vsduser 2565 Sep 15 2020 .magicrc
-rw-rw-r--  1 vsduser vsduser 1198 Sep 15 2020 mcon.mag
-rw-rw-r--  1 vsduser vsduser 2103 Sep 15 2020 met1.mag
-rw-rw-r--  1 vsduser vsduser 1799 Sep 15 2020 met2.mag
-rw-rw-r--  1 vsduser vsduser 1500 Sep 16 2020 met3.mag
-rw-rw-r--  1 vsduser vsduser 1114 Sep 16 2020 met4.mag
-rw-rw-r--  1 vsduser vsduser  757 Sep 15 2020 met5.mag
-rw-rw-r--  1 vsduser vsduser 1948 Sep 15 2020 npc.mag
-rw-rw-r--  1 vsduser vsduser 2497 Sep 15 2020 nsd.mag
-rw-rw-r--  1 vsduser vsduser 1351 Sep 16 2020 nwell.mag
-rw-rw-r--  1 vsduser vsduser  536 Sep 15 2020 pad.mag
-rw-rw-r--  1 vsduser vsduser 5588 Sep 16 2020 poly.mag
-rw-rw-r--  1 vsduser vsduser 2565 Sep 15 2020 psd.mag
-rw-rw-r--  1 vsduser vsduser 3025 Sep 15 2020 rpm.mag
-rw-rw-r--  1 vsduser vsduser 135962 Sep 16 2020 sky130A.tech
-rw-rw-r--  1 vsduser vsduser 2476 Sep 16 2020 tunn.mag
-rw-rw-r--  1 vsduser vsduser 4114 Sep 16 2020 varac.mag
-rw-rw-r--  1 vsduser vsduser 1271 Sep 15 2020 via2.mag
-rw-rw-r--  1 vsduser vsduser 1267 Sep 15 2020 via3.mag
-rw-rw-r--  1 vsduser vsduser  966 Sep 15 2020 via4.mag
-rw-rw-r--  1 vsduser vsduser  955 Sep 15 2020 via.mag
```

Open .magicrc file in vim

```
vsduser@vsdsquadron:~/drc_tests$ vi .magicrc
```

```
puts stdout "Sourcing design .magicrc for technology sky130A ..."

# Put grid on 0.005 pitch. This is important, as some commands don't
# rescale the grid automatically (such as lef read?).

set scalefac [tech lambda]
if {[llength $scalefac] < 2} {
    scalegrid 1 2
}

# drc off
drc euclidean on

# Allow override of PDK path from environment variable PDKPATH
if {[catch {set PDKPATH $env(PDKPATH)}]} {
    set PDKPATH "~/cad/pdk/sky130A"
}

# loading technology
# tech load $PDKPATH/libs.tech/magic/sky130A.tech
tech load sky130A.tech

# load device generator
# source $PDKPATH/libs.tech/magic/sky130A.tcl

# load bind keys (optional)
# source $PDKPATH/libs.tech/magic/sky130A-BindKeys

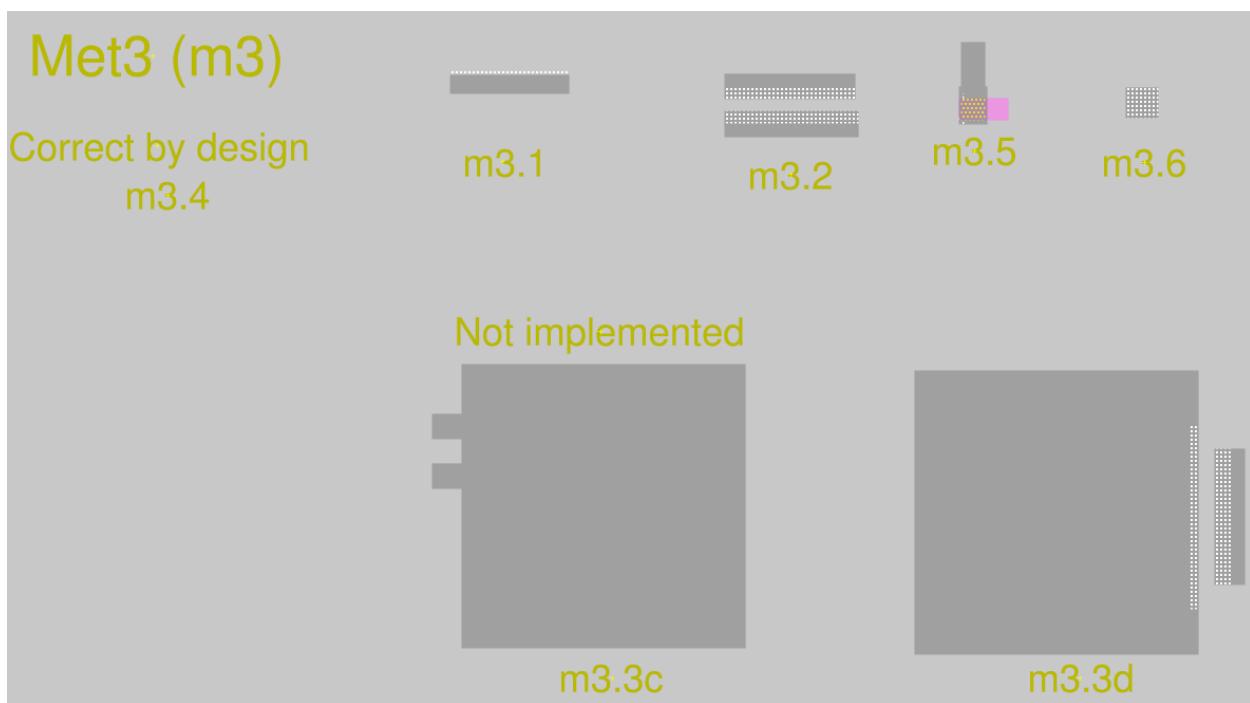
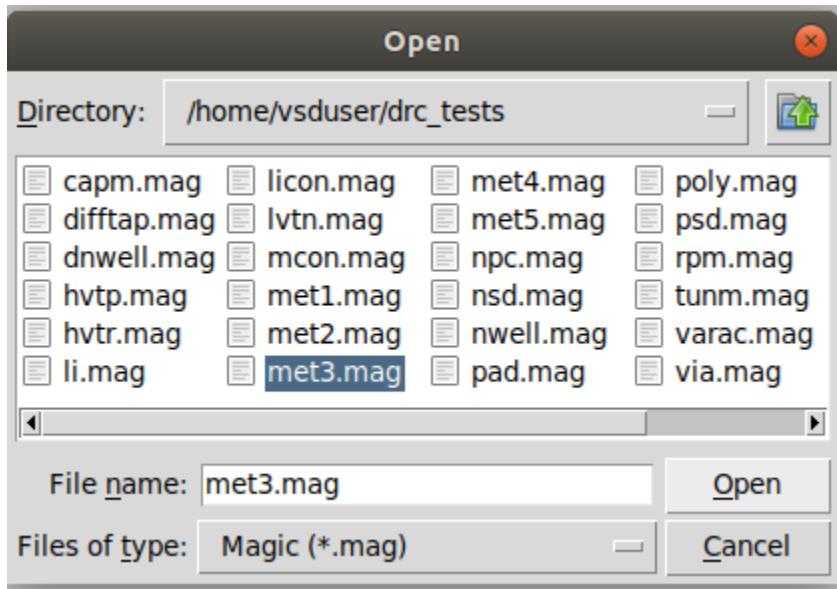
# set units to lambda grid
snap lambda

# set sky130 standard power, ground, and substrate names
set VDD VPWR
set GND VGND
set SUB VSUBS
".magicrc" 74L, 256SC
```

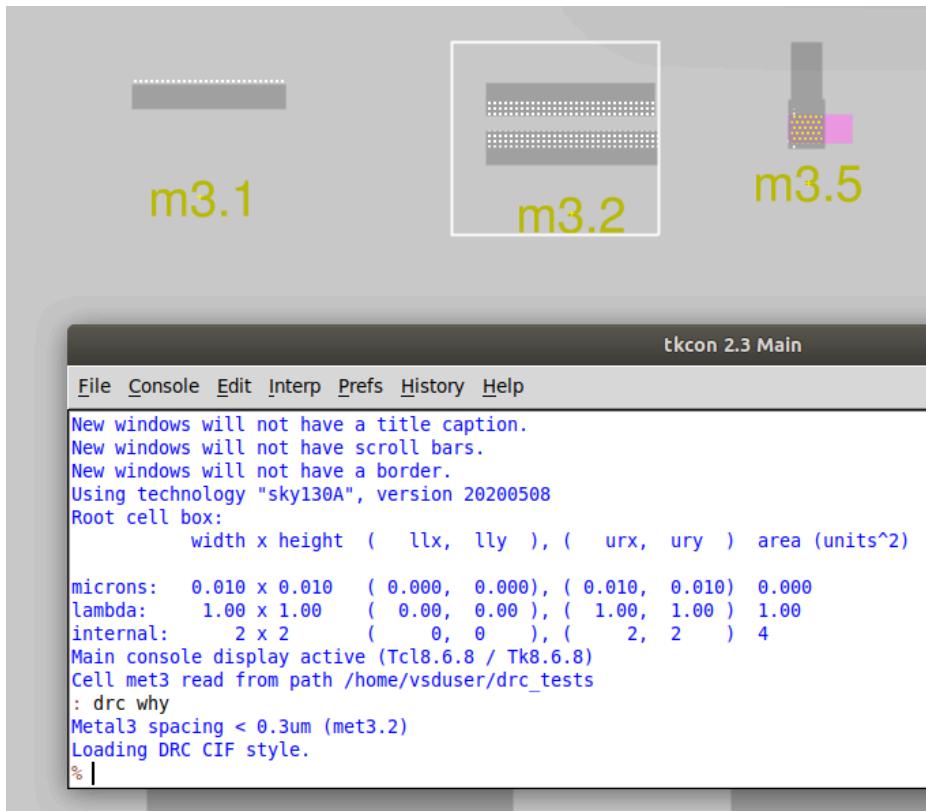
Open magic

```
vsduser@vsdsquadron:~/drc_tests$ magic -d XR
```

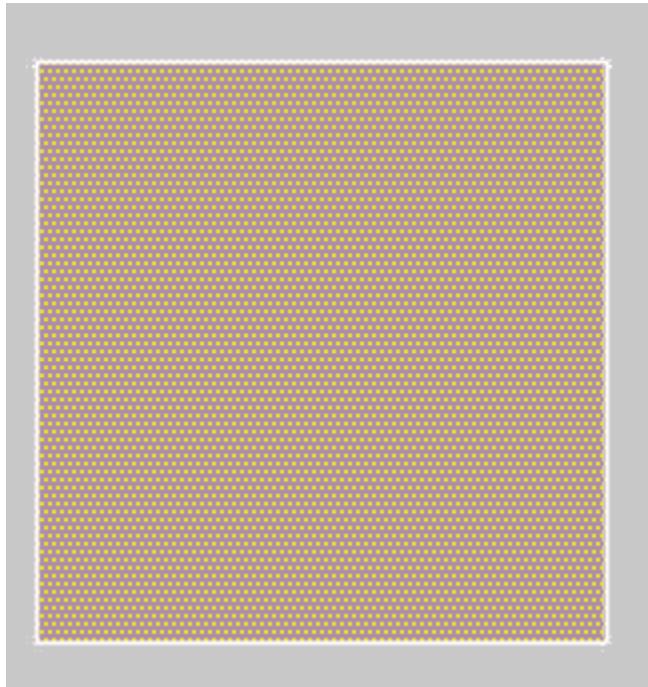
Open met3.mag file in magic



Selecting something and typing drc why in the console will give you more info on the error

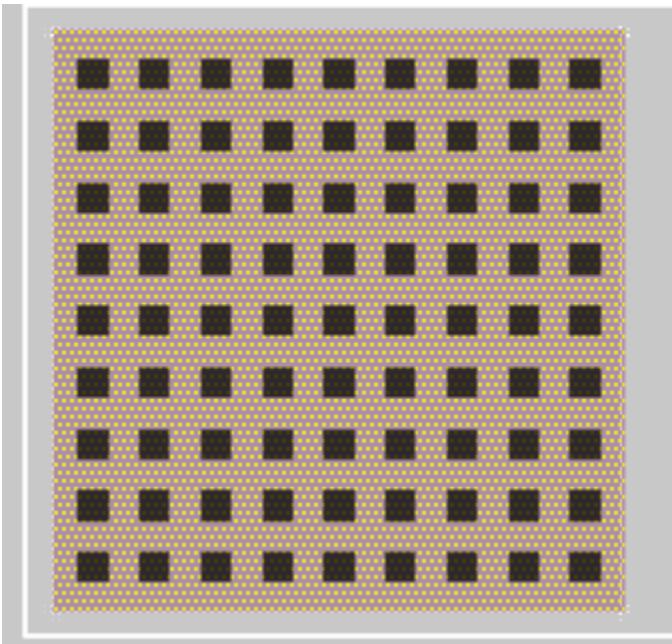


Make an m3contact by selecting an area and middle clicking on the m3contact on the side



To show contacts, keep the box selected and type:

```
% cif see VIA2
```

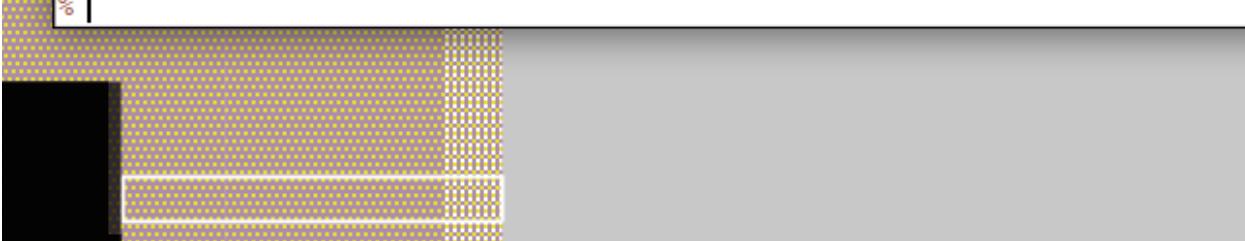


To keep your cursor on the grid:

```
% snap int
```

Type box to measure distance

```
% box
Root cell box:
    width x height  ( llx, lly ), ( urx, ury ) area (units^2)
microns:  0.165 x 0.020  ( 5.445, 5.465), ( 5.610, 5.485)  0.003
lambda:   16.50 x 2.00   ( 544.50, 546.50), ( 561.00, 548.50) 33.00
internal: 33 x 4        ( 1089, 1093 ), ( 1122, 1097 ) 132
%
```



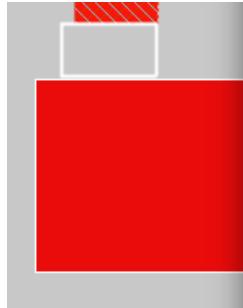
Load the poly

```
% load poly
Cell poly read from current working directory
```

Select a part and type what in the console to see what layer it is

```
% what  
Selected mask layers:  
    npolyres ( Topmost cell in the window )
```

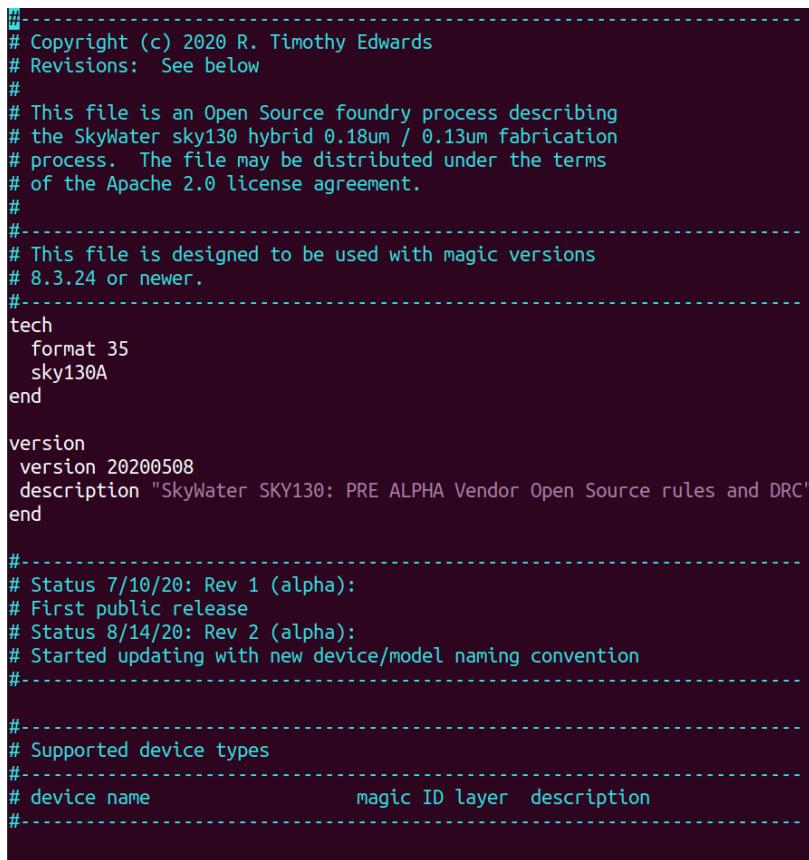
Measure the distance between the npolyres and the poly with box



```
npolyres ( Topmost cell in the window )  
: what  
Selected mask layers:  
    poly      ( Topmost cell in the window )  
% box  
Root cell box:  
    width x height ( llx, lly ), ( urx, ury ) area (units^2)  
  
microns: 0.365 x 0.205 ( 17.815, 4.280), ( 18.180, 4.485) 0.075  
lambda: 36.50 x 20.50 ( 1781.50, 428.00), ( 1818.00, 448.50) 748.25  
internal: 73 x 41 ( 3563, 856 ), ( 3636, 897 ) 2993
```

Open the sky130A.tech file

```
vsduser@vsdsquadron:~/drc_tests$ vi sky130A.tech
```



```
-----  
# Copyright (c) 2020 R. Timothy Edwards  
# Revisions: See below  
#  
# This file is an Open Source foundry process describing  
# the SkyWater sky130 hybrid 0.18um / 0.13um fabrication  
# process. The file may be distributed under the terms  
# of the Apache 2.0 license agreement.  
#-----  
# This file is designed to be used with magic versions  
# 8.3.24 or newer.  
#-----  
tech  
    format 35  
    sky130A  
end  
  
version  
    version 20200508  
    description "SkyWater SKY130: PRE ALPHA Vendor Open Source rules and DRC"  
end  
  
#-----  
# Status 7/10/20: Rev 1 (alpha):  
# First public release  
# Status 8/14/20: Rev 2 (alpha):  
# Started updating with new device/model naming convention  
#-----  
#-----  
# Supported device types  
#-----  
# device name          magic ID layer  description  
#-----
```

Add these lines into the file after the second instance of poly.9. You can use /poly.9 to find where poly.9 occurs in the file

```
spacing xhrpoly,uhrpoly,xpc *poly.480 touching_illegal \  
    "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
```

Search for aliases with /aliases and identify the allpolynonres category

```
allpolynonres *poly,allfets,xpc
```

Revise the line we just changed with allpolynonres since it fits our needs better

```
spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
    "xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
```

Add in the highlighted lines where the other instance of poly.9 appears

```
width allpoly 150 "poly.width < %d (poly.1a)"
spacing allpoly allpoly 210 touching_ok "poly.spacing < %d (poly.2)"
spacing allpolynonfet alldiffvnonfet 75 corner_ok allfets \
    "poly.spacing to Diffusion < %d (poly.4a)"
spacing npres *nsd 480 touching_illegal \
    "poly.resistor spacing to N-tap < %d (poly.9)"
spacing npres allpolynonres 480 touching_illegal \
    "poly.resistor spacing to N-tap < %d (poly.9)"
overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of n"
overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of n"
overhang *mvndiff,mvrndiff mvnfet,mvnnfet 250 \
    "N-Diffusion overhang of nmos < %d (poly.7)"
overhang *pdiff,rpdiff pfet,scpfet,ppu 250 "P-Diffusion overhang of pmos <
overhang *mvpdiff,mvrpdiff mvpfet 250 "P-Diffusion overhang of pmos < %d (p
overhang *poly allfets 130 "poly.overhang of transistor < %d (poly.8)"
rect_only allfets "No bends in transistors (poly.11)"
rect_only xhrpoly,uhrpoly "No bends in poly resistors (poly.11)"
extend xpc/a xhrpoly,uhrpoly 2160 \
    "poly.contact extends poly resistor by < %d (licon.1c + li.5)"
spacing xhrpoly,uhrpoly xhrpoly,uhrpoly 1240 touching_illegal \
    "Distance between precision resistors < %d (rpm.2 + 2 * rpm.3)"
```

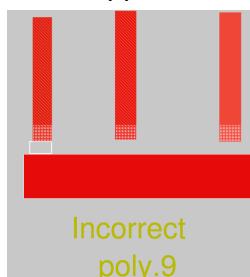
Load the tech file in magic

```
% tech load sky130A.tech
```

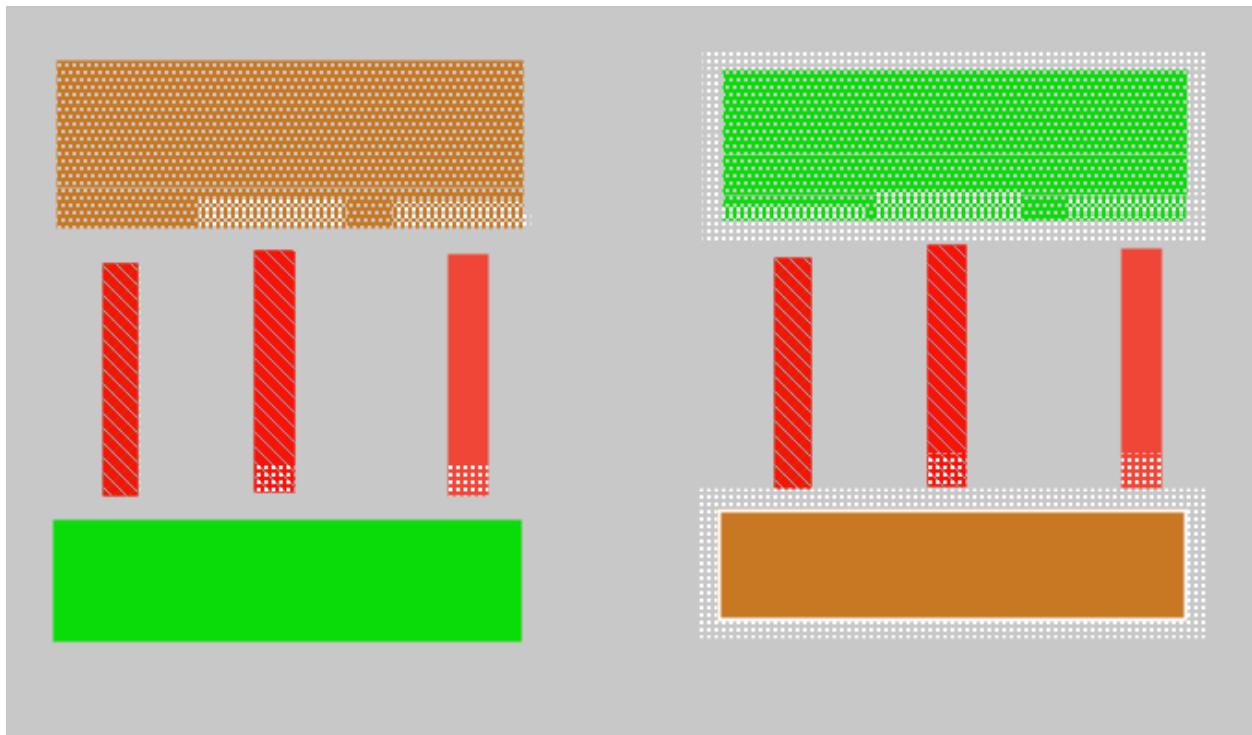
Have the DRC check everything again

```
% drc check
Loading DRC CIF style.
```

Errors appear now



Make 2 copies of the 3 resistors and add ndiff under one and pdiff under another. Then add rectangles of the following materials (clockwise starting from top left): psubstratediff, nsubstratendiff, pdiffusion, ndiffusion



Edit this part of the sky130.tech file to show the DRC errors

```
#-----
# POLY
#-----

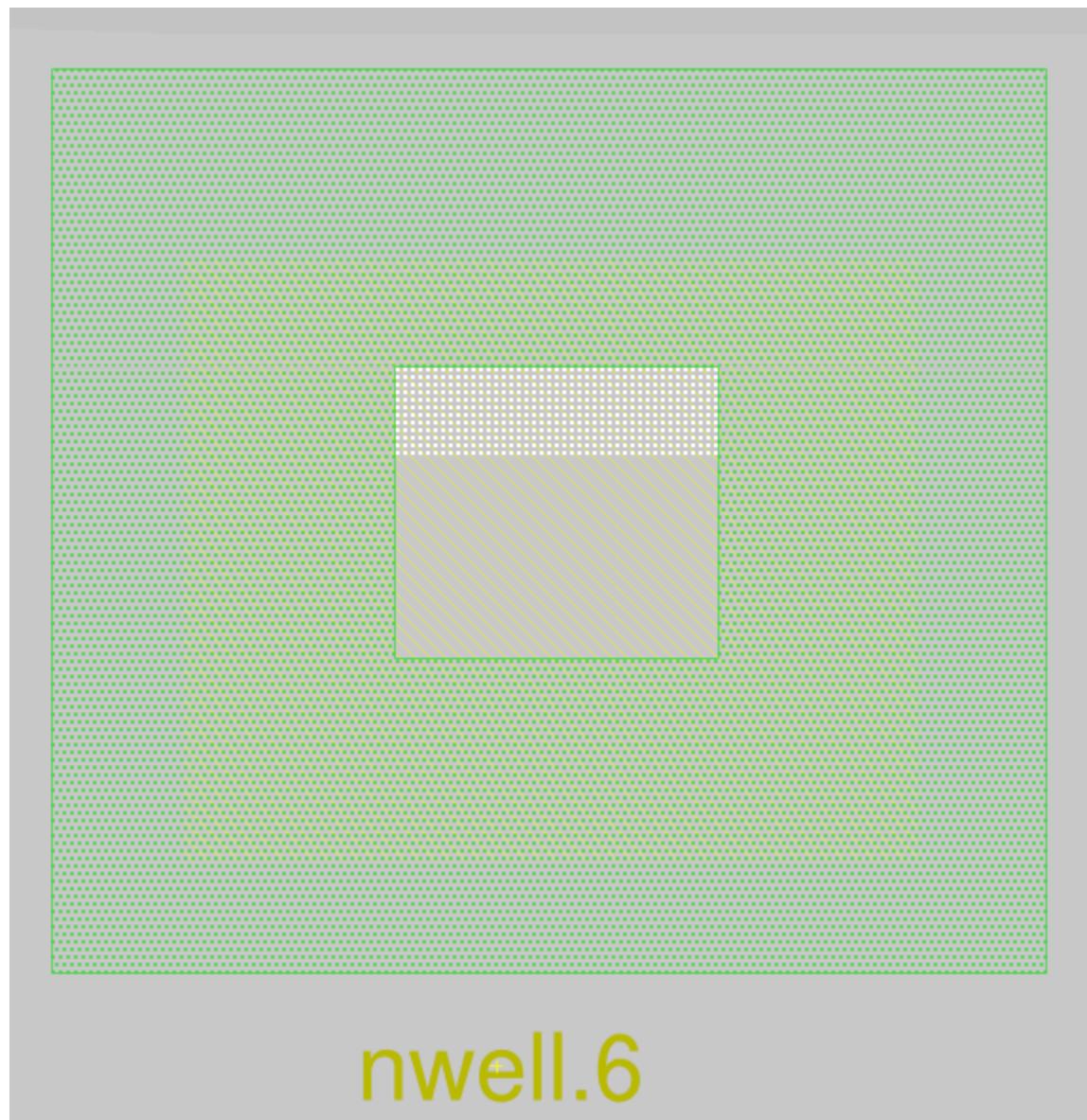
width allpoly 150 "poly.width < %d (poly.1a)"
spacing allpoly allpoly 210 touching_ok "poly.spacing < %d (poly.2)"
spacing allpolynonfet alldiffvnonfet 75 corner_ok allfets \
    "poly.spacing to Diffusion < %d (poly.4a)"
spacing npres alldiff 480 touching_illegal \
    "poly.resistor spacing to N-tap < %d (poly.9)"
spacing npres allpolynonres 480 touching_illegal \
    "poly.resistor spacing to N-tap < %d (poly.9)"
overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of pmos"
overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of nmos"
overhang *mvndiff,mvrndiff mvnfet,mvnfnfet 250 \
    "N-Diffusion overhang of nmos < %d (poly.7)"
overhang *pdiff,rpdiff pfet,scpfet,ppu 250 "P-Diffusion overhang of pmos"
overhang *mvpdiff,mvrpdiff mypfet 250 "P-Diffusion overhang of pmos < %d (poly.7)"
overhang *poly allfets 130 "poly.overhang of transistor < %d (poly.8)"
rect_only allfets "No bends in transistors (poly.11)"
rect_only xhrpoly,uhrpoly "No bends in poly resistors (poly.11)"
extend xpc/a xhrpoly,uhrpoly 2160 \
    "poly.contact extends poly resistor by < %d (lcon.1c + li.5)"
spacing xhrpoly,uhrpoly xhrpoly,uhrpoly 1240 touching_illegal \
    "Distance between precision resistors < %d (rpn.2 + 2 * rpn.3)"
```

Then do drc check

```
% tech load sky130A.tech
Input style sky130: scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
    mvpbase nnmos obsactive mvobactive obslil obsli1c obsml obsm2 obsm3 obsm4 obsm5 obsmrnl fillblock comment o
t res0p35 res0p69 res1p41 res2p85 res5p73
Scaled tech values by 2 / 1 to match internal grid scaling
Existing layout may be invalid.
% drc check
Loading DRC CIF style.
```

Load nwell in magic

```
% load nwell
Cell nwell read from current working directory
Scaled magic input cell nwell geometry by factor of 2
```



Change output style and shrink

```
% cif ostyle drc  
CIF output style is now "drc"  
% cif see dnwell_shrink
```

Clear feed and see nwell_missing

```
% feed clear  
% cif see nwell_missing
```

Then clear again (same as above)

Add the highlighted lines in sky130A.tech

```
#-----  
# N WELL  
#-----  
  
width allnwell 840 "N-well width < %d (nwell.1)"  
spacing allnwell allnwell 1270 touching_ok "N-well spacing < %d (nwell.2a)"  
  
cifmaxwidth nwell_untapped 0 bend_illegal \  
    "Nwell missing tap (nwell.4)"
```

```
templayer nwell_missing dnwell  
grow 400  
and-not dnwell_shrink  
and-not nwell
```

```
templayer nwell_tapped  
bloat-all nsc nwell
```

```
templayer nwell_untapped nwell  
and-not nwell_tapped
```

```
# SONOS nFET devices must be in deep nwell  
templayer dnwell_missing nsonos  
and-not dnwell
```

Add variants around the previous updated lines

```
variants (full)  
cifmaxwidth nwell_untapped 0 bend_illegal \  
    "Nwell missing tap (nwell.4)"  
variants *
```

Save the file, do tech load, and drc check

```
% tech load sky130A.tech
Input style sky130: scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
    mvpbase nnmos obsactive mvobsactive obslil obslilc obsml obsm2 obsm3 obsm4 obsm5 obsmrld fillblock comment o
t res0p35 res0p69 res1p41 res2p85 res5p73
Scaled tech values by 2 / 1 to match internal grid scaling
Existing layout may be invalid.
% drc check
```

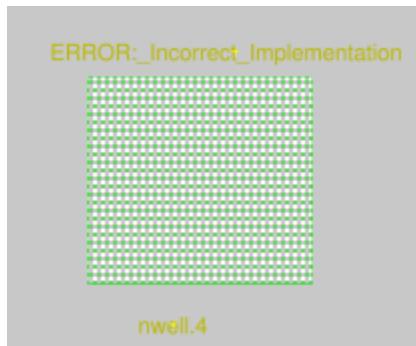
Change drc style to full

```
% drc style drc(full)
DRC style is now "drc(full)"
```

Do drc check

```
% drc check
```

Now the errors should show



Check that the rules are correct by duplicating the nwell and adding a nsubstratecontact in it, it should have no errors

