

Day 2

Print working directory and ls in openlane configurations

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/configuration$ pwd
/home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/configuration
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/configuration$ ls -ltr
total 64
-rwxr-xr-x 1 vsduser docker 1117 Jun 29 2021 synthesis.tcl
-rwxr-xr-x 1 vsduser docker 1897 Jun 29 2021 routing.tcl
-rw-r--r-- 1 vsduser docker 31784 Jun 29 2021 README.md
-rwxr-xr-x 1 vsduser docker 1288 Jun 29 2021 placement.tcl
-rwxr-xr-x 1 vsduser docker 69 Jun 29 2021 lvs.tcl
-rwxr-xr-x 1 vsduser docker 2358 Jun 29 2021 general.tcl
-rwxr-xr-x 1 vsduser docker 1527 Jun 29 2021 floorplan.tcl
-rwxr-xr-x 1 vsduser docker 808 Jun 29 2021 cts.tcl
-rwxr-xr-x 1 vsduser docker 1113 Jun 29 2021 checkers.tcl
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/configuration$
```

Open readme file

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/configuration$ less README.md
```

```
# Variables information

This page describes configuration variables and their default values.

## Required variables

| Variable | Description |
|-----|-----|
| `DESIGN_NAME` | The name of the top level module of the design |
| `VERILOG_FILES` | The path of the design's verilog files |
| `CLOCK_PERIOD` | The clock period for the design in ns |
| `CLOCK_NET` | The name of the Net input to root clock buffer used in Clock Tree Synthesis. |
| `CLOCK_PORT` | The name of the design's clock port used in Static Timing Analysis. |

## Optional variables

These variables are optional that can be specified in the design configuration file.

### Synthesis

| Variable | Description |
|-----|-----|
| `LIB_SYNTH` | The library used for synthesis by yosys. <br> (Default: `$::env(PDK_ROOT)/$::env(PDK)/libs.ref/$::env(STD_CELL_LIBRARY)/lib/sky130_fd_sc_hd_tt_025C_1v80.lib`) |
| `SYNTH_BIN` | The yosys binary used in the flow. <br> (Default: `yosys`) |
| `SYNTH_DRIVING_CELL` | The cell to drive the input ports. <br>(Default: `sky130_fd_sc_hd_inv_8`) |
| `SYNTH_DRIVING_CELL_PIN` | The name of the SYNTH_DRIVING_CELL output pin. <br>(Default: `Y`) |
| `SYNTH_CAP_LOAD` | The capacitive load on the output ports in femtofarads. <br> (Default: `17.65` ff) |
| `SYNTH_MAX_FANOUT` | The max load that the output ports can drive. <br> (Default: `5` cells) |
| `SYNTH_MAX_TRAN` | The max transition time (slew) from high to low or low to high on cell inputs in ns. Used in synthesis <br> (Default: Calculated at runtime as `10%` of the provided clock period, unless this exceeds a set DEFAULT_MAX_TRAN, in which case it will be used as is) |
| `SYNTH_STRATEGY` | Strategies for abc logic synthesis and technology mapping <br> Possible values are `DELAY/AREA 0-3/0-2`; the first part refers to the optimization target of the synthesis strategy (area vs. delay) and the second one is an index. <br> (Default: `AREA 0`) |
| `SYNTH_BUFFERING` | Enables abc cell buffering <br> Enabled = 1, Disabled = 0 <br> (Default: `1`)|
```

Open floorplan.tcl

```

vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/configuration$ less floorplan.tcl
# Copyright 2020 Efabless Corporation
#
# Licensed under the Apache License, Version 2.0 (the "License");
# you may not use this file except in compliance with the License.
# You may obtain a copy of the License at
#
#     http://www.apache.org/licenses/LICENSE-2.0
#
# Unless required by applicable law or agreed to in writing, software
# distributed under the License is distributed on an "AS IS" BASIS,
# WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
# See the License for the specific language governing permissions and
# limitations under the License.

# Floorplan defaults
set ::env(FP_IO_VMETAL) 3
set ::env(FP_IO_HMETAL) 4

set ::env(FP_SIZING) relative
set ::env(FP_CORE_UTIL) 50
set ::env(FP_CORE_MARGIN) 0
set ::env(FP_ASPECT_RATIO) 1

set ::env(FP_PDN_VOFFSET) 16.32
set ::env(FP_PDN_VPITCH) 153.6
set ::env(FP_PDN_HOFFSET) 16.65
set ::env(FP_PDN_HPITCH) 153.18

set ::env(FP_PDN_AUTO_ADJUST) 1

set ::env(FP_PDN_CORE_RING) 0
set ::env(FP_PDN_ENABLE_RAILS) 1

set ::env(FP_PDN_CHECK_NODES) 1

floorplan.tcl

```

Print working directory and ls in picorv32a

```

vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ pwd
/home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ ls -ltr
total 32
drwxr-xr-x 2 vsduser docker 4096 Jun 29 2021 src
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_ms_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_ls_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_hs_config.tcl
-rw-r--r-- 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_hdll_config.tcl
-rwxr-xr-x 1 vsduser docker 209 Jun 29 2021 sky130A_sky130_fd_sc_hd_config.tcl
-rwxr-xr-x 1 vsduser docker 444 Jun 29 2021 config.tcl
drwxr-xr-x 3 vsduser vsduser 4096 Jul 16 10:25 runs
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ 

```

Open config.tcl

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ less config.tcl
# Design
set ::env(DESIGN_NAME) "picorv32a"

set ::env(VERILOG_FILES) "./designs/picorv32a/src/picorv32a.v"
set ::env(SDC_FILE) "./designs/picorv32a/src/picorv32a.sdc"

set ::env(CLOCK_PERIOD) "5.000"
set ::env(CLOCK_PORT) "clk"

set ::env(CLOCK_NET) $::env(CLOCK_PORT)

set filename $::env(OPENLANE_ROOT)/designs/$::env(DESIGN_NAME)/$::env(PDK)_$::env(STD_CELL_LIBRARY)_config.tcl
if { [file exists $filename] == 1 } {
    source $filename
}
config.tcl (END)
```

run_floorplan

```
% run_floorplan
[INFO]: Running Floorplanning...
[INFO]: Running Initial Floorplanning...
[INFO]: current step index: 3
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd_tt_025C_1v80.lib line
31, default_operating_condition tt_025C_1v80 not found.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged_unpadded.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 440 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged_unpadded.lef
[INFO] IFP-0001 Added 238 rows of 1412 sites.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 660.685 671.405 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/16-07_04-55/reports/floorplan/3-verilog2def.die_area.rpt.
[INFO] Floorplanned on a core area of 5.52 10.88 655.04 658.24 (microns). Saving to /openLANE_flow/designs/picorv32a/runs/16-07_04-55/reports/floorplan/3-verilog2def.core_area.rpt.
[INFO]: Core area width: 649.52
[INFO]: Core area height: 647.36
[INFO]: Changing layout from 0 to /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/floorplan/3-verilog2def_openroad.def
[INFO]: Running IO Placement...
[INFO]: current step index: 4
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 440 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/floorplan/3-verilog2def_openroad.def
Notice 0: Design: picorv32a
```

Finished running floorplan

```
[WARNING PSM-0030] Vsrc location at (425.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (42  
6.600um, 103.880um).  
[WARNING PSM-0030] Vsrc location at (565.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (56  
7.000um, 103.880um).  
[WARNING PSM-0030] Vsrc location at (285.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (2  
86.200um, 103.880um).  
[WARNING PSM-0030] Vsrc location at (425.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (4  
26.600um, 103.880um).  
[WARNING PSM-0030] Vsrc location at (565.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5  
67.000um, 103.880um).  
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5  
67.000um, 257.060um).  
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.4  
00um, 410.240um).  
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (1  
45.800um, 410.240um).  
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (2  
86.200um, 410.240um).  
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (4  
26.600um, 410.240um).  
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5  
67.000um, 410.240um).  
[WARNING PSM-0030] Vsrc location at (285.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (2  
86.200um, 563.420um).  
[WARNING PSM-0030] Vsrc location at (425.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (4  
26.600um, 563.420um).  
[WARNING PSM-0030] Vsrc location at (565.520um, 570.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5  
67.000um, 563.420um).  
[INFO PSM-0031] Number of nodes on net VGND = 19223.  
[INFO PSM-0037] G matrix created sucessfully.  
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.  
[INFO] PDN generation was successful.  
[INFO] Changing layout from /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/floorplan/picorv32a.floorplan.def to /openLANE_flow desi  
gns/picorv32a/runs/16-07_04-55/tmp/floorplan/7-pdn.def  
1  
%
```

ls and identify latest generated folder

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ ls -ltr  
total 4  
drwxr-xr-x 6 vsduser vsduser 4096 Jul 17 01:15 16-07_04-55  
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$
```

Go into the folder and ls

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd 16-07_04-55/  
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55$ ls -ltr  
total 52  
-rwxr-xr-x 1 vsduser vsduser 170 Jun 28 2021 PDK_SOURCES  
drwxr-xr-x 11 vsduser vsduser 4096 Jul 16 10:25 results  
drwxr-xr-x 11 vsduser vsduser 4096 Jul 16 10:25 reports  
-rw-r--r-- 1 vsduser vsduser 15 Jul 16 10:25 OPENLANE_VERSION  
drwxr-xr-x 11 vsduser vsduser 4096 Jul 16 10:25 logs  
drwxr-xr-x 11 vsduser vsduser 4096 Jul 16 10:48 tmp  
-rw-r--r-- 1 vsduser vsduser 4047 Jul 17 01:15 cmds.log  
-rw-r--r-- 1 vsduser vsduser 21023 Jul 17 01:15 config.tcl  
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55$
```

Go into logs/floorplan and ls

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55$ cd logs/floorplan  
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/logs/floorplan$ ls -ltr  
total 40  
-rw-r--r-- 1 vsduser vsduser 1204 Jul 17 01:15 3-verilog2def.openroad.log  
-rw-r--r-- 1 vsduser vsduser 12 Jul 17 01:15 3-verilog2def_openroad_runtime.txt  
-rw-r--r-- 1 vsduser vsduser 1043 Jul 17 01:15 4-ioPlacer.log  
-rw-r--r-- 1 vsduser vsduser 12 Jul 17 01:15 4-ioPlacer_runtime.txt  
-rw-r--r-- 1 vsduser vsduser 1198 Jul 17 01:15 5-tapcell.log  
-rw-r--r-- 1 vsduser vsduser 12 Jul 17 01:15 5-tapcell_runtime.txt  
-rw-r--r-- 1 vsduser vsduser 8950 Jul 17 01:15 7-pdn.log  
-rw-r--r-- 1 vsduser vsduser 12 Jul 17 01:15 7-pdn_runtime.txt  
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/logs/floorplan$
```

Open ioPlacer.log

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/logs/floorplan$ less 4-ioPlacer.log
```

Use shift+G to go to the end of the file

```
OpenROAD 0.9.0 1415572a73
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged.lef
Notice 0:     Created 13 technology layers
Notice 0:     Created 25 technology vias
Notice 0:     Created 440 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/floorplan/3-verilog2def_openroad.def
Notice 0: Design: picorv32a
Notice 0:     Created 409 pins.
Notice 0:     Created 14876 components and 115597 component-terminals.
Notice 0:     Created 14978 nets and 56051 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/floorplan/3-verilog2def_openroad.def
#Macro blocks found: 0
Using 5u default boundaries offset
Random pin placement
RandomMode Even
(END)
```

cd back and open config.tcl

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/logs/floorplan$ cd ../..
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55$ less config.tcl
```

```
# Run configs
set ::env(PDK_ROOT) "/home/vsduser/Desktop/work/tools/openlane_working_dir/pdks"
set ::env(BASE_SDC_FILE) "/openLANE_flow/scripts/base.sdc"
set ::env(BOTTOM_MARGIN_MULT) "4"
set ::env(CARRY_SELECT_ADDER_MAP) "/home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/openlane/sky130_fd_sc_hd/csa_map.v"
set ::env(CELLS_LEF) "/openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged.lef"
set ::env(CELLS_LEF_UNPADDDED) "/openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged_unpadded.lef"
set ::env(CELL_CLK_PORT) "CLK"
set ::env(CELL_PAD) "4"
set ::env(CELL_PAD_EXCLUDE) "sky130_fd_sc_hd__tap* sky130_fd_sc_hd__decap* sky130_fd_sc_hd__fill*"
set ::env(CHECK_ASSIGN_STATEMENTS) "0"
set ::env(CHECK_UNMAPPED_CELLS) "1"
set ::env(CLK_BUFFER) "sky130_fd_sc_hd__clkbuf_4"
set ::env(CLK_BUFFER_INPUT) "A"
set ::env(CLK_BUFFER_OUTPUT) "X"
set ::env(CLOCK_BUFFER_FANOUT) "16"
set ::env(CLOCK_NET) "clk"
set ::env(CLOCK_PERIOD) "24.73"
set ::env(CLOCK_PORT) "clk"
set ::env(CLOCK_TREE_SYNTH) "1"
set ::env(CONFIGS) "/openLANE_flow/configuration/floorplan.tcl /openLANE_flow/configuration/synthesis.tcl /openLANE_flow/configuration/general.tcl /openLANE_flow/configuration/checkers.tcl /openLANE_flow/configuration/lvs.tcl /openLANE_flow/configuration/cts.tcl /openLANE_flow/configuration/routing.tcl /openLANE_flow/configuration/placement.tcl"
set ::env(CTS_CLK_BUFFER_LIST) "sky130_fd_sc_hd__clkbuf_1 sky130_fd_sc_hd__clkbuf_2 sky130_fd_sc_hd__clkbuf_4 sky130_fd_sc_hd__clkbuf_8"
set ::env(CTS_MAX_CAP) "1.53169"
set ::env(CTS_REPORT_TIMING) "1"
set ::env(CTS_ROOT_BUFFER) "sky130_fd_sc_hd__clkbuf_16"
set ::env(CTS_SINK_CLUSTERING_MAX_DIAMETER) "50"
set ::env(CTS_SINK_CLUSTERING_SIZE) "20"
set ::env(CTS_SQR_CAP) "0.258e-3"
set ::env(CTS_SQR_RES) "0.125"
set ::env(CTS_TARGET_SKW) "200"
set ::env(CTS_TECH_DIR) "N/A"
set ::env(CTS_TOLERANCE) "100"
config.tcl
```

Open sky130A_sky130_fd_sc_hd_config.tcl

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ less sky130A_sky130_fd_sc_hd_config.tcl
```

```
# SCL Configs
set ::env(GLB_RT_ADJUSTMENT) 0.1

set ::env(SYNTH_MAX_FANOUT) 6
set ::env(CLOCK_PERIOD) "24.73"
set ::env(FP_CORE_UTIL) 35
set ::env(PL_TARGET_DENSITY) [ expr ($::env(FP_CORE_UTIL)+5) / 100.0 ]

sky130A_sky130_fd_sc_hd_config.tcl (END)
```

Go to floorplan folder and ls

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ cd runs/16-07_04-55/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55$ cd results/floorplan
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/floorplan$ ls -ltr
total 2644
lrwxrwxrwx 1 vsduser vsduser    29 Jul 16 10:25 merged_unpadded.lef -> ../../tmp/merged_unpadded.lef
-rw-r--r-- 1 vsduser vsduser 2436735 Jul 17 01:15 picorv32a.floorplan.def
-rw-r--r-- 1 vsduser vsduser  266915 Jul 17 01:15 picorv32a.floorplan.def.png
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/floorplan$
```

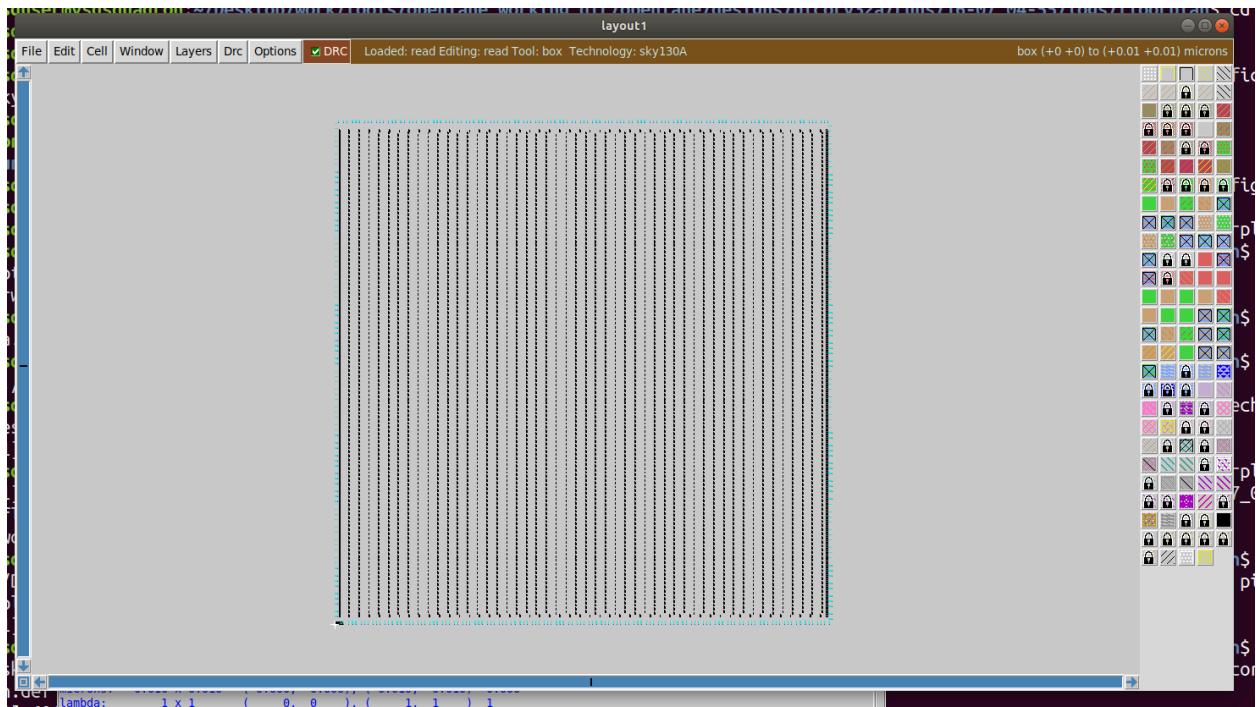
Open the def file

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openLane/designs/picorv32a/runs/16-07_04-55/results/floorplan$ less picorv3  
2a.floorplan.def
```

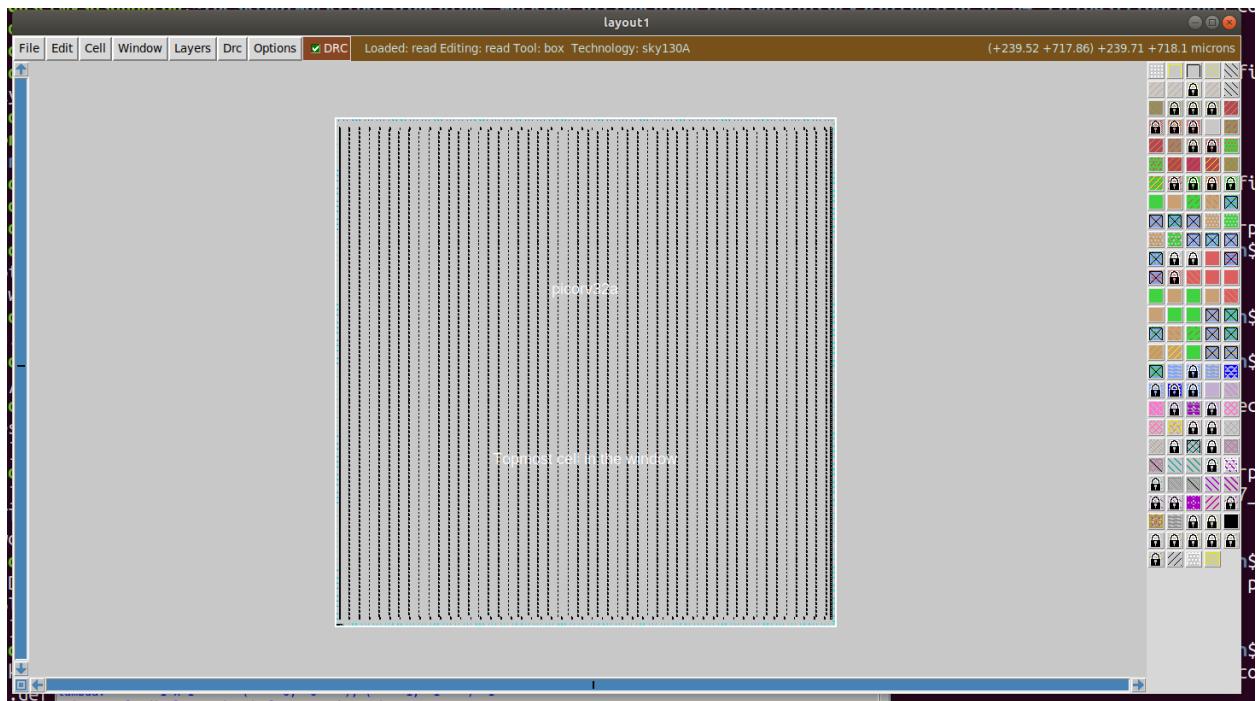
```
ROW ROW_0 unithd 5520 10880 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_1 unithd 5520 13600 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_2 unithd 5520 16320 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_3 unithd 5520 19040 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_4 unithd 5520 21760 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_5 unithd 5520 24480 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_6 unithd 5520 27200 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_7 unithd 5520 29920 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_8 unithd 5520 32640 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_9 unithd 5520 35360 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_10 unithd 5520 38080 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_11 unithd 5520 40800 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_12 unithd 5520 43520 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_13 unithd 5520 46240 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_14 unithd 5520 48960 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_15 unithd 5520 51680 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_16 unithd 5520 54400 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_17 unithd 5520 57120 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_18 unithd 5520 59840 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_19 unithd 5520 62560 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_20 unithd 5520 65280 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_21 unithd 5520 68000 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_22 unithd 5520 70720 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_23 unithd 5520 73440 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_24 unithd 5520 76160 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_25 unithd 5520 78880 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_26 unithd 5520 81600 FS DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_27 unithd 5520 84320 N DO 1412 BY 1 STEP 460 0 ;  
ROW ROW_28 unithd 5520 87040 FS DO 1412 BY 1 STEP 460 0 ;  
picorv32a.floorplan.def
```

Use magic to view floorplan

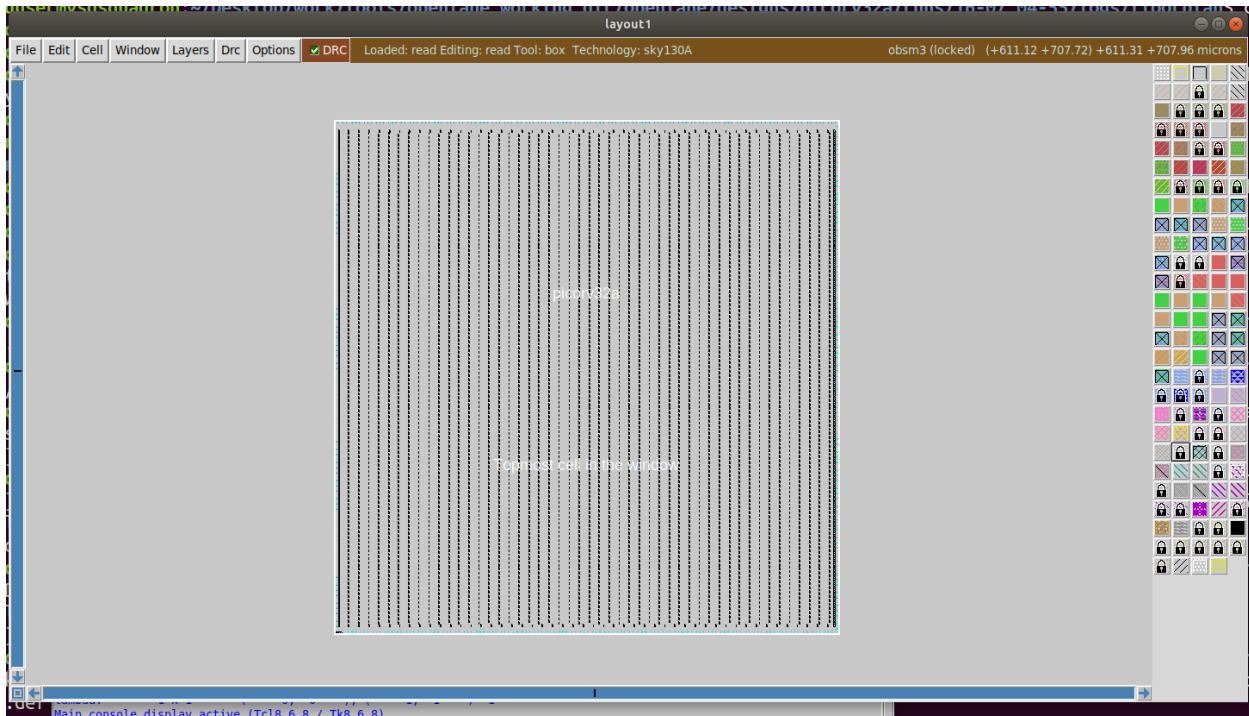
```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/floorplan$ magic -T ~/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.floorplan.def &
```



Press s to select



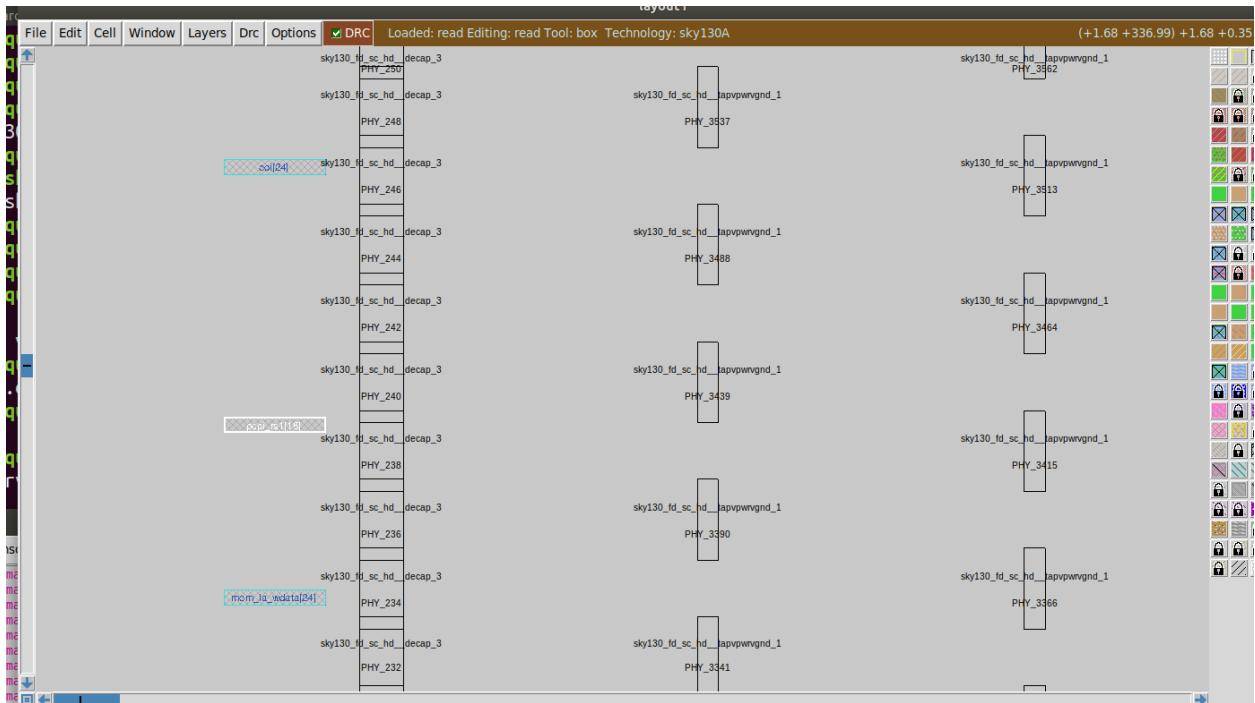
Press v to center



Press z to zoom in



Select an object by hovering over it and pressing s



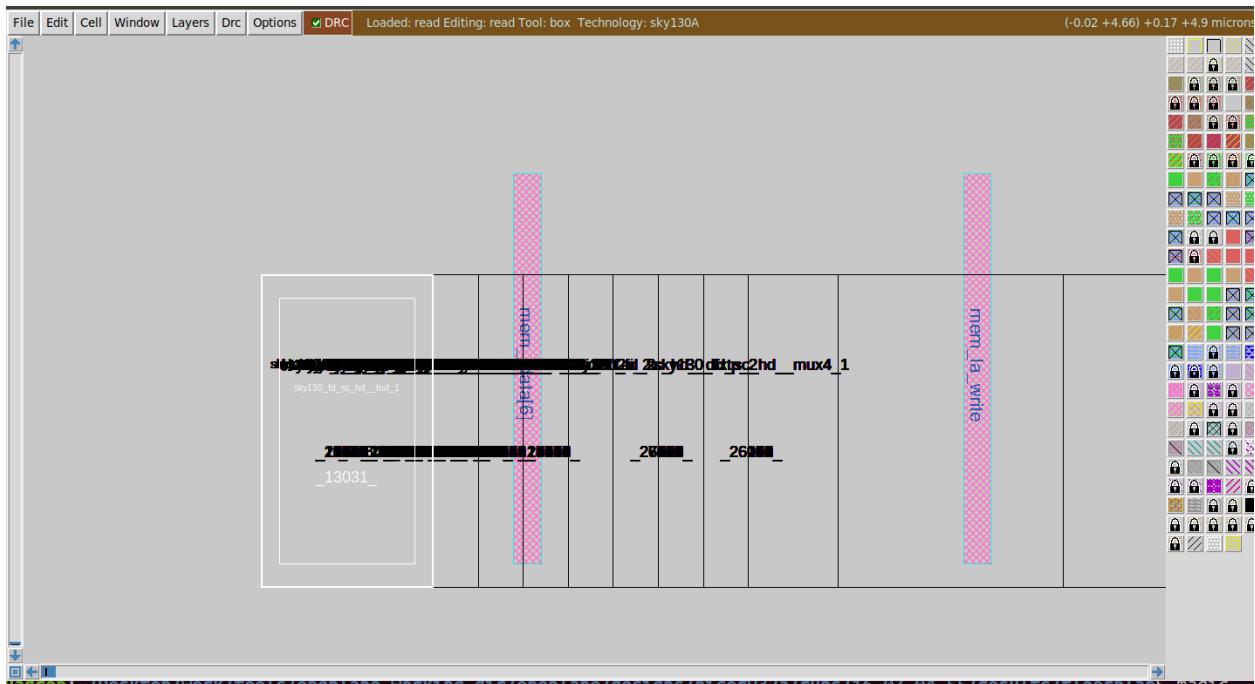
Use what to show what layer it's in

```
% what
Selected mask layers:
metal3  ( Topmost cell in the window )
Selected label(s):
"pcpi_rs1[18]" is attached to metal3 in cell def picorv32a
%
```

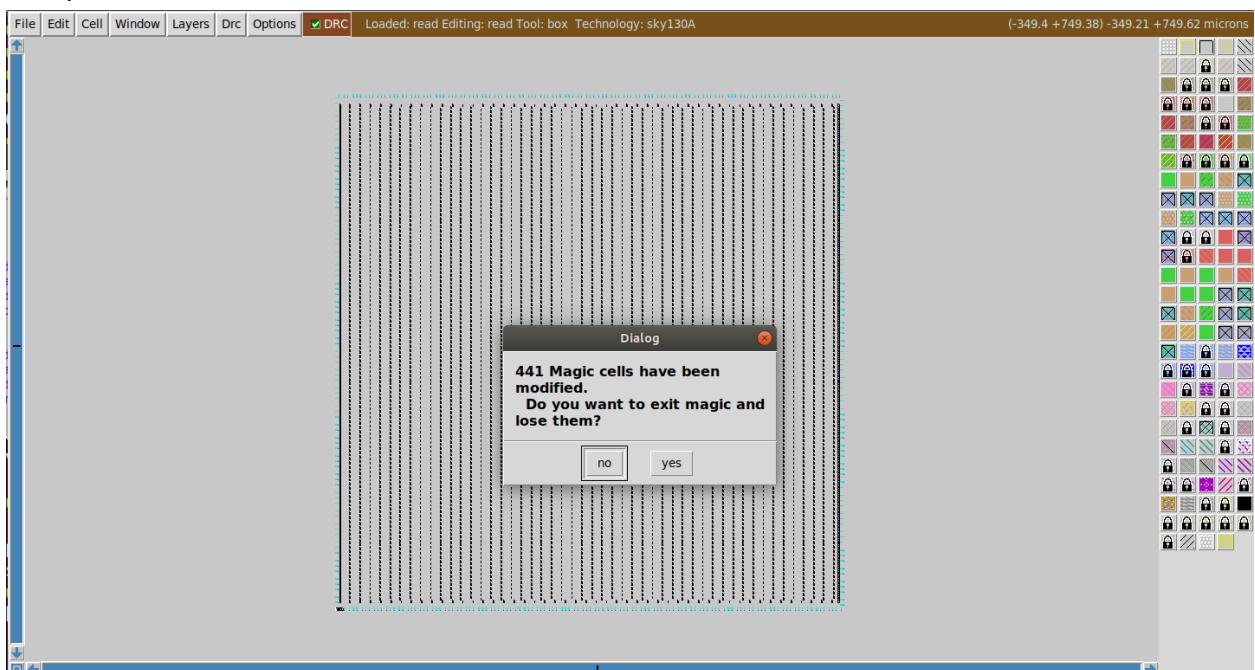
what with vertical metal

```
@vsdsq@tkcon 2.3 Main
File Console Edit Interp Prefs History Help
Unknown macro or short command: 'XK_Delete'
% what
Selected mask layers:
metal3  ( Topmost cell in the window )
Selected label(s):
"pcpi_rs1[18]" is attached to metal3 in cell def picorv32a
Created database crash recovery file /tmp//MAG6010.HE1QbA
% what
Selected mask layers:
metal2  ( Topmost cell in the window )
Selected label(s):
"mem_addr[24]" is attached to metal2 in cell def picorv32a
%
/picorv32a@vsdsq@tkcon 2.3 Main
3
@vsdsq@tkcon 2.3 Main
one
Lan/tm
: ~/De
@vsdsq@tkcon 2.3 Main
op/wor
```

Select a standard cell



file>quit to close



run_placement

run_placement

```

nets 15449
design area 420473.3 u^2
fixed area 9141.3 u^2
movable area 147800.5 u^2
utilization 36 %
utilization padded 55 %
rows 238
row height 2.7 u

Placement Analysis
-----
total displacement 0.0 u
average displacement 0.0 u
max displacement 0.0 u
original HPWL 766080.0 u
legalized HPWL 779196.5 u
delta HPWL 2 %

[INFO DPL-0020] Mirrored 6193 instances
[INFO DPL-0021] HPWL before 779196.5 u
[INFO DPL-0022] HPWL after 766080.0 u
[INFO DPL-0023] HPWL delta -1.7 %
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/placement/8-resizer.def to /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/placement/picorv32a.placement.def
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/placement/picorv32a.placement.def
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 12
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/placement/picorv32a.placement.def
[INFO] Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/klayout/sky130A.lyt
[INFO] Reading Layout file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/placement/picorv32a.placement.def
[INFO] Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/placement/picorv32a.placement.def.png'
Done
[INFO]: Screenshot taken.
%

```

Look at placement folder

```

vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/floorplan$ cd ../placement/
[2]+ Done          magic -T ~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.floorplan.def (wd: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/floorplan)
(wd now: ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/placement)
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/placement$ ls
merged_unpadded.lef picorv32a.placement.def picorv32a.placement.def.png
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/placement$ 

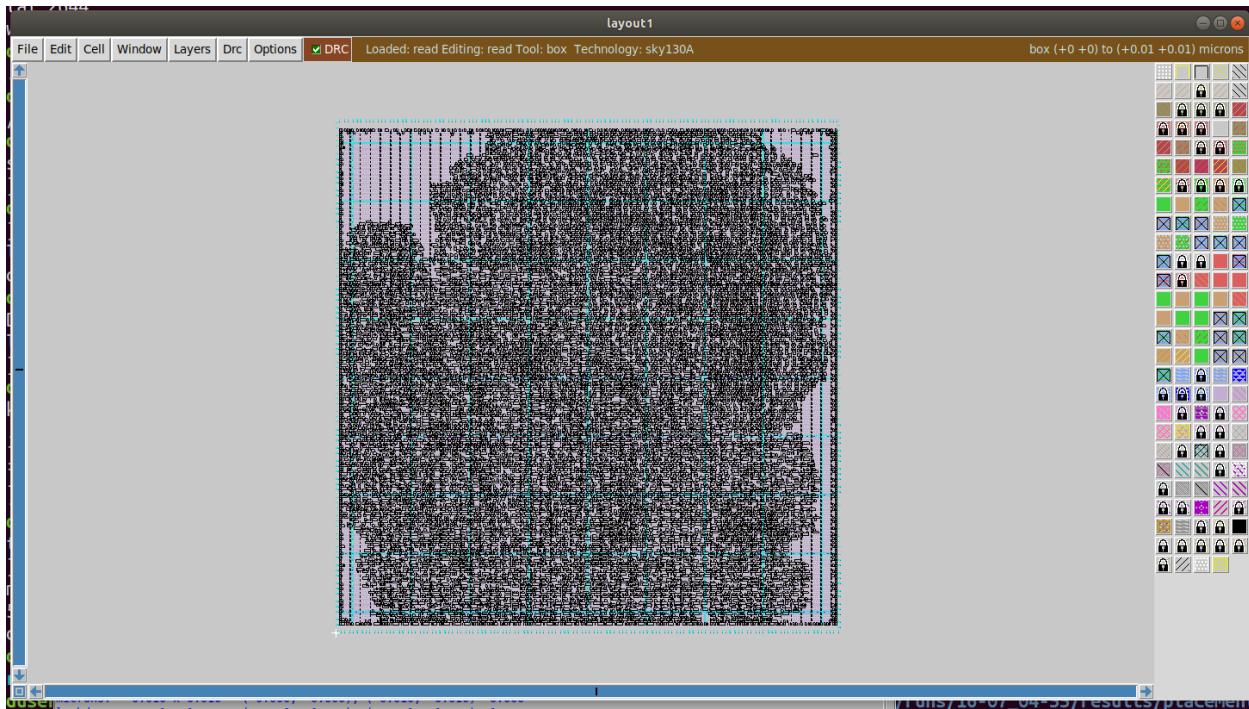
```

Use magic to look at picorv32a.placement.def

```

vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/placement$ magic -T ~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def &

```



Zoomed in

