

Day 4

Run magic

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ magic -T sky130A.tech sky130_inv.mag &|  
cd to sky130_fd_sc_hd
```

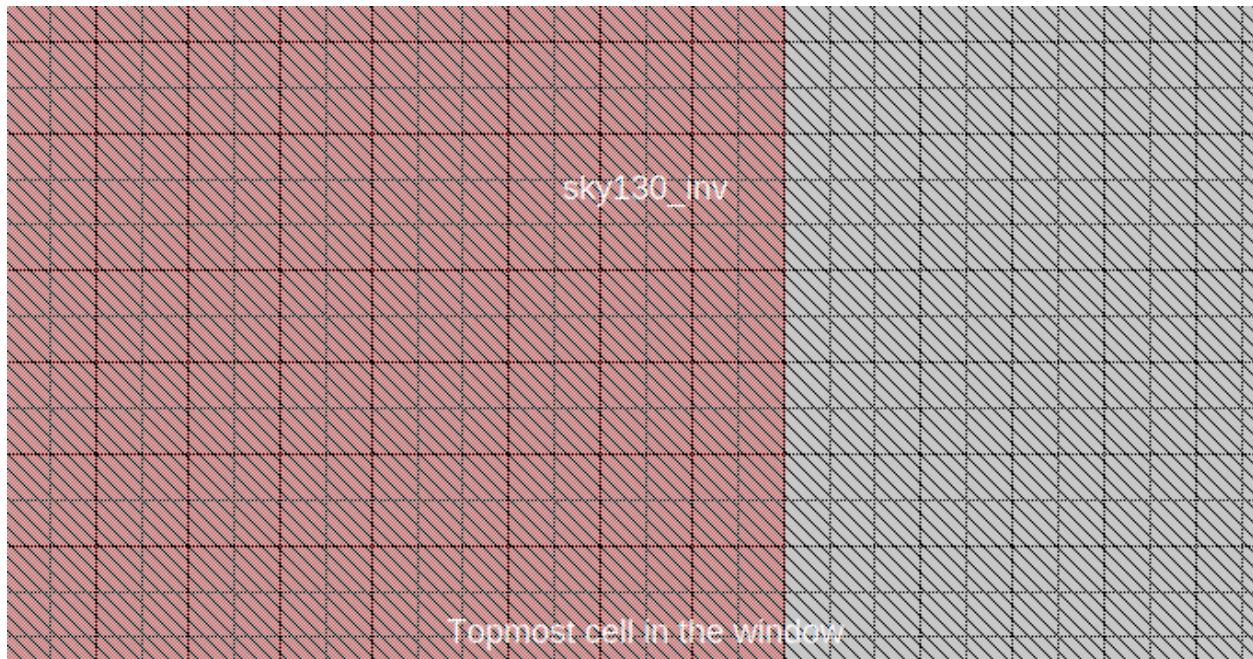
```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd ../pdks/sky130A/libs.tech/openlane/sky130_fd_sc_hd
```

View tracks.info file

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/openlane/sky130_fd_sc_hd$ less tracks.info
```

```
li1 X 0.23 0.46  
li1 Y 0.17 0.34  
met1 X 0.17 0.34  
met1 Y 0.17 0.34  
met2 X 0.23 0.46  
met2 Y 0.23 0.46  
met3 X 0.34 0.68  
met3 Y 0.34 0.68  
met4 X 0.46 0.92  
met4 Y 0.46 0.92  
met5 X 1.70 3.40  
met5 Y 1.70 3.40  
tracks.info (END)
```

Press g to activate grids



Use help grid to see info on grid commands

```
% help grid

Global Commands
-----
Layout Commands
-----
grid [xSpacing [ySpacing [x0Origin y0Origin]]]
    toggle grid on/off (and set parameters)
scalegrid a b    scale magic units vs. lambda by a / b
snap [internal|lambda|user]
    cause box to snap to the selected grid when moved
    by the cursor
```

Use grid to show bigger grid



```
% grid 0.46um 0.34um 0.23um 0.17um
```

ls to see contents of vsdstdcelldesign

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 192
-rw-rw-r-- 1 vsduser vsduser 13525 Jul 18 08:12 README.md
-rw-rw-r-- 1 vsduser vsduser 11357 Jul 18 08:12 LICENSE
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 Images
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 extras
-rw-rw-r-- 1 vsduser vsduser 2716 Jul 18 08:12 sky130_inv.mag
-rwxr-xr-x 1 vsduser vsduser 136710 Jul 18 08:44 sky130A.tech
-rw-rw-r-- 1 vsduser vsduser 1365 Jul 21 04:34 sky130_inv.ext
drwxrwxr-x 2 vsduser vsduser 4096 Jul 21 05:49 libs
-rw-rw-r-- 1 vsduser vsduser 219 Jul 21 06:55 bsim4v5.out
-rw-rw-r-- 1 vsduser vsduser 565 Jul 21 06:57 sky130_inv.spice
```

Save and exit

```
% save sky130_vsdinv.mag
% exit|
```

Open magic

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ magic -T sky130A.tech sky130_vsdinv.mag &
```

Create lef file

```
% lef write
Generating LEF output sky130_vsdinv.lef for cell sky130_vsdinv:
Diagnostic: Write LEF header for cell sky130_vsdinv
Diagnostic: Writing LEF output for cell sky130_vsdinv
Diagnostic: Scale value is 0.010000
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 200
-rw-rw-r-- 1 vsduser vsduser 13525 Jul 18 08:12 README.md
-rw-rw-r-- 1 vsduser vsduser 11357 Jul 18 08:12 LICENSE
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 Images
drwxrwxr-x 2 vsduser vsduser 4096 Jul 18 08:12 extras
-rw-rw-r-- 1 vsduser vsduser 2716 Jul 18 08:12 sky130_inv.mag
-rw-r-xr-x 1 vsduser vsduser 136710 Jul 18 08:44 sky130A.tech
-rw-rw-r-- 1 vsduser vsduser 1365 Jul 21 04:34 sky130_inv.ext
drwxrwxr-x 2 vsduser vsduser 4096 Jul 21 05:49 libs
-rw-rw-r-- 1 vsduser vsduser 219 Jul 21 06:55 bsim4v5.out
-rw-rw-r-- 1 vsduser vsduser 565 Jul 21 06:57 sky130_inv.spice
-rw-rw-r-- 1 vsduser vsduser 2716 Jul 22 09:23 sky130_vsdinv.mag
-rw-rw-r-- 1 vsduser vsduser 1517 Jul 22 09:26 sky130_vsdinv.lef
```

Open lef file

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ less sky130_vsdinv.lef
VERSION 5.7 ;
NOWIREEXTENSIONATPIN ON ;
DIVIDERCHAR "/" ;
BUSBITCHARS "[]" ;
MACRO sky130_vsdinv
  CLASS CORE ;
  FOREIGN sky130_vsdinv ;
  ORIGIN 0.000 0.000 ;
  SIZE 1.380 BY 2.720 ;
  SITE unithd ;
  PIN A
    DIRECTION INPUT ;
    USE SIGNAL ;
    ANTENNAGATEAREA 0.165600 ;
    PORT
      LAYER li1 ;
      RECT 0.060 1.180 0.510 1.690 ;
    END
  END A
  PIN Y
    DIRECTION OUTPUT ;
    USE SIGNAL ;
    ANTENNADIFFAREA 0.287800 ;
    PORT
      LAYER li1 ;
      RECT 0.760 1.960 1.100 2.330 ;
      RECT 0.880 1.690 1.050 1.960 ;
      RECT 0.880 1.180 1.330 1.690 ;
      RECT 0.880 0.760 1.050 1.180 ;
      RECT 0.780 0.410 1.130 0.760 ;
    END
  END Y
  PIN VPWR
    DIRECTION INOUT ;
    USE POWER ;
skv130 vsdinv.lef
```

ls to see contents

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src$ ls -ltr
total 96
-rw-r--r-- 1 vsduser docker 92423 Jun 29 2021 picorv32a.v
-rw-r--r-- 1 vsduser docker     77 Jun 29 2021 picorv32a.sdc
```

Copy the file to src

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cp sky130_vsdinv.lef /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src
```

Check if it was copied successfully

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src$ ls -ltr
total 100
-rw-r--r-- 1 vsduser docker 92423 Jun 29 2021 picorv32a.v
-rw-r--r-- 1 vsduser docker     77 Jun 29 2021 picorv32a.sdc
-rw-rw-r-- 1 vsduser vsduser 1517 Jul 22 09:40 sky130_vsdinv.lef
```

cd to libs then ls

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cd libs
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign/libs$ ls
nshort.lib  pshort.lib  sky130A.tech  sky130_fd_sc_hd_fast.lib  sky130_fd_sc_hd_slow.lib  sky130_fd_sc_hd_typical.lib
```

View the file

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign/libs$ less sky130_fd_sc_hd_typical.lib
library ("sky130_fd_sc_hd_tt_025C_1v80") {
    define(def_sim_opt,library,string);
    define(default_arc_mode,library,string);
    define(default_constraint_arc_mode,library,string);
    define(driver_model,library,string);
    define(leakage_sim_opt,library,string);
    define(min_pulse_width_mode,library,string);
    define(simulator,library,string);
    define(switching_power_split_model,library,string);
    define(sim_opt,timing,string);
    define(violation_delay_degrade_pct,timing,string);
    technology("cmos");
    delay_model : "table_lookup";
    bus_naming_style : "%s[%d]";
    time_unit : "1ns";
    voltage_unit : "1V";
    leakage_power_unit : "1nW";
    current_unit : "1mA";
    pulling_resistance_unit : "1kohm";
    capacitive_load_unit(1.0000000000, "pf");
    revision : 1.000000000;
    default_cell_leakage_power : 0.0000000000;
    default_fanout_load : 0.0000000000;
    default_inout_pin_cap : 0.0000000000;
    default_input_pin_cap : 0.0000000000;
    default_max_transition : 1.5000000000;
    default_output_pin_cap : 0.0000000000;
    default_arc_mode : "worst_edges";
    default_constraint_arc_mode : "worst";
    default_leakage_power_density : 0.0000000000;
    operating_conditions ("tt_025C_1v80") {
        voltage : 1.8000000000;
        process : 1.0000000000;
        temperature : 25.0000000000;
        tree_type : "balanced_tree";
    }
}
```

Do the same for the two other lib files

Copy all the lib files

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign/libs$ cp sky130_fd_sc_hd_* /home/vsduser/Desktop/work/tools/openlane/working_dir/openlane/designs/picorv32a/src
```

Is to check that they've been copied

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src$ ls -ltr
total 37428
-rw-r--r-- 1 vsduser docker      92423 Jun 29  2021 picorv32a.v
-rw-r--r-- 1 vsduser docker        77 Jun 29  2021 picorv32a.sdc
-rw-rw-r-- 1 vsduser vsduser     1517 Jul 22 09:40 sky130_vsdinv.lef
-rw-rw-r-- 1 vsduser vsduser 12753932 Jul 22 09:49 sky130_fd_sc_hd_fast.lib
-rw-rw-r-- 1 vsduser vsduser 12732258 Jul 22 09:49 sky130_fd_sc_hd_slow.lib
-rw-rw-r-- 1 vsduser vsduser 12732345 Jul 22 09:49 sky130_fd_sc_hd_typical.lib
```

cd back and open config.tcl

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src$ cd ..  
vsduser@vsdsquadron:~/Desktop/work/tools/openlane working dir/openlane/designs/picorv32a$ vim config.tcl
```

Open docker and run flow.tcl

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dtr/openlane$ docker  
bash-4.2$ ./flow.tcl -interactive  
[INFO]:  
[INFO]: Version: v0.21  
[INFO]: Running interactively  
%
```

```
% package require openlane 0.9  
0.9
```

See how many runs there are

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a$ cd runs  
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ ls  
16-07_04-55
```

Prepare the design

```
% prep -design picorv32a -tag 16-07_04-55 -overwrite  
[INFO]: Using design configuration at /openLANE_flow/designs/picorv32a/config.tcl  
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl  
[INFO]: PDKs root directory: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks  
[INFO]: PDK: sky130A  
[INFO]: Setting PDKPATH to /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A  
[INFO]: Standard Cell Library: sky130_fd_sc_hd  
[INFO]: Sourcing Configurations from /openLANE_flow/designs/picorv32a/config.tcl  
[WARNING]: Removing existing run /openLANE_flow/designs/picorv32a/runs/16-07_04-55  
[INFO]: Current run directory is /openLANE_flow/designs/picorv32a/runs/16-07_04-55  
[INFO]: Preparing LEF Files  
[INFO]: Extracting the number of available metal layers from /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd.lef  
[INFO]: The number of available metal layers is 6  
[INFO]: The available metal layers are l1 met1 met2 met3 met4 met5  
[INFO]: Merging LEF Files...  
mergelef.py : Merging LEFs  
sky130_fd_sc_hd.lef: SITEs matched found: 0  
sky130_fd_sc_hd.lef: MACROs matched found: 437  
sky130_ef_sc_hd_fill_12.lef: SITEs matched found: 0  
sky130_ef_sc_hd_fill_12.lef: MACROs matched found: 1  
sky130_ef_sc_hd_decap_12.lef: SITEs matched found: 0  
sky130_ef_sc_hd_decap_12.lef: MACROs matched found: 1  
sky130_ef_sc_hd_fakediode_2.lef: SITEs matched found: 0  
sky130_ef_sc_hd_fakediode_2.lef: MACROs matched found: 1  
mergelef.py : Merging LEFs complete  
[INFO]: Trimming Liberty...  
[INFO]: Generating Exclude List...  
[INFO]: Storing configs into config.tcl ...  
[INFO]: Preparation complete
```

Set and add lefs

```
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]  
/openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef  
% add_lefs -src $lefs  
[INFO]: Merging /openLANE_flow/designs/picorv32a/src/sky130_vsdinv.lef
```

Run synthesis

```
% run_synthesis
```

```
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>  
  
This is free software, and you are free to change and redistribute it  
under certain conditions; type 'show_copyright' for details.  
This program comes with ABSOLUTELY NO WARRANTY; for details type 'show_warranty'.  
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd_ff_n40C_1v95.lib line 31, defau  
lt_operating_condition ff_n40C_1v95 not found.  
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd_ss_100C_1v60.lib line 32, defau  
lt_operating_condition ss_100C_1v60 not found.  
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)  
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]  
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]  
puts "[INFO]: Setting output delay to: $output_delay_value"  
[INFO]: Setting output delay to: 4.9460000000000001  
puts "[INFO]: Setting input delay to: $input_delay_value"  
[INFO]: Setting input delay to: 4.9460000000000001  
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]  
set_clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]  
#set_rst_indx [lsearch [all_inputs] [get_port resetn]]  
set_all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]  
#set_all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]  
set_all_inputs_wo_clk_rst $all_inputs_wo_clk  
# correct resetn  
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst  
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] [resetn]  
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]  
# TODO set this as parameter  
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]  
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]  
puts "[INFO]: Setting load to: $cap_load"  
[INFO]: Setting load to: 0.01765  
set_load $cap_load [all_outputs]  
tns -759.46  
wns -24.89  
[INFO]: Synthesis was successful
```

Cd into configuration and open README.md

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd configuration/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/configuration$ less README.md
```

```
# Variables information

This page describes configuration variables and their default values.

## Required variables

| Variable | Description |
|-----|-----|
| `DESIGN_NAME` | The name of the top level module of the design |
| `VERILOG_FILES` | The path of the design's verilog files |
| `CLOCK_PERIOD` | The clock period for the design in ns |
| `CLOCK_NET` | The name of the Net input to root clock buffer used in Clock Tree Synthesis. |
| `CLOCK_PORT` | The name of the design's clock port used in Static Timing Analysis. |

## Optional variables

These variables are optional that can be specified in the design configuration file.

### Synthesis

| Variable | Description |
|-----|-----|
| `LIB_SYNTH` | The library used for synthesis by yosys. <br> (Default: `$:env(PDK)/$:env(STD_CELL_LIBRARY)/lib/sky130_fd_sc_hd_tt_025C_1v80.lib`) |
| `SYNTH_BIN` | The yosys binary used in the flow. <br> (Default: `yosys`) |
| `SYNTH_DRIVING_CELL` | The cell to drive the input ports. <br>(Default: `sky130_fd_sc_hd_inv_8`)|
| `SYNTH_DRIVING_CELL_PIN` | The name of the SYNTH_DRIVING_CELL output pin. <br>(Default: `V`)|
| `SYNTH_CAP_LOAD` | The capacitive load on the output ports in femtofarads. <br>(Default: `17.65` ff)|
| `SYNTH_MAX_FANOUT` | The max load that the output ports can drive. <br>(Default: `5` cells) |
| `SYNTH_MAX_TRAN` | The max transition time (slew) from high to low or low to high on cell inputs in ns. Used in synthesis <br> (Default: Calculated at runtime as `10%` of the provided clock period, unless this exceeds a set DEFAULT_MAX_TRAN, in which case it will be used as is). |
| `SYNTH_STRATEGY` | Strategies for abc logic synthesis and technology mapping <br> Possible values are `DELAY/AREA 0-3/0-2`; the first part refers to the optimization target of the synthesis strategy (area vs. delay) and the second one is an index. <br>(Default: `AREA 0`)|
| `SYNTH_BUFFERING` | Enables abc cell buffering <br> Enabled = 1, Disabled = 0 <br>(Default: `1`)|
| `SYNTH_SIZING` | Enables abc cell sizing (instead of buffering) <br> Enabled = 1, Disabled = 0 <br>(Default: `0`)|
```

Check the value of SYNTH_STRATEGY

```
% echo $::env(SYNTH_STRATEGY)
AREA 0
```

Set it to 1

```
% set ::env(SYNTH_STRATEGY) 1
1
```

Check the value of SYNTH_BUFFERING

```
% echo $::env(SYNTH_BUFFERING)
1
```

Check the value of SYNTH_SIZING

```
% echo $::env(SYNTH_SIZING)
0
```

Set SYNTH_SIZING to 1

```
% set ::env(SYNTH_SIZING) 1
1
```

Check the value of SYNTH_SIZING_CELL

```
% echo $::env(SYNTH_DRIVING_CELL)
sky130_fd_sc_hd_inv_8
```

Run synthesis again

```
% run_synthesis
```

```
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>

This is free software, and you are free to change and redistribute it
under certain conditions; type 'show_copyright' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type 'show_warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd_ff_n40C_1v95.lib line 3
lt_operating_condition ff_n40C_1v95 not found.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd_ss_100C_1v60.lib line 3
lt_operating_condition ss_100C_1v60 not found.
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "[INFO]: Setting output delay to: $output_delay_value"
[INFO]: Setting output delay to: 4.946000000000001
puts "[INFO]: Setting input delay to: $input_delay_value"
[INFO]: Setting input delay to: 4.946000000000001
set_max_fanout $::env(SYNTH_MAX_FANOUT) [current_design]
set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk
# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] [resetn]
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]
# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to: $cap_load"
[INFO]: Setting load to: 0.01765
set_load $cap_load [all_outputs]
tns -759.46
wns -24.89
```

Run floorplan

```
% run_floorplan
```

cd to tmp in most recent run

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs$ cd 16-07_04-55/tmp
```

View merged.lef

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/tmp$ less merged.lef

# Copyright 2020 The SkyWater PDK Authors
#
# Licensed under the Apache License, Version 2.0 (the "License");
# you may not use this file except in compliance with the License.
# You may obtain a copy of the License at
#
#     https://www.apache.org/licenses/LICENSE-2.0
#
# Unless required by applicable law or agreed to in writing, software
# distributed under the License is distributed on an "AS IS" BASIS,
# WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
# See the License for the specific language governing permissions and
# limitations under the License.
#
# SPDX-License-Identifier: Apache-2.0

VERSION 5.7 ;

BUSBITCHARS "[]";
DIVIDERCHAR "/" ;

UNITS
  TIME NANoseconds 1 ;
  CAPACITANCE PICOFARADS 1 ;
  RESISTANCE OHMS 1 ;
  DATABASE MICRONS 1000 ;
END UNITS

MANUFACTURINGGRID 0.005 ;

PROPERTYDEFINITIONS
  LAYER LEF58 TYPE STRING ;
END PROPERTYDEFINITIONS

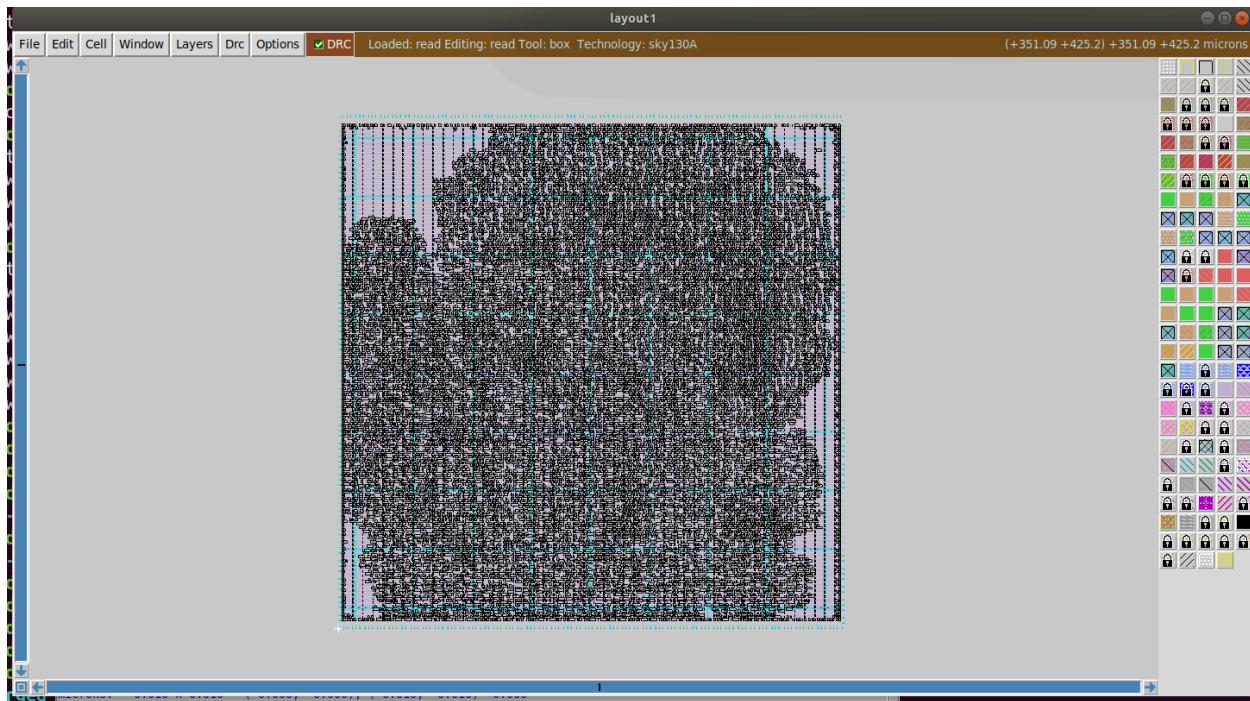
# High density, single height
merged.lef
```

Run placement

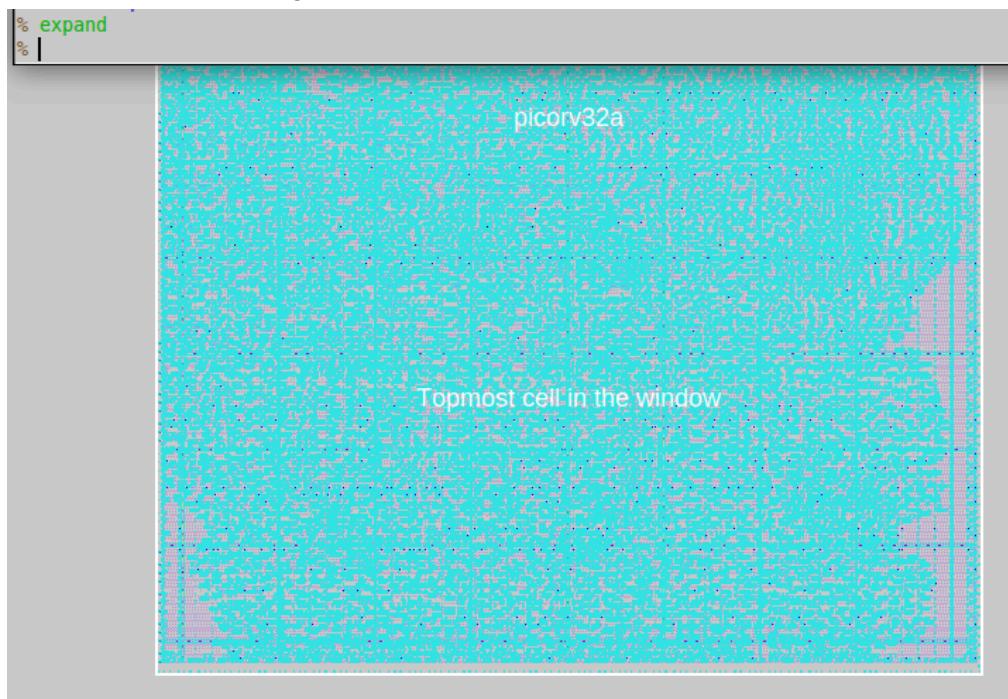
```
% run_placement
```

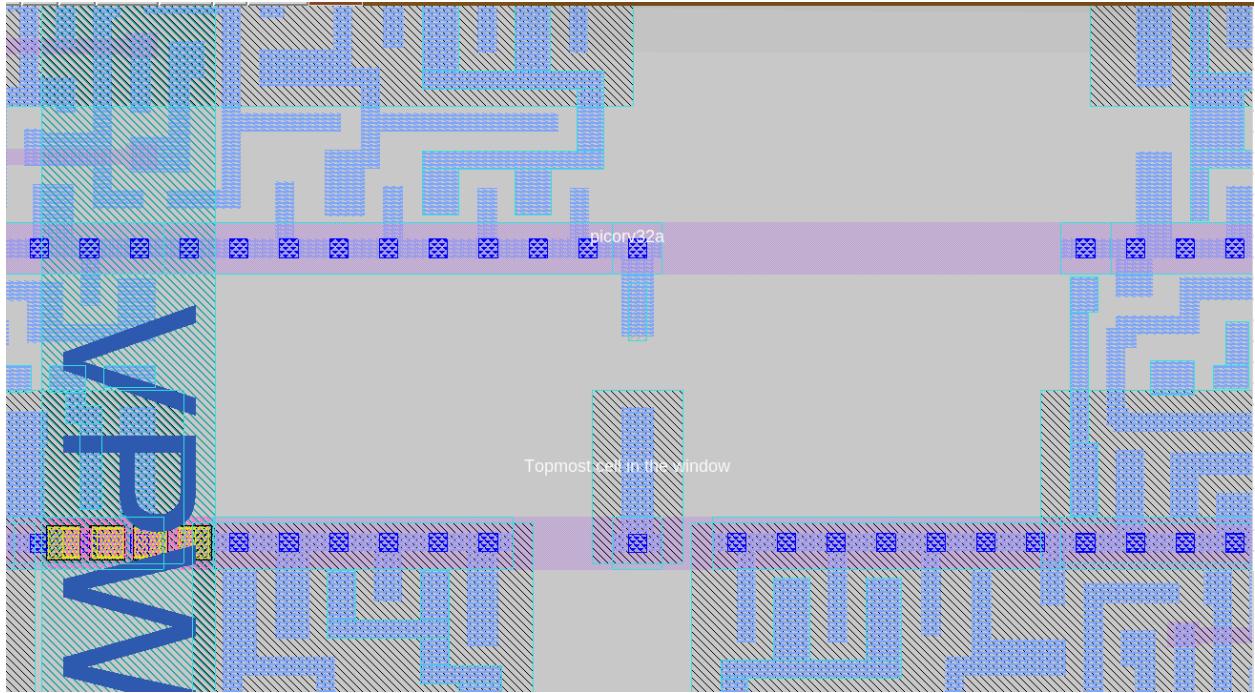
Run magic

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/placement$ magic -T ~/Desktop/work/tool/s/openlane_working_dir/pdk/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.lef def read picorv32a.placement.def &
```



Run expand in the magic console





Open pre_sta.conf

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ vim pre_sta.conf
```

```
set_cmd_units -time ns -capacitance pF -current mA -voltage V -resistance kOhm -distance um
read.liberty -max ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib
read.liberty -min ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib
read.verilog ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/synthesis/picorv32a.synthesis.v
link_design picorv32a
read.sdc ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/base.sdc
report_checks -path_delay min_max -fields {slew trans net cap input_pin}
report_tns
report_wns
```

Open mybase.sdc

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src$ less my_base.sdc
```

```
GNU nano 2.9.3                                         my_base.sdc
set ::env(CLOCK_PORT) clk
set ::env(CLOCK_PERIOD) 12.000
#set ::env(SYNTH_DRIVING_CELL) sky130_vsdinv
set ::env(SYNTH_DRIVING_CELL) sky130_fd_sc_hd_buf_16
set ::env(SYNTH_DRIVING_CELL_PIN) X
set ::env(SYNTH_CAP_LOAD) 13.6
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set IO_PCT 0.2
set input_delay_value [expr $::env(CLOCK_PERIOD) * $IO_PCT]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $IO_PCT]
puts "\[INFO\]: Setting output delay to:$output_delay_value"
puts "\[INFO\]: Setting input delay to:$input_delay_value"

set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk

# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] (resetn)
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]

# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL)
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
set_load $cap_load [all_outputs]
```

Open my_base.sdc with vim and edit the highlighted lines

```

set ::env(CLOCK_PORT) clk
set ::env(CLOCK_PERIOD) 12.000
#set ::env(SYNTH_DRIVING_CELL) sky130_vsdinv
set ::env(SYNTH_DRIVING_CELL) sky130_fd_sc_hd_inv_8
set ::env(SYNTH_DRIVING_CELL_PIN) Y
set ::env(SYNTH_CAP_LOAD) 17.65
create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -period $::env(CLOCK_PERIOD)
set IO_PCT 0.2
set input_delay_value [expr $::env(CLOCK_PERIOD) * $IO_PCT]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $IO_PCT]
puts "\[INFO\]: Setting output delay to:$output_delay_value"
puts "\[INFO\]: Setting input delay to:$input_delay_value"

set clk_indx [lsearch [all_inputs] [get_port $::env(CLOCK_PORT)]]
#set rst_indx [lsearch [all_inputs] [get_port resetn]]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx]
set all_inputs_wo_clk_rst $all_inputs_wo_clk

# correct resetn
set_input_delay $input_delay_value -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] (resetn)
set_output_delay $output_delay_value -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]

# TODO set this as parameter
set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) [all_inputs]
set_cap_load [expr $::env(SYNTH_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
set_load $cap_load [all_outputs]

```

Open pre_sta.conf and edit highlighted part

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ vim pre_sta.conf
```

```

set_cmd_units -time ns -capacitance pF -current mA -voltage V -resistance kOhm -distance um
read.liberty -max ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib
read.liberty -min ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib
read_verilog ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/synthesis/picorv32a.synthesis.v
link_design picorv32a
read_sdc ~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/my_base.sdc
report_checks -path_delay min_max -fields {slew trans net cap input_pin}
report_tns
report_wns

```

Do sta

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
```

```

2  0.01   0.13   0.67   46.15 v  _13747 / (sky130_fd_sc_hd__or2_2)
      0.13   0.00   46.15 v  _13867 / (net)
      0.14   0.69   46.84 v  _13748 / (sky130_fd_sc_hd__or2_2)
      0.14   0.00   46.84 v  _13749 / (sky130_fd_sc_hd__or2_2)
      0.13   0.67   47.51 v  _13750 / (sky130_fd_sc_hd__or2_2)
      0.13   0.00   47.51 v  _13750 / (sky130_fd_sc_hd__or2_2)
      0.14   0.69   48.29 v  _13750 / (sky130_fd_sc_hd__or2_2)
      0.14   0.00   48.29 v  _13750 / (sky130_fd_sc_hd__or2_2)
      0.14   0.69   48.29 v  _13751 / (sky130_fd_sc_hd__or2_2)
      0.14   0.00   48.29 v  _13751 / (sky130_fd_sc_hd__or2_2)
      0.14   0.68   48.88 v  _13754 / (sky130_fd_sc_hd__or2_2)
      0.14   0.00   48.88 v  _13754 / (sky130_fd_sc_hd__or2_2)
      0.07   0.44   49.33 v  _13754 / (sky130_fd_sc_hd__or21a_2)
      0.07   0.00   49.33 v  _27762 / (sky130_fd_sc_hd_dfxtp_2)
      0.07   0.00   49.33 v  _27762 / (sky130_fd_sc_hd_dfxtp_2)
      49.33   data arrival time
      0.00   12.00   clock clk (rise edge)
      0.00   12.00   clock network delay (ideal)
      0.00   12.00   clock reconvergence pessimism
      12.00 ^  _27762 / CLK (sky130_fd_sc_hd_dfxtp_2)
      -0.29   0.00   11.71 v  _27762 / (sky130_fd_sc_hd_dfxtp_2)
      11.71   data required time
      -49.33   data arrival time
      -37.62   slack (VIOLATED)

tns -3987.75
wns -37.62

```

Set SYNTH_MAX_FANOUT to 4

```
% set ::env(SYNTH_MAX_FANOUT) 4
```

Run synthesis

```
% run_synthesis
```

See details of netlist pins

```
% report_net -connections _14635_
```

Run sta

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
```

2	0.01				_10967_ (net)
		0.13	0.00	46.15 v	_13748_/B (sky130_fd_sc_hd_or2_2)
		0.14	0.69	46.84 v	_13748_/X (sky130_fd_sc_hd_or2_2)
3	0.01				_10968_ (net)
		0.14	0.00	46.84 v	_13749_/B (sky130_fd_sc_hd_or2_2)
		0.13	0.67	47.51 v	_13749_/X (sky130_fd_sc_hd_or2_2)
2	0.01				_10969_ (net)
		0.13	0.00	47.51 v	_13750_/B (sky130_fd_sc_hd_or2_2)
		0.14	0.69	48.20 v	_13750_/X (sky130_fd_sc_hd_or2_2)
3	0.01				_10970_ (net)
		0.14	0.00	48.20 v	_13751_/B (sky130_fd_sc_hd_or2_2)
		0.14	0.68	48.88 v	_13751_/X (sky130_fd_sc_hd_or2_2)
2	0.01				_10971_ (net)
		0.14	0.00	48.88 v	_13754_/B2 (sky130_fd_sc_hd_o221a_2)
		0.07	0.44	49.33 v	_13754_/X (sky130_fd_sc_hd_o221a_2)
1	0.00				_03928_ (net)
		0.07	0.00	49.33 v	_27762_/D (sky130_fd_sc_hd_dfxtpl_2)
				49.33	data arrival time
		0.00	12.00	12.00	clock clk (rise edge)
		0.00	12.00	12.00	clock network delay (ideal)
		0.00	12.00	12.00	clock reconvergence pessimism
		12.00	^	_27762_/CLK (sky130_fd_sc_hd_dfxtpl_2)	
		-0.29	11.71	library setup time	
			11.71	data required time	
			11.71	data required time	
			-49.33	data arrival time	
			-37.62	slack (VIOLATED)	
tns	-3987.75				
wns	-37.62				
%					

See details of netlist pins again

```
% report_net -connections _11344_
Net _11344_
Driver pins
_14442/_X output (sky130_fd_sc_hd_buf_1)

Load pins
_14443/_A1 input (sky130_fd_sc_hd_a22o_2)
_15088/_B1 input (sky130_fd_sc_hd_a22o_2)
_16440/_A1 input (sky130_fd_sc_hd_a21oi_2)
_18536/_A input (sky130_fd_sc_hd_inv_2)
_18641/_B1 input (sky130_fd_sc_hd_a22o_2)
_18869/_A1 input (sky130_fd_sc_hd_a21o_2)
```

Then do replace_cell (you can use help for more info about the replace_cell command)

```
% replace_cell _41882_ sky130_fd_sc_hd_buf_4
```

Report_checks will report then split it into 4 layers

```
% report_checks -fields {net cap slew input_pins} -digits 4
```

		0.1424	0.0000	45.4765 v _13747/_B (sky130_fd_sc_hd_or2_2)
		0.1308	0.6746	46.1511 v _13747/_X (sky130_fd_sc_hd_or2_2)
2	0.0056			_10967_ (net)
		0.1308	0.0000	46.1511 v _13748/_B (sky130_fd_sc_hd_or2_2)
		0.1424	0.6872	46.8383 v _13748/_X (sky130_fd_sc_hd_or2_2)
3	0.0079			_10968_ (net)
		0.1424	0.0000	46.8383 v _13749/_B (sky130_fd_sc_hd_or2_2)
		0.1308	0.6746	47.5128 v _13749/_X (sky130_fd_sc_hd_or2_2)
2	0.0056			_10969_ (net)
		0.1308	0.0000	47.5128 v _13750/_B (sky130_fd_sc_hd_or2_2)
		0.1424	0.6872	48.2000 v _13750/_X (sky130_fd_sc_hd_or2_2)
3	0.0079			_10970_ (net)
		0.1424	0.0000	48.2000 v _13751/_B (sky130_fd_sc_hd_or2_2)
		0.1356	0.6819	48.8819 v _13751/_X (sky130_fd_sc_hd_or2_2)
2	0.0066			_10971_ (net)
		0.1356	0.0000	48.8819 v _13754/_B2 (sky130_fd_sc_hd_o221a_2)
		0.0708	0.4435	49.3254 v _13754/_X (sky130_fd_sc_hd_o221a_2)
1	0.0016			_03928_ (net)
		0.0708	0.0000	49.3254 v _27762/_D (sky130_fd_sc_hd_dfxtp_2)
				49.3254 data arrival time
		0.0000	12.0000	clock clk (rise edge)
		0.0000	12.0000	clock network delay (ideal)
		0.0000	12.0000	clock reconvergence pessimism
		12.0000	^ _27762/_CLK (sky130_fd_sc_hd_dfxtp_2)	
		-0.2937		11.7063 library setup time
				11.7063 data required time

				11.7063 data required time
				-49.3254 data arrival time

				-37.6191 slack (VIOLATED)

Do replace_cell with 44322

```
% replace_cell _44322_ sky130_fd_sc_hd_buf_4
```

Do report_checks again

```
% report_checks -fields {net cap slew input_pins} -digits 4
```

		0.1424	0.0000	45.4765 v _13747_/B (sky130_fd_sc_hd_or2_2)
		0.1308	0.6746	46.1511 v _13747_/X (sky130_fd_sc_hd_or2_2)
2	0.0056			_10967_ (net)
		0.1308	0.0000	46.1511 v _13748_/B (sky130_fd_sc_hd_or2_2)
		0.1424	0.6872	46.8383 v _13748_/X (sky130_fd_sc_hd_or2_2)
3	0.0079			_10968_ (net)
		0.1424	0.0000	46.8383 v _13749_/B (sky130_fd_sc_hd_or2_2)
		0.1308	0.6746	47.5128 v _13749_/X (sky130_fd_sc_hd_or2_2)
2	0.0056			_10969_ (net)
		0.1308	0.0000	47.5128 v _13750_/B (sky130_fd_sc_hd_or2_2)
		0.1424	0.6872	48.2000 v _13750_/X (sky130_fd_sc_hd_or2_2)
3	0.0079			_10970_ (net)
		0.1424	0.0000	48.2000 v _13751_/B (sky130_fd_sc_hd_or2_2)
		0.1356	0.6819	48.8819 v _13751_/X (sky130_fd_sc_hd_or2_2)
2	0.0066			_10971_ (net)
		0.1356	0.0000	48.8819 v _13754/B2 (sky130_fd_sc_hd_o221a_2)
		0.0708	0.4435	49.3254 v _13754/X (sky130_fd_sc_hd_o221a_2)
1	0.0016			_03928_ (net)
		0.0708	0.0000	49.3254 v _27762/D (sky130_fd_sc_hd_dfxtp_2)
				49.3254 data arrival time
		0.0000	12.0000	clock clk (rise edge)
		0.0000	12.0000	clock network delay (ideal)
		0.0000	12.0000	clock reconvergence pessimism
		12.0000	^ _27762/CLK (sky130_fd_sc_hd_dfxtp_2)	
		-0.2937	11.7063	library setup time
			11.7063	data required time
			11.7063	data required time
			-49.3254	data arrival time
				-37.6191 slack (VIOLATED)

```
%
```

Do report_checks again

```
% report_checks -from _50144_ -to _50075_ -through _44322_
```

Do report_tns

```
% report_tns  
tns -3987.75
```

Do report_wns

```
% report_wns  
wns -37.62
```

Do replace_cell with 47972

```
% replace_cell _47972_ sky130_fd_sc_hd_buf_8
```

Do report_checks

```
% report_checks -fields {net cap slew input_pin}
```

		0.14	0.00	45.48 v _13747_/B (sky130_fd_sc_hd_or2_2)
		0.13	0.67	46.15 v _13747_/X (sky130_fd_sc_hd_or2_2)
2	0.01			_10967_ (net)
		0.13	0.00	46.15 v _13748_/B (sky130_fd_sc_hd_or2_2)
		0.14	0.69	46.84 v _13748_/X (sky130_fd_sc_hd_or2_2)
3	0.01			_10968_ (net)
		0.14	0.00	46.84 v _13749_/B (sky130_fd_sc_hd_or2_2)
		0.13	0.67	47.51 v _13749_/X (sky130_fd_sc_hd_or2_2)
2	0.01			_10969_ (net)
		0.13	0.00	47.51 v _13750_/B (sky130_fd_sc_hd_or2_2)
		0.14	0.69	48.20 v _13750_/X (sky130_fd_sc_hd_or2_2)
3	0.01			_10970_ (net)
		0.14	0.00	48.20 v _13751_/B (sky130_fd_sc_hd_or2_2)
		0.14	0.68	48.88 v _13751_/X (sky130_fd_sc_hd_or2_2)
2	0.01			_10971_ (net)
		0.14	0.00	48.88 v _13754_/B2 (sky130_fd_sc_hd_o221a_2)
		0.07	0.44	49.33 v _13754_/X (sky130_fd_sc_hd_o221a_2)
1	0.00			_03928_ (net)
		0.07	0.00	49.33 v _27762_/D (sky130_fd_sc_hd_dfxtpl_2)
				49.33 data arrival time
		0.00	12.00	clock clk (rise edge)
		0.00	12.00	clock network delay (ideal)
		0.00	12.00	clock reconvergence pessimism
		12.00	^ _27762_/CLK (sky130_fd_sc_hd_dfxtpl_2)	
		-0.29	11.71	library setup time
			11.71	data required time
			11.71	data required time
			-49.33	data arrival time
			-37.62	slack (VIOLATED)

```
%
```

Do replace_cell with 33697

```
% replace_cell _33697_ sky130_fd_sc_hd_buf_4
```

Do report_checks

```
% report_checks -fields {net cap slew input_pin}
```

```

          0.14  0.00  45.48 v _13747_/B (sky130_fd_sc_hd_or2_2)
          0.13  0.67  46.15 v _13747_/X (sky130_fd_sc_hd_or2_2)
                           _10967_ (net)
2   0.01           0.13  0.00  46.15 v _13748_/B (sky130_fd_sc_hd_or2_2)
          0.14  0.69  46.84 v _13748_/X (sky130_fd_sc_hd_or2_2)
                           _10968_ (net)
3   0.01           0.14  0.00  46.84 v _13749_/B (sky130_fd_sc_hd_or2_2)
          0.13  0.67  47.51 v _13749_/X (sky130_fd_sc_hd_or2_2)
                           _10969_ (net)
2   0.01           0.13  0.00  47.51 v _13750_/B (sky130_fd_sc_hd_or2_2)
          0.14  0.69  48.20 v _13750_/X (sky130_fd_sc_hd_or2_2)
                           _10970_ (net)
3   0.01           0.14  0.00  48.20 v _13751_/B (sky130_fd_sc_hd_or2_2)
          0.14  0.68  48.88 v _13751_/X (sky130_fd_sc_hd_or2_2)
                           _10971_ (net)
2   0.01           0.14  0.00  48.88 v _13754_/B2 (sky130_fd_sc_hd_o221a_2)
          0.07  0.44  49.33 v _13754_/X (sky130_fd_sc_hd_o221a_2)
                           _03928_ (net)
1    0.00           0.07  0.00  49.33 v _27762_/D (sky130_fd_sc_hd_dfxtp_2)
                           49.33 data arrival time

          0.00  12.00  12.00  clock clk (rise edge)
          0.00  12.00  12.00  clock network delay (ideal)
          0.00  12.00  12.00  clock reconvergence pessimism
          12.00 ^ _27762_/CLK (sky130_fd_sc_hd_dfxtp_2)
-0.29      11.71 library setup time
           11.71 data required time
-----
           11.71 data required time
-49.33   data arrival time
-----
-37.62   slack (VIOLATED)

%
```

Do write_verilog to update the file picorv32a.synthesis.v

```
% write_verilog /home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/synthesis/picorv32a.synthesis.v
```

You can check if it was overwritten successfully by checking the modification date of the file or opening the file and checking a specific update

Run floorplan

```
% run_floorplan
```

```
[WARNING PSM-0030] Vsrc location at (5.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 107.180um).
[WARNING PSM-0030] Vsrc location at (145.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 107.180um).
[WARNING PSM-0030] Vsrc location at (285.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 107.180um).
[WARNING PSM-0030] Vsrc location at (425.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 107.180um).
[WARNING PSM-0030] Vsrc location at (565.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 107.180um).
[WARNING PSM-0030] Vsrc location at (285.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 107.180um).
[WARNING PSM-0030] Vsrc location at (425.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 107.180um).
[WARNING PSM-0030] Vsrc location at (565.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 107.180um).
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 260.360um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 413.540um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 413.540um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 413.540um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 413.540um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 413.540um).
[INFO PSM-0031] Number of nodes on net VGND = 19223.
[INFO PSM-0037] G matrix created sucessfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/floorplan/19-pdn.def
1
%
```

Run placement

```
% run_placement
```

Run cts

```
% run_cts
```

```
26577 /CLK ^
 1.20      0.00      3.41

[INFO]: Clock Tree Synthesis was successful
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/placement/picorv32a.placement.def to /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def
[INFO]: Writing Verilog...
[INFO]: current step index: 26
OpenROAD 0.9.0 1415572a73
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Components of this program may be licensed under more restrictive licenses which must be honored.
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged_unpadded.lef
Notice 0:   Created 13 technology layers
Notice 0:   Created 25 technology vias
Notice 0:   Created 441 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged_unpadded.lef
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:   Created 411 pins.
Notice 0:   Created 22023 components and 134015 component-terminals.
Notice 0:   Created 2 special nets and 0 connections.
Notice 0:   Created 15771 nets and 57637 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def
[INFO]: Changing netlist from /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/synthesis/picorv32a.synthesis_optimized.v to /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/synthesis/picorv32a.synthesis_cts.v
[INFO]: Taking a Screenshot of the Layout Using Klayout...
[INFO]: current step index: 27
Using Techfile: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/klayout/sky130A.lyt
Using layout file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def
[INFO]: Reading tech file: /home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.tech/klayout/sky130A.lyt
[INFO]: Reading Layout file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def
[INFO]: Writing out PNG screenshot '/openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def.png'
Done
[INFO]: Screenshot taken.
%
```

Check for cts file to confirm that cts was successful

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/16-07_04-55/results/synthesis$ ls -ltr
total 5308
lrwxrwxrwx 1 vsduser vsduser    29 Jul 22 10:02 merged_unpadded.lef -> ../../tmp/merged_unpadded.lef
-rw-r--r-- 1 vsduser vsduser 1740683 Jul 27 02:48 picorv32a.synthesis.v
-rw-r--r-- 1 vsduser vsduser 1816220 Jul 27 02:59 picorv32a.synthesis_optimized.v
-rw-r--r-- 1 vsduser vsduser 1873523 Jul 27 03:04 picorv32a.synthesis_cts.v
```

There are tcl files for all of the openlane commands

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/scripts/tcl_commands$ ls -ltr
total 148
-rwxr-xr-x 1 vsduser docker 7752 Jun 29 2021 synthesis.tcl
-rwxr-xr-x 1 vsduser docker 15625 Jun 29 2021 routing.tcl
-rwxr-xr-x 1 vsduser docker 600 Jun 29 2021 refresh.tcl
-rw-r--r-- 1 vsduser docker 223 Jun 29 2021 README.md
-rwxr-xr-x 1 vsduser docker 12305 Jun 29 2021 placement.tcl
-rwxr-xr-x 1 vsduser docker 1602 Jun 29 2021 pkgIndex.tcl
-rwxr-xr-x 1 vsduser docker 11325 Jun 29 2021 magic.tcl
-rwxr-xr-x 1 vsduser docker 5873 Jun 29 2021 lvs.tcl
-rw-r--r-- 1 vsduser docker 1448 Jun 29 2021 list.txt
-rwxr-xr-x 1 vsduser docker 7190 Jun 29 2021 klayout.tcl
-rwxr-xr-x 1 vsduser docker 1739 Jun 29 2021 init_design.tcl
-rwxr-xr-x 1 vsduser docker 11739 Jun 29 2021 floorplan.tcl
-rwxr-xr-x 1 vsduser docker 3278 Jun 29 2021 cvc.tcl
-rwxr-xr-x 1 vsduser docker 3941 Jun 29 2021 cts.tcl
-rwxr-xr-x 1 vsduser docker 6538 Jun 29 2021 checkers.tcl
-rwxr-xr-x 1 vsduser docker 31103 Jun 29 2021 all.tcl
```

Open cts.tcl

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/scripts/tcl_commands$ less cts.tcl
# Copyright 2020 Efabless Corporation
#
# Licensed under the Apache License, Version 2.0 (the "License");
# you may not use this file except in compliance with the License.
# You may obtain a copy of the License at
#
#     http://www.apache.org/licenses/LICENSE-2.0
#
# Unless required by applicable law or agreed to in writing, software
# distributed under the License is distributed on an "AS IS" BASIS,
# WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
# See the License for the specific language governing permissions and
# limitations under the License.

global script_path
set script_path [ file dirname [ file normalize [ info script ] ] ]

proc set_core_dims {args} {
    puts_info "Setting Core Dimensions..."
    set options {{-log_path required}}
    parse_key_args "set_core_dims" args values $options
    set log_path $values(-log_path)
    set FpOutDef ${::env(CURRENT_DEF)}
    set def_units ${::env(DEF_UNITS_PER_MICRON)}
    set coreinfo [join [exec ${::env(SCRIPTS_DIR)}/extract_coreinfo.sh $FpOutDef] " "]
    set sites_per_row [lindex $coreinfo 8]
    set step [lindex $coreinfo 9]
    set core_area_llx [expr { [lindex $coreinfo 4]/double($def_units) }]
    set core_area_urx [expr { ([lindex $coreinfo 6]+$step*$sites_per_row)/double($def_units) }]
    set core_area_lly [expr { [lindex $coreinfo 5]/double($def_units) }]
    set core_area_ury [expr { [lindex $coreinfo 7]/double($def_units) }]
    set ::env(CORE_WIDTH) [expr {$core_area_urx - $core_area_llx}]
    set ::env(CORE_HEIGHT) [expr {$core_area_ury - $core_area_lly}]
    puts "$::env(CORE_WIDTH) $::env(CORE_HEIGHT)"
}

cts.tcl
```

Contents show what actually runs when you run_cts

```
proc run_cts {args} {
    if { ! [info exists ::env(CLOCK_PORT)] && ! [info exists ::env(CLOCK_NET)] } {
        puts_info "::env(CLOCK_PORT) is not set"
        puts_warn "Skipping CTS..."
        set ::env(CLOCK_TREE_SYNTH) 0
    }

    if {$::env(CLOCK_TREE_SYNTH)} {
        puts_info "Running TritonCTS..."
        set ::env(CURRENT_STAGE) cts
        TIMER::timer_start

        if { ! [info exists ::env(CLOCK_NET)] } {
            set ::env(CLOCK_NET) $::env(CLOCK_PORT)
        }

        set ::env(SAVE_DEF) $::env(cts_result_file_tag).def
        set report_tag_holder $::env(cts_report_file_tag)
        set ::env(cts_report_file_tag) [ index_file $::env(cts_report_file_tag) ]
        # trim the lib to exclude cells with drc errors
        if { ! [info exists ::env(LIB_CTS)] } {
            set ::env(LIB_CTS) $::env(TMP_DIR)/cts.lib
            trim_lib -input $::env(LIB_SYNTH_COMPLETE) -output $::env(LIB_CTS) -drc_exclude_only
        }
        tryCatch openroad -exit $::env(SCRIPTS_DIR)/openroad/or_cts.tcl |& tee $::env(TERMINAL_OUTPUT) [index_file $::env(cts_log_file_tag)].log
    }

    check_cts_clock_nets
    set ::env(cts_report_file_tag) $report_tag_holder
    TIMER::timer_stop
    exec echo "[TIMER::get_runtime]" >> [index_file $::env(cts_log_file_tag)_runtime.txt 0]

    set_def $::env(SAVE_DEF)
    write_verilog $::env(yosys_result_file_tag).cts.v
    set_netlist $::env(yosys_result_file_tag).cts.v
}
```

Use echo to see the directories and values

```
% echo $::env(LIB_SYNTH_COMPLETE)
/home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd_tt_025C_1v80.lib

% echo $::env(LIB_TYPICAL)
/home/vsduser/Desktop/work/tools/openlane_working_dir/pdk/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd_tt_025C_1v80.lib

% echo $::env(CURRENT_DEF)
/openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def

% echo $::env(CTN_MAX_TRAN)
2.4730000000000003

% echo $::env(CTS_MAX_CAP)
1.53169
```

```
% echo $::env(CTS_CLK_BUFFER_LIST)
sky130_fd_sc_hd_clkbuf_1 sky130_fd_sc_hd_clkbuf_2 sky130_fd_sc_hd_clkbuf_4 sky130_fd_sc_hd_clkbuf_8
% echo $::env(CTS_ROOT_BUFFER)
sky130_fd_sc_hd_clkbuf_16
```

Open openroad

```
% openroad
OpenROAD 0.9.0 1415572a73
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```

Run read_lef

```
% read_lef /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged.lef

Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged.lef
Notice 0:      Created 13 technology layers
Notice 0:      Created 25 technology vias
Notice 0:      Created 441 library cells
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged.lef
```

Run read_def

```
% read_def /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def
Notice 0:
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def
Notice 0: Design: picorv32a
Notice 0:     Created 411 pins.
Notice 0:     Created 22023 components and 134015 component-terminals.
Notice 0:     Created 2 special nets and 0 connections.
Notice 0:     Created 15771 nets and 57637 connections.
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def
```

Create a db file

```
% write_db pico_cts.db
```

Read the file

```
% read_db pico_cts.db
```

Read verilog file

```
% read_verilog /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/synthesis/picorv32a.synthesis_cts.v
```

Read liberty cell

```
% read_liberty -max $::env(LIB_MAX)
```

```
% read_liberty -min $::env(LIB_MIN)
```

Read sdc file

```
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc
```

Set propagated clock

```
% set_propogated_clock [all_clocks]
```

Report checks with the clock

```
% report_checks -path_delay min_max -format full_clock_expanded -digits 4
```

Exit openroad

```
% exit
```

Go back into openroad

```
% openroad
OpenROAD 0.9.0 1415572a73
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```

Read_db

```
% read_db pico_cts.db
```

read_verilog again

```
% read_verilog /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/synthesis/picorv32a.synthesis_cts.v
```

read_library

```
% read_liberty $::env(LIB_SYNTH_COMPLETE)
```

Link the design

```
% link_design picorv32a
```

```
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o2bb2a_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_and4b_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o2bb2ai_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a31oi_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_nor2b_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a21boi_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a2bb2o_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a21boi_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a2bb2oi_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a21bo_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a2bb2oi_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_and4_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_or2b_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o31a_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a2bb2o_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o221a_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o21a_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o32a_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o21ba_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_and4_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o31a_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o2bb2ai_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o41a_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_conb_1 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_mux2_8 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_mux2_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_mux2_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_mux4_1 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_mux4_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_dfxtp_1 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_dfxtp_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_dfxtp_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_clkbuf_16 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_buf_12 has no liberty cell.
```

```
%
```

read_sdc again

```
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc  
[INFO]: Setting output delay to:2.4000000000000004  
[INFO]: Setting input delay to:2.4000000000000004
```

Set propagated clock again

```
% set_propogated_clock [all_clocks]
```

Do report checks again

```
% report_checks -path_delay min_max -fields {slew trans net cap input_pin} -format full_clock_expanded -digits 4
```

Do sta pre_sta.conf again

```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ sta pre_sta.conf
```

2	0.01			_10967_ (net)
		0.13	0.00	46.15 v _13748_/B (sky130_fd_sc_hd_or2_2)
		0.14	0.69	46.84 v _13748_/X (sky130_fd_sc_hd_or2_2)
3	0.01			_10968_ (net)
		0.14	0.00	46.84 v _13749_/B (sky130_fd_sc_hd_or2_2)
		0.13	0.67	47.51 v _13749_/X (sky130_fd_sc_hd_or2_2)
2	0.01			_10969_ (net)
		0.13	0.00	47.51 v _13750_/B (sky130_fd_sc_hd_or2_2)
		0.14	0.69	48.20 v _13750_/X (sky130_fd_sc_hd_or2_2)
3	0.01			_10970_ (net)
		0.14	0.00	48.20 v _13751_/B (sky130_fd_sc_hd_or2_2)
		0.14	0.68	48.88 v _13751_/X (sky130_fd_sc_hd_or2_2)
2	0.01			_10971_ (net)
		0.14	0.00	48.88 v _13754_/B2 (sky130_fd_sc_hd_o221a_2)
		0.07	0.44	49.33 v _13754_/X (sky130_fd_sc_hd_o221a_2)
1	0.00			_03928_ (net)
		0.07	0.00	49.33 v _27762_/D (sky130_fd_sc_hd_dfxtip_2)
				49.33 data arrival time
		0.00	12.00	12.00 clock clk (rise edge)
			0.00	12.00 clock network delay (ideal)
			0.00	12.00 clock reconvergence pessimism
			12.00	^ _27762_/CLK (sky130_fd_sc_hd_dfxtip_2)
		-0.29	11.71	library setup time
			11.71	data required time
			11.71	data required time
			-49.33	data arrival time
				-37.62 slack (VIOLATED)
				tns -3987.75
				wns -37.62

Remove the first item in the CTS_CLK_BUFFER_LIST

```
% lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0
```

Need to use set so that it actually updates the code

```
% set ::env(CTS_CLK_BUFFER_LIST) [lreplace $::env(CTS_CLK_BUFFER_LIST) 0 0]
```

Run cts again

```
% run_cts
```

Edit CURRENT_DEF

```
% set ::env(CURRENT_DEF) /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/placement/picorv32a.placement.def  
/openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/placement/picorv32a.placement.def  
% echo $::env(CURRENT_DEF)  
/openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/placement/picorv32a.placement.def
```

Run cts again

```
% run_cts
```

Open openroad

```
% openroad  
OpenROAD 0.9.0 1415572a73  
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```

Do read_lef and read_def from before

```
% read_lef /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged.lef  
Notice 0: Reading LEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged.lef  
Notice 0:     Created 13 technology layers  
Notice 0:     Created 25 technology vias  
Notice 0:     Created 441 library cells  
Notice 0: Finished LEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/tmp/merged.lef  
% read_def /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def  
Notice 0:  
Reading DEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def  
Notice 0: Design: picorv32a  
Notice 0:     Created 411 pins.  
Notice 0:     Created 22023 components and 134015 component-terminals.  
Notice 0:     Created 2 special nets and 0 connections.  
Notice 0:     Created 15771 nets and 57637 connections.  
Notice 0: Finished DEF file: /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/cts/picorv32a.cts.def
```

Create a db file

```
% write_db pico_cts1.db
```

Read the file

```
% read_db pico_cts1.db
```

Do read_verilog and read_library like before

```
% read_verilog /openLANE_flow/designs/picorv32a/runs/16-07_04-55/results/synthesis/picorv32a.synthesis_cts.v
```

```
% read_liberty $::env(LIB_SYNTH_COMPLETE)
```

Link the design again

```
% link_design picorv32a
```

```
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o2bb2a_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_and4b_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o2bb2ai_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a31oi_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_nor2b_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a21boi_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a2bb2o_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a21boi_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a2bb2oi_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a21bo_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a2bb2oi_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_and4_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_or2b_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o31a_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_a2bb2o_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o221a_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o21a_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o32a_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o21ba_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_and4_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o31a_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o2bb2ai_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_o41a_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_conb_1 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_mux2_8 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_mux2_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_mux2_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_mux4_1 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_mux4_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_dfxtp_1 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_dfxtp_2 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_dfxtp_4 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_clkbuf_16 has no liberty cell.  
[WARNING ORD-1000] LEF master sky130_fd_sc_hd_buf_12 has no liberty cell.  
%
```

read_sdc again

```
% read_sdc /openLANE_flow/designs/picorv32a/src/my_base.sdc  
[INFO]: Setting output delay to:2.4000000000000004  
[INFO]: Setting input delay to:2.4000000000000004
```

Set propagated clock again

```
% set_propogated_clock [all_clocks]
```

Do report checks again

```
% report_checks -path_delay min_max -fields {slew trans net cap input_pin} -format full_clock_expanded -digits 4
```

Do report_clock_skew to check the clock skew

```
% report_clock_skew -hold
```

```
% report_clock_skew -setup
```

Add an item into the CTS_CLK_BUFFER_LIST

```
% set ::env(CTS_CLK_BUFFER_LIST) [linsert ${::env(CTS_CLK_BUFFER_LIST)} 0 sky130_fd_sc_hd_clkbuf_1]
```