ANJUN GU

Education

The University of California, San Diego — June 2016
Master of Science, Electrical and Computer Engineering

The University of Texas at Austin — December 2013
Bachelor of Science, Electrical and Computer Engineering
Bachelor of Arts, Mathematics

Related Courses

- VLSI Advanced Topics (ranked **# 1** in class)
- VLSI Algorithms & Architectures
- Digital System Design Using HDL
- VLSI Integrated Circuits & Systems Design
- Digital Logic Design
- Embedded Systems Design Lab
- Algorithm Design and Analysis
- Advance Data Structures
- Software Design & Implementation
- Real-time Digital Signal Processing Lab
- Digital Signal Processing I
- Probability and Random Processes
- Digital Image Processing
- Digital Signal Processing II
- Automatic Control (ranked **# 1** in class)
- Analog IC Design
- Electronic Circuits
- Biomedical IC Digital

Skills

- **Programming Languages:** C, C++, JAVA, VHDL, Verilog, and assembly languages (Freescale 9S12, ARM)
- **Software:** Xilinx ISE, Modelsim, MATLAB, LabVIEW, Cadence, CodeWarrior, CPLEX, Visual Studio, Android Studio and Eclipse
- **Languages:** Chinese and English

Selected Projects

AudaExplore Hackathon Contest, (Team Santa Monica, 2nd place) — 8/21/2015 – 8/23/2015

- Led a four-person team that created an android app for guiding user to take good quality pictures for filing insurance claim purpose
  - Used program language: xml and java
  - Selected additional library implemented: cropper, OpenCV
- Gave a presentation about the created android app, the concept/idea behind it, and the future work

Embedded Hardware Design of AES Encryption Co-processor, VLSI Advanced Topic — Spring 2015

- Implemented a AES encryption co-processor using Verilog with the goal to minimize total area – the area is 20% smaller than the sample best result
- Implemented a AES encryption co-processor using Verilog with the goal to minimize area*delay product – the product is 35% smaller than the sample best result

Leakage Power Minimization, VLSI Integrated Circuits & Systems Design — Winter 2015

- Used Synopsys PrimeTime and PT-PX for timing and power analysis
- Ran tcl script to minimize leakage power with implementing strategies for gate sizing and Vt-swapping

Low Power Design of a 4-bit Processor with Specified ISA, VLSI Algorithms and Architectures — Fall 2014

- Achieve the **1st place** by giving the lowest power consumption in 27 project designs
- Analyzed the constraints of the circuit (Frequency, VDD, etc.), applied techniques accordingly
- Creatively improved the traditional control unit structure to better meet the requirement
- Completed schematic and layout level design

Optimizing the Mobile Web Browsing Experience, Senior Design Project — Spring 2013 – Fall 2013

- Discussed with teammates about how to develop software tool on optimizing mobile websites
- Worked with Pandaboard and Odroid board for analyzing the relation between web page performance and power, and use the collected data to create the prediction model for power consumption
- Designed a tool that helps web designers to optimize web pages by analyzing web page performance and power on mobile

Implementing and characterizing memory using Cadence, Introduction to VLSI Design Fall 2013

- Implemented and optimized a 4-bit SRAM cell using 45 nm CMOS in both layout and schematic
- Modeled and characterized a 32-bit X 32-bit memory array in schematic

Designing an Arithmetic Logic Unit using Cadence, Introduction to VLSI Design Fall 2013

- Implemented a 16-bit Kogge-Stone adder
- Designed a 16-bit Arithmetic Logic Unit and optimize it for speed in schematic and simulation
- Wrote testbench in Verilog to verify the functionality

Simulating MIPS ISA using VHDL, Digital System Design Using HDL Fall 2012

- Synthesized and simulated a MIPS processor on Xilinx Spartan 3 FPGA board
- Added ARM instructions to the MIPS ISA simulation model

Timing Power Controller, Embedded Systems Design Lab Fall 2012

- Created a timing power controller that turns on/off power based on the timing setting. User is able to set the timing by using the switches and LCD screen. Used TI LM3S1968 (ARM Cortex-M3) microcontroller.
  - Designed **PCB** layout
  - Wrote code (in **C**) and loaded it to the embedded system via JTAG

Research Experience

Graduate Research Assistant, Silicon-Photonic Network-on-Chip (NoC) Research 3/2015 – 3/2016

- Designed a policy that allocates the threads to minimize the tuning power for the optical Network on Chip (NoC)
- Wrote **C++** and CPLEX code for designing a CAD tool to generate optical NoC floorplan
- Wrote script in **Tcl script** and **CShell** to run HotSpot for temperature simulation
- Wrote **Matlab** code to process and analysis data

Undergraduate Research Assistant, Test Vector Decompression Research 01/2013 – 10/2013

- Learned the concepts and theories about test vector compression and decompression
- Investigated more efficient strategies for test vector decompression in software

Work Experience

Teaching Assistant, Electrical and Computer Engineering Department 08/2013 – 12/2013

- Assisted professor with observing lectures and collecting students' feedbacks
- Helped students understand the material
- Created and graded assignments and exams

Learning Assistant, Math Department at the College of Natural Sciences 08/2012 – 12/2013

- Assisted professor with observing lectures and collecting students' feedbacks
- Held office hours to help students understand the material

Grader, Math Department at the College of Natural Sciences 08/2012 – 05/2013

- Assisted professors to provide good lectures by analyzing students' assignments
- Helped students to learn knowledge by grading and making comments on their assignments

Student Assistant, Learning Resource Center at the School of Social Work 08/2011 – 08/2012

- Assisted students and faculty members with reserving and checking-out learning materials and facilities
- Processed and archived incoming academic journals and dubbing videotapes to/from DVDs

Accomplishments

- Member, Phi Beta Kappa (PBK) 11/2013 – Present
- Member, Institute of Electrical and Electronics Engineers (IEEE) 10/2012 – Present
- Member, National Society of Collegiate Scholars (NSCS) 02/2010 – Present
- Member, Christian Students on Campus 08/2010 – 12/2013
- Vice President, Conceptual Self-defense Club (CSC) 02/2011 – 12/2013

Honors

- University of California, San Diego ECE Department Fellowship Fall 2014 – Spring 2015
- Robbie & Roy Sorenson Endowed Electrical Engineering Scholarship Fall 2013
- College of Natural Sciences Scholarship Fall 2013
- University Honors – Five Semesters Fall 2010 – Fall 2013
- College Scholars – Two Years Spring 2012 – Spring 2013

- Peer Leader Academy Development Certification — Spring 2013
- Student Employee Excellence Development Certification — Fall 2012

Publication

- A. Coskun, **A. Gu**, W. Jin, A. J. Joshi, A. B. Kahng, J. Klamkin, Y. Ma, J. Recchio, V. Srinivas and T. Zhang, "Cross-Layer Floorplan Optimization For Silicon Photonic NoCs In Many-Core Systems", *Proc. DATE*, 2016.
- J. L. Abellán, A. K. Coskun, **A. Gu**, W. Jin, A. Joshi, A. B. Kahng, J. Klamkin, C. Morales, J. Recchio, V. Srinivas and T. Zhang, "Adaptive Tuning of Photonic Devices in a Photonic NoC Through Dynamic Workload Allocation", *TCAD*, 2016.