Race around Condition.

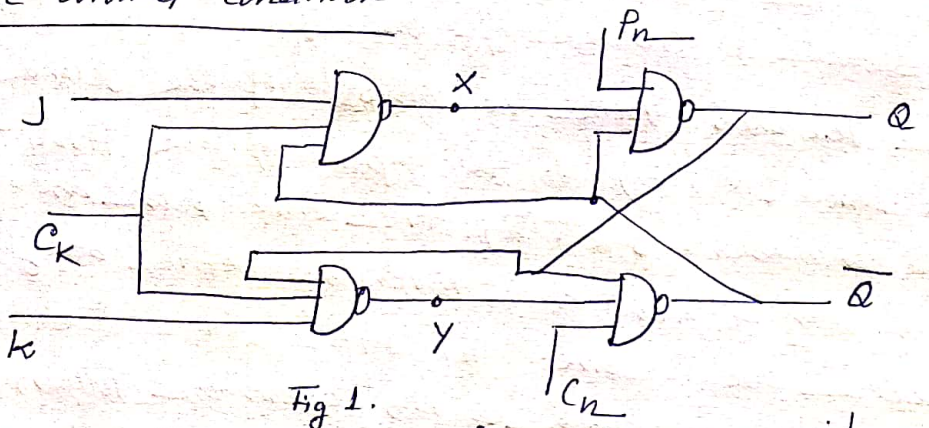

Fig 1.

For the J-K FF in fig 1 let us consider the assignment of excitations J=K=1. If the width of the clock pulse tp is too long, the state of the FF will keep on changing from 0 to 1, 1 to 0, 0 to 1 & so on & the at the end of the clock pulse, its state will be uncertain. This phenomenon is called the race around condition. The output Q & $\bar{Q}$ will change on their own if the clock pulse width tp is too long compared with the propagation delay γ of each Nand gate.

tp = clock pulse width

γ = propagation delay

T = ~~time~~ pulse time period.

It can be avoided if $t_p < \gamma < T$.

However, with IC components the propagation delay is very small, usually much less the pulse width tp. Hence the above inequality is not satisfied & the output is indeterminate. If loop delay ~~Gate~~ increased beyond tp than race-around condition can be avoided.

Master-Slave FF avoide race-around condition

Master Slave J-K FF.

Fig ② is shown a cascade of one J-k & one S-R F.F with feedback from the output of the second (called the slave - S-R F.F) to the input of the first (called the master - J-K F.F). +ve clock pulse are applied to the master & these are inverted before being used to excite the slave. For Pr=1, Cr=1 & Ck=1, the master is enabled & its operation follows the J-k truth table. Furthermore, since $\overline{Ck}=0$, the slave S-R FF is inhibited, so that Qn is invariant for the pulse duration t_p. Therefore, the race-around difficulty is circumvented with the master-slave topology.

After the pulse passes, Ck=0, so that the master is inhibited & $\overline{Ck}=1$, which causes the slave to be enabled. The slave is an S-R FF, which follows the logic in Fig ③.

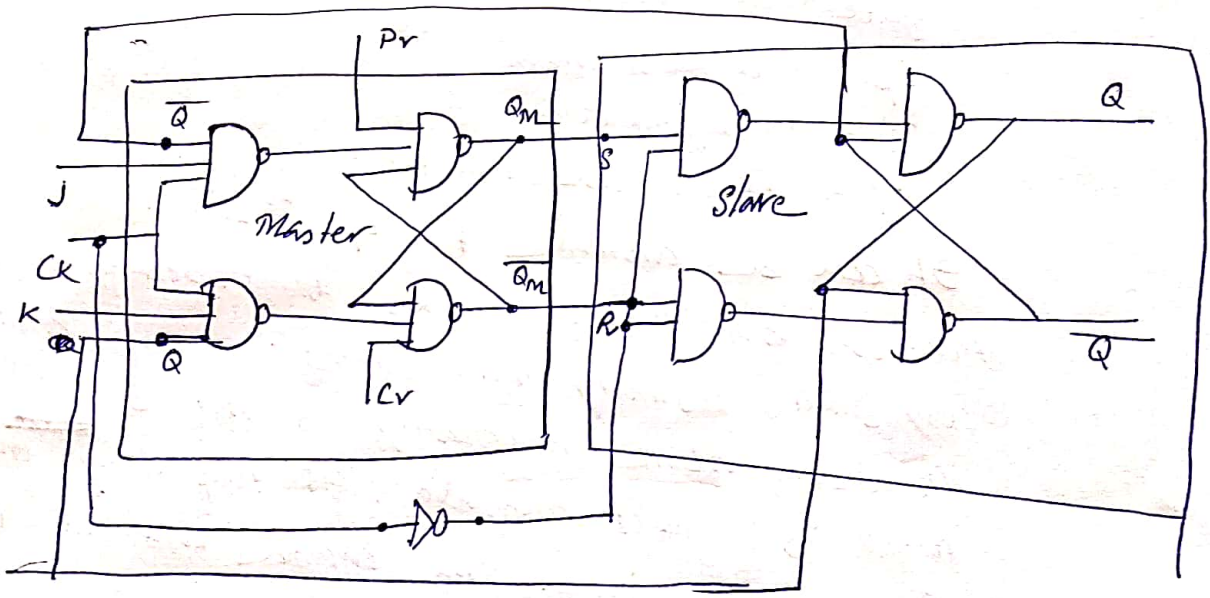

Fig ②

S	R	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	?