

Power Aware CTS

Delay Table for CBUF '1'

	10fF	30fF	50fF	70fF	90fF	110fF
20ps	x1	x2	x3	x4	x5	x6
40ps	x7	x8	x9	x10	x11	x12
60ps	x13	x14	x15	x16	x17	x18
80ps	x19	x20	x21	x22	x23	x24

Input-skew

Delay Table for CBUF '2'

	10fF	30fF	50fF	70fF	90fF	110fF
20ps	y1	y2	y3	y4	y5	y6
40ps	y7	y8	y9	y10	y11	y12
60ps	y13	y14	y15	y16	y17	y18
80ps	y19	y20	y21	y22	y23	y24

Observations

- 2 levels of buffering
- At every level, each node driving same load
- Identical buffer at same level

Let us assume  $C_1 = C_2 = C_3 = C_4 = 25fF$

How about creating a buffer tree at node 'A'

Let us assume  $C_{buf1} = C_{buf2} = 30fF$

Therefore, total Cap at node 'A'  $\Rightarrow 60fF$

Therefore, total Cap at node 'B'  $\Rightarrow 50fF$

Therefore, total Cap at node 'C'  $\Rightarrow 50fF$

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Next lecture L2 Introduction... →

SIMPLY VLSI

Threshold Voltage Equation:

$$V_t = V_{to} + \gamma(\sqrt{|-2\Phi_f + V_{sb}|} - \sqrt{|-2\Phi_f|})$$

Where

$V_{to}$  = Threshold voltage at  $V_{sb} = 0$ , and is a function of manufacturing process

$\gamma$  = body effect coefficient, expresses the impact of changes in body bias  $V_{sb}$  (Unit is  $V^{0.5}$ )

$\Phi_f$  = Fermi Potential (Covered in Semiconductor Physics Slides)

$$\gamma = \frac{\sqrt{2qNA\varepsilon_s}}{C_{ox}}$$

$\varepsilon_s$  = relative permittivity of silicon = 11.7

$N_A$  = doping concentration

$q$  = charge of the electron

$C_{ox}$  = oxide capacitance

$$\Phi_f = -\Phi_T * \ln \frac{N_A}{n_i}$$

$n_i$  = intrinsic doping parameter for the substrate

$V_{sb} = +ve$  value

Semiconductor surface inverts to n-type material at voltage  $V_{gs} = V_{to} + V_1$

$V_{sb} = 0$

Semiconductor surface inverts to n-type material at voltage  $V_{gs} = V_{to}$  (say)

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$V_{sb} = 0$

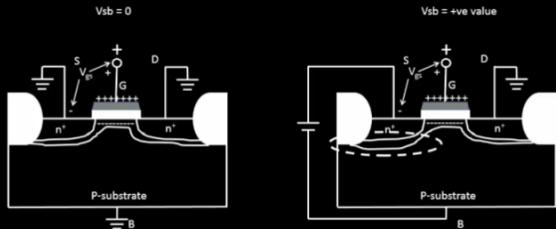
$V_{sb} = +ve$  value

Due to +ve  $V_{sb}$ , few charges from channel are pulled towards source 'S'

Additional Reverse bias between source 'S' and substrate (or Bulk) 'B'

Therefore, depletion layer width is slightly high near 'S'

Increase 'Vgs'



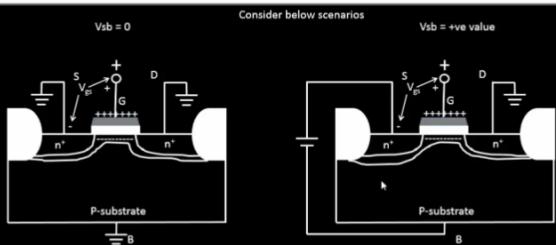
Additional Reverse bias between source 'S' and substrate (or Bulk) 'B'  
Therefore, depletion layer width is slightly high near 'S'

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Consider below scenarios

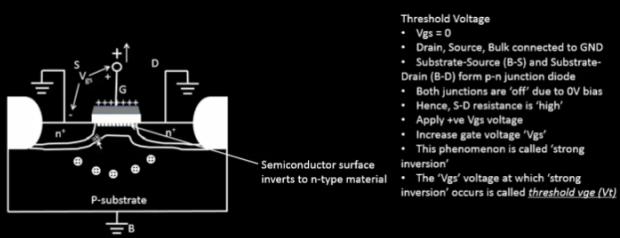
Vsb = +ve value

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#### Threshold Voltage

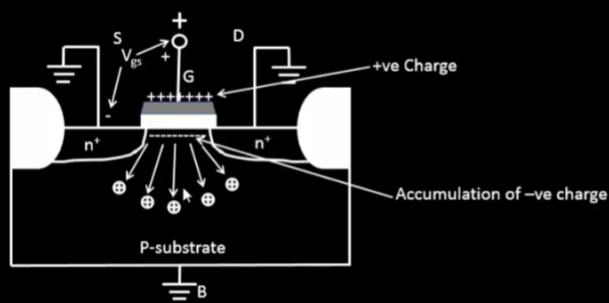
- $V_{gs} = 0$
- Drain, Source, Bulk connected to GND
- Substrate-Source (B-S) and Substrate-Drain (B-D) form p-n junction diode
- Both junctions are 'off' due to 0V bias
- Hence, S-D resistance is 'high'
- Apply +ve  $V_{gs}$  voltage
- Increase gate voltage ' $V_{gs}$ '
- This phenomenon is called 'strong inversion'
- The ' $V_{gs}$ ' voltage at which 'strong inversion' occurs is called **threshold vge ( $V_t$ )**

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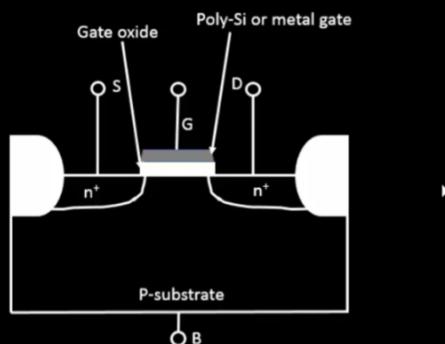
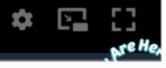
#### Threshold Voltage

- $V_{GS} = 0$
- Drain, Source, Bulk connected to GND
- Substrate-Source (B-S) and Substrate-Drain (B-D) form p-n junction diode
- Both junctions are 'off' due to 0V bias
- Hence, S-D resistance is 'high'
- Apply +ve  $V_{GS}$  voltage

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#### NMOS

- 4 terminal Device
- Consists of P-Substrate
- Isolation Region ( $\text{SiO}_2$ )
- $n^+$  Diffusion Region
- Gate Oxide
- Poly-Si or metal gate
- G – Gate
- S – Source
- D – Drain
- B – Body

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