The Power Bottleneck

How Back-Side Power Delivery Unlocks the Next Generation of Chip Scaling

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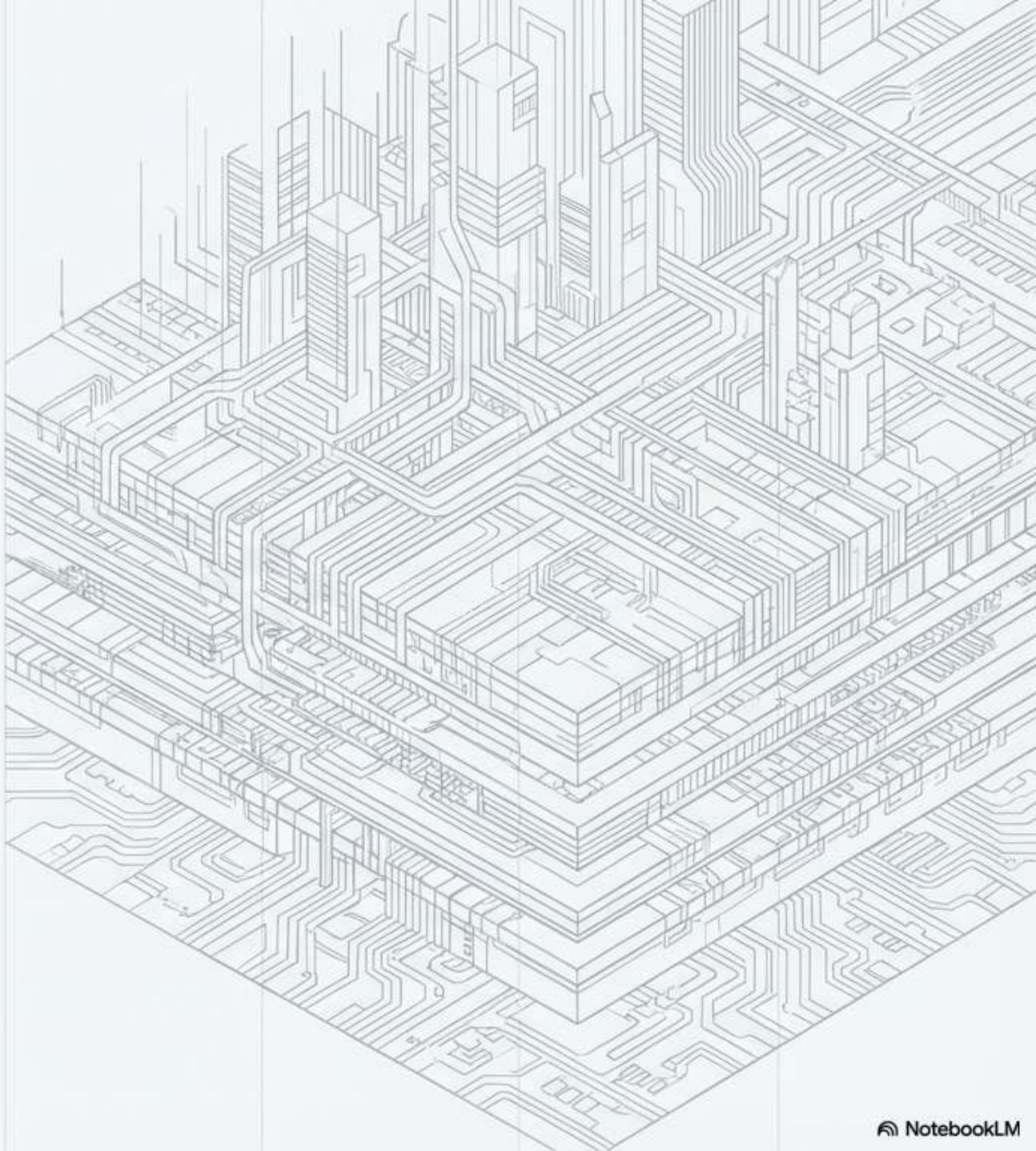


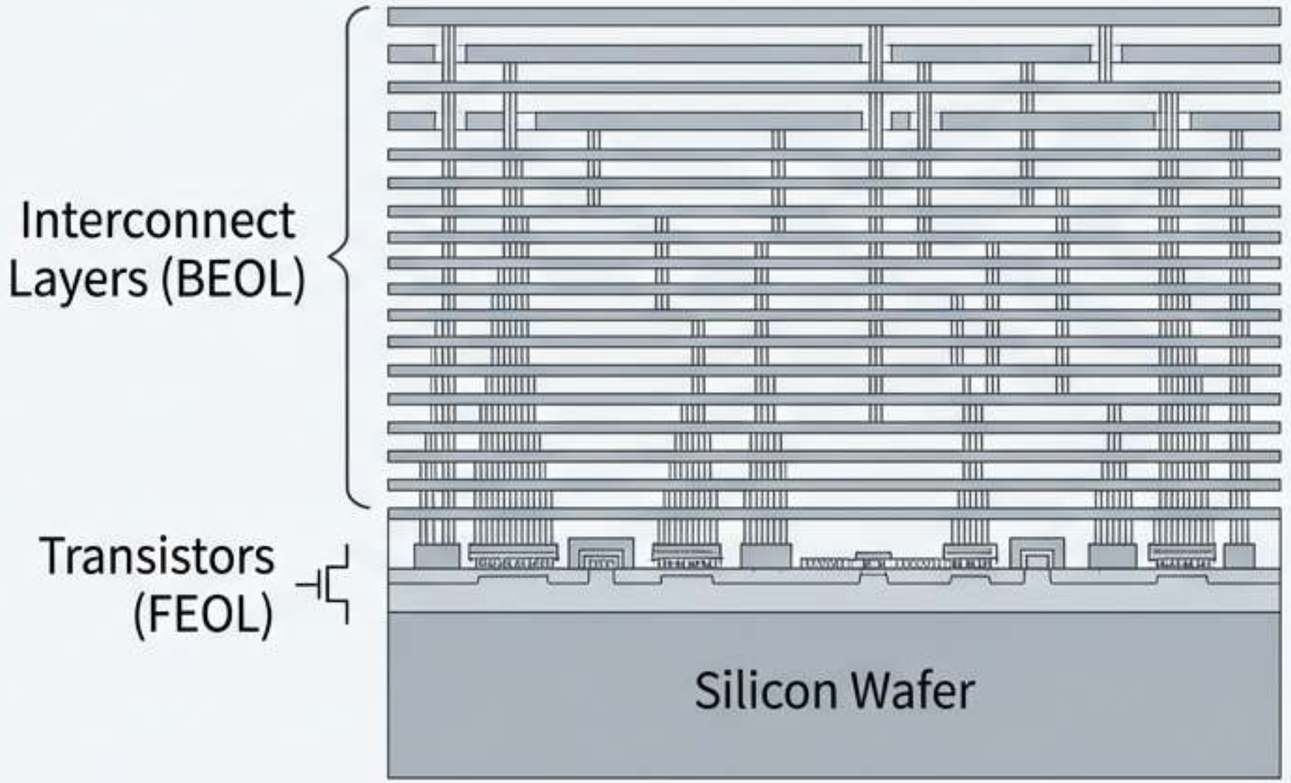
The Anatomy of a Modern Chip

Today’s chips are multi-story skyscrapers of circuitry, with with transistors at the bottom and a dense network of interconnects built on top.

Transistors (the “Front End of Line”) are fabricated on the silicon wafer.

Above them, a complex web of up to 17-18 metal layers provides the pathways for power and data signals.

All power and signals have traditionally been routed from this “front side”.



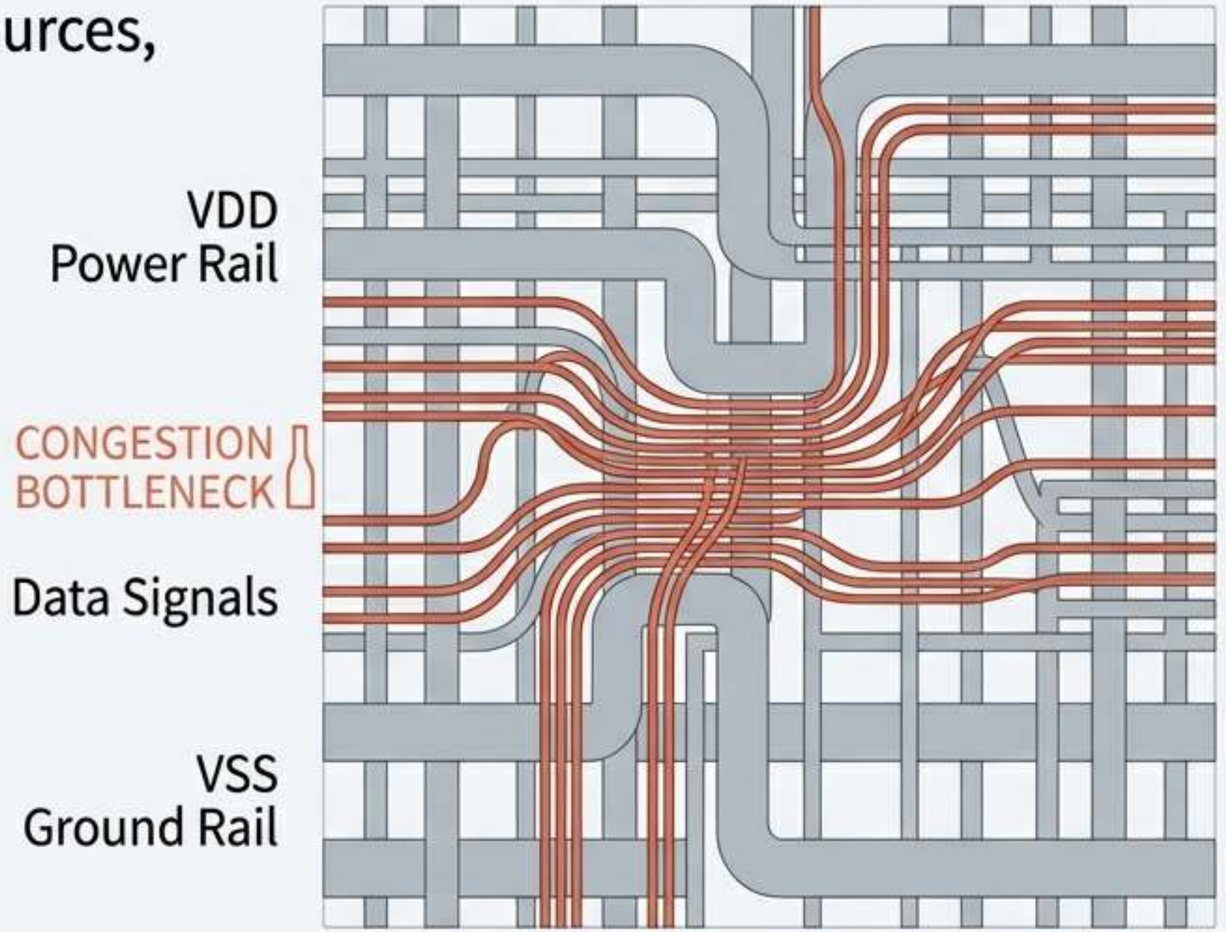
The Front-Side Traffic Jam

On the front side, power and signal lines compete compete for the same limited routing resources, creating congestion and inefficiency.

A significant portion of the valuable front-side routing tracks is consumed by wide power (VDD) and ground (VSS) lines.

Critical data signals must navigate this crowded environment, sharing space with the a power delivery network.

The power itself must travel a long and tortuous path from the top-most metal layers down to the transistors.

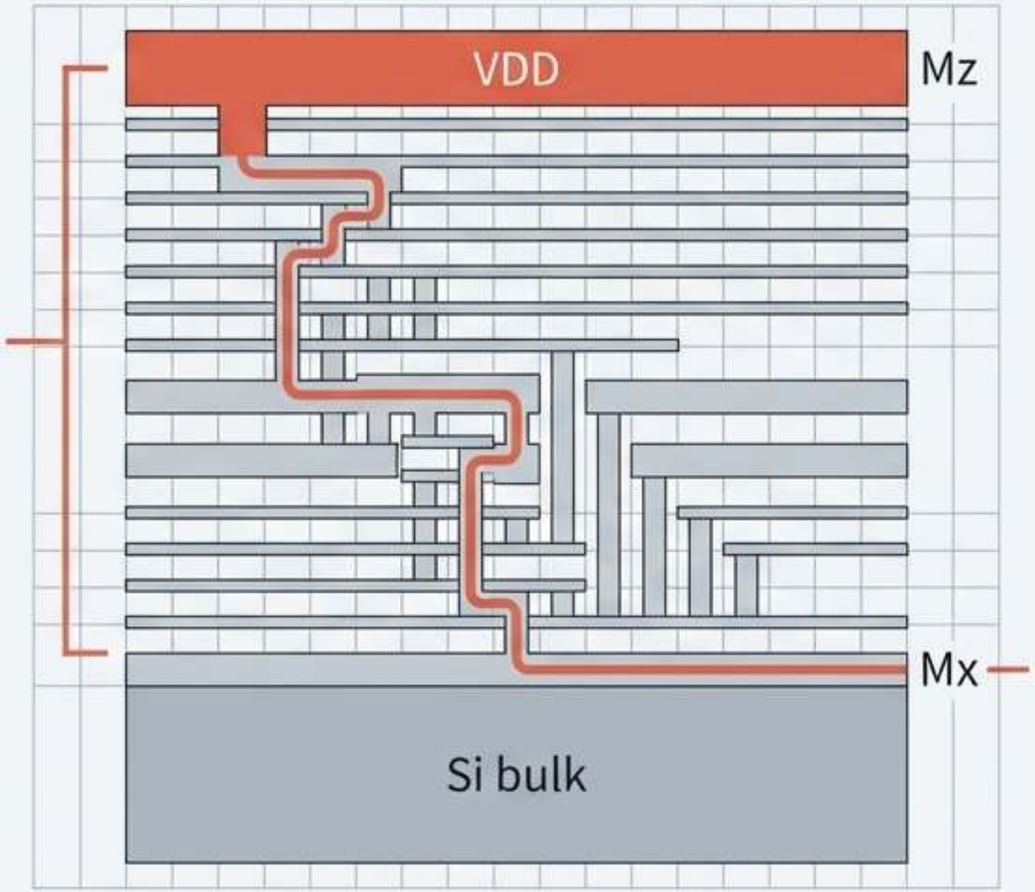


The High Cost of a Long Journey

Forcing power through 18 layers of metal and vias creates a path of **extremely** high electrical resistance.

~300 Ω

Resistance from the vertical journey

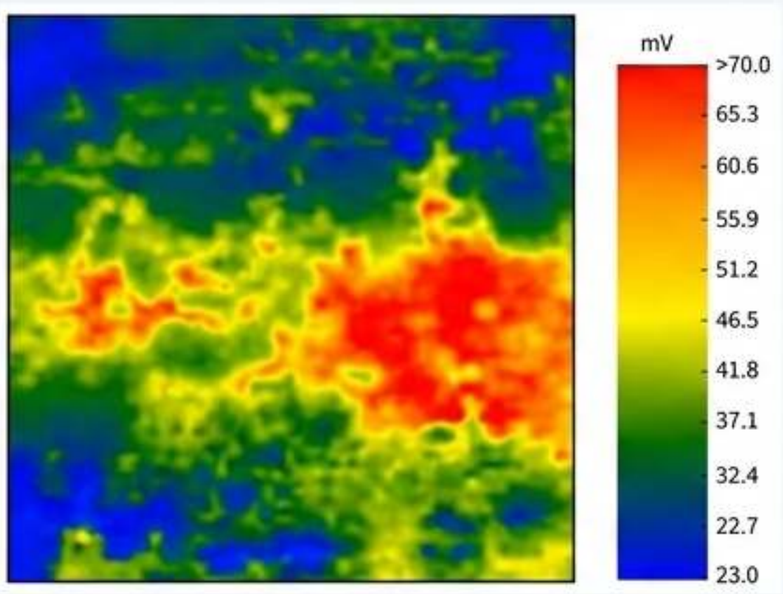


~170 Ω/µm

Additional resistance from the final M0 metal line

The Consequence: A Severe Power Deficit

This high resistance causes a significant voltage drop (IR Drop), starving the transistors of the power they need to perform optimally.



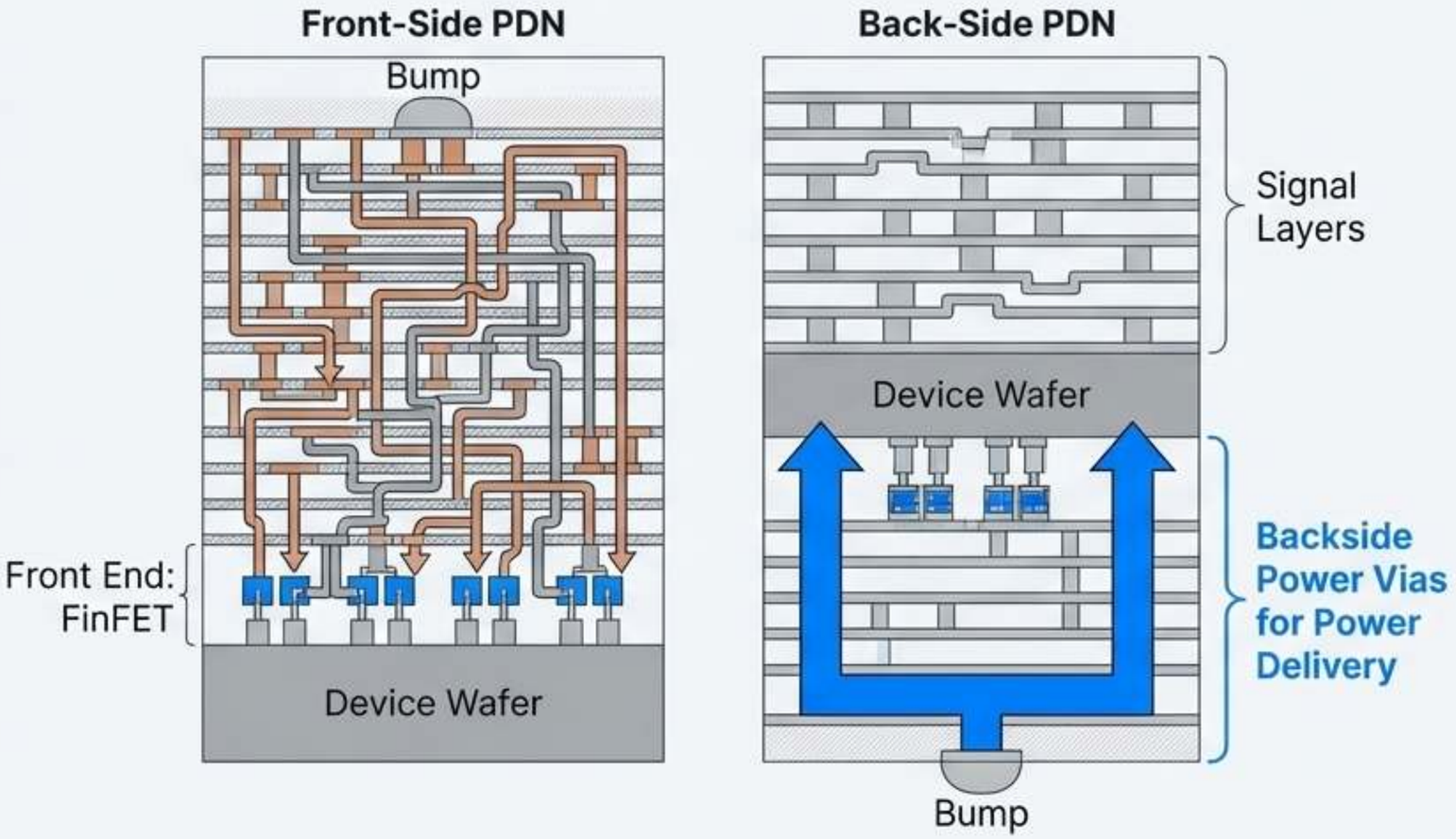
Front-Side Power Delivery: High IR Drop

The voltage that reaches the transistor is significantly lower than the voltage supplied at the package level, leading to reduced performance and increased heat.

What if we delivered power from underneath?

The Innovation: Back-Side Power Delivery

BS-PDN creates a dedicated, direct superhighway for power on the back side of the wafer, completely separating it from the signal interconnects.

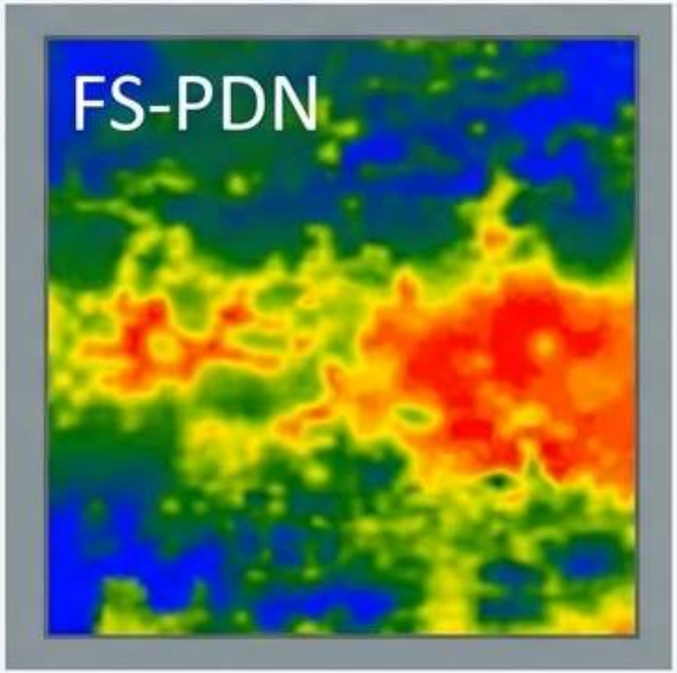


- Power is delivered directly to the transistors from below via "**Backside Power Vias**".
- This eliminates the long, high-resistance journey through the front-side metal stack.
- Signal interconnects now have the entire front-side routing resources to themselves.

Impact 1: Erasing the Power Deficit

By providing a direct, low-resistance path, BS-PDN minimizes IR drop and ensures transistors receive stable, robust power.

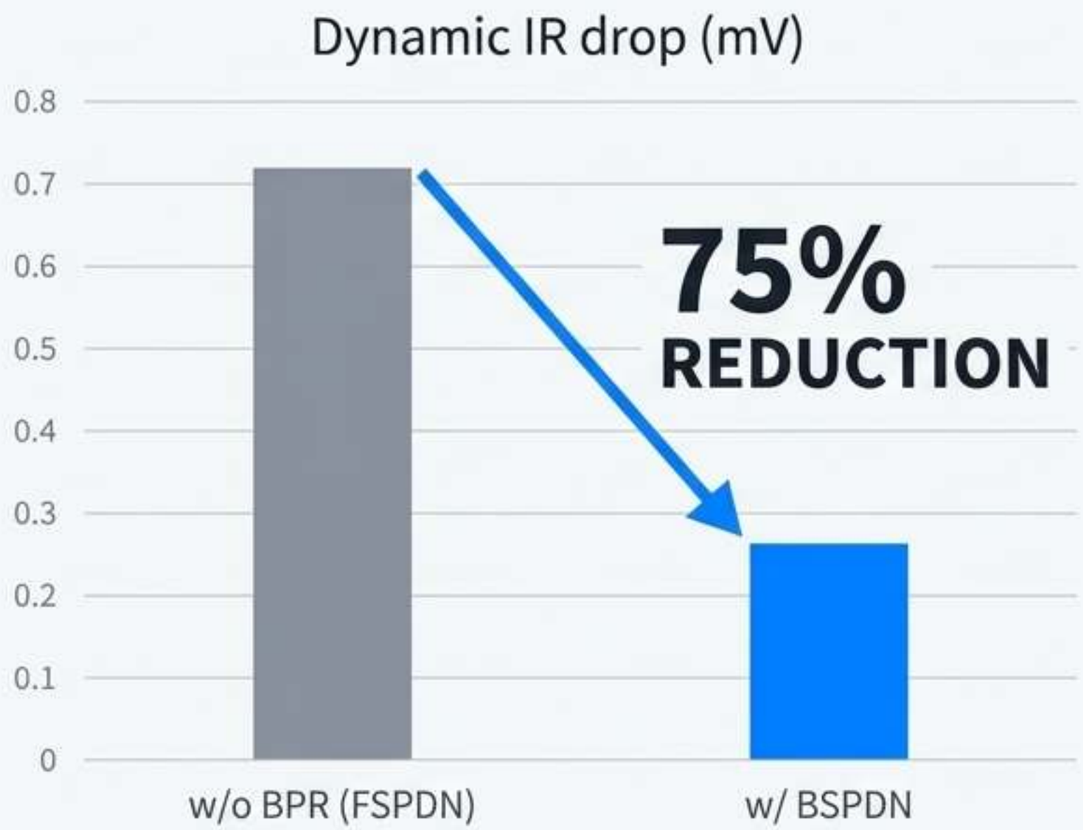
Before: High IR Drop

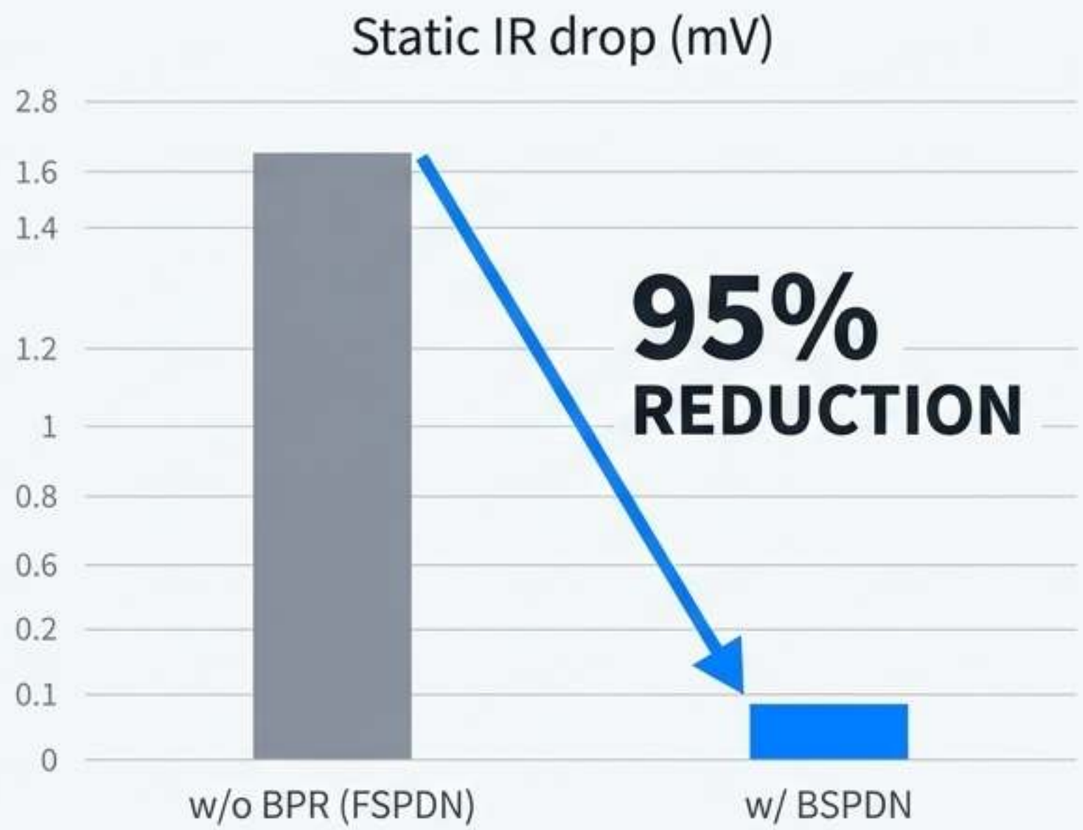


After: Minimal IR Drop

The Performance Gain, Quantified

The improvement in power delivery translates to a massive reduction in both dynamic and static IR drop.





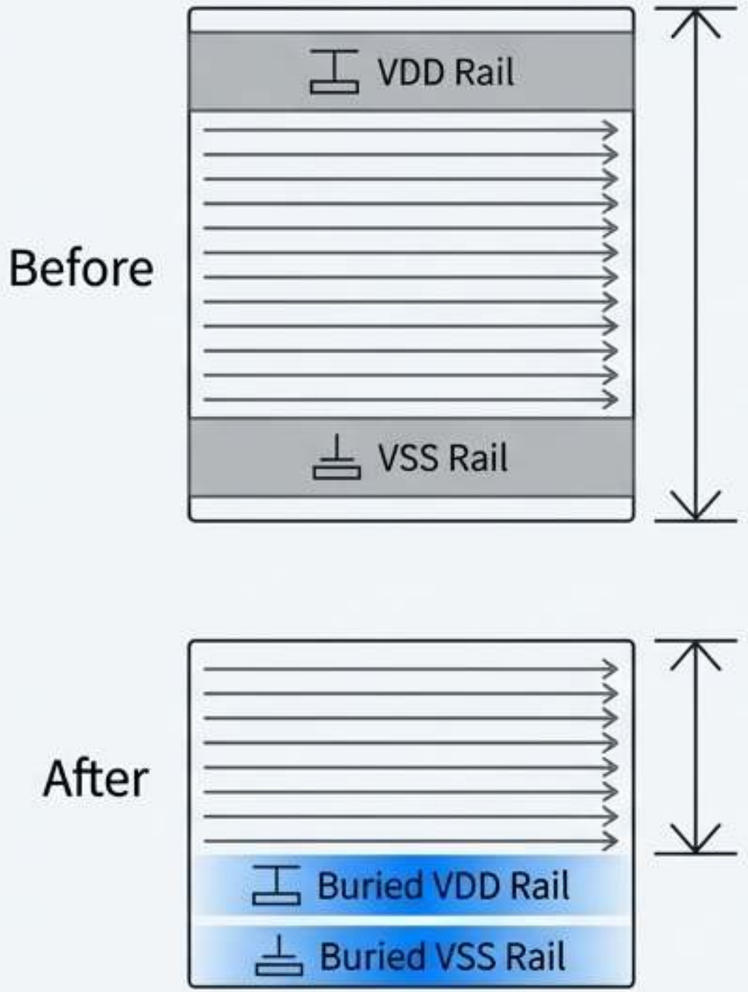
Impact 2: Gaining New Room for Density

Moving the wide power rails to the back side allows for a significant reduction in the height of standard cells.

In traditional designs, bulky VDD and VSS rails dictate the height of a logic cell.

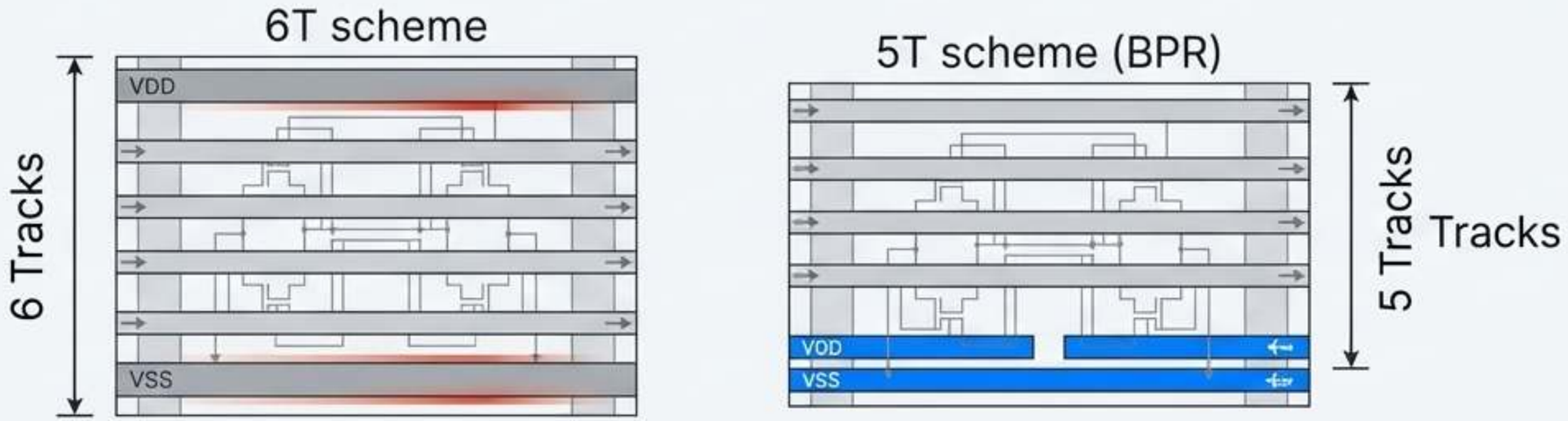
By “burying” these power rails underneath the transistors, the cell height can be compressed without sacrificing any tracks for signal wiring.

This technique is known as Buried Power Rail (BPR).



The Density Gain, Quantified

BS-PDN with Buried Power Rails enables a direct reduction in cell area, allowing more transistors to be packed into the same space.



23% SMALLER

Standard Cell Area

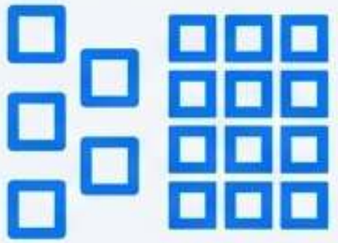
The BS-PDN Advantage: A Trifecta of Gains

PERFORMANCE

Drastically reduced IR drop ensures transistors operate at their peak potential.

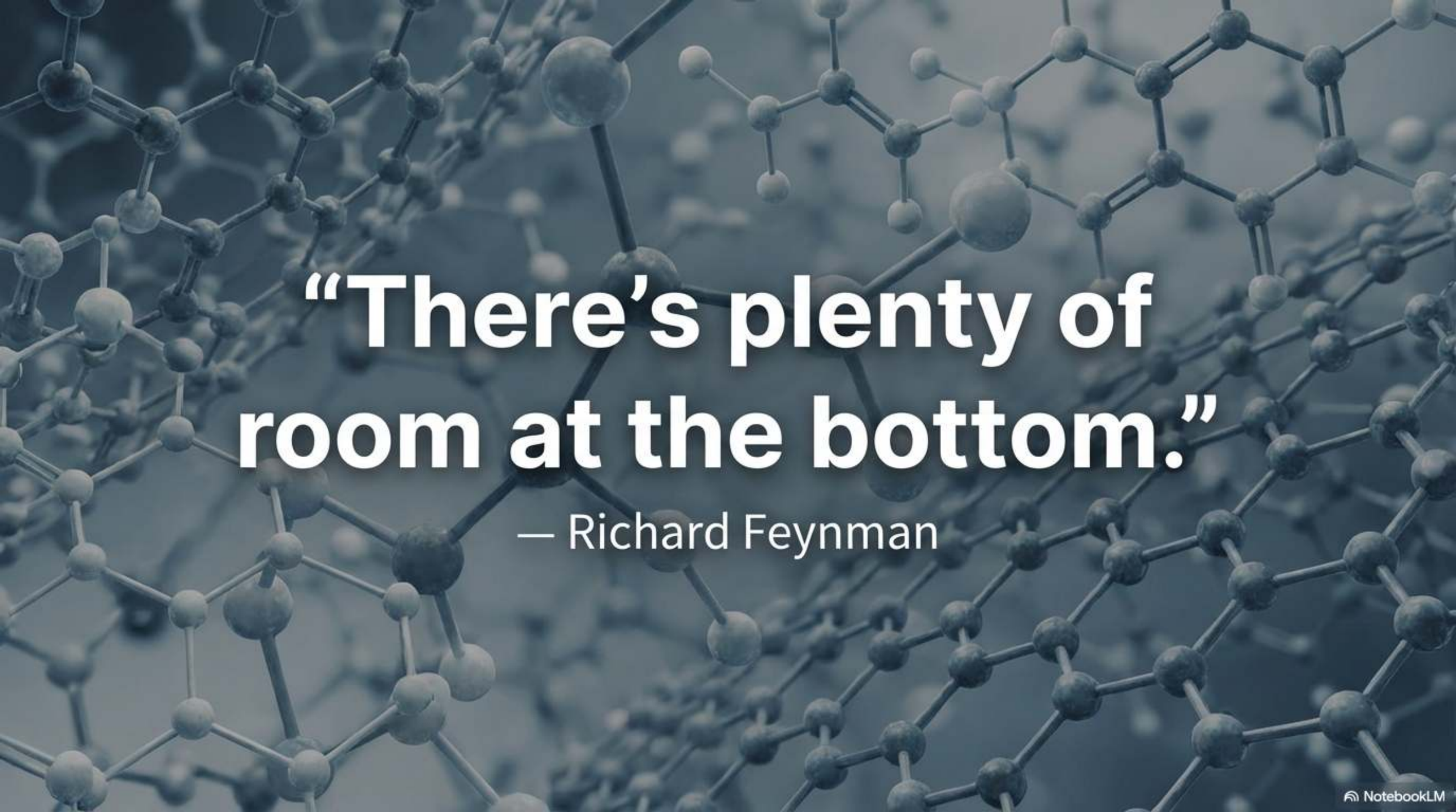
EFFICIENCY

A lower resistance power network reduces wasted energy and heat.



DENSITY

Smaller standard cells enable more logic to be packed on a chip, continuing the path of scaling.


“There’s plenty of room at the bottom.”
— Richard Feynman
NotebookLM