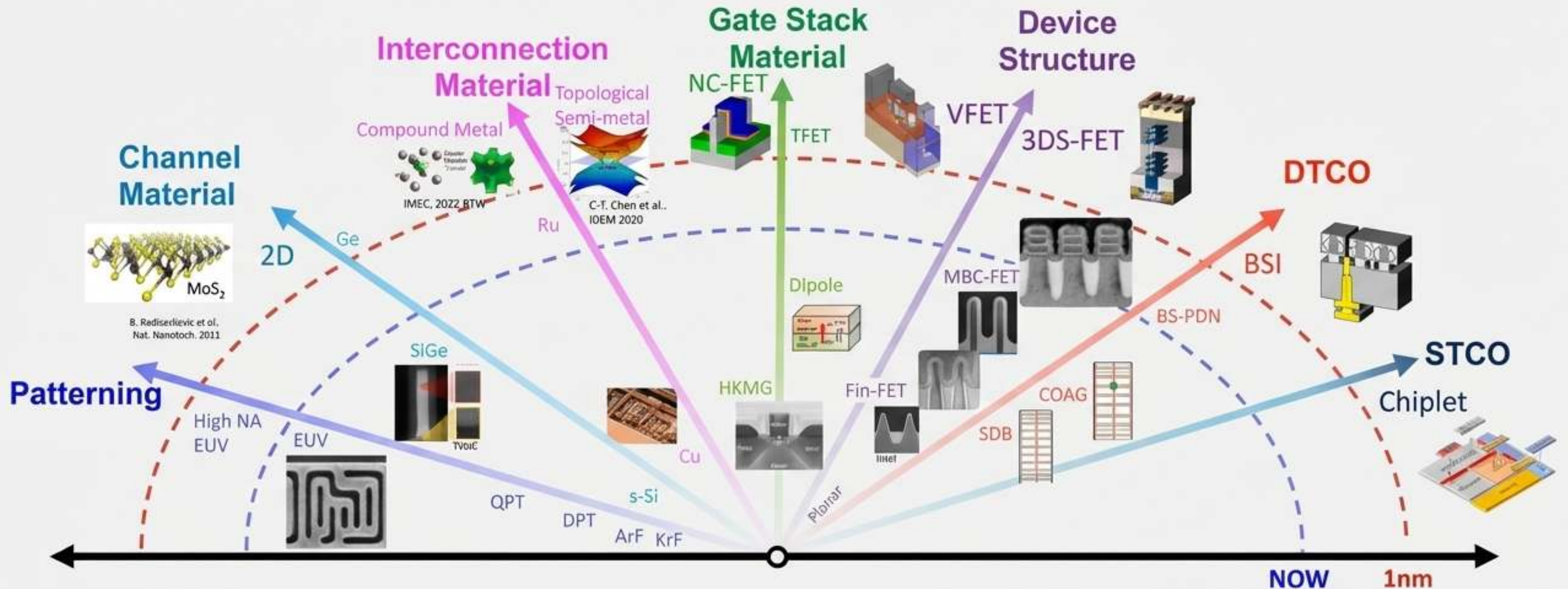


# **The Roadmap to 1nm and Beyond**

Navigating the Six Vectors of CMOS Innovation

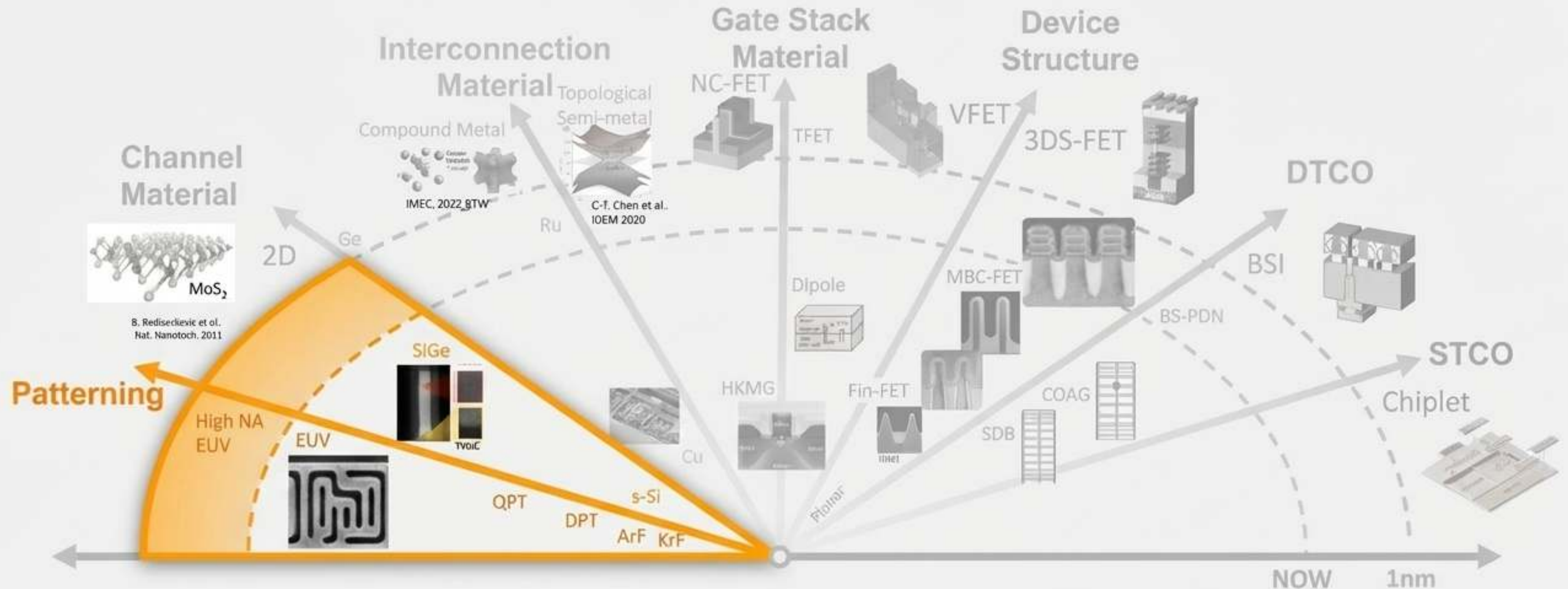
# The End of Simple Scaling Requires a New Map

For decades, Moore's Law provided a simple path forward: shrink the transistor. That era is over. Continuing performance gains toward the 1-nanometer node and beyond requires simultaneous, coordinated innovation across six critical and interconnected fronts. This diagram is our roadmap for exploring that future.



# Vector 1: Patterning — Drawing the Blueprints of Computation

The ability to print infinitesimally small features onto silicon is the most fundamental step in semiconductor manufacturing. As we approach atomic limits, the light we use to draw these circuits must evolve.



# A Journey to Finer Light



## Legacy: ArF (Argon Fluoride) Lithography

**What:** The workhorse of the industry for decades, using deep ultraviolet light (193nm) to pattern chips.

**Why it hit a limit:** Wavelength became too large to pattern the smallest features required by advanced nodes without complex and costly multi-patterning techniques.

## Now: EUV (Extreme Ultraviolet) Lithography

**What:** A revolutionary shift to a much shorter wavelength of light (13.5nm), enabling the patterning of features for 7nm and 5nm nodes.

**Why it was necessary:** Drastically simplifies the manufacturing process for leading-edge chips and enables continued scaling.

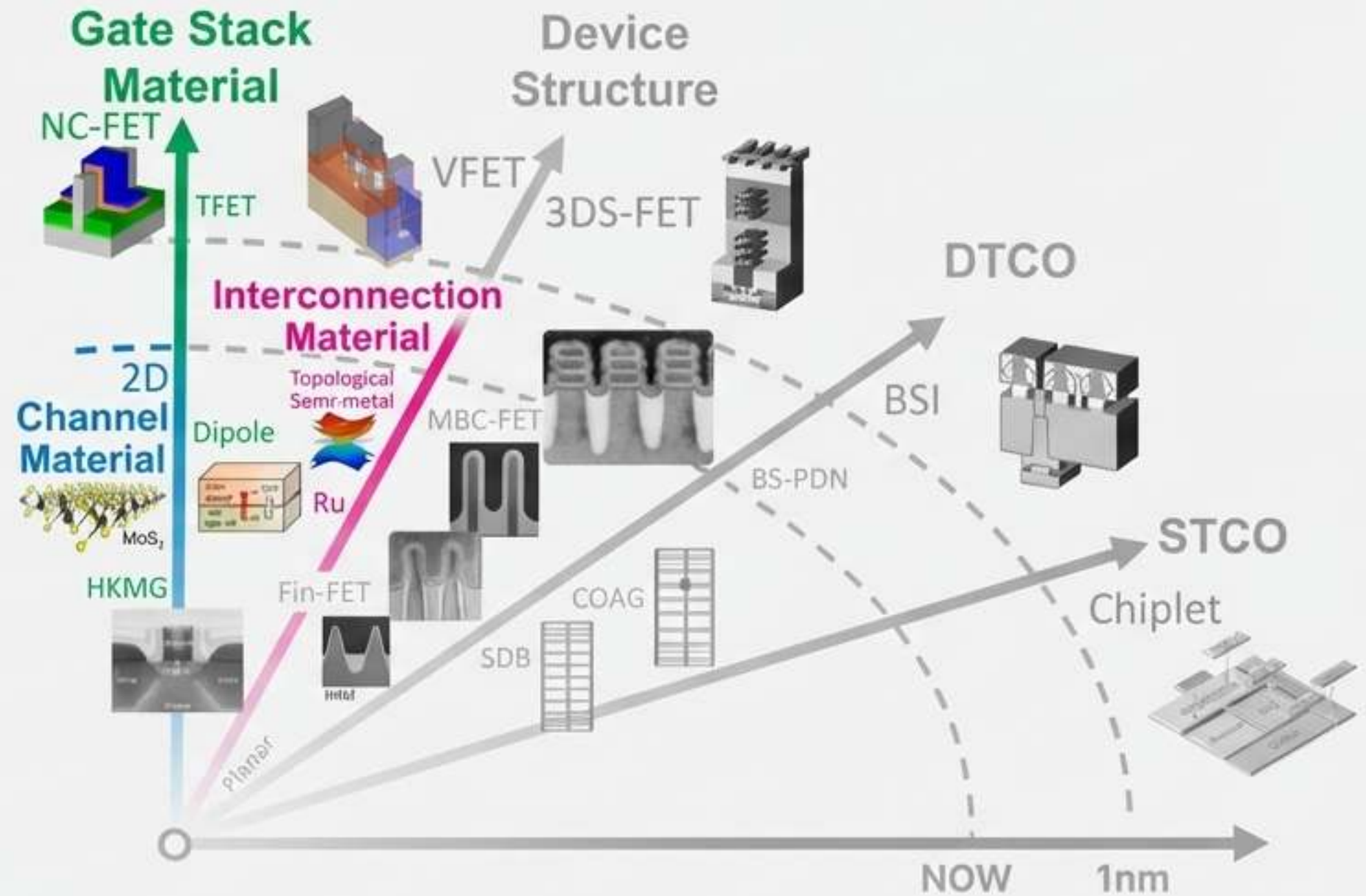
## Next: High NA (Numerical Aperture) EUV

**What:** The next generation of EUV, using more complex optics to achieve even higher resolution.

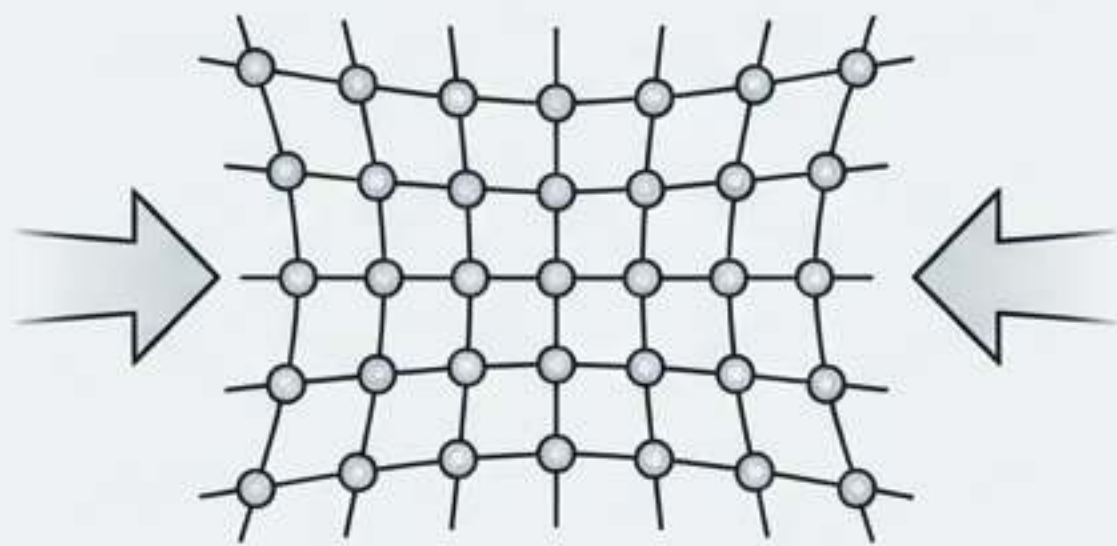
**Why it's the future:** Essential for pushing beyond the 3nm node and defining the features of chips at the 1nm scale.

# Vectors 2, 3 & 4: The Fundamental Materials Revolution

A modern transistor is a marvel of material science. To continue scaling, the very atoms we use for the channel, the interconnect wiring, and the gate stack must be re-engineered for higher performance and lower power.



# Innovating the Channel: Beyond Silicon



## Boosting Silicon

**Technology:** s-Si (Strained Silicon) & SiGe (Silicon-Germanium)

**What:** Techniques that intentionally stretch or compress the silicon crystal lattice.

**Why:** This strain allows electrons to flow with less resistance, increasing transistor switching speed and performance without changing the fundamental material.



## Replacing Silicon

**Technology:** Ge (Germanium) & 2D Materials (e.g.,  $\text{MoS}_2$ )

**What:** The move to entirely new channel materials. 2D materials are single-atom-thick sheets with exceptional electronic properties.

**Why:** They offer intrinsically higher carrier mobility and superior gate control in ultra-thin form factors, making them a leading candidate for the transistors of the post-FinFET era.

# Reinventing the Wires and the Gates

## The Interconnect Challenge

**The Problem:** As wires (interconnects) shrink, the resistance of Copper (Cu) skyrockets, creating a performance bottleneck.

**The Evolution:**

- **Now:** Advanced processing of Copper (QPT).
- **Next:** Moving to new metals like Ruthenium (Ru) and advanced Compound Metals which have better resistance properties at nanoscale dimensions.
- **Future:** Exploring exotic materials like Topological Semimetals for near-lossless conductivity.

## The Gate Stack Challenge

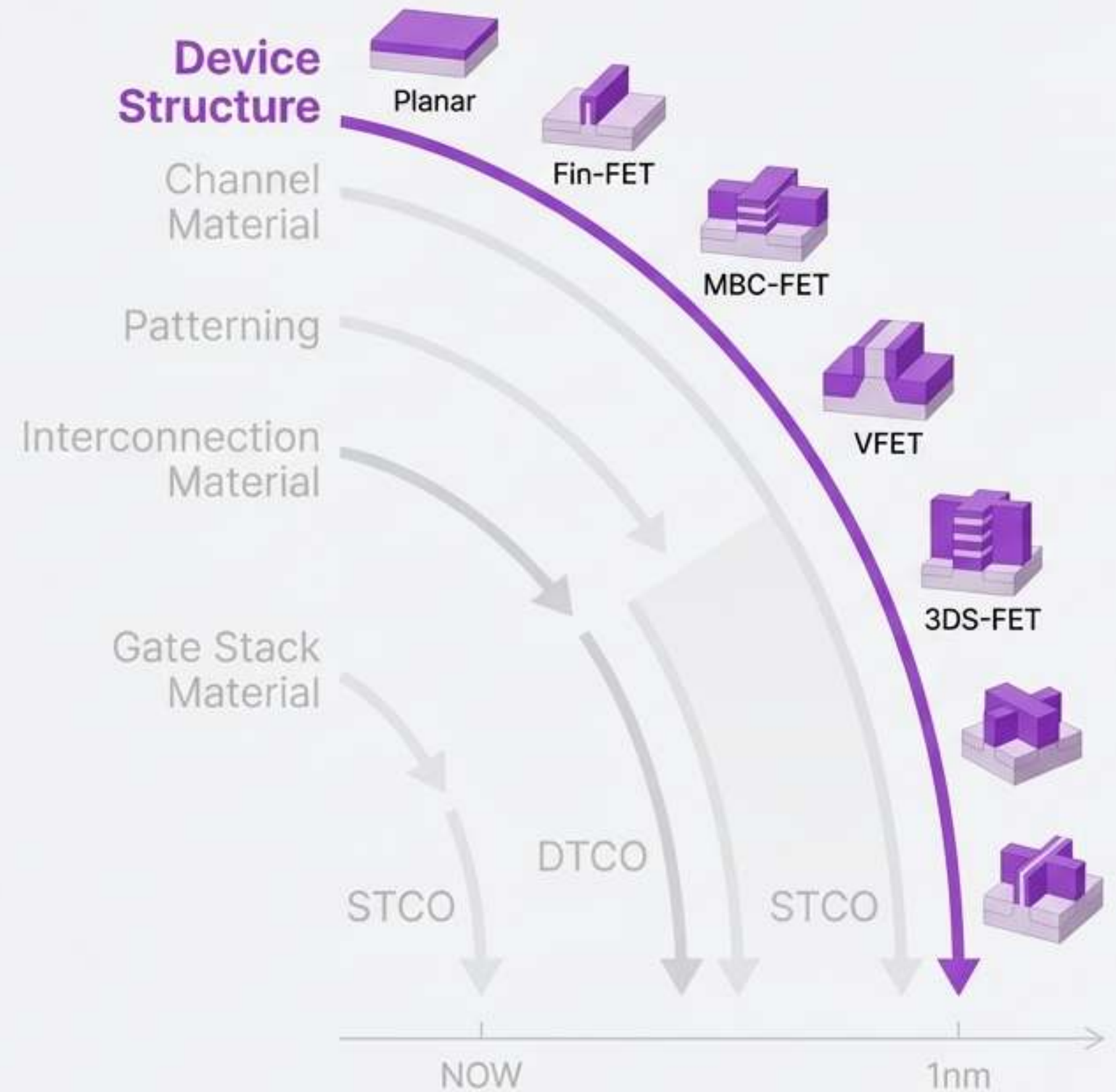
**The Problem:** Traditional silicon dioxide gates became so thin they leaked current, wasting power.

**The Evolution:**

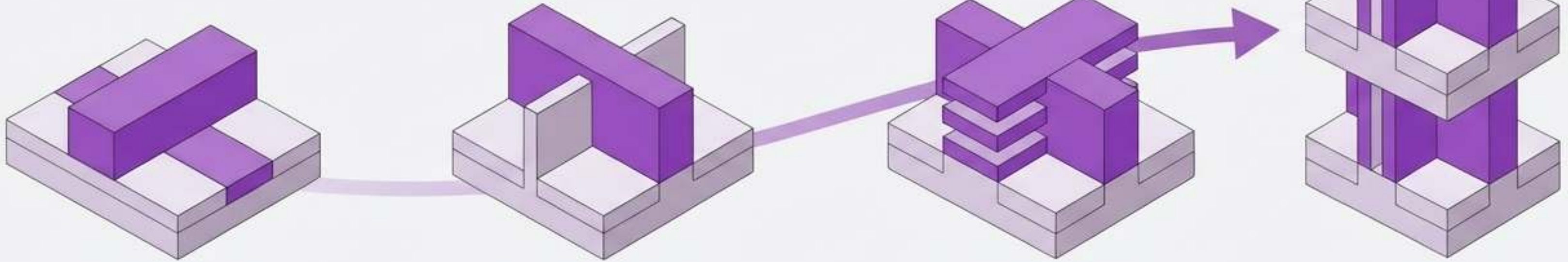
- **Past:** HKMG (High-k Metal Gate) was a landmark innovation that plugged this leakage, enabling further scaling.
- **Future:** Technologies like NC-FET (Negative-Capacitance FET) and TFET (Tunnel FET) are being researched to overcome the fundamental voltage limits of transistors, promising a dramatic reduction in power consumption.

# Vector 5: Device Structure — Building in Three Dimensions

As shrinking features further became difficult, engineers turned to a new dimension: height. The evolution of the transistor is a story of moving from a flat, 2D plane to complex 3D architectures for superior control and density.



# The Architectural Leap: From Flat to Vertical



## Past: Planar FET

**What:** The classic, flat transistor. The gate controls the channel from only one side.

**Why it was replaced:** Suffered from poor electrostatic control and severe current leakage at smaller scales ('short-channel effects').

## Now: FinFET (Fin Field-Effect Transistor)

**What:** The current industry standard. The channel is a 3D 'fin' and the gate wraps around it on three sides.

**Why it works:** Provides vastly superior gate control, slashing leakage and enabling scaling down to the 5nm node.

## Next: MBC-FET / VFET

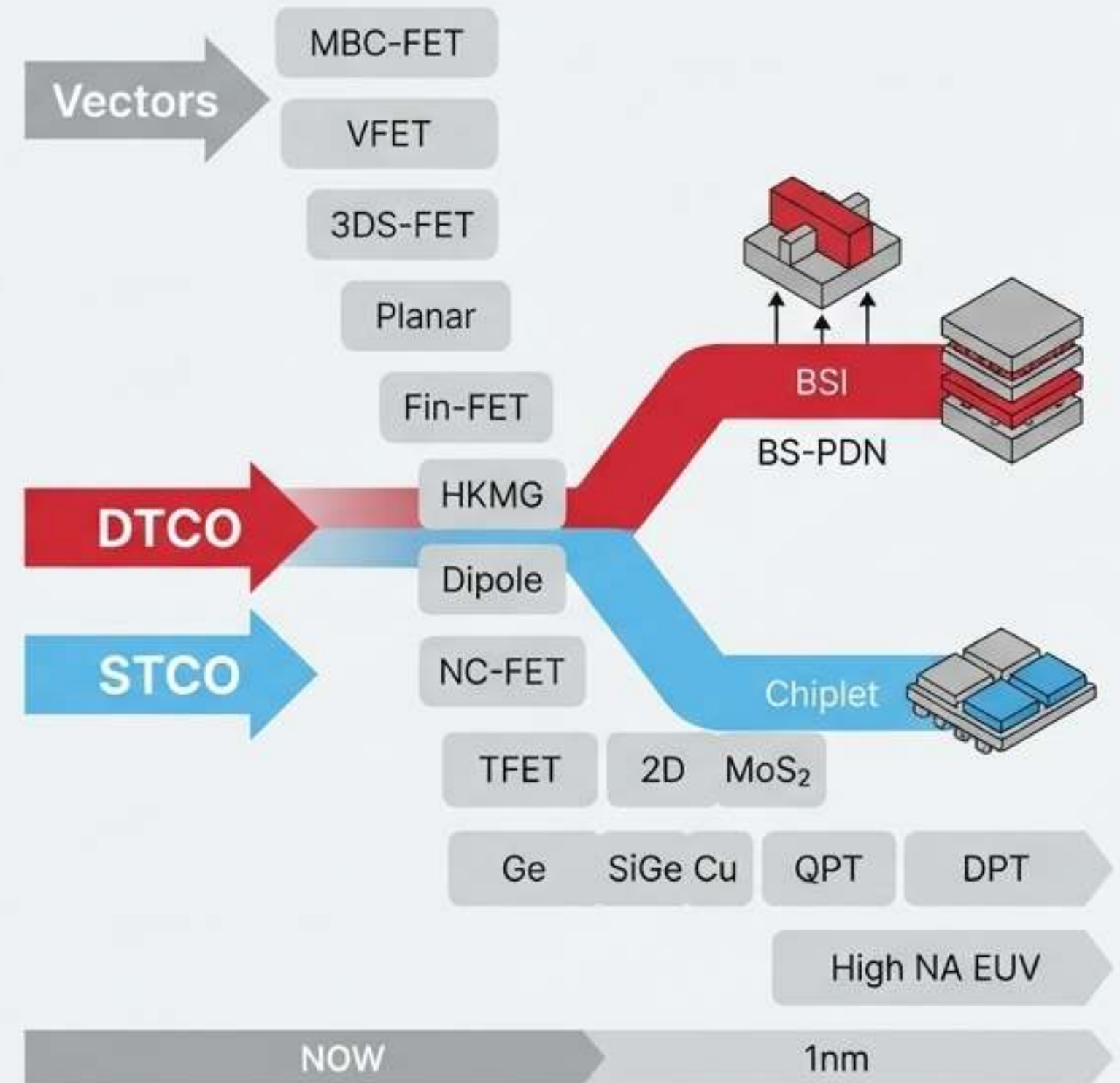
**What:** MBC-FET (Multi-Bridge Channel) or 'Gate-All-Around' FETs wrap the gate around all four sides of nanosheet channels. VFETs (Vertical FETs) stack transistors on top of each other.

**Why they are the future.**

**Why they are the future:** MBC-FET offers the ultimate electrostatic control. VFET offers a path to dramatically increasing transistor density beyond the limits of 2D floor space.

# Vector 6: System Integration — Smarter Design is the New Scaling

The greatest future gains will not come from a single material or device, but from optimizing how they all work together. Design-Technology Co-Optimization (DTCO) and System-Technology Co-Optimization (STCO) represent a paradigm shift from scaling components to scaling the entire system.

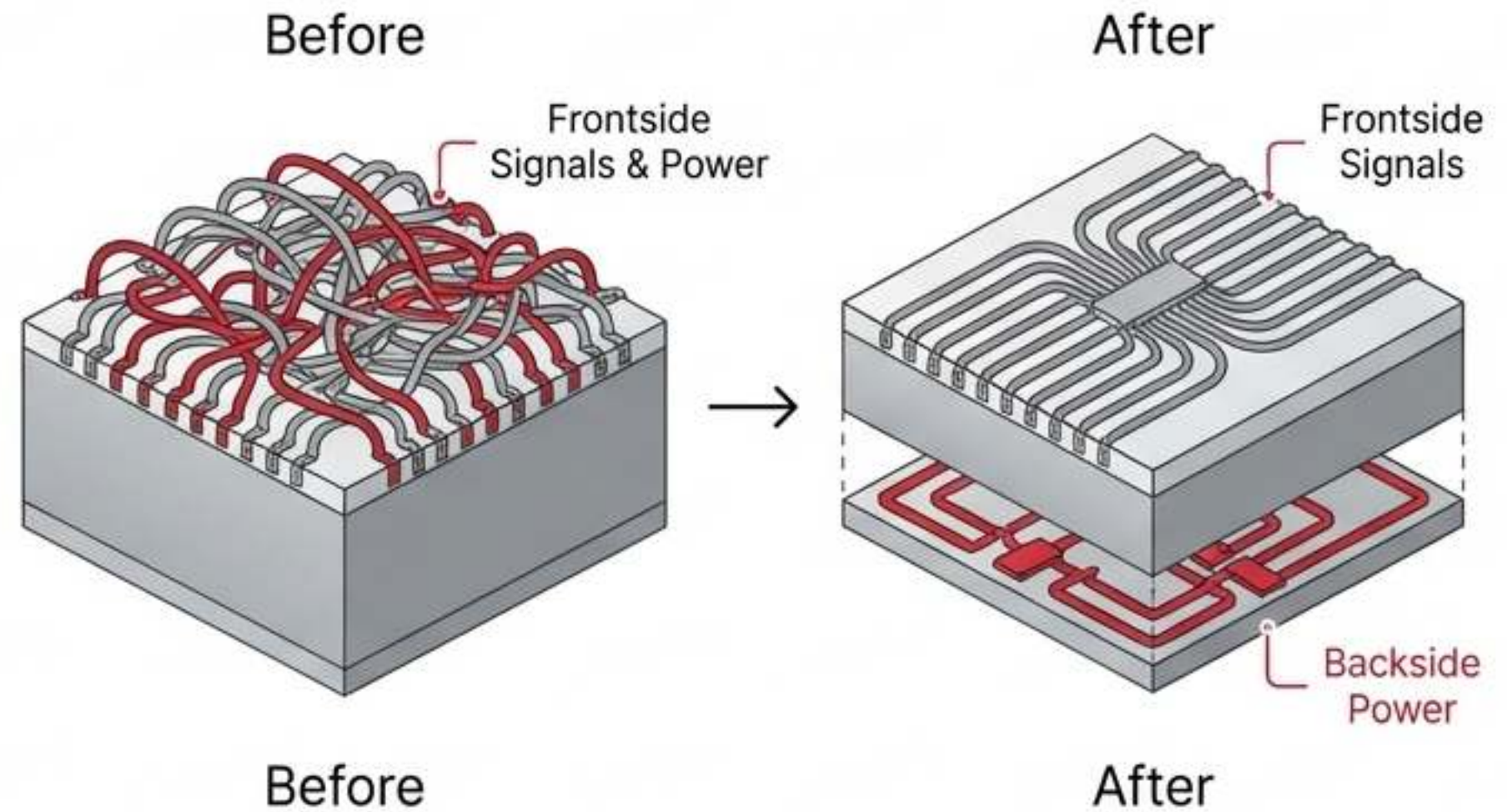


# DTCO: Design and Technology in Harmony

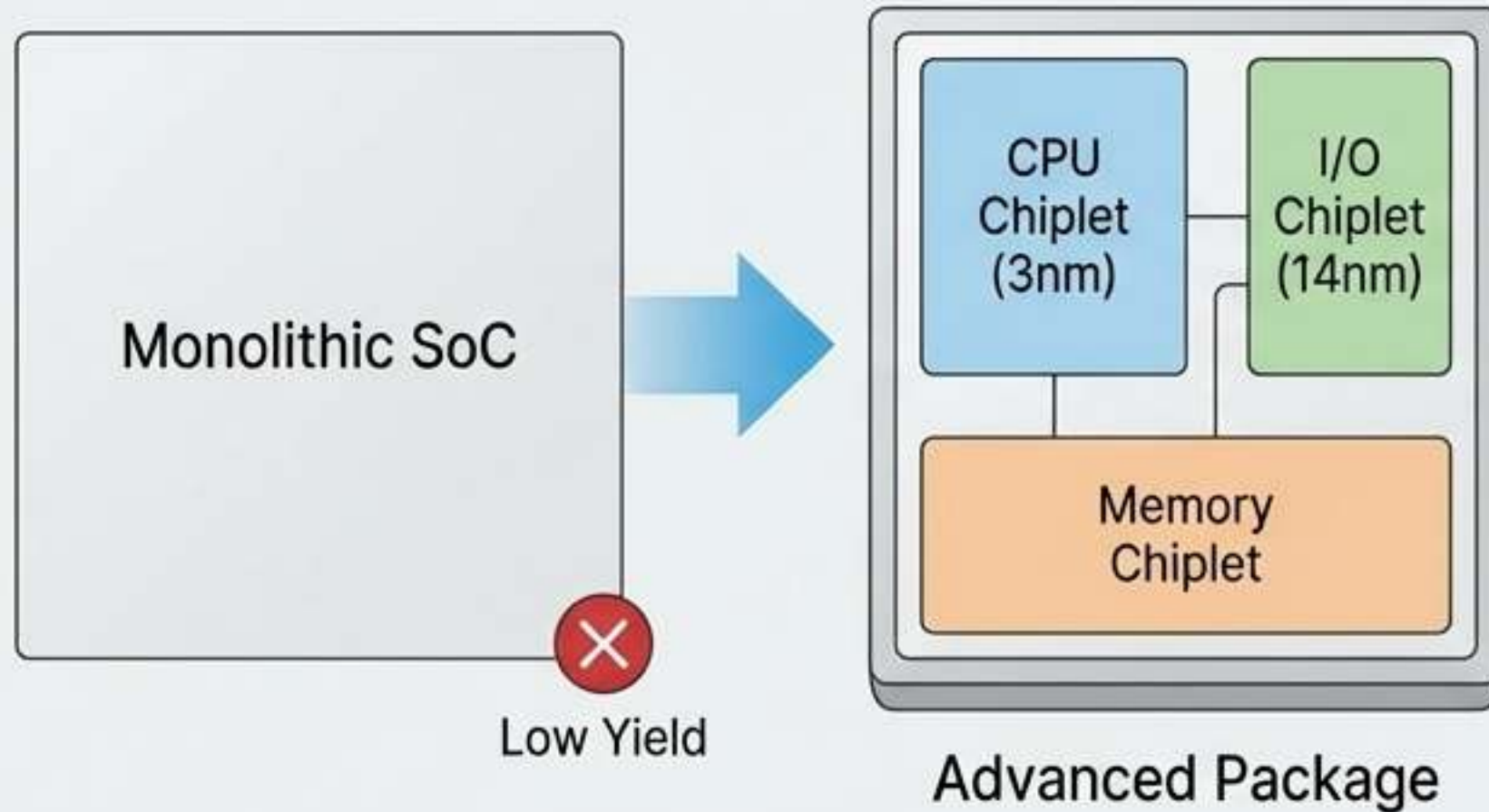
**What it is:** A design philosophy where chip architecture and the manufacturing process are developed in tandem. The constraints and opportunities of the foundry's technology directly inform the chip's design from day one, and vice-versa.

**Why it Matters:** It unlocks performance and density gains that are impossible if design and manufacturing are treated as separate, sequential steps. It's about finding clever architectural solutions to physical limitations.

## Key Enabler: BS-PDN (Backside Power Delivery Network)



# STCO: The Inevitable Rise of the Chiplet

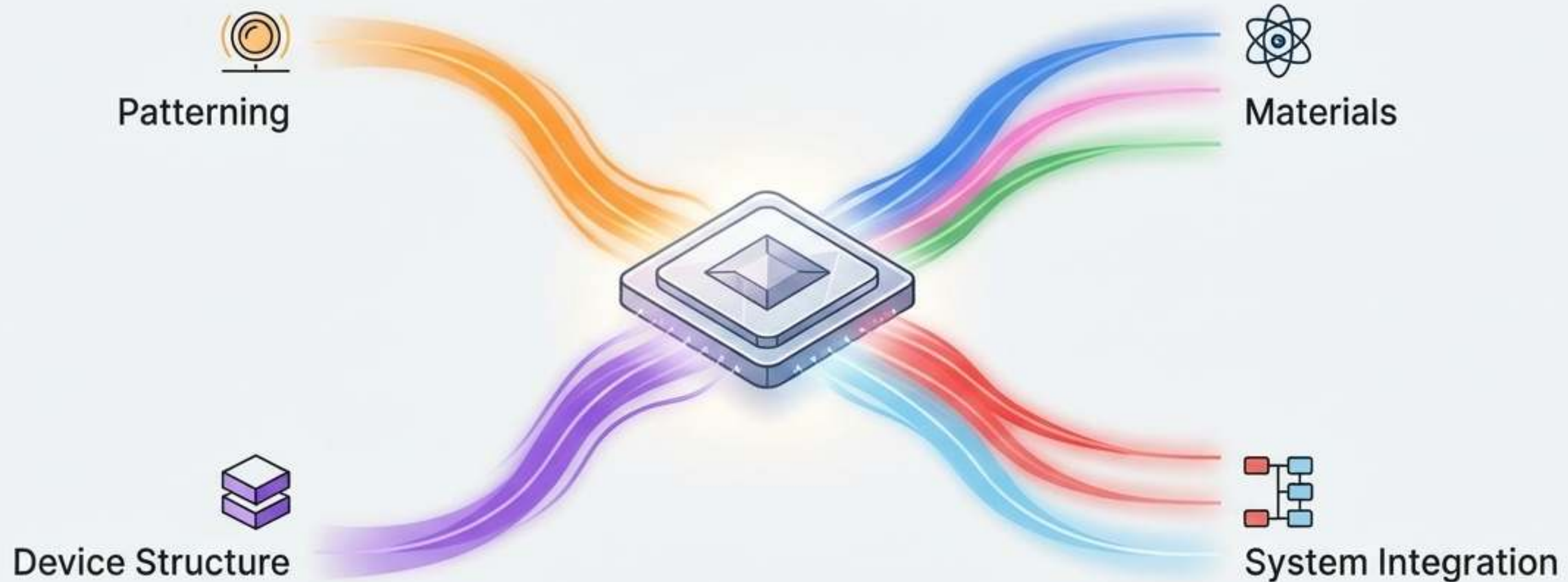


**What it is:** Instead of building one giant, monolithic chip, a system is constructed from multiple smaller, specialized dies ("chiplets") in an advanced package.

## Why it Matters:

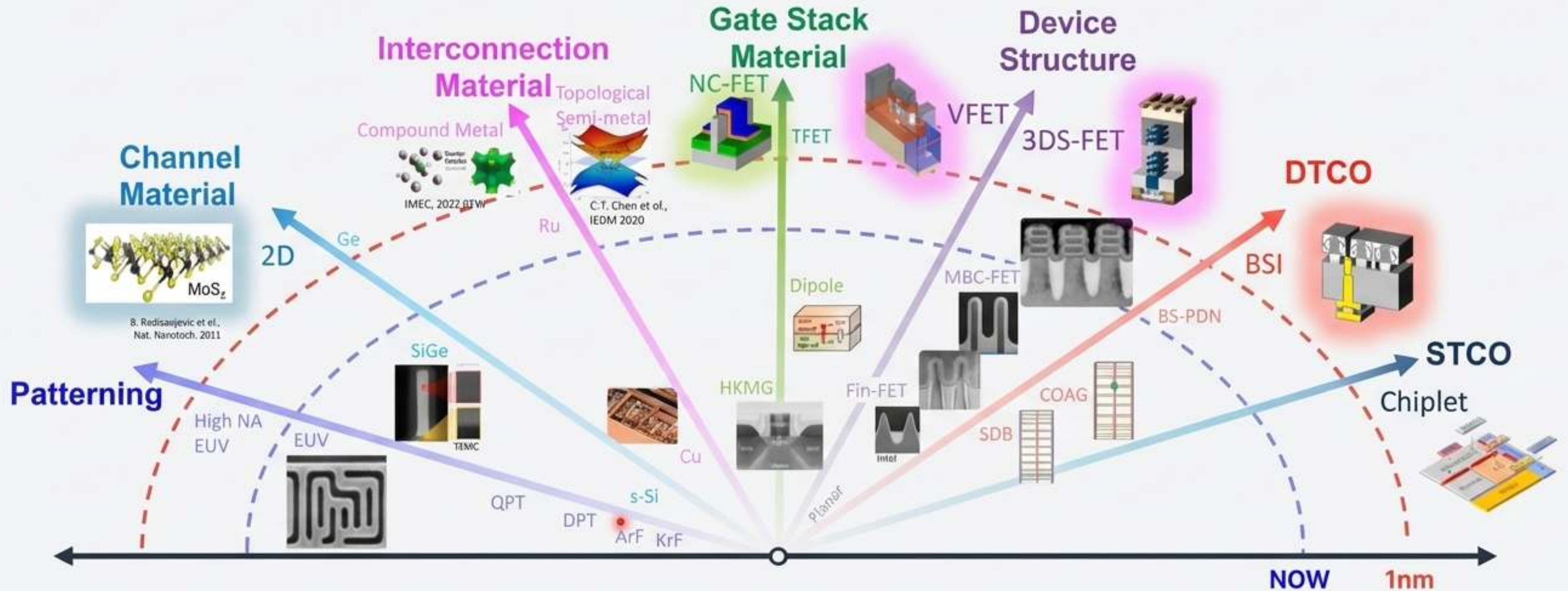
- **Yield:** It's easier to produce multiple small, perfect dies than one enormous one.
- **Flexibility:** Allows designers to mix and match process nodes. A high-performance CPU core can be on a 3nm process, while I/O controllers are on a more mature, cheaper 14nm process.
- **Scalability:** Enables the creation of systems far larger and more complex than any single chip could be. This is a key tenet of the 'More than Moore' era.

# The New Scaling: A Convergence of Innovation



The path to 1nm and beyond is not linear. It is a convergence. It demands simultaneous breakthroughs in how we **pattern** circuits, the **materials** we use, the 3D **structures** we build, and the **integrated systems** we design. The simple act of shrinking is replaced by the complex art of co-optimization.

# The Roadmap, Revisited



This is the unified strategy for the future of computation. Each path on this map, from the atomic level of 2D materials to the system level of chiplets, is a critical vector in the relentless pursuit of performance. The journey continues.