Module 3 Assignment

Bandgap Reference Design and Simulation using Xschem

Objective

This assignment guides you through the design and simulation of a Bandgap Reference Circuit using Xschem and Ngspice. You'll validate key behaviors like temperature stability and line regulation.

Instructions

1. Open the schematic provided in the GitHub repo under `Bandgap_SCMB_Xschem/`.
2. Run DC simulations to extract output voltage (V_{ref}) at various V_{DD} values and temperatures.
3. Observe the startup behavior using transient analysis.
4. Record key performance metrics in the table below.

Characterization Table

S.No	V_{DD} (V)	Temp (°C)	V_{ref} (V)	Line Reg. (mV/V)	Startup Time (ns)
1	0.8	27			
2	0.9	27			
3	1.0	27			
4	1.0	-40			
5	1.0	125			

How to Ensure Unique Results

To make your simulation unique and traceable, use this resistor-based method:

- Select a resistor value using the ASCII sum of your username:

  ```
  Runiq net1 net2 <ASCII_sum_in_ohms>
  ```

  Example: Username `anita` → ASCII (97+110+105+116+97 = 525) Use:

  ```
  Runiq bias out 525
  ```

- Use this resistor in the startup branch or bias network—its value will slightly alter V_{ref}.

Submission Checklist

- Screenshot of Xschem schematic
- Filled characterization table (PDF or image)
- Transient waveform showing startup
- SPICE netlist with unique resistor

Reminder: You are expected to complete this module within 3 days after completing Module 2 assignment.