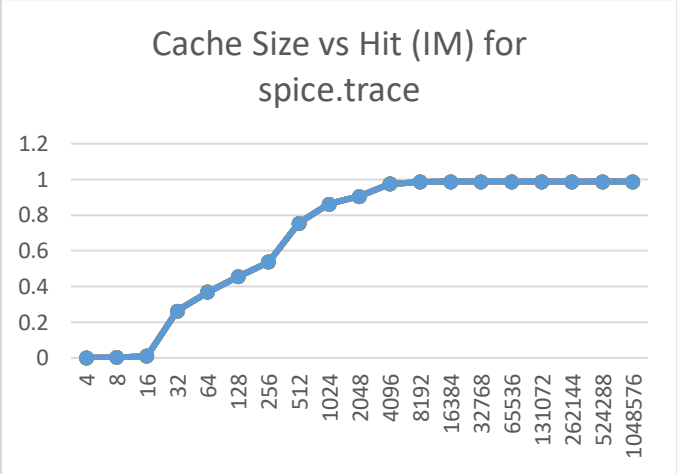
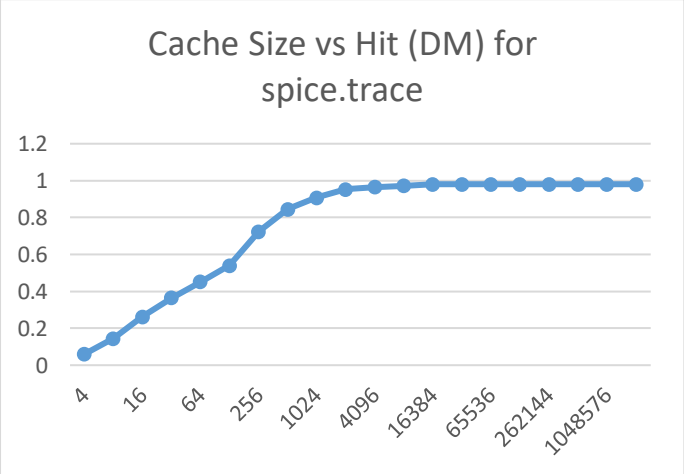
COP 290: Cache Simulator Report

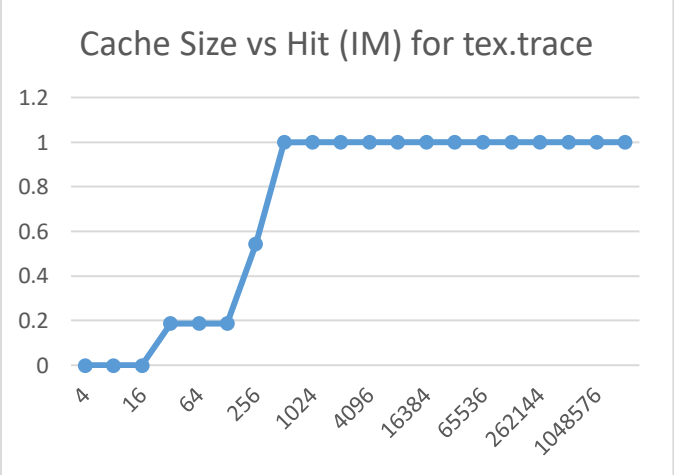
Submitted by:
Suyash Agrawal (2015CS10262)
Ankesh Gupta (2015CS10435)

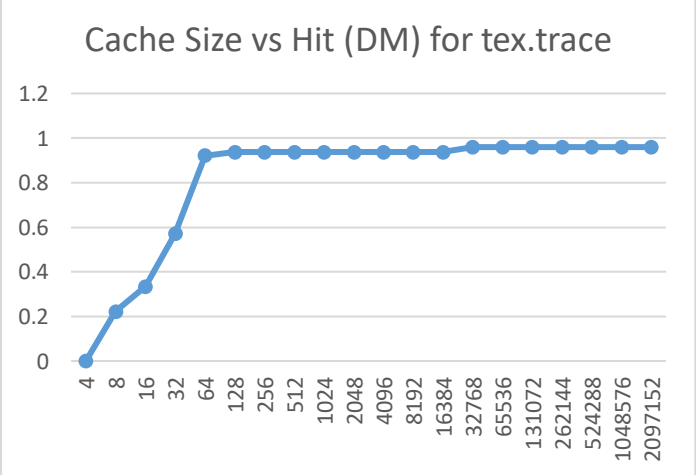
Analysing Cache Size Effects

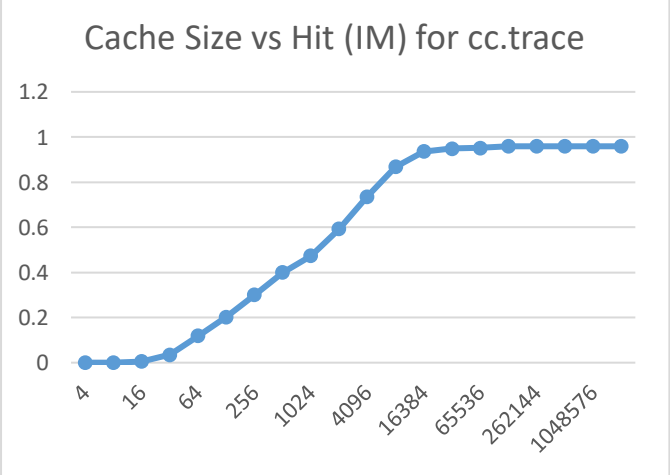
Charts

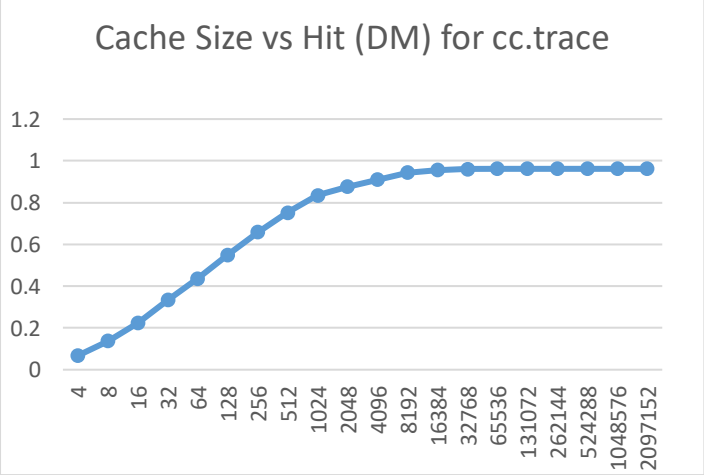












Hit rate of the cache as a function of cache size

spice.trace

CS	I- vs D-	BS	Assoc	Write	Alloc	Instructions Misses	Instructions Repl	Instructions Hit Rate	Data Misses	Data Repl	Data Hit Rate	Total DF	Total CB
4	Split	4	1	WB	WA	782764	782763	0.0000	204118	204117	0.0604	986882	65759
8	Split	4	2	WB	WA	782764	782762	0.0000	185640	185638	0.1454	968404	64499
16	Split	4	4	WB	WA	780135	780131	0.0034	160277	160273	0.2622	940412	61780
32	Split	4	8	WB	WA	774870	774862	0.0101	137747	137739	0.3659	912617	55950
64	Split	4	16	WB	WA	576445	576429	0.2636	119032	119016	0.4521	695477	49991
128	Split	4	32	WB	WA	494190	494158	0.3687	100030	99998	0.5395	594220	41819
256	Split	4	64	WB	WA	426746	426682	0.4548	59898	59834	0.7243	486644	27201
512	Split	4	128	WB	WA	362575	362447	0.5368	33711	33583	0.8448	396286	17750
1024	Split	4	256	WB	WA	191922	191666	0.7548	19993	19737	0.9080	211915	9784
2048	Split	4	512	WB	WA	107987	107475	0.8620	10170	9658	0.9532	118157	5703
4096	Split	4	1024	WB	WA	73811	72787	0.9057	7475	6451	0.9656	81286	4708
8192	Split	4	2048	WB	WA	19782	17734	0.9747	5950	3902	0.9726	25732	3977
16384	Split	4	4096	WB	WA	10620	6524	0.9864	4225	129	0.9806	14845	3029
32768	Split	4	8192	WB	WA	8964	772	0.9885	4225	0	0.9806	13189	3029
65536	Split	4	16384	WB	WA	8964	0	0.9885	4225	0	0.9806	13189	3029

Instruction Accesses => 782764 | Data Accesses => 217237

tex.trace

CS	I- vs D-	BS	Assoc	Write	Alloc	Instructions Misses	Instructions Repl	Instructions Hit Rate	Data Misses	Data Repl	Data Hit Rate	Total DF	Total CB
4	Split	4	1	WB	WA	597309	597308	0.0000	235156	235155	0.0001	832465	104513
8	Split	4	2	WB	WA	597309	597307	0.0000	182914	182912	0.2222	780223	82127
16	Split	4	4	WB	WA	597309	597305	0.0000	156786	156782	0.3333	754095	82124
32	Split	4	8	WB	WA	485394	485386	0.1874	100815	100807	0.5713	586209	74659
64	Split	4	16	WB	WA	485394	485378	0.1874	18714	18698	0.9204	504108	7502
128	Split	4	32	WB	WA	485394	485362	0.1874	14944	14912	0.9365	500338	7478
256	Split	4	64	WB	WA	272807	272743	0.5433	14944	14880	0.9365	287751	7478
512	Split	4	128	WB	WA	530	402	0.9991	14944	14816	0.9365	15474	7478
1024	Split	4	256	WB	WA	160	0	0.9997	14944	14688	0.9365	15104	7478
2048	Split	4	512	WB	WA	160	0	0.9997	14944	14432	0.9365	15104	7478

Instruction Accesses => 597309 | Data Accesses => 235168

cc.trace

CS	I- vs D-	BS	Assoc	Write	Alloc	Instructions Misses	Instructions Repl	Instructions Hit Rate	Data Misses	Data Repl	Data Hit Rate	Total DF	Total CB
4	Split	4	1	WB	WA	757341	757340	0.0000	226269	226268	0.0676	983610	82235
8	Split	4	2	WB	WA	757341	757339	0.0000	209336	209334	0.1373	966677	80732
16	Split	4	4	WB	WA	753804	753800	0.0047	188581	188577	0.2229	942385	78613
32	Split	4	8	WB	WA	730580	730572	0.0353	161866	161858	0.3330	892446	71550
64	Split	4	16	WB	WA	666884	666868	0.1194	136720	136704	0.4366	803604	65243
128	Split	4	32	WB	WA	604143	604111	0.2023	109141	109109	0.5502	713284	55752
256	Split	4	64	WB	WA	529362	529298	0.3010	82925	82861	0.6583	612287	43787
512	Split	4	128	WB	WA	454953	454825	0.3993	60111	59983	0.7523	515064	31820
1024	Split	4	256	WB	WA	398640	398384	0.4736	40189	39933	0.8344	438829	21005
2048	Split	4	512	WB	WA	308232	307720	0.5930	29941	29429	0.8766	338173	16088
4096	Split	4	1024	WB	WA	199920	198896	0.7360	21715	20691	0.9105	221635	13354
8192	Split	4	2048	WB	WA	99691	97643	0.8684	13670	11622	0.9437	113361	9713
16384	Split	4	4096	WB	WA	48500	44404	0.9360	10797	6701	0.9555	59297	7990
32768	Split	4	8192	WB	WA	38475	30283	0.9492	9554	1362	0.9606	48029	7285
65536	Split	4	16384	WB	WA	37005	20621	0.9511	9273	0	0.9618	46278	7234
131072	Split	4	32768	WB	WA	31195	0	0.9588	9273	0	0.9618	40468	7234
262144	Split	4	65536	WB	WA	31195	0	0.9588	9273	0	0.9618	40468	7234

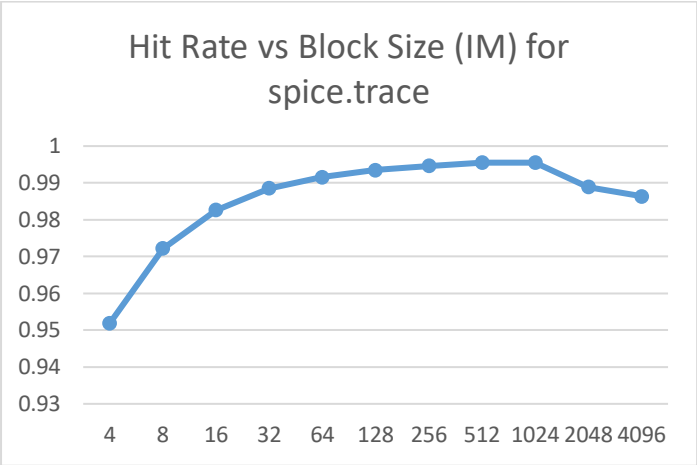
Instruction Accesses => 757341 | Data Accesses => 242661

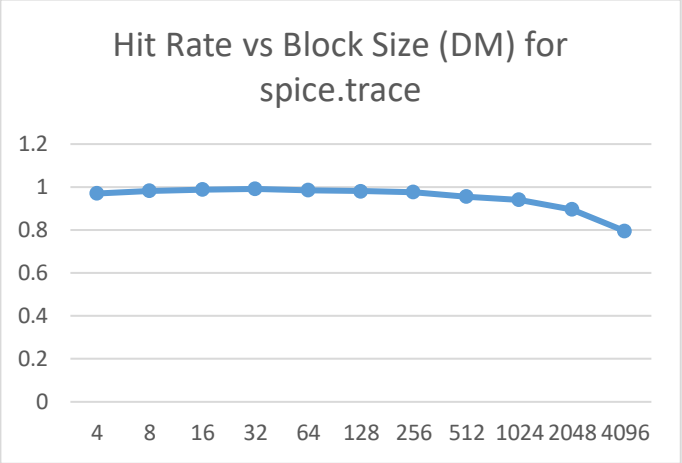
Detailed Analysis

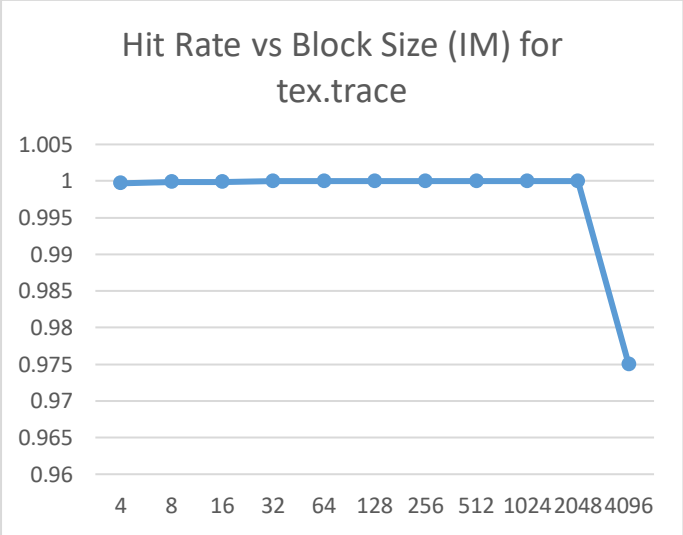
1. The focus here is on studying the effect of increasing cache size on hit rate.
2. As seen and intuitive too, increasing cache size increases the hit % and also decreases misses. The larger the Cache size, the lesser is the probability of a conflict arising.
3. But as we keep increasing the block size, it reaches a saturation, upto a point where there are only **compulsory misses** in the Cache. The cache is now, large enough to accommodate all the data accessed during the execution of the program.
4. Here, all the 3 trace files shows same pattern because of aforementioned reasons.
5. Separate data memory and instruction memory behaviour patterns are inline with above observations as both function independently and the misses saturate after a point.

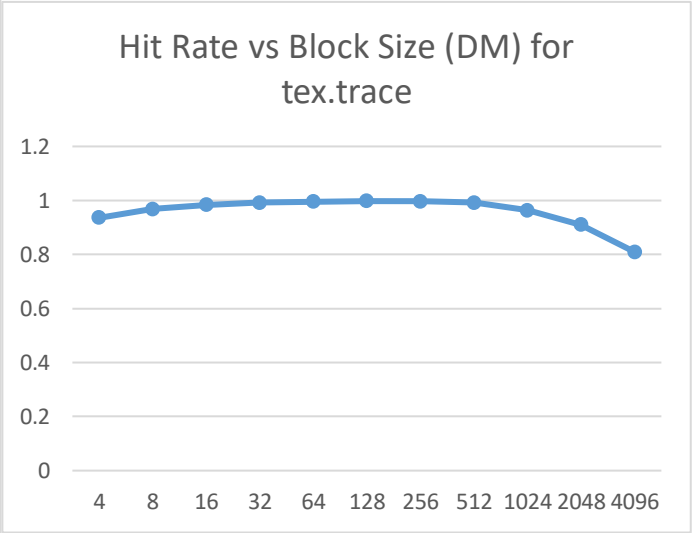
Analysing Block Size Effects

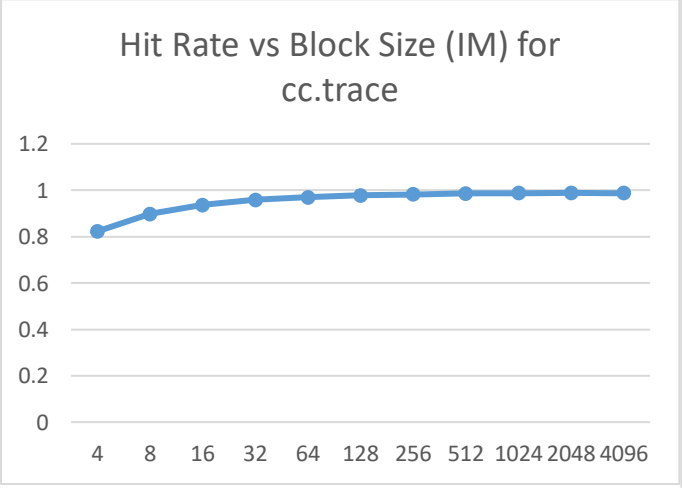
Charts

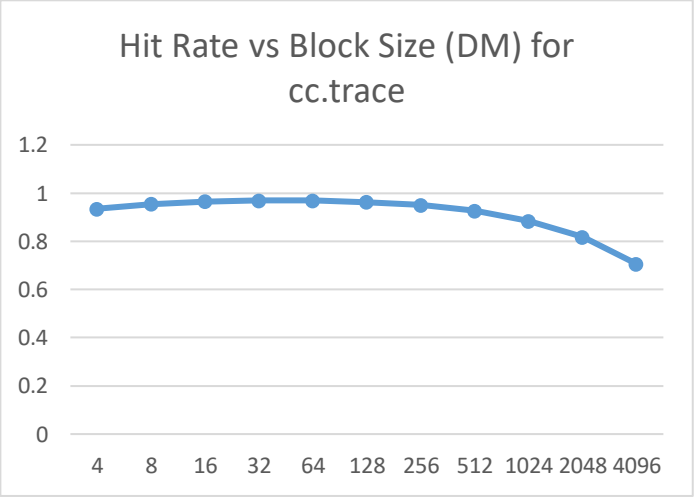












Hit rate of the cache as a function of block size

spice.trace

						Instructions			Data			Total	
CS	I- vs D-	BS	Assoc	Write	Alloc	Misses	Repl	Hit Rate	Misses	Repl	Hit Rate	DF	CB
8192	Split	4	2	WB	WA	37618	35570	0.9519	6491	4443	0.9701	44109	4315
8192	Split	8	2	WB	WA	21743	20719	0.9722	3683	2659	0.9830	50852	4696
8192	Split	16	2	WB	WA	13585	13073	0.9826	2467	1955	0.9886	64208	5752
8192	Split	32	2	WB	WA	8976	8720	0.9885	1913	1657	0.9912	87112	7920
8192	Split	64	2	WB	WA	6590	6462	0.9916	3160	3032	0.9855	156000	18880
8192	Split	128	2	WB	WA	5073	5009	0.9935	4039	3975	0.9814	291584	36256
8192	Split	256	2	WB	WA	4230	4198	0.9946	5157	5125	0.9763	600768	136448
8192	Split	512	2	WB	WA	3543	3527	0.9955	9479	9463	0.9564	1666816	661504
8192	Split	1024	2	WB	WA	3516	3508	0.9955	12701	12693	0.9415	4151552	1752832
8192	Split	2048	2	WB	WA	8681	8677	0.9889	22415	22411	0.8968	15921152	5174784
8192	Split	4096	2	WB	WA	10638	10636	0.9864	44607	44605	0.7947	56570880	20675584

tex.trace

						Instructions			Data			Total	
CS	I- vs D-	BS	Assoc	Write	Alloc	Misses	Repl	Hit Rate	Misses	Repl	Hit Rate	DF	CB
8192	Split	4	2	WB	WA	160	0	0.9997	14944	12896	0.9365	15104	7478
8192	Split	8	2	WB	WA	87	0	0.9999	7478	6454	0.9682	15130	7484
8192	Split	16	2	WB	WA	51	0	0.9999	3745	3233	0.9841	15184	7500
8192	Split	32	2	WB	WA	29	0	1.0000	1882	1626	0.9920	15288	7544
8192	Split	64	2	WB	WA	20	0	1.0000	961	833	0.9959	15696	7664
8192	Split	128	2	WB	WA	13	0	1.0000	566	502	0.9976	18528	8608
8192	Split	256	2	WB	WA	10	0	1.0000	734	702	0.9969	47616	18304
8192	Split	512	2	WB	WA	15	8	1.0000	1900	1884	0.9919	245120	113280
8192	Split	1024	2	WB	WA	12	6	1.0000	8620	8612	0.9633	2209792	966400
8192	Split	2048	2	WB	WA	11	7	1.0000	21175	21171	0.9100	10847232	5104128
8192	Split	4096	2	WB	WA	14936	14934	0.9750	44798	44796	0.8095	61167616	22935552

cc.trace

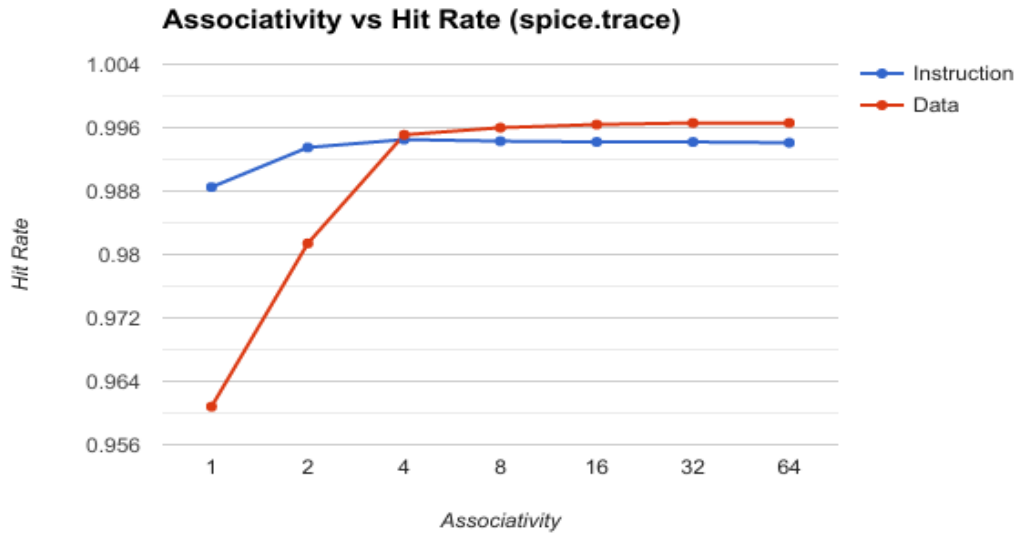
						Instructions			Data			Total	
CS	I- vs D-	BS	Assoc	Write	Alloc	Misses	Repl	Hit Rate	Misses	Repl	Hit Rate	DF	CB
8192	Split	4	2	WB	WA	134420	132372	0.8225	16045	13998	0.9339	150465	10544
8192	Split	8	2	WB	WA	77069	76045	0.8982	11059	10035	0.9544	176256	12782
8192	Split	16	2	WB	WA	47894	47382	0.9368	8582	8070	0.9646	225904	16960
8192	Split	32	2	WB	WA	31983	31727	0.9578	7397	7141	0.9695	315040	24408
8192	Split	64	2	WB	WA	23040	22912	0.9696	7521	7393	0.9690	488976	41840
8192	Split	128	2	WB	WA	17301	17237	0.9772	9225	9161	0.9620	848832	91744
8192	Split	256	2	WB	WA	13624	13592	0.9820	11937	11905	0.9508	1635904	234560
8192	Split	512	2	WB	WA	10679	10663	0.9859	17793	17777	0.9267	3644416	755840
8192	Split	1024	2	WB	WA	9713	9705	0.9872	28109	28101	0.8842	9682432	2336256
8192	Split	2048	2	WB	WA	8709	8705	0.9885	44295	44291	0.8175	27138048	7123968
8192	Split	4096	2	WB	WA	9347	9345	0.9877	71292	71290	0.7062	82574336	24226816

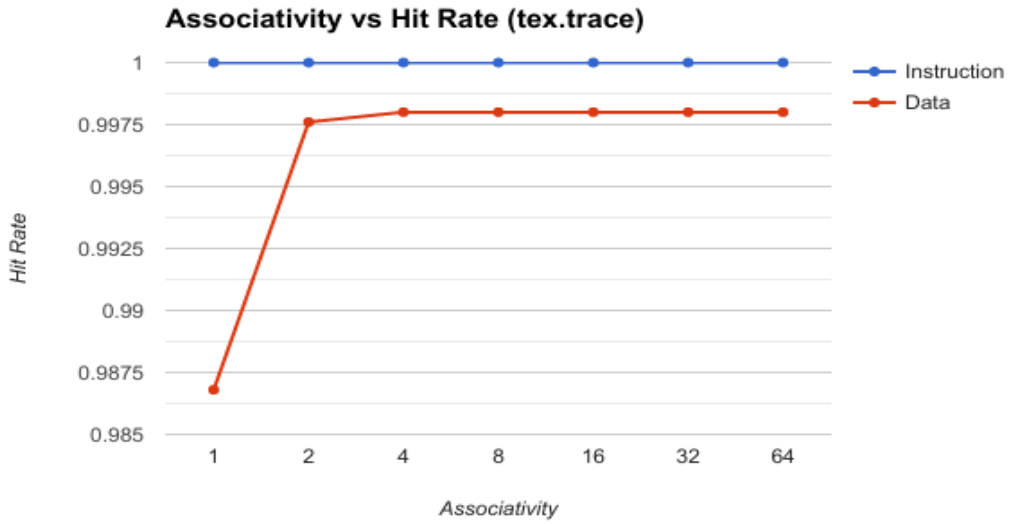
Detailed Analysis

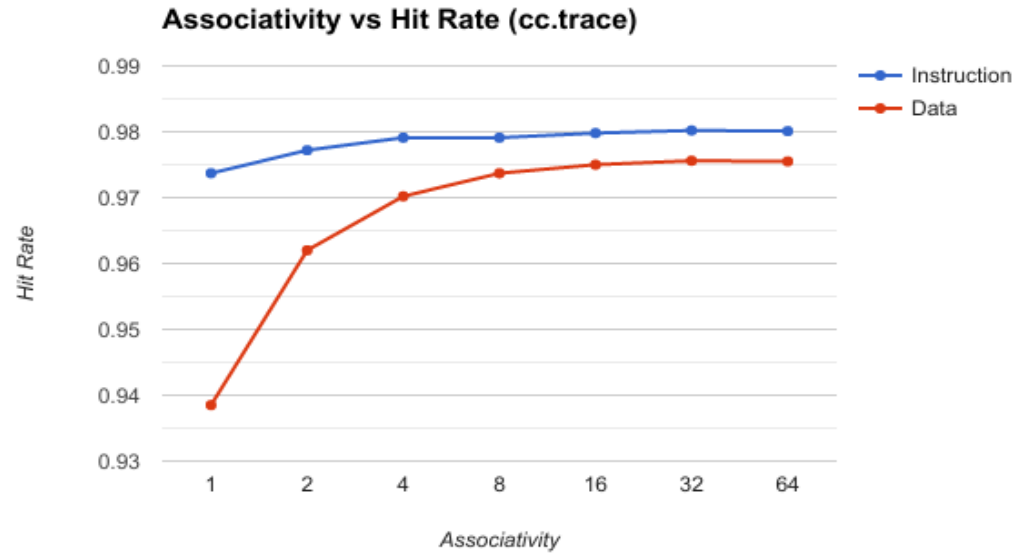
1. The focus here is on studying the effect of varying block size on hit rate.
2. As expected, the hit rate follows a **convex pattern** with increasing block size.
3. The initial increase is because small block sizes do not take maximum advantage of **spatial locality.**
4. The hit rate keeps on increasing with increasing block size as more and more spatial locality is exploited.
5. The decrease in the end is because when block size becomes large, there are fewer blocks available giving rise to higher **potential conflicts**.
6. The 2 memories shows different performance here. Increasing size of block in Instruction cache keeps on increasing the hit rate whereas Data Memory shows performance as mentioned above.
7. This is because instruction memory has a continuous access trace (mostly) and thus increasing block size decreases the number of lookup's in memory. Whole block can be fetched in single access which shows up as improve in performance when compared to word by word transfer.
8. The optimal block size for Data Cache was in range of **64 – 256 bytes** per block whereas Instruction cache showed no such distinctive maxima's.
9. Hence, we can conclude that Instruction references are much more **ordered and continuous** when compared with Data references.

Analysing Associativity Effects

Charts







Hit rate of the cache as a function of associativity

spice.trace

						Instructions			Data			Total	
CS	I- vs D-	BS	Assoc	Write	Alloc	Misses	Repl	Hit Rate	Misses	Repl	Hit Rate	DF	CB
8192	Split	128	1	WB	WA	9018	8954	0.9885	8519	8455	0.9608	561184	79232
8192	Split	128	2	WB	WA	5073	5009	0.9935	4039	3975	0.9814	291584	36256
8192	Split	128	4	WB	WA	4273	4209	0.9945	1075	1011	0.9951	171136	14592
8192	Split	128	8	WB	WA	4457	4393	0.9943	860	796	0.9960	170144	11360
8192	Split	128	16	WB	WA	4511	4447	0.9942	789	725	0.9964	169600	10432
8192	Split	128	32	WB	WA	4553	4489	0.9942	730	666	0.9966	169056	10176
8192	Split	128	64	WB	WA	4591	4527	0.9941	728	664	0.9966	170208	10272

tex.trace

						Instructions			Data			Total	
CS	I- vs D-	BS	Assoc	Write	Alloc	Misses	Repl	Hit Rate	Misses	Repl	Hit Rate	DF	CB
8192	Split	128	1	WB	WA	18	6	1.0000	3107	3043	0.9868	100000	53120
8192	Split	128	2	WB	WA	13	0	1.0000	566	502	0.9976	18528	8608
8192	Split	128	4	WB	WA	13	0	1.0000	476	412	0.9980	15648	7648
8192	Split	128	8	WB	WA	13	0	1.0000	476	412	0.9980	15648	7648
8192	Split	128	16	WB	WA	13	0	1.0000	476	412	0.9980	15648	7648
8192	Split	128	32	WB	WA	13	0	1.0000	476	412	0.9980	15648	7648
8192	Split	128	64	WB	WA	13	0	1.0000	476	412	0.9980	15648	7648

cc.trace

						Instructions			Data			Total	
CS	I- vs D-	BS	Assoc	Write	Alloc	Misses	Repl	Hit Rate	Misses	Repl	Hit Rate	DF	CB
8192	Split	128	1	WB	WA	19894	19830	0.9737	14934	14870	0.9385	1114496	161984
8192	Split	128	2	WB	WA	17301	17237	0.9772	9225	9161	0.9620	848832	91744
8192	Split	128	4	WB	WA	15819	15755	0.9791	7232	7168	0.9702	737632	68384
8192	Split	128	8	WB	WA	15823	15759	0.9791	6386	6322	0.9737	710688	58624
8192	Split	128	16	WB	WA	15275	15211	0.9798	6067	6003	0.9750	682944	56416
8192	Split	128	32	WB	WA	15033	14969	0.9802	5919	5855	0.9756	670464	53696
8192	Split	128	64	WB	WA	15065	15001	0.9801	5946	5882	0.9755	672352	53856

Detailed Analysis

1. Here, the focus is on studying variation of set associativity against hit rate.
2. The pattern is first increasing and then saturates.
3. Highly associative caches have a lower miss rate because of more **flexible placement** of blocks within a set.
4. The fully associative cache are the most performance efficient but constant time search amongst tag bits is too hardware intensive.
5. Varying associativity didn't improve much on performance of instruction cache whereas significant improvement was seen on performance of data cache.
6. Instruction references poses less conflicts because of ordering in which they are accessed and most miss are **Compulsory Misses.**

Analysing effect on Memory Traffic

Comparing Write Allocate and Write no allocate

spice.trace
Write No Allocate

CS	I- vs D-	BS	Assoc	Write	Alloc	Instructions Misses	Instructions Repl	Instructions Hit Rate	Data Misses	Data Repl	Data Hit Rate	Total DF	Total CB
8192	Split	64	2	WB	WNA	6590	6462	0.9916	8638	2726	0.9602	151104	13624
16384	Split	64	2	WB	WNA	3006	2750	0.9962	5449	324	0.9749	57008	8252
8192	Split	128	2	WB	WNA	5073	5009	0.9935	9940	3637	0.9542	280768	32287
16384	Split	128	2	WB	WNA	2490	2362	0.9968	5388	310	0.9752	93632	9880
8192	Split	64	4	WB	WNA	6025	5897	0.9923	5596	553	0.9742	107296	9219
16384	Split	64	4	WB	WNA	1924	1668	0.9975	4984	203	0.9771	38064	7681
8192	Split	128	4	WB	WNA	4273	4209	0.9945	5858	733	0.9730	162240	13733
16384	Split	128	4	WB	WNA	1665	1537	0.9979	4893	218	0.9775	64320	9668

Write Allocate

CS	I- vs D-	BS	Assoc	Write	Alloc	Instructions Misses	Instructions Repl	Instructions Hit Rate	Data Misses	Data Repl	Data Hit Rate	Total DF	Total CB
8192	Split	64	2	WB	WA	6590	6462	0.9916	3160	3032	0.9855	156000	18880
16384	Split	64	2	WB	WA	3006	2750	0.9962	735	500	0.9966	59856	6208
8192	Split	128	2	WB	WA	5073	5009	0.9935	4039	3975	0.9814	291584	36256
16384	Split	128	2	WB	WA	2490	2362	0.9968	604	478	0.9972	99008	9088
8192	Split	64	4	WB	WA	6025	5897	0.9923	875	747	0.9960	110400	7296
16384	Split	64	4	WB	WA	1924	1668	0.9975	559	306	0.9974	39728	5280
8192	Split	128	4	WB	WA	4273	4209	0.9945	1075	1011	0.9951	171136	14592
16384	Split	128	4	WB	WA	1665	1537	0.9979	407	280	0.9981	66304	7200

tex.trace
Write No Allocate

CS	I- vs D-	BS	Assoc	Write	Alloc	Instructions Misses	Instructions Repl	Instructions Hit Rate	Data Misses	Data Repl	Data Hit Rate	Total DF	Total CB
8192	Split	64	2	WB	WNA	20	0	1.0000	30031	32	0.8723	2880	29903
16384	Split	64	2	WB	WNA	20	0	1.0000	29995	0	0.8725	2464	29909
8192	Split	128	2	WB	WNA	13	0	1.0000	29967	32	0.8726	3488	29935
16384	Split	128	2	WB	WNA	13	0	1.0000	29931	0	0.8727	2656	29957
8192	Split	64	4	WB	WNA	20	0	1.0000	30058	59	0.8722	3312	29903
16384	Split	64	4	WB	WNA	20	0	1.0000	29995	0	0.8725	2464	29909
8192	Split	128	4	WB	WNA	13	0	1.0000	29985	50	0.8725	4064	29935
16384	Split	128	4	WB	WNA	13	0	1.0000	29931	0	0.8727	2656	29957

Write Allocate

CS	I- vs D-	BS	Assoc	Write	Alloc	Instructions Misses	Instructions Repl	Instructions Hit Rate	Data Misses	Data Repl	Data Hit Rate	Total DF	Total CB
8192	Split	64	2	WB	WA	20	0	1.0000	961	833	0.9959	15696	7664
16384	Split	64	2	WB	WA	20	0	1.0000	711	455	0.9970	11696	7616
8192	Split	128	2	WB	WA	13	0	1.0000	566	502	0.9976	18528	8608
16384	Split	128	2	WB	WA	13	0	1.0000	415	287	0.9982	13696	8256
8192	Split	64	4	WB	WA	20	0	1.0000	943	815	0.9960	15408	7568
16384	Split	64	4	WB	WA	20	0	1.0000	635	379	0.9973	10480	7568
8192	Split	128	4	WB	WA	13	0	1.0000	476	412	0.9980	15648	7648
16384	Split	128	4	WB	WA	13	0	1.0000	337	209	0.9986	11200	7648

cc.trace
Write No Allocate

CS	I- vs D-	BS	Assoc	Write	Alloc	Instructions Misses	Instructions Repl	Instructions Hit Rate	Data Misses	Data Repl	Data Hit Rate	Total DF	Total CB
8192	Split	64	2	WB	WNA	23040	22912	0.9696	17883	6473	0.9263	474256	39426
16384	Split	64	2	WB	WNA	12582	12326	0.9834	11526	2918	0.9525	252096	24048
8192	Split	128	2	WB	WNA	17301	17237	0.9772	19007	8391	0.9217	824192	78872
16384	Split	128	2	WB	WNA	10139	10011	0.9866	11021	3507	0.9546	440768	40538
8192	Split	64	4	WB	WNA	21095	20967	0.9721	15259	5221	0.9371	423104	32102
16384	Split	64	4	WB	WNA	10468	10212	0.9862	10276	2096	0.9577	205120	19588
8192	Split	128	4	WB	WNA	15819	15755	0.9791	15919	6515	0.9344	716736	59292
16384	Split	128	4	WB	WNA	8305	8177	0.9890	9785	2618	0.9597	353632	31103

Write Allocate

CS	I- vs D-	BS	Assoc	Write	Alloc	Instructions Misses	Instructions Repl	Instructions Hit Rate	Data Misses	Data Repl	Data Hit Rate	Total DF	Total CB
8192	Split	64	2	WB	WA	23040	22912	0.9696	7521	7393	0.9690	488976	41840
16384	Split	64	2	WB	WA	12582	12326	0.9834	3746	3490	0.9846	261248	23584
8192	Split	128	2	WB	WA	17301	17237	0.9772	9225	9161	0.9620	848832	91744
16384	Split	128	2	WB	WA	10139	10011	0.9866	4106	3978	0.9831	455840	46048
8192	Split	64	4	WB	WA	21095	20967	0.9721	6118	5990	0.9748	435408	33216
16384	Split	64	4	WB	WA	10468	10212	0.9862	2793	2537	0.9885	212176	18208
8192	Split	128	4	WB	WA	15819	15755	0.9791	7232	7168	0.9702	737632	68384
16384	Split	128	4	WB	WA	8305	8177	0.9890	3051	2923	0.9874	363392	32512

Analysing effect of Write back vs Write through

1. Write back has smaller memory traffic then write through.
2. This is because both the policies perform equally on **demand fetches** but write back perform outperforms Write through when studying copies back.
3. This is because Write back keeps both the cache and memory **simultaneously** updated whereas, writes back lazily when it becomes imperative.
4. Generally, write back has smaller memory traffic than write through except cases when:
   - Block size of Cache <= 4 bytes (Word Size)
   - When a particular index in cache continuously gets written and replaced (because of a conflict).

Analysing effect of Write allocate vs Write no allocate

1. The aim here is studying effect of Write Allocate and No Write Allocate policies, given Write Back strategy is followed.
2. Here, the performance is mixed and both perform at par with the other when traffic is concerned.
3. When a write miss occurs, and the same address is continuously accessed, write allocate is superior as it would have already bought the data into memory.
4. When we are filling some memory block and need not read it, then bringing it back to memory makes no sense and thus write no allocate reduces traffic by not bringing it back to memory.
5. The above 2 policies are situation dependent because of aforementioned reasons.

Comparing Write through and Write back

spice.trace
Write Back

						Instructions			Data			Total	
CS	I- vs D-	BS	Assoc	Write	Alloc	Misses	Repl	Hit Rate	Misses	Repl	Hit Rate	DF	CB
8192	Split	64	2	WB	WNA	6590	6462	0.9916	8638	2726	0.9602	151104	13624
16384	Split	64	2	WB	WNA	3006	2750	0.9962	5449	324	0.9749	57008	8252
8192	Split	128	2	WB	WNA	5073	5009	0.9935	9940	3637	0.9542	280768	32287
16384	Split	128	2	WB	WNA	2490	2362	0.9968	5388	310	0.9752	93632	9880
8192	Split	64	4	WB	WNA	6025	5897	0.9923	5596	553	0.9742	107296	9219
16384	Split	64	4	WB	WNA	1924	1668	0.9975	4984	203	0.9771	38064	7681
8192	Split	128	4	WB	WNA	4273	4209	0.9945	5858	733	0.9730	162240	13733
16384	Split	128	4	WB	WNA	1665	1537	0.9979	4893	218	0.9775	64320	9668

Write Through

						Instructions			Data			Total	
CS	I- vs D-	BS	Assoc	Write	Alloc	Misses	Repl	Hit Rate	Misses	Repl	Hit Rate	DF	CB
8192	Split	64	2	WT	WNA	6590	6462	0.9916	8638	2726	0.9602	151104	66538
16384	Split	64	2	WT	WNA	3006	2750	0.9962	5449	324	0.9749	57008	66538
8192	Split	128	2	WT	WNA	5073	5009	0.9935	9940	3637	0.9542	280768	66538
16384	Split	128	2	WT	WNA	2490	2362	0.9968	5388	310	0.9752	93632	66538
8192	Split	64	4	WT	WNA	6025	5897	0.9923	5596	553	0.9742	107296	66538
16384	Split	64	4	WT	WNA	1924	1668	0.9975	4984	203	0.9771	38064	66538
8192	Split	128	4	WT	WNA	4273	4209	0.9945	5858	733	0.9730	162240	66538
16384	Split	128	4	WT	WNA	1665	1537	0.9979	4893	218	0.9775	64320	66538

tex.trace
Write Back

						Instructions			Data			Total	
CS	I- vs D-	BS	Assoc	Write	Alloc	Misses	Repl	Hit Rate	Misses	Repl	Hit Rate	DF	CB
8192	Split	64	2	WB	WNA	20	0	1.0000	30031	32	0.8723	2880	29903
16384	Split	64	2	WB	WNA	20	0	1.0000	29995	0	0.8725	2464	29909
8192	Split	128	2	WB	WNA	13	0	1.0000	29967	32	0.8726	3488	29935
16384	Split	128	2	WB	WNA	13	0	1.0000	29931	0	0.8727	2656	29957
8192	Split	64	4	WB	WNA	20	0	1.0000	30058	59	0.8722	3312	29903
16384	Split	64	4	WB	WNA	20	0	1.0000	29995	0	0.8725	2464	29909
8192	Split	128	4	WB	WNA	13	0	1.0000	29985	50	0.8725	4064	29935
16384	Split	128	4	WB	WNA	13	0	1.0000	29931	0	0.8727	2656	29957

Write Through

						Instructions			Data			Total	
CS	I- vs D-	BS	Assoc	Write	Alloc	Misses	Repl	Hit Rate	Misses	Repl	Hit Rate	DF	CB
8192	Split	64	2	WT	WNA	20	0	1.0000	30031	32	0.8723	2880	104513
16384	Split	64	2	WT	WNA	20	0	1.0000	29995	0	0.8725	2464	104513
8192	Split	128	2	WT	WNA	13	0	1.0000	29967	32	0.8726	3488	104513
16384	Split	128	2	WT	WNA	13	0	1.0000	29931	0	0.8727	2656	104513
8192	Split	64	4	WT	WNA	20	0	1.0000	30058	59	0.8722	3312	104513
16384	Split	64	4	WT	WNA	20	0	1.0000	29995	0	0.8725	2464	104513
8192	Split	128	4	WT	WNA	13	0	1.0000	29985	50	0.8725	4064	104513
16384	Split	128	4	WT	WNA	13	0	1.0000	29931	0	0.8727	2656	104513

cc.trace
Write Back

						Instructions			Data			Total	
CS	I- vs D-	BS	Assoc	Write	Alloc	Misses	Repl	Hit Rate	Misses	Repl	Hit Rate	DF	CB
8192	Split	64	2	WB	WNA	23040	22912	0.9696	17883	6473	0.9263	474256	39426
16384	Split	64	2	WB	WNA	12582	12326	0.9834	11526	2918	0.9525	252096	24048
8192	Split	128	2	WB	WNA	17301	17237	0.9772	19007	8391	0.9217	824192	78872
16384	Split	128	2	WB	WNA	10139	10011	0.9866	11021	3507	0.9546	440768	40538
8192	Split	64	4	WB	WNA	21095	20967	0.9721	15259	5221	0.9371	423104	32102
16384	Split	64	4	WB	WNA	10468	10212	0.9862	10276	2096	0.9577	205120	19588
8192	Split	128	4	WB	WNA	15819	15755	0.9791	15919	6515	0.9344	716736	59292
16384	Split	128	4	WB	WNA	8305	8177	0.9890	9785	2618	0.9597	353632	31103

Write Through

						Instructions			Data			Total	
CS	I- vs D-	BS	Assoc	Write	Alloc	Misses	Repl	Hit Rate	Misses	Repl	Hit Rate	DF	CB
8192	Split	64	2	WT	WNA	23040	22912	0.9696	17883	6473	0.9263	474256	83030
16384	Split	64	2	WT	WNA	12582	12326	0.9834	11526	2918	0.9525	252096	83030
8192	Split	128	2	WT	WNA	17301	17237	0.9772	19007	8391	0.9217	824192	83030
16384	Split	128	2	WT	WNA	10139	10011	0.9866	11021	3507	0.9546	440768	83030
8192	Split	64	4	WT	WNA	21095	20967	0.9721	15259	5221	0.9371	423104	83030
16384	Split	64	4	WT	WNA	10468	10212	0.9862	10276	2096	0.9577	205120	83030
8192	Split	128	4	WT	WNA	15819	15755	0.9791	15919	6515	0.9344	716736	83030
16384	Split	128	4	WT	WNA	8305	8177	0.9890	9785	2618	0.9597	353632	83030