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Design and Implementation of 4-bit Array Multiplier for Low Power in 45nm CMOS Technology

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***Abstract*— This paper will represent the design and implementation of 4 bit Array Multiplier, using four different CMOS topology as static or conventional CMOS, Gate diffusion input(GDI), Low Power Feed Through Logic(LP-FTL) and High Speed Feed Through Logic(HS-FTL). Adder is the basic building for all arithmetic operations like addition, subtraction and multiplication, we have implemented the 4 bit Array multiplier in BPTM 45nm CMOS technology in LT spice IV.**

Keywords—CMOS, GDI, BPTM, HS-FTL, LP-FTL

I. INTRODUCTION

Multiplier plays a significant role in high speed digital signal processing. It's the most important part of the Arithmetic Logic Unit (ALU), FPU and ASIC"s where high processing speed is required. Currently, the importance of low power design increases rapidly due to the increasing demand for portable and mobile systems.

High performance dynamic circuits due to their compactness and higher speed as compared to static CMOS [1] are increasingly being used, mainly in wide fan in circuits. However the major drawback with this logic is its excessive power dissipation due to the switching activity and clock, also it suffers from charge leakage, charge sharing and requirement of additional output inverter during cascading of logic blocks. As we know Full adders are important components in applications such as digital signal processors (DSP) architectures and microprocessors. Apart from the basic addition adders also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc.

Power consumption and it's minimization is one of the primary concerns in today VLSI design methodologies because of two main reasons one is the long battery operating life requirement of mobile and portable devices and second is due to increasing number of transistors on a single chip leads to high power dissipation and it can lead to reliability and IC packaging problems.

A 4x4 bit Array multiplier is constructed as the basic building block for higher order multipliers. In Fig. 1 the sketch diagram of the multiplier and 4 bit array architecture is shown with two major blocks as AND gate logic and 1-bit full adder in Fig. 2. Let A0 –A3 be the word length of multiplicand, and B0 – B3 be the word length of the multiplier. After multiplication we can observe the P0 - P7 are final results. During the whole process we found that we can built multiplier with help of 1 bit full adder and basic AND gate logic.

			×	A3 B3	A2 B2	A1 B1	A0 B0
				P_{30}	P_{20}	P_{10}	P_{00}
+			P_{31}	P_{21}	P_{11}	P_{01}	—
+		P_{32}	P_{22}	P_{12}	P_{02}	—	—
+	P_{33}	P_{23}	P_{13}	P_{03}	—	—	—
	P_{33} =	P_{32}+ P_{23} =	P_{31}+ P_{22}+ P_{13} =	P_{30}+ P_{21}+ P_{12} + P_{03} =	P_{20}+ P_{11} + P_{02} =	P_{10} + P_{01} =	P_{00} =
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Fig.1 4-bit Multiplier Structure

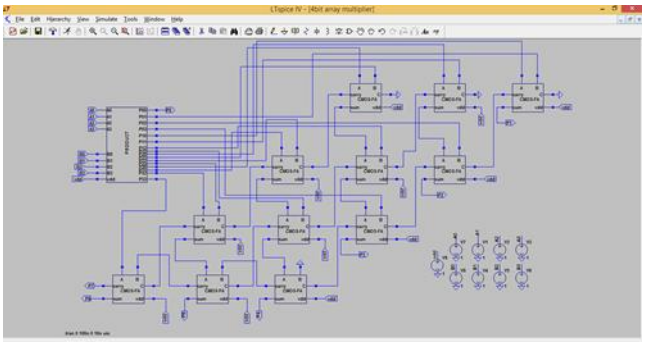

Fig. 2 4-bit Multiplier Architecture

II. IMPLEMENTATION OF 4 BIT ARRAY MULTIPLIER

A. Conventional CMOS Logic

As the static or conventional CMOS style is the basic style used in VLSI implementation and basic logic for the development in power reduction technology. A 4 bit CMOS

array block representation shown in figure 3 and it's simulation result shown in figure 4 and figure 5 respectively.

B. Gate Diffusion Input(GDI)

A new low power design technique that solves most of the problems known as Gate-Diffusion-Input (GDI) is proposed. This technique allows reducing power consumption, propagation delay, and area of digital circuits. A basic GDI cell contains four terminals – G (common gate input of nMOS and pMOS transistors), P (the outer diffusion node of pMOS transistor), N (the outer diffusion node of nMOS transistor), and D (common diffusion node of both transistors). As shown in figure 7 and figure 8 we can observe the simulation results for the Gate Diffusion input array multiplier.

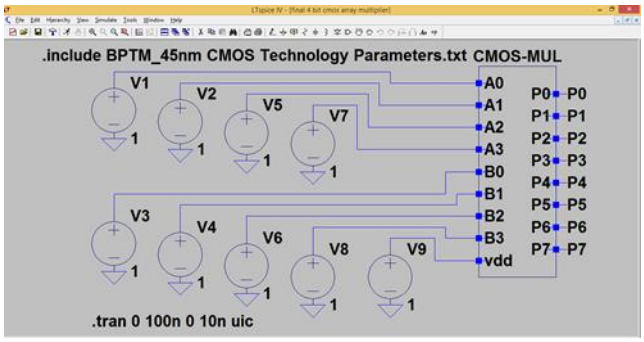

Fig. 3 Block diagram of 4-bit CMOS Array Multiplier

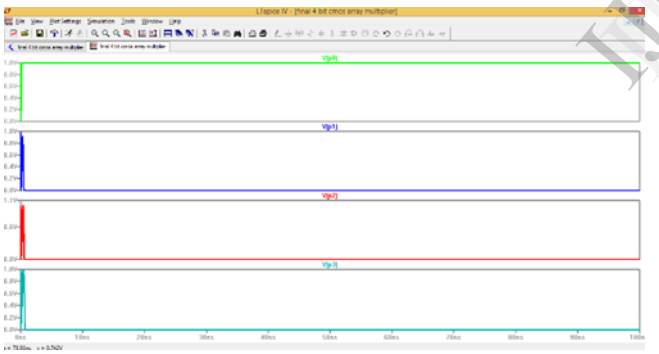

Fig. 4 Simulation result for 4-bit CMOS Array Multiplier (P0 – P3)

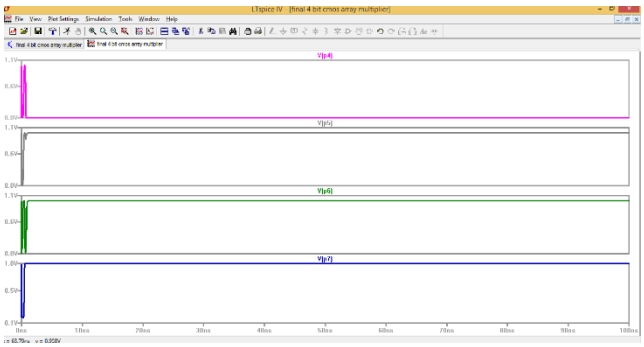

Fig. 5 Simulation result for 4-bit CMOS Array Multiplier (P4 – P7)

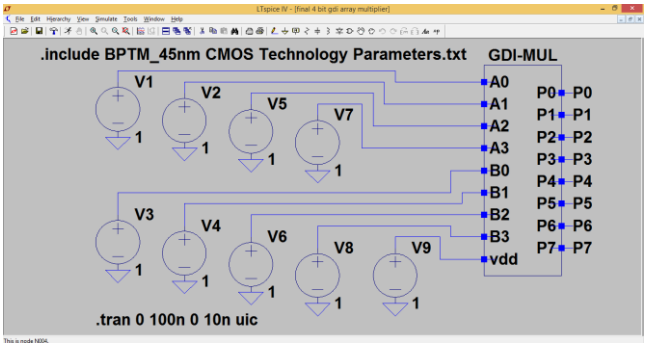

Fig. 6 Block diagram of 4-bit GDI Array Multiplier

C. Feed Through Logic

A feed through logic is a widely used Dynamic logic for power reduction in VLSI designs. It has two types one is for low power and second for the high speed so we had implemented both architecture as shown in figure 9, figure 10 and figure 11 shows for the low power feed through logic (LS-FTL), where figure 12, figure 13 and figure 14 shows for the high speed feed through logic (HS-FTL).

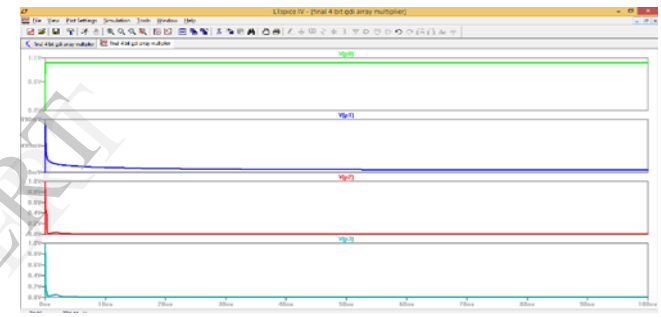

Fig. 7 Simulation result for 4-bit GDI Array Multiplier (P0 – P3)

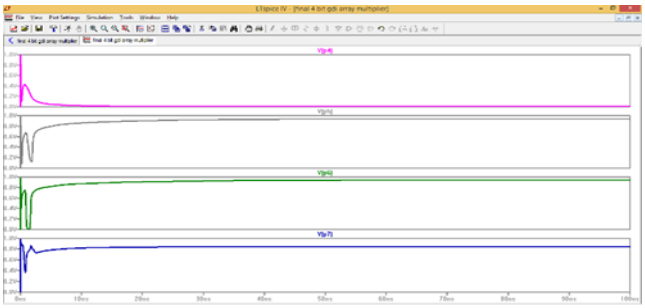

Fig. 8 Simulation result for 4-bit GDI Array Multiplier (P4 – P7)

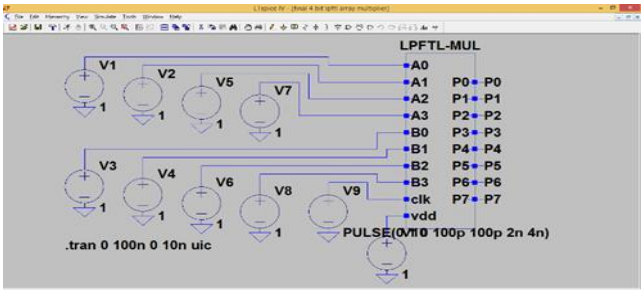

Fig. 9 Block diagram of 4-bit LPFTL Array Multiplier

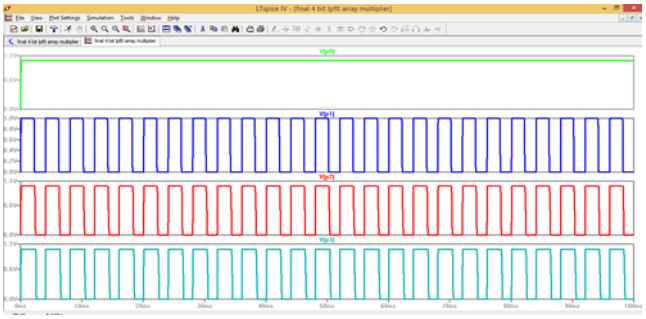

Fig. 10 Simulation result for 4-bit LPFTL Array Multiplier (P0 – P3)

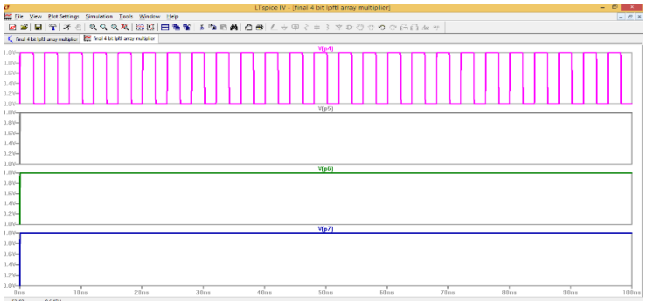

Fig. 11 Simulation result for 4-bit LPFTL Array Multiplier (P4 – P7)

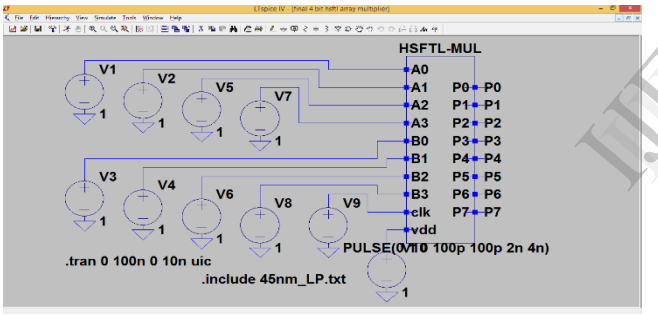

Fig. 12 Block diagram of 4-bit HSFTL Array Multiplier

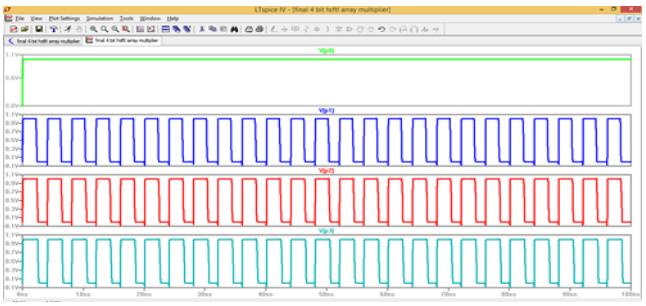

Fig. 13 Simulation result for 4-bit HSFTL Array Multiplier (P0 – P3)

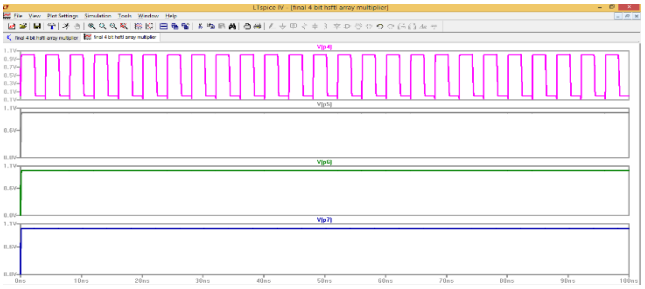

Fig. 14 Simulation result for 4-bit HSFTL Array Multiplier (P4 – P7)

III. COMPARATIVE ANALYSIS OF 4 BIT ARRAY MULTIPLIERS

As shown in the table 1 demonstrate the power consumption and integral power delay product of all 4 bit array multiplier. We found that Lop Power Feed through Logic (LP-FTL) has the least power dissipation compared to the GDI and static CMOS logic adder and High Speed Feed through Logic (HS-FTL).

TABLE I POWER DISSIPATION AND POWER PRODUCT DELAY OF 4 BIT ARRAY MULTIPLIERS

Average Power Dissipation (in uW)			
Static CMOS	**HS-FTL**	**LP-FTL**	**GDI**
76.545	158.41	23.93	56.052
Power Delay Product (in pJ)			
Static CMOS	**HS-FTL**	**LP-FTL**	**GDI**
7.6545	15.841	2.394	5.6052

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REFERENCES

[1] Sauvagya Ranjan Sahoo, Kamala Kanta Mahapatra, "Design of Low Power and High Speed Ripple Carry Adder Using Modified Feedthrough Logic " in 2012 International Conference on Communications, Devices and Intelligent Systems (CODIS) , 978-1-4673-4700-6/12/$3l.00 ©2012 IEEE.

[2] Soolmaz Abbasalizadeh, Behjat Forouzandeh, "Full Adder Design with GDI Cell and Independent Double Gate Transistor " in 20th Iranian Conference on Electrical Engineering, (lCEE2012), May 15-17,2012, Tehran, Iran , 978-1-4673-1148-9/12/$3l.00 ©2012 IEEE.

[3] Praveen Saxena, dinesh Chandra and Sampath kumar, Design Of A 1-Bit Full Adder For Low Power Application, in (IJAEST) International Journal Of Advanced Engineering Sciences And Technologies Vol No. 10, Issue No. 1, 019 – 025, 2011.

[4] Y. Sunil Gavaskar Reddy and V.V.G.S.Rajendra Prasad, The Power Comparison Of Cmos And Adiabatic Full Adder Circuits in International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.3, September 2011.

[5] Subodh Wairya, Rajendra Kumar Nagaria and Sudarshan Tiwari, "Comparative Performance Analysis of XOR/XNOR Function Based High-Speed CMOS Full Adder Circuits For Low Voltage VLSI Design," in International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.2, April 2012.

[6] Manoj Kumar, Sandeep K. Arya and Sujata Pandey, Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate in International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.4, December 2011.

[7] R.UMA, Vidya Vijayan, M. Mohanapriya, Sharon Paul, Area, Delay and Power Comparison of Adder Topologies in International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, February,12.

[8] A. Kishore Kumar, D. Somasundareswari, V. Duraisamy, T. Shunbaga Pradeepa, Design of Low Power Full Adder using Asynchronous Adiabatic Logic in European Journal of Scientific Research ISSN 1450-216X Vol.63 No.3 (2011), pp. 358-367.