ANKIT KAUL

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Short bio: Ph.D. in Electrical and Computer Engineering with a focus on 3D integration of compute in-memory (CIM) systems. Experience in: Device-package-application analysis of heterogeneous integration for CIM, 3D integration using hybrid bonding, power/thermal management techniques, die-to-die interconnection evaluation, power delivery circuits, micro-architecture analysis.

EDUCATION

Georgia Institute of Technology, Atlanta, GA	**Ph.D., Electrical and Computer Engineering** **Minor**: Computer Science	*May 2018 – Aug. 2023*
Georgia Institute of Technology, Atlanta, GA	**Master of Science, Electrical and Computer Engineering** **Focus**: Digital systems and Computer architecture	*Aug. 2016 – May 2018*
R.V. College of Engineering, Bangalore, India	**Bachelors, Electrical Engineering, GPA: 9.05/10.0**	*Aug. 2009 – May 2013*

EXPERIENCE

Member of Technical Staff – Advanced Technology and Integration, AMD – Austin, TX   *Sept. 2022 – Present*
Computational modeling and pathfinding for 3D heterogeneous integration and advanced semiconductor packaging.
Mentors: Kaushik Mysore, Hemanth Dhavaleswarapu

Graduate Research Assistant, Integrated 3D systems lab, (SRC ASCENT student) Georgia Institute of technology – Atlanta, GA
May 2018 – Aug 2023
- **Research focus**:
  - Impact of 3D integration on emerging non-volatile memory-based compute in-memory (CIM) inference accelerators
  - Die-to-die interconnection evaluation, power/thermal management techniques, novel power delivery techniques for 2.5D/3D
- **Adviser: Dr. Muhannad Bakir** (https://bakirlab.gatech.edu/)

Research Intern – Advanced Packaging, AMD – Austin, TX   *Jan. 2022 – May 2022*
- Computational modeling and pathfinding of 3D V-cache integration architectures and advanced materials for superior thermal and electrical performance (**Python, 3D partitioning**). **Advisers**: Hemanth Dhavaleswarapu, Rahul Agarwal

Ph.D. Intern - Advanced Products, Physical IP, Arm Inc. – Austin, TX   *May 2020 – Aug. 2020*
Project: Power-performance-thermal evaluation for 2.5D integration of arm-based 7nm high-performance systems
- Developed a methodology to explore relationship between core implementation targets, DVFS points, thermal limits, and system throughput for multi-die integration architectures. (**Python, Celsius, Tcl**) **Advisers:** Jim Dodrill, Saurabh Sinha
- **DAC 2022** poster titled: "Signaling and Thermal Considerations for 2.5D Integration of Arm-Based 7nm High-Performance Systems," journal publication in progress.
- *Impact:* Improved Arm's 2.5D modeling methodology by developing multi-core SiP analyses capability for large-scale compute

UTC Aerospace Systems, Hardware Engineer – Bangalore, India   *Jul. 2013 – Jul. 2016*
Led platform circuit performance analysis of an Electronic Control and power quality Monitoring (ECM) unit for Boeing's 777x
- *Impact:* Achieved **$50k savings** by improving circuit performance via analysis of tolerance bottlenecks using Allegro AMS Simulator

RESEARCH PUBLICATIONS[#]

A. Conference Publications (Refereed):

C1. **A. Kaul**, X. Peng, S. K. Rajan, S. Yu and M. S. Bakir, "Thermal Modeling of 3D Polylithic Integration and Implications on BEOL RRAM Performance," *IEEE International Electron Devices Meeting (IEDM)*, 2020, pp. 13.1.1-13.1.4, doi: 10.1109/IEDM13553.2020.9371983.

C2. Y. Luo, S. Dutta, **A. Kaul**, S. Lim, M. Bakir, S. Datta, S. Yu, "Monolithic 3D Compute-in-Memory Accelerator with BEOL Transistor based Reconfigurable Interconnect," *IEEE International Electron Devices Meeting (IEDM)*, 2021, pp. 25.3.1-25.3.4, doi: 10.1109/IEDM19574.2021.9720690.

C3. X. Peng, W. Chakraborty, **A. Kaul**, W. Shim, M. S. Bakir, S. Datta, S. Yu, "Benchmarking Monolithic 3D Integration for Compute-in-Memory Accelerators: Overcoming ADC Bottlenecks and Maintaining Scalability to 7nm or Beyond," *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, Dec. 2020.

C4. **A. Kaul**, Y. Luo, X. Peng, S. Yu and M. S. Bakir, "Thermal Reliability Considerations of Resistive Synaptic Devices for 3D CIM System Performance," *IEEE International 3D System Integration Conference (3DIC)*, 2021.

C5. L. Zhu, T. Ta, R. Liu, R. Mathur, X. Xu, S. Das, **A. Kaul**, A. Rico, D. Joseph, B. Cline, S. K. Lim, "Power Delivery and Thermal-Aware Arm-Based Multi-Tier 3D Architecture," *IEEE/ACM Inter. Symp. on Low Power Elec. and Design (ISLPED)*, 2021, pp. 1-6, doi: 10.1109/ISLPED52811.2021.9502481.

C6. **A. Kaul**, S. K. Rajan, M. O. Hossen, G. S. May, and M. S. Bakir, "BEOL-Embedded 3D Polylithic Integration: Thermal and Interconnection Considerations," *IEEE Electronic Components and Technology Conf. (ECTC)*, Orlando, FL, May 2020 (***Nominated for EPS/ECTC Student Travel Award: Top 22 out of 71 student submissions***).

C7. S. K. Rajan, **A. Kaul**, T. Sarvey, G. S. May and M. S. Bakir, "Design Considerations, Demonstration, and Benchmarking of Silicon Microcold Plate and Monolithic Microfluidic Cooling for 2.5D ICs," ***IEEE 71st Electronic Components and Technology Conference (ECTC)***, 2021, pp. 1418-1426, doi: 10.1109/ECTC32696.2021.00227.

C8. R. Saligram, **A. Kaul**, M. S Bakir and A. Raychowdhury, "A Model Study of Multilevel Signaling for High-Speed Chiplet-to-Chiplet Communication in 2.5D Integration," *IFIP/IEEE Inter. Conf. on Very Large Scale Integration (VLSI-SoC)*, Salt Lake City, UT, Oct. 2020.

B.   Journal Publications (Refereed):

J1. **A. Kaul**, Y. Luo, X. Peng, M. Manley, S. Yu and M. S. Bakir, "3-D Heterogeneous Integration of RRAM-Based Compute-In-Memory: Impact of Integration Parameters on Inference Accuracy," in IEEE Transactions on Electron Devices (***TED***), vol. 70, no. 2, pp. 485-492, Feb. 2023, doi: 10.1109/TED.2022.3231570.

J2. X. Peng, **A. Kaul**, M. S. Bakir, and S. Yu, "Heterogeneous 3D Integration of Multi-Tier Compute-in-Memory Accelerators: An Electrical-Thermal Co-Design," *IEEE Transactions on Electron Devices (**TED**)*, Sep. 2021 doi: 10.1109/TED.2021.3111857.

J3. Y. Luo, S. Dutta, **A. Kaul**, S. Lim, M. Bakir, S. Datta, S. Yu, "A Compute-in-Memory Hardware Accelerator Design With Back-End-of-Line (BEOL) Transistor Based Reconfigurable Interconnect," in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (**JETCAS**)*, vol. 12, no. 2, pp. 445-457, June 2022, doi: 10.1109/JETCAS.2022.3177577.

J4. J. Sharda, M. Manley, **A. Kaul**, W. Li, M. Bakir and S. Yu, "Design and Thermal Analysis of 2.5D and 3D Integrated System of a CMOS Image Sensor and a Sparsity-Aware Accelerator for Autonomous Driving," in *IEEE Journal of the Electron Devices Society*, doi: 10.1109/JEDS.2024.3354621

J5. S. K. Rajan, **A. Kaul**, T. E. Sarvey, G. S. May and M. S. Bakir, "Monolithic Microfluidic Cooling of a Heterogeneous 2.5-D FPGA With Low-Profile 3-D Printed Manifolds," in *IEEE Transactions on Components, Packaging and Manufacturing Technology (**TCPMT**)*, vol. 11, no. 6, pp. 974-982, June 2021, doi: 10.1109/TCPMT.2021.3082013.

J6. M. O. Hossen, **A. Kaul**, I. Ganusov, E. Nurvitadhi, M. Pant, R. Gutala, A. Dasu, and M. S. Bakir, "Modeling of Power Delivery Network (PDN) in Bridge-Chips for 2.5-D Heterogeneous Integration Technologies," in *IEEE Transactions on Components, Packaging and Manufacturing Technology (**TCPMT**), 2021 (to appear)*.

J7. T. E. Sarvey, **A. Kaul**, S. K. Rajan, A. Dasu, R. Gutala and M. S. Bakir, "Microfluidic Cooling of a 14-nm 2.5-D FPGA With 3-D Printed Manifolds for High-Density Computing: Design Considerations, Fabrication, and Electrical Characterization," in *IEEE Transactions on Components, Packaging and Manufacturing Technology (**TCPMT**)*, vol. 9, no. 12, pp. 2393-2403, Dec. 2019, doi: 10.1109/TCPMT.2019.2930481.

C.   Book Chapters:

BC1. T. E. Sarvey, **A. Kaul**, and M. S. Bakir, "Monolithic Microfluidic Cooling: Design Considerations, Experimental Validation, and Integration with an FPGA," in *"Embedded Cooling of Electronic Devices: Conduction, Evaporation, and Single-and Two-Phase Convection*", **World Scientific Publications,** 2024. https://doi.org/10.1142/9789811279379_0008

BC2. T. Zheng*, **A. Kaul***, S. Kochupurackal Rajan* and M.S. Bakir (2022), "Polylithic Integrated Circuits using 2.5D and 3D Heterogeneous Integration: Electrical and Thermal Design Considerations and Demonstrations," in *Embedded and Fan-Out Wafer and Panel Level Packaging Technologies for Advanced Application Spaces* (eds B. Keser and S. Kröhnert), (pp. 261-287) ***Wiley***, 2021. https://doi.org/10.1002/9781119793908.ch11.

BC3. R. Saligram, **A. Kaul**, M. S. Bakir, and A. Raychowdhury, "*Multilevel Signaling for High-Speed Chiplet-to-Chiplet Communication*," in VLSI-SoC: Design Trends, Cham, 2021, pp. 149–178. doi: 10.1007/978-3-030-81641-4_8.

#: Complete list: https://tinyurl.com/54tc9zbj

***:* equal contribution

AWARDS AND RECOGNITION

- **EPS Certificate of Achievement**: For contributions in the field of Electronics Packaging, Dec. 09, 2022.
- Awarded the **J.N. Tata Endowment**: Scholarship for graduate research, selected among top 40 from 1000+ applicants, 2016-18.
- Nominated for the **Colonel Oscar P. Cleaver Award** for most outstanding Ph.D. dissertation proposal, Georgia Tech. ECE, 2021.
- Work on "3D polylithic integration of BEOL RRAM" was covered in Chip Scale Review, July-August 2021.
- Nominated for the **EPS/ECTC Conference Student Travel Award**: Top 22 out of 71 student research papers, 2020.

PROFESSIONAL ACTIVITIES AND SERVICE

A.   **Professional Contribution**:
- **Technical Journal Referee**: IEEE Transactions on Electron Devices (TED), IEEE Electron Devices Letters (EDL), IEEE Journal on Exploratory Solid-State Computational Devices Circuits, 2021-2022, IEEE TCAD, Elsevier Microelectronics

B.   Membership:
- Graduate Student Member: IEEE, Electron Devices Society (EDS), Electronics Packaging Society (EPS)

C.   Mentorship:
- Biya Haile, previously BS AE/ECE, current Ph.D. student, ECE, Georgia Tech., bhaile3@gatech.edu.
- Madison Manley, current Ph.D. student, ECE, Georgia Tech., madison.manley@gatech.edu.

TECHNOLOGY SUMMARY

Languages: Python, Matlab, Verilog HDL, C++, shell, D3.js

EDA tools: HSPICE, Cadence Celsius, Cadence Virtuoso, ANSYS Mechanical and Fluent, Synopsys VCS, Calibre, Allegro PCB

Skills: 3D Integration, SoIC design and process flow, hybrid bonding, microelectronic packaging, 3DIC partitioning and non-volatile memory/logic integration, electrical modeling and evaluation of die-to-die signaling metrics, thermal and power delivery modeling for heterogeneous integration, TSV and I/O HSPICE modeling, analytical multi-physics device-system analyses, vector-based power and thermal analysis for multi-core SiPs, computer architecture, unix, data analytics and visualization