

ANKIT KAUL

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EDUCATION

Georgia Institute of Technology, Atlanta, GA **Ph.D., Electrical and Computer Engineering, GPA: 4.0** May 2018 – Dec. 2022 (Expected)

Georgia Institute of Technology, Atlanta, GA **Master of Science, Electrical and Computer Engineering, GPA: 3.65** Aug. 2016 – May 2018
Focus: Digital systems and Computer architecture

Coursework completed: Hardware acceleration for Machine Learning, Interconnection Networks (Network on Chips), Advanced Digital Design with Verilog, Computer Architecture, Advanced VLSI Systems, Digital Systems at Nanometer Nodes.

R.V. College of Engineering, Bangalore, India **Bachelors, Electrical Engineering, GPA: 9.05/10.0** Aug. 2009 – May 2013

EXPERIENCE

Ph.D. intern - Advanced Products, Physical IP, arm – Austin, TX May 2020 – Aug. 2020

Project: Optimization of multi-core system specifications for 2.5D ICs.

- Developed a framework to enable exploration of relationship between core implementation targets, DVFS options, thermal limits, and system throughput for multi-core enterprise server systems. (**Python, Celsius, Voltus**) **Adviser:** Jim Dodrill

Graduate Research Assistant, Integrated 3D systems lab, Georgia Institute of technology – Atlanta, GA May 2018 – Present

- Research focus:** Analytical modeling of thermal coupling, signaling, and power supply noise effects in 2.5D and polyolithic-3D IC systems.
- Adviser:** Dr. Muhannad Bakir (<http://bakirlab.gatech.edu/>) **Funding org.:** SRC

UTC Aerospace Systems, Hardware Engineer – Bangalore, India Jul. 2013 – Jul. 2016

Responsible for board-level circuit performance analysis of an Electronic Control and power quality Monitoring (ECM) unit for Boeing's 777x

Impact: Achieved **\$50k savings** by improving ECM circuit performance via analysis of tolerance bottlenecks using Allegro AMS Simulator

PUBLICATIONS

- A. Kaul**, X. Peng, S. Kochupurackal Rajan, S. Yu, and M.S. Bakir, "Thermal Modeling of 3D Polyolithic Integration and Implications on BEOL RRAM Performance," *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, Dec. 2020.
- A. Kaul**, S. K. Rajan, M. O. Hossen, G. S. May, and M. S. Bakir, "BEOL-Embedded 3D Polyolithic Integration: Thermal and Interconnection Considerations," *IEEE Electronic Components and Technology Conf. (ECTC)*, Orlando, FL, May 2020.
- T. E. Sarvey, **A. Kaul**, S. K. Rajan, A. Dasu, R. Gutala and M. S. Bakir, "Microfluidic Cooling of a 14nm 2.5D FPGA with 3D Printed Manifolds for High Density Computing: Design Considerations, Fabrication, and Electrical Characterization," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2019. (doi: 10.1109/TCPMT.2019.2930481)

TECHNOLOGY SUMMARY

Languages: Matlab, Python, Verilog HDL, C++, shell

Tools: Cadence Celsius, Cadence Virtuoso, ANSYS Mechanical and Fluent, Synopsys VCS, HSPICE, Calibre, Allegro PCB

Skills: Finite difference techniques for modelling thermal and power delivery network in advanced IC integration, vector-based power and thermal analysis, computer architecture, unix

ACADEMIC PROJECTS

Study of limits on accelerator performance due to DRAM performance degradation – individual Jan. 2019 – May 2019

Characterized temperature-driven bandwidth loss in DRAMs and studied the impact of this loss on the runtime performance of systolic CNN hardware accelerator configurations (evaluation tool: **SCALE-SIM systolic CNN accelerator simulator**)

- Established that ~12% temperature-driven DRAM BW loss can lead to 50% increase in runtime for considered MLPerf DNN workloads (**Report:** https://www.dropbox.com/s/jprs23jbmr3kh9c/Kaul_ece8893_final_report.pdf?dl=0)

Achieving High-Radix Topology Performance using SMART Networks – individual Jan. 2018 – May 2018

Proposed a design with multiple SMART (Single-Cycle Multihop Asynchronous Repeated Traversal) Network-on-Chip (NoC) mesh networks in parallel to achieve saturation throughput comparable to high-radix topologies (evaluation tool: **Garnet 2.0 NoC architecture simulator**)

- Demonstrated higher theoretical throughput of a SMART mesh over fbfly variants for heterogeneous traffic with 64 routers (**Report:** https://www.dropbox.com/s/v5bvtq33uehfn3s/CS8803-Report_Kaul.pdf?dl=0)

Systolic array RTL implementation, simulation and synthesis for CNN accelerators – individual (course: H/W for ML) Mar. 2019

Implemented (**Verilog**) a systolic array of processing elements (PE) to demonstrate matrix multiplication using output stationary dataflow

- Performed functional verification (**DVE**) and estimated area and power (**Design Compiler**)
- Synthesized design using Nangate 15nm targeting 1GHz, and reported 9.217 mW at an area of 11809 μm^2 for an 8x8 array of PEs

Simulation and Performance Analysis of Caches – individual Jul. 2017 – Aug. 2017

Investigated effect of cache configurations on performance by designing a cache simulator to measure latencies and read/write miss rates

- Determined optimal cache parameters such as cache and block size, associativity to achieve minimum AMAT (**C++, shell**)

A 3 stage Pipelined Memory and Arithmetic Unit (45nm) – 4-member team Sep. 2016 – Dec. 2016

Implemented backend design of a 64-byte 6T SRAM Array, driver circuit for a 150ff interconnect, and a 16-bit carry look-ahead adder

- Achieved 1.9x target frequency (1.9GHz) at 0.8V consuming 471 uW (Design: **Virtuoso, Spectre**)