ANKIT KAUL

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Short bio: Ph.D. candidate in Electrical and Computer Engineering with a focus on identifying thermal, power delivery, and die-to-die signaling challenges in 2.5D and 3D ICs. I also investigate the impact of 3D integration on emerging non-volatile memory device-based compute in-memory inference models. For my research, I leverage analytical techniques for system level modeling of heterogeneous integration schemes.

EDUCATION

Georgia Institute of Technology, Atlanta, GA — **Ph.D., Electrical and Computer Engineering**, **GPA: 3.68** *May 2018 – Dec. 2022 (expected)*
Minor: Computer Science

Georgia Institute of Technology, Atlanta, GA — **Master of Science, Electrical and Computer Engineering**, **GPA: 3.65** *Aug. 2016 – May 2018*
Focus: Digital systems and Computer architecture

Key coursework (MS+Ph.D) : IC Fabrication, Hardware acceleration for Machine Learning, Advanced Computer Architecture, Interconnection Networks (Network on Chip), Digital Systems at Nanometer Nodes, Advanced Digital Design with Verilog, Advanced VLSI Systems.

R.V. College of Engineering, Bangalore, India — **Bachelors, Electrical Engineering, GPA: 9.05/10.0** *Aug. 2009 – May 2013*

EXPERIENCE

Graduate Research Assistant, Integrated 3D systems lab, Georgia Institute of technology – Atlanta, GA *May 2018 – Present*

- **Research focus**:
  - Impact of 3D integration on emerging non-volatile memory device-based compute in-memory (CIM) inference engine models
  - Analytical modeling of thermal coupling, die-to-die signaling, and power supply noise effects in 2.5D and polylithic-3D IC systems.
- **Adviser: Dr. Muhannad Bakir** (https://bakirlab.gatech.edu/) **Research organization: SRC**

Ph.D. Intern - Advanced Products, Physical IP, arm – Austin, TX *May 2020 – Aug. 2020*

Project: Thermal Design Considerations for 2.5D integration of Arm-based 7nm High-Performance Systems

- Developed a framework to enable exploration of relationship between core implementation targets, DVFS options, thermal limits, and system throughput for multi-core enterprise server systems. (**Python, Celsius, Voltus**) **Adviser:** Jim Dodrill

Impact: Improved Arm's thermal modeling methodology by developing 2.5D multi-core SoC analyses capability for large-scale compute

UTC Aerospace Systems, Hardware Engineer – Bangalore, India *Jul. 2013 – Jul. 2016*

Responsible for board-level circuit performance analysis of an Electronic Control and power quality Monitoring (ECM) unit for Boeing's 777x

Impact: Achieved **$50k savings** by improving ECM circuit performance via analysis of tolerance bottlenecks using Allegro AMS Simulator

AWARDS

- **The J.N. Tata Endowment**, Scholarship for graduate studies at Georgia Tech., selected among top 40 from 1000+ applicants (2016-17).

RESEARCH PUBLICATIONS[#]

A. Conference Publications (Refereed):

C1. L. Zhu, T. Ta, R. Liu, R. Mathur, X. Xu, S. Das, **A. Kaul**, A. Rico, D. Joseph, B. Cline, S. K. Lim, "Power Delivery and Thermal-Aware Arm-Based Multi-Tier 3D Architecture," *IEEE/ACM Inter. Symp. on Low Power Elec. and Design (ISLPED)*, 2021, pp. 1-6, doi: 10.1109/ISLPED52811.2021.9502481.

C2. S. K. Rajan, **A. Kaul**, T. Sarvey, G. S. May and M. S. Bakir, "Design Considerations, Demonstration, and Benchmarking of Silicon Microcold Plate and Monolithic Microfluidic Cooling for 2.5D ICs," *IEEE 71st Electronic Components and Technology Conference (ECTC)*, 2021, pp. 1418-1426, doi: 10.1109/ECTC32696.2021.00227.

C3. **A. Kaul**, X. Peng, S. K. Rajan, S. Yu and M. S. Bakir, "Thermal Modeling of 3D Polylithic Integration and Implications on BEOL RRAM Performance," *IEEE International Electron Devices Meeting (IEDM)*, 2020, pp. 13.1.1-13.1.4, doi: 10.1109/IEDM13553.2020.9371983. *(invited)*.

C4. X. Peng, W. Chakraborty, **A. Kaul**, W. Shim, M. S. Bakir, S. Datta, S. Yu, "Benchmarking Monolithic 3D Integration for Compute-in-Memory Accelerators: Overcoming ADC Bottlenecks and Maintaining Scalability to 7nm or Beyond," *IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, Dec. 2020.

C5. R. Saligram, **A. Kaul**, M. S Bakir and A. Raychowdhury, "A Model Study of Multilevel Signaling for High-Speed Chiplet-to-Chiplet Communication in 2.5D Integration," *IFIP/IEEE Inter. Conf. on Very Large Scale Integration (VLSI-SoC)*, Salt Lake City, UT, Oct. 2020.

C6. **A. Kaul**, S. K. Rajan, M. O. Hossen, G. S. May, and M. S. Bakir, "BEOL-Embedded 3D Polylithic Integration: Thermal and Interconnection Considerations," *IEEE Electronic Components and Technology Conf. (ECTC)*, Orlando, FL, May 2020 ***(Nominated for EPS/ECTC Student Travel Award: Top 22 out of 71 student submissions)***.

B. Journal Publications (Refereed):

J1. X. Peng, **A. Kaul**, M. S. Bakir, and S. Yu, "Heterogeneous 3D Integration of Multi-Tier Compute-in-Memory Accelerators: An Electrical-Thermal Co-Design," *IEEE Transactions on Electron Devices (TED)*, 2021 *(accepted, in press)*.

J2. S. K. Rajan, **A. Kaul**, T. E. Sarvey, G. S. May and M. S. Bakir, "Monolithic Microfluidic Cooling of a Heterogeneous 2.5-D FPGA With Low-Profile 3-D Printed Manifolds," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 11, no. 6, pp. 974-982, June 2021, doi: 10.1109/TCPMT.2021.3082013.

J3. M. O. Hossen, **A. Kaul**, I. Ganusov, E. Nurvitadhi, M. Pant, R. Gutala, A. Dasu, and M. S. Bakir, "Modeling of Power Delivery Network (PDN) in Bridge-Chips for 2.5-D Heterogeneous Integration Technologies," in *IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021 (submitted, under review)*.

J4. T. E. Sarvey, **A. Kaul**, S. K. Rajan, A. Dasu, R. Gutala and M. S. Bakir, "Microfluidic Cooling of a 14-nm 2.5-D FPGA With 3-D Printed Manifolds for High-Density Computing: Design Considerations, Fabrication, and Electrical Characterization," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 9, no. 12, pp. 2393-2403, Dec. 2019, doi: 10.1109/TCPMT.2019.2930481.

C. Book Chapters (Refereed):

BC1. M. S. Bakir, T. Zheng*, **A. Kaul***, and S. K. Rajan*, "Polylithic Integrated Circuits using 2.5D and 3D Heterogeneous Integration: Electrical and Thermal Design Considerations and Demonstrations," in "*Embedded and Fan-Out Wafer and Panel Level Packaging Technologies*", Wiley Publications, USA, 2021 *(submitted, under review)*.

BC2. R. Saligram, **A. Kaul**, M. S. Bakir, and A. Raychowdhury, "Multilevel Signaling for High-Speed Chiplet-to-Chiplet Communication," in VLSI-SoC: Design Trends, Cham, 2021, pp. 149–178. doi: 10.1007/978-3-030-81641-4_8.

BC3. T. E. Sarvey, **A. Kaul**, and M. S. Bakir, "Monolithic Microfluidic Cooling: Design Considerations, Experimental Validation, and Integration with an FPGA," in "Embedded Cooling of Electronic Devices: Encyclopedia of Thermal Packaging", World Scientific Publications, 2018 *(submitted, under review)*.

#: Complete list: https://tinyurl.com/54tc9zbj

***: equal contribution*

OTHER PROFESSIONAL ACTIVITIES AND SERVICE

A. Professional Contribution:
- Technical Journal Referee: IEEE Transactions on Electron Devices (TED), IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2021

B. Membership:
- Student Member, The Institute of Electrical and Electronics Engineers (IEEE)
- Student Member, Electron Devices Society (EDS)

C. Mentorship:
- Biya Haile, previously BS AE/ECE, current Ph.D. student, ECE, Georgia Tech., bhaile3@gatech.edu.

TECHNOLOGY SUMMARY

Languages: Python, Matlab, Verilog HDL, C++, shell

EDA tools: Cadence Celsius, HSPICE, Cadence Virtuoso, ANSYS Mechanical and Fluent, Synopsys VCS, Calibre, Allegro PCB

Skills: Finite difference techniques for modelling thermal and power delivery network in advanced IC integration, analytical multi-physics device-system simulations, vector-based power and thermal analysis, computer architecture, unix, data analytics and visualization

ACADEMIC PROJECTS

Study of limits on hardware accelerator performance due to DRAM performance degradation *Jan. 2019 – May 2019*

Characterized temperature-driven bandwidth loss in DRAMs and studied the impact of this loss on the runtime performance of systolic CNN hardware accelerator configurations (evaluation tool: **SCALE-SIM systolic CNN accelerator simulator**)

- Established that ~12% temperature-driven DRAM BW loss can lead to 50% increase in runtime for considered MLPerf DNN workloads

(**Report**: https://www.dropbox.com/s/jprs23jbmr3kh9c/Kaul_ece8893_final_report.pdf?dl=0)

Achieving High-Radix Topology Performance using SMART Networks *Jan. 2018 – May 2018*

Proposed a design with multiple SMART (Single-Cycle Multihop Asynchronous Repeated Traversal) Network-on-Chip (NoC) mesh networks in parallel to achieve saturation throughput comparable to high-radix topologies (evaluation tool: **Garnet 2.0 NoC architecture simulator**)

- Demonstrated higher theoretical throughput of a SMART mesh over fbfly variants for heterogeneous traffic with 64 routers

(**Report**: https://www.dropbox.com/s/v5bvtq33uehfn3s/CS8803-Report_Kaul.pdf?dl=0)

TECHNOLOGY SUMMARY

Languages: Python, Matlab, Verilog HDL, C++, shell, D3.js

Tools: Cadence Celsius, Cadence Virtuoso, ANSYS Mechanical and Fluent, Synopsys VCS, HSPICE, Calibre, Allegro PCB

Technical Skills: Finite difference techniques for modelling thermal and power delivery network in advanced IC integration, vector-based power and thermal analysis, analytical multi-physics device-system simulations, computer architecture, data visualization, unix