MAULANA AZAD NATIONAL INSTITUTE OF TECHNOLOGY, BHOPAL
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
MID TERM EXAMINATION (March-2021)

Sub:ComputerArchitecture **Sub Code: CSE- 222**
Time: 9:30 am to 11:00 am (90 Minutes) **Branch & Sem: CSE IV Sem**
Date-02/03/2021 **Max. Marks: 40**

<table>
<tr><th>Q.No</th><th>Questions</th><th>Marks</th></tr>
<tr><td>1.</td><td>i) Consider the following statement executed on the stack CPU.
Z = ((A*B+C) + (D*(E+F))) +Y
CPU word length is 16 bit and supports 24 bit address. CPU contain 1 word opcode. How much space is required for the program in Bytes?

ii) Consider the following statement executed on the accumulator CPU.
X = (A+B) * (C+D) + (E+F) / (G+H)
What are the minimum number of machine instructions required to execute the above statement?</td><td>08</td></tr>
<tr><td>2.</td><td>i) A 20 bit instruction is placed in 512W memory. If there exist 3 two address instructions and 256 one address instructions. Then how many zero address instructions can be formulated by considering a processor which uses expand opcode technique ?

ii) A hypothetical processor uses load and store instructions to access the memory. CPU always takes the operands from the registers. Identify the minimum number of registers required to evaluate the statement.
A = (X+Y) * (P+Q)</td><td>08</td></tr>
<tr><td>3.</td><td>Consider a hypothetical processor which supports both one address and zero address instructions. Processsor supports 4K word memory. A 32 bit instruction is placed in memory.
a) What is the range of one address and zero address instructions possible in the processor?
b) If there exist 24 one address instructions then how many zero address instructions can be formulated?</td><td>08</td></tr>
<tr><td>4.</td><td>Consider 16 way set associative cache of 64KB organized into a 32 byte blocks. CPU generates 36 bit physical address to access the data. In the cache controller, each tag is comprising of 1 valid bit and a write through procedure is used. Calculate the following-
(i) Number of sets in cache
(ii) Show the address binding
(iii) Number of tag bits in the line of a set
(iv) Tag memory size</td><td>08</td></tr>
<tr><td>5.</td><td>A control unit supports 7 groups of mutually exclusive control signals given below:
<table><tr><td>Group</td><td>G1</td><td>G2</td><td>G3</td><td>G4</td><td>G5</td><td>G6</td><td>G7</td></tr><tr><td>Control Signals</td><td>3</td><td>1</td><td>15</td><td>91</td><td>44</td><td>89</td><td>36</td></tr></table>How many bits are saved using vertical over horizontal programming?</td><td>08</td></tr>
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