BIRLA INSTITUTE OF TECHNOLOGY, MESRA, RANCHI
(MID SEMESTER EXAMINATION SP2023)

CLASS: BTECH **SEMESTER :VI**
BRANCH: ECE/MECH/EEE **SESSION : SP/2023**

SUBJECT:CS203 COMPUTER ORGANIZATION & ARCHITECTURE

TIME: 02 Hours **FULL MARKS: 25**

INSTRUCTIONS:
1. The question paper contains 5 questions each of 5 marks and total 25 marks.
2. Attempt all questions.
3. The missing data, if any, may be assumed suitably.
***4*. Tables/Data handbook/Graph paper etc., if applicable, will be supplied to the candidates**

			CO	BL
Q.1(a)	Distinguish between Computer Organization and Architecture. Out of CO & CA which one has undergone more change with respect to time?	[2]	1	4
Q.1(b)	Explain the functions of IR, MAR, MDR registers present in the CPU	[3]	2	2
Q.2(a)	What do you mean by computer performance? What are the relevant parameters which affect mostly the performance of computer?	[2]	1	1
Q.2(b)	i) Perform following operations in 2's complement representation of binary numbers: (+7) + (-4) and (-4) – (-7) ii) Convert number $(777)_8$ to $(\ )_5$	[3]	3	4
Q.3(a)	Explain instruction sequencing with the help of suitable example.	[2]	2	2
Q.3(b)	Represent the decimal -20.125 into its IEEE754 Single Precision floating point format.	[3]	2	4
Q.4(a)	What do you mean by Byte addressability? Differentiate Big-Endian and Little-Endian Assignments.	[2]	2	1
Q.4(b)	Draw the flowchart of booths algorithms. Multiply (-8) X (9) using booths multiplication algorithm.	[3]	3	4
Q.5(a)	What is relative addressing mode? Explain with the help of example.	[2]	2	2
Q.5(b)	An instruction is stored at location 400 with its address fields at location 401. The address field has the value 500. A processor register R1 contains the number 300. Evaluate the effective address if the addressing mode of the instruction is (i) Direct (ii) Immediate (iii) Relative (iv) Register Indirect (v) Index with R1 as the Index register.	[3]	2	4

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