FIFO depth Calculation

- FIFO can be used to avoid overflow and underflow conditions .
- The scenario can be two of following
  - Writing is faster than reading then there is possibility of overflow
  - Writing is slower than reading then there is possibility of underflow.
- Consider the worst case in FIFO depth calculation.
- Size of FIFO basically implies that how much data is required to buffer .
- FIFO depth depends on data rate of reading and writing.
- The logic in fixing the size of the FIFO is to find the no. of data items which are not read in a period in which writing process is done.
- In other words, FIFO depth will be equal to the no. of data items that are left without reading.

Case: 1 (Write frequency > read frequency)

- Fwrite = 80 MHz , Fread = 50 MHz
- Burst Length = No. of data items to be transferred= D = 120.
- There are no idle cycles in both reading and writing which means that, all the items in the burst will be written and read in consecutive clock cycles

Solution:

- Time required to write one data item = $\frac{1}{80\ MHz}$ = 12.5 nSec.
- Time required to write all the data in the burst = 120 * 12.5 nSec. = 1500 nSec.
- Time required to read one data item = $\frac{1}{50\ MHz}$ = 20 nSec.
- So, for every 20nSec, the module B is going to read one data in the burst.
- So, in a period of 1500nSec, 120 no. of data items can be written.
- And the no. of data items can be read in a duration of 1500 nSec = $\left(\frac{1500\ nSec}{20\ nSec}\right) = 75$
- The remaining no. of bytes to be stored in the FIFO = 120 – 75 = 45.
- So, the FIFO which has to be in this scenario must be capable of storing 45 data items.

- **Case: 2 (Write frequency > read frequency)**
- Fwrite >Fread with one clk cycle delay between two successive reads and writes.

Solution:

This is similar to case 1.

Case: 3 (Write frequency > read frequency)

- Fwrite = 80 MHz , Fread = 50 MHz
- Burst Length = No. of data items to be transferred= D = 120.
- No. of idle cycles between two successive writes is = 1.
- No. of idle cycles between two successive reads is = 3.

Solution:

- The no. of idle cycles between two successive writes is 1 clock cycle. It means that, after writing one data, module A is waiting for one clock cycle, to initiate the next write. So, it can be understood that for every **two** clock cycles, one data is written.
- The no. of idle cycles between two successive reads is 3 clock cycles. It means that, after reading one data, module B is waiting for 3 clock cycles, to initiate the next read. So, it can be understood that for every **four** clock cycles, one data is read.
- Time required to write one data item = $2 * \frac{1}{80\ MHz} = 25$ nSec.
- Time required to write all the data in the burst = 120 * 25 nSec. = 3000 nSec.
- Time required to read one data item = $4 * \frac{1}{50\ MHz} = 80$ nSec.
- So, for every 80 nSec, the module B is going to read one data in the burst.
- So, in a period of 3000 nSec, 120 no. of data items can be written.
- The no. of data items can be read in a period of 3000 nSec = $\left(\frac{3000\ nSec}{80\ nSec}\right) = 37.5 \simeq 37$
- The remaining no. of bytes to be stored in the FIFO = 120 – 37 = 83.
- **So, the FIFO which has to be in this scenario must be capable of storing 83 data items.**

Case: 4 (Write frequency > read frequency)

- Fwrite = 80 MHz , Fread = 50 MHz
- Burst Length = No. of data items to be transferred= D = 120.
- Duty cycle of wr_enb (write enable) = 50 % = ½.
- Duty cycle of rd_enb (read enable) = 25 % = ¼.

Solution:

This scenario is no way different from the previous scenario (case - 3), because, in this case also, one data item will be written in 2 clock cycles and one data item will be read in 4 clock cycles.

Depth of FIFO Should be 83

- **Case: 5 (Write frequency < read frequency)**
- Fwrite = 30 MHz , Fread = 50 MHz
- Burst Length = No. of data items to be transferred= D = 120.
- There are no idle cycles in both reading and writing which means that, all the items in the burst will be written and read in consecutive clock cycles

Solution:

In this case, a **FIFO of depth '1'** will be sufficient because, there will not be any data loss since the reading is faster than writing.

Case: 6 (Write frequency < read frequency)

- Fwrite = 30 MHz , Fread = 50 MHz
- Burst Length = No. of data items to be transferred= D = 120.
- Duty cycle of wr_enb (write enable) = 50 % = ½.
- Duty cycle of rd_enb (read enable) = 25 % = ¼.

Solution:

- The no. of idle cycles between two successive writes is 1 clock cycle. It means that, after writing one data, module A is waiting for one clock cycle, to initiate the next write. So, it can be understood that for every **two** clock cycles, one data is written.
- The no. of idle cycles between two successive reads is 3 clock cycles. It means that, after reading one data, module B is waiting for 3 clock cycles, to initiate the next read. So, it can be understood that for every **four** clock cycles, one data is read.
- Time required to write one data item = $2 * \frac{1}{30\ MHz}$ = 66.667 nSec.
- Time required to write all the data in the burst = 120 * 66.667 nSec. = 8000 nSec.
- Time required to read one data item = $4 * \frac{1}{50\ MHz}$ = 80 nSec.
- So, for every 80 nSec, the module B is going to read one data item in the burst.
- So, in a period of 8000 nSec, 120 no. of data items can be written.
- The no. of data items can be read in a period of 8000 nSec = $\left(\frac{8000\ nSec}{80\ nSec}\right) = 100$
- The remaining no. of bytes to be stored in the FIFO = 120 – 100 = 20.
- **So, the FIFO which has to be in this scenario must be capable of storing 20 data items.**

- **Case: 7 (Write frequency = read frequency)**
- Fwrite = 30 MHz , Fread = 30 MHz
- Burst Length = No. of data items to be transferred= D = 120.
- There are no idle cycles in both reading and writing which means that, all the items in the burst will be written and read in consecutive clock cycles

Solution:

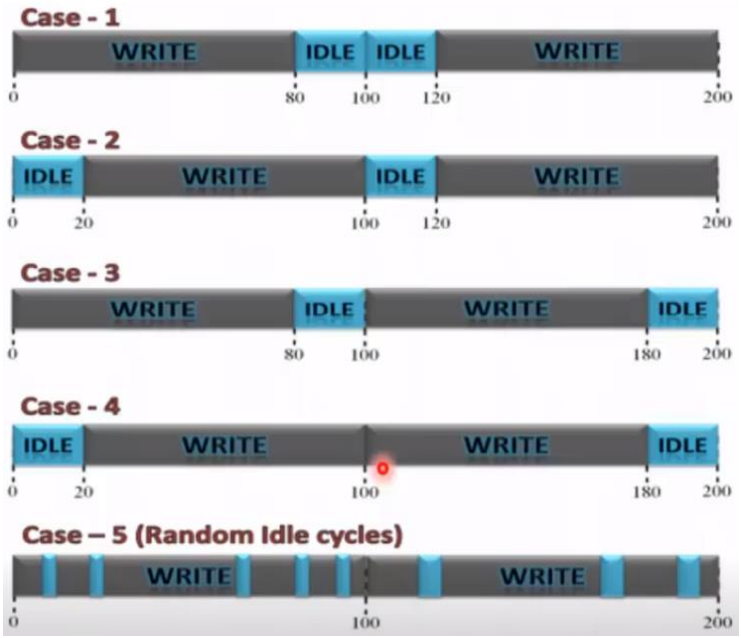
FIFO is not required, if both write and read clocks are in same phase.

FIFO of depth '1' if both write and read clocks are out of phase

- **Case: 8 (Write frequency = read frequency)**
- Fwrite = 50 MHz , Fread = 50 MHz
- Burst Length = No. of data items to be transferred= D = 120.
- No. of idle cycles between two successive writes is = 1.
- No. of idle cycles between two successive reads is = 3.

Solution:

- The no. of idle cycles between two successive writes is 1 clock cycle. It means that, after writing one data, module A is waiting for one clock cycle, to initiate the next write. So, it can be understood that for every **two** clock cycles, one data is written.
- The no. of idle cycles between two successive reads is 3 clock cycles. It means that, after reading one data, module B is waiting for 3 clock cycles, to initiate the next read. So, it can be understood that for every **four** clock cycles, one data is read.
- Time required to write one data item = $2 * \frac{1}{50\ MHz} = 40$ nSec.
- Time required to write all the data in the burst = 120 * 40 nSec. = 4800 nSec.
- Time required to read one data item = $4 * \frac{1}{50\ MHz} = 80$ nSec.
- So, for every 80 nSec, the module B is going to read one data item in the burst.
- So, in a period of 4800 nSec, 120 no. of data items can be written.
- The no. of data items can be read in a period of 4800 nSec = $\left(\frac{4800\ nSec}{80\ nSec}\right) = 60$
- The remaining no. of bytes to be stored in the FIFO = 120 – 60 = 60.
- **So, the FIFO which has to be in this scenario must be capable of storing 60 data items.**



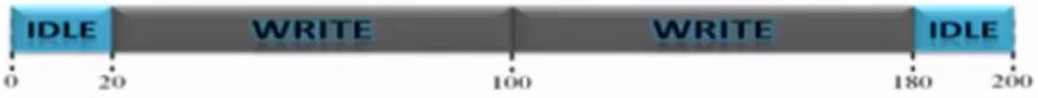
Case	No. of cycles taken to complete write
1	200
2	180
3	180
4	160
5	200

- **Case: 9 (Writing frequency = reading frequency)**
- **Writing Data = 80 DATA/100 Clock (Randomization of 20 Data's)**
- **Outgoing Data= 8 DATA/10 Clock**

Solution:

We will consider worst case

So let us consider 200 Cycles.



In 200 Cycle 160 Data is written. it means 160 data continuously written in 160 clock it is the worst case .

10 clocks→8 read data.

160 clocks→ 8x160/10 =128 read data.

So the Difference between Written Data and Read Back Data is = 160-128=32.

- **Case: 10 Specifications in a different way**
- Given the following FIFO rules, how deep does the FIFO need to be to prevent underflow or overflow?
- Frequency (clk A) = frequency (clk B)/4
- Period (en_B) = period (clk_A)*100
- Duty cycle (en_B) = 25%
- Assume some numerical values, if the specifications are in this way.
- Assume frequency of clk_B = 100MHz
- So, the frequency of clk_A = 100MHz /4 = 25MHz.
- In the specifications given, the burst length is not specified . The burst length is assumed as 100.
- Time required to write one data item = $\frac{1}{25\ MHz}$ = 40 nSec.
- Time required to write all the data in the burst = 100 * 40 nSec. = 4000 nSec.
- And the duty cycle of en_B is 25 % means that, out of 4000 nSec in which the writing process is completed, reading is done only in a period of 1000 nSec (25% of 4000 nSec.)
- So, the FIFO should be capable of holding the data which is being written in the remaining 3000 nSec.
- The no. of data items can be read in a period of 3000 nSec = $\left(\frac{3000\ nSec}{40\ nSec}\right) = 75$