a small blue box around it and produce a dialog box for the change. For the source, a dialog box labeled **DC_POWER** will result, in which the heading **Label** is selected and the **refDEs** retyped as **E**. Click **OK** and the label **E** will appear. The same procedure can change the value to 20 V, although in this case the **Value** heading is chosen and the units are chosen using the scroll at the right of the entered value.

The next step is to determine what quantities are to be measured and how to measure them. For this network a multimeter will be used to measure the current through the resistor **R1**. The multimeter is found at the top of the **Instrument** toolbar. After selection it can be placed on the screen in the same manner as the other elements. Double-clicking the meter will then result in the **Multimeter-XXM1** dialog box, in which **A** is selected to set the multimeter as an ammeter. In addition, the **DC** box (a straight line) must be selected because we are dealing with dc voltages. The current through the diode **D1** and the voltage across the resistor **R2** will be found using **Indicators**, which are found as the tenth option to the right on the **Component** toolbar. The software symbol looks like an LED with a red dashed figure eight inside. Click on this option and a **Select a Component** dialog box will appear. Under **Family**, select **AMMETER** and then take note of the **Component** listing and the four options for the orientation of the indicator. For our analysis the **AMMETER_H** will be chosen since the plus sign or entering point for the current is on the left for the diode **D1**. Click **OK** and the indicator can be placed to the left of the diode **D1**. For the voltage across the resistor **R2**, the option **VOLTMETER_HR** is chosen so the polarity matches that across the resistor.

Finally, all the components and meters must be connected. This is accomplished by simply placing the cursor at the end of an element until a small circle and a set of crosshairs appear to designate the starting point. Once these are in place, click the location and an **x** will appear at the terminal. Then move to the end of the other element and left-click the mouse again—a red connecting wire will automatically appear with the most direct route between the two elements. The process is called **Automatic Wiring**.

Now that all the components are in place it is time to initiate the analysis of the circuit, an operation that can be performed in one of three ways. One option is to select **Simulate** at the head of the screen followed by **Run**. The next is the green arrow in the **Simulation** toolbar. The last is to simply toggle the switch at the head of the screen to the **1** position. In each case a solution appears in the indicators after a few seconds that seems to flicker over time. This flickering simply indicates the software package is repeating the analysis over time. To accept the solution and stop the continuing simulation, either toggle the switch to the **0** position or select the lightning bolt keypad again.

The current through the diode is 3.349 mA, which compares well with the 3.32 mA in Example 2.13. The voltage across the resistor R_2 is 18.722 V, which is close to the 18.6 V of the same example. After the simulation, the multimeter can be displayed as shown in Fig. 2.151 by double-clicking on the meter symbol. By clicking anywhere on the meter, the top portion is dark blue, and the meter can be moved to any location by simply clicking on the blue region and dragging it to the desired location. The current of 193.285 μA is very close to the 212 μA of Example 2.13. The differences are primarily due to the fact that each diode voltage is assumed to be 0.7 V, whereas in fact it is different for each diode of Fig. 2.151 since the current through each is different. In all, however, the Multisim solution is a very close match with the approximate solution of Example 2.13.

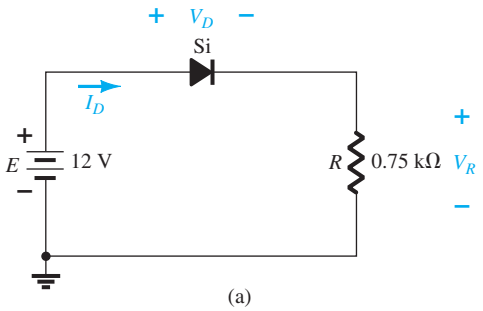
PROBLEMS

**Note:* Asterisks indicate more difficult problems.

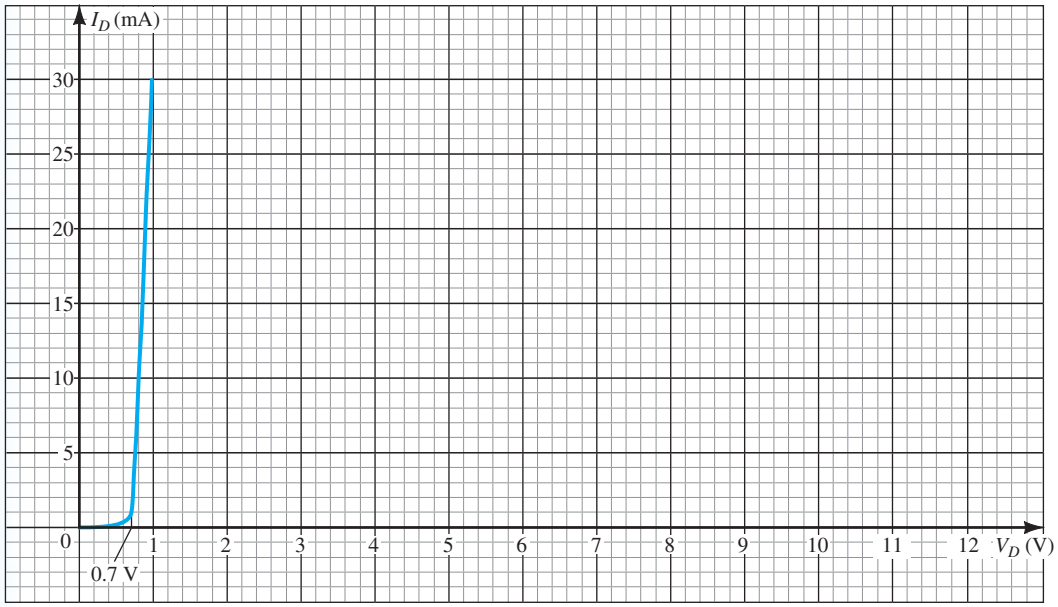
2.2 Load-Line Analysis

1. **a.** Using the characteristics of Fig. 2.152b, determine I_D, V_D, and V_R for the circuit of Fig. 2.152a.
   b. Repeat part (a) using the approximate model for the diode, and compare results.
   c. Repeat part (a) using the ideal model for the diode, and compare results.
2. **a.** Using the characteristics of Fig. 2.152b, determine I_D and V_D for the circuit of Fig. 2.153.
   b. Repeat part (a) with $R = 0.47\ \text{k}\Omega$.
   c. Repeat part (a) with $R = 0.68\ \text{k}\Omega$.
   d. Is the level of V_D relatively close to 0.7 V in each case?

How do the resulting levels of I_D compare? Comment accordingly.



(a)



(b)

FIG. 2.152
Problems 1 and 2.

3. Determine the value of R for the circuit of Fig. 2.153 that will result in a diode current of 10 mA if $E = 7$ V. Use the characteristics of Fig. 2.152b for the diode.

4. a. Using the approximate characteristics for the Si diode, determine V_D, I_D, and V_R for the circuit of Fig. 2.154.

b. Perform the same analysis as part (a) using the ideal model for the diode.

c. Do the results obtained in parts (a) and (b) suggest that the ideal model can provide a good approximation for the actual response under some conditions?

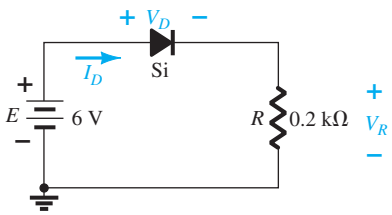


FIG. 2.153
Problems 2 and 3.

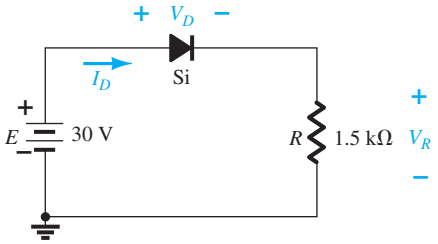


FIG. 2.154
Problem 4.

5. Determine the current I for each of the configurations of Fig. 2.155 using the approximate equivalent model for the diode.

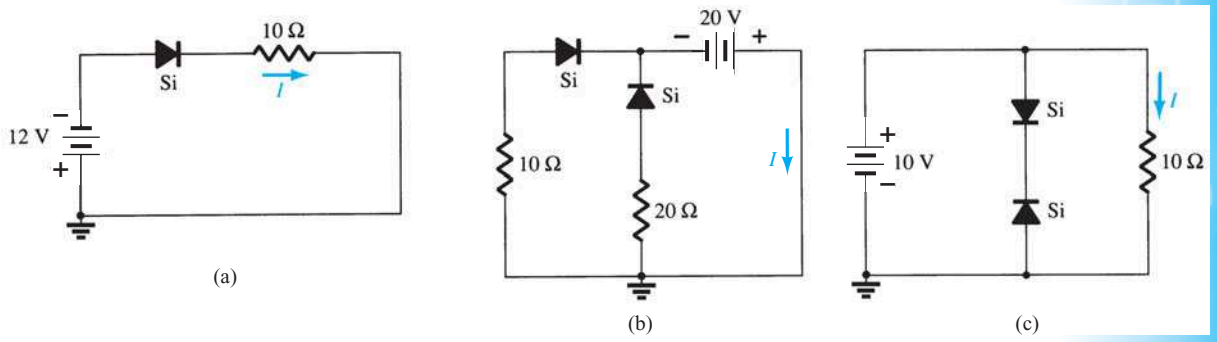


FIG. 2.155
Problem 5.

6. Determine V_o and I_D for the networks of Fig. 2.156.

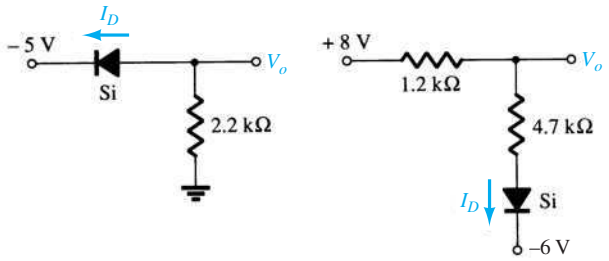


FIG. 2.156
Problems 6 and 49.

***7.** Determine the level of V_o for each network of Fig. 2.157.

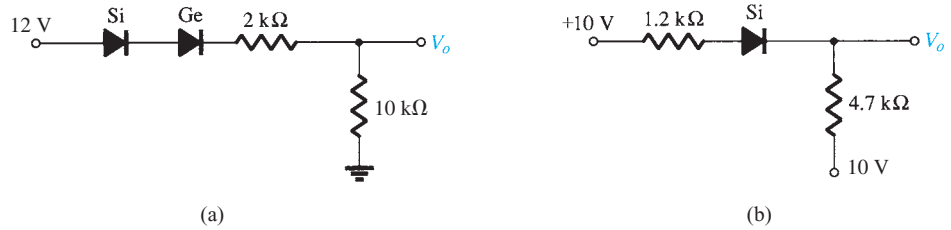


FIG. 2.157
Problem 7.

***8.** Determine V_o and I_D for the networks of Fig. 2.158.

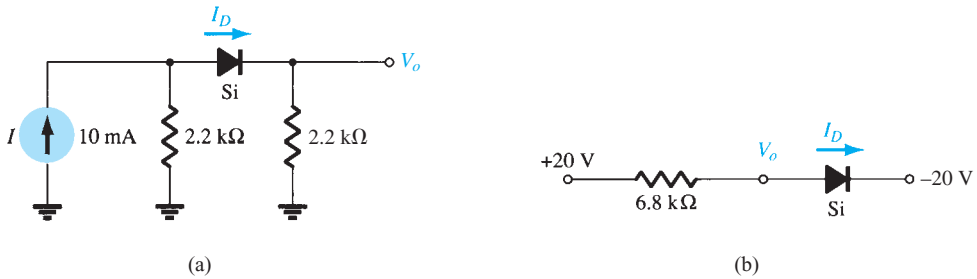


FIG. 2.158
Problem 8.

*9. Determine V_{o_1} and V_{o_2} for the networks of Fig. 2.159.

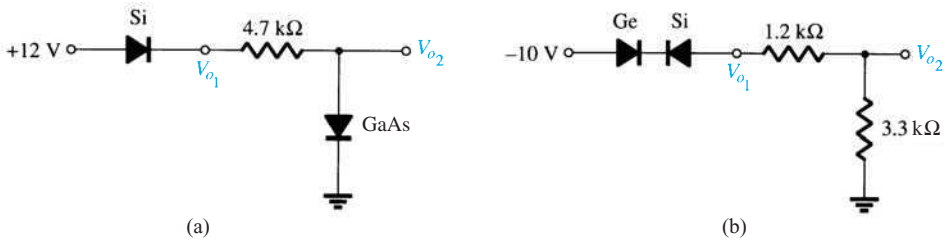


FIG. 2.159
Problem 9.

2.4 Parallel and Series–Parallel Configurations

10. Determine V_o and I_D for the networks of Fig. 2.160.

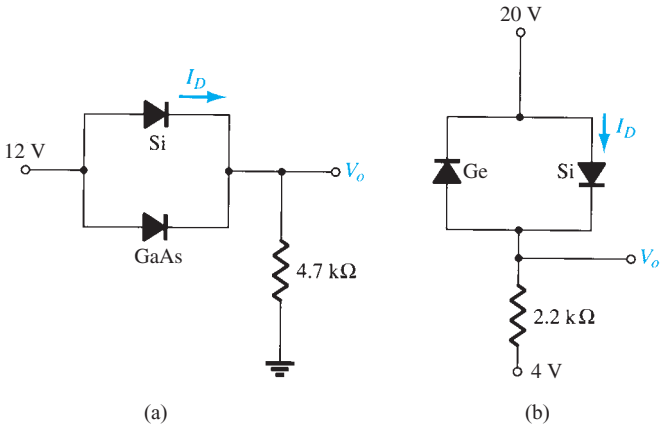


FIG. 2.160
Problems 10 and 50.

*11. Determine V_o and I for the networks of Fig. 2.161.

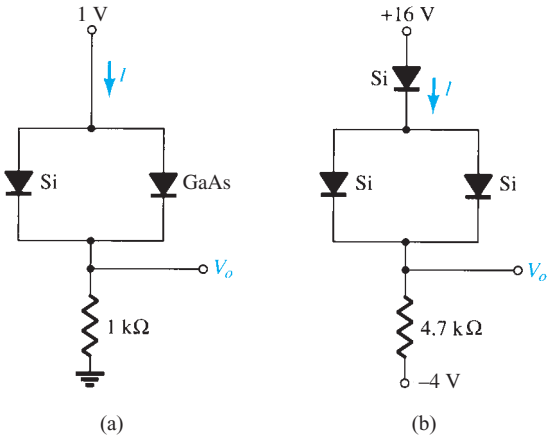


FIG. 2.161
Problem 11.

12. Determine V_{o_1}, V_{o_2}, and I for the network of Fig. 2.162.

*13. Determine V_o and I_D for the network of Fig. 2.163.

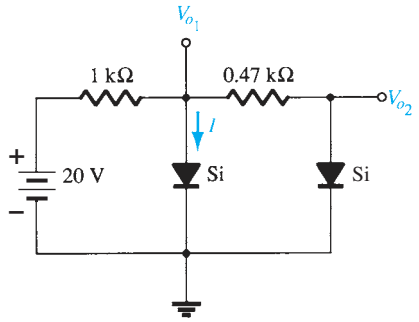


FIG. 2.162
Problem 12.

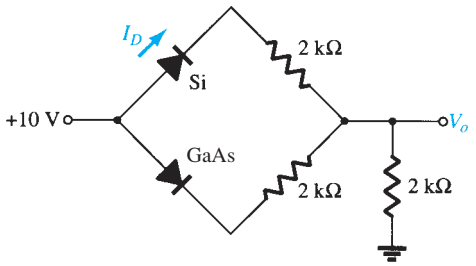


FIG. 2.163
Problems 13 and 51.

2.5 AND/OR Gates

14. Determine V_o for the network of Fig. 2.39 with 0 V on both inputs.

15. Determine V_o for the network of Fig. 2.39 with 10 V on both inputs.

16. Determine V_o for the network of Fig. 2.42 with 0 V on both inputs.

17. Determine V_o for the network of Fig. 2.42 with 10 V on both inputs.

18. Determine V_o for the negative logic OR gate of Fig. 2.164.

19. Determine V_o for the negative logic AND gate of Fig. 2.165.

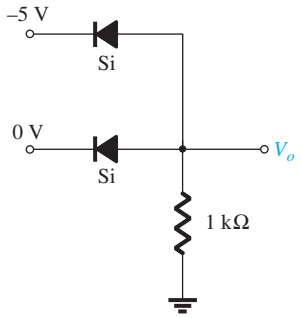


FIG. 2.164
Problem 18.

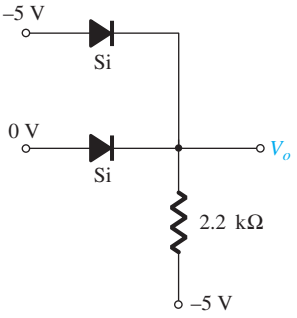


FIG. 2.165
Problem 19.

20. Determine the level of V_o for the gate of Fig. 2.166.

21. Determine V_o for the configuration of Fig. 2.167.

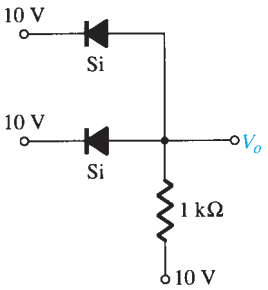


FIG. 2.166
Problem 20.

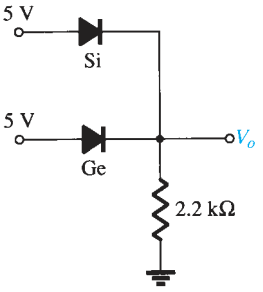


FIG. 2.167
Problem 21.

2.6 Sinusoidal Inputs; Half-Wave Rectification

22. Assuming an ideal diode, sketch v_i, v_d, and i_d for the half-wave rectifier of Fig. 2.168. The input is a sinusoidal waveform with a frequency of 60 Hz. Determine the profit value of v_i from the given dc level.

23. Repeat Problem 22 with a silicon diode ($V_K = 0.7$ V).

24. Repeat Problem 22 with a 10 kΩ load applied as shown in Fig. 2.169. Sketch v_L and i_L.

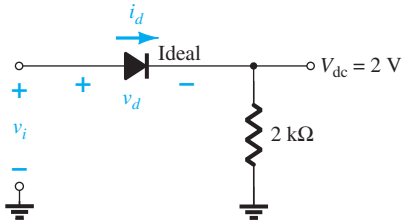


FIG. 2.168
Problems 22 through 24.

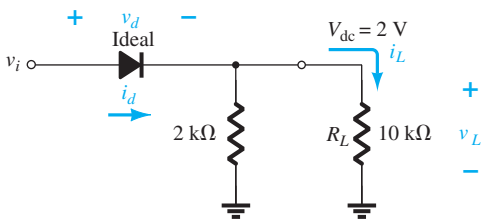


FIG. 2.169
Problem 24.

25. For the network of Fig. 2.170, sketch v_o and determine V_{dc}.

***26.** For the network of Fig. 2.171, sketch v_o and i_R.

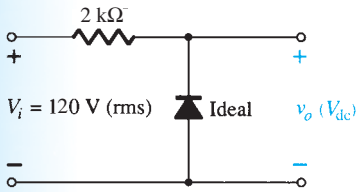


FIG. 2.170
Problem 25.

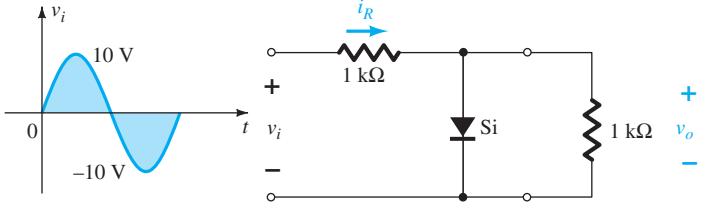


FIG. 2.171
Problem 26.

***27.** **a.** Given $P_{max} = 14$ mW for each diode at Fig. 2.172, determine the maximum current rating of each diode (using the approximate equivalent model).
b. Determine I_{max} for the parallel diodes.
c. Determine the current through each diode at $V_{i_{max}}$ using the results of part (b).
d. If only one diode were present, which would be the expected result?

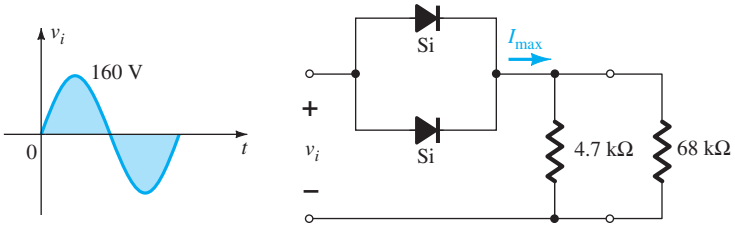


FIG. 2.172
Problem 27.

2.7 Full-Wave Rectification

28. A full-wave bridge rectifier with a 120-V rms sinusoidal input has a load resistor of 1 kΩ.
a. If silicon diodes are employed, what is the dc voltage available at the load?
b. Determine the required PIV rating of each diode.
c. Find the maximum current through each diode during conduction.
d. What is the required power rating of each diode?

29. Determine v_o and the required PIV rating of each diode for the configuration of Fig. 2.173. In addition, determine the maximum current through each diode.

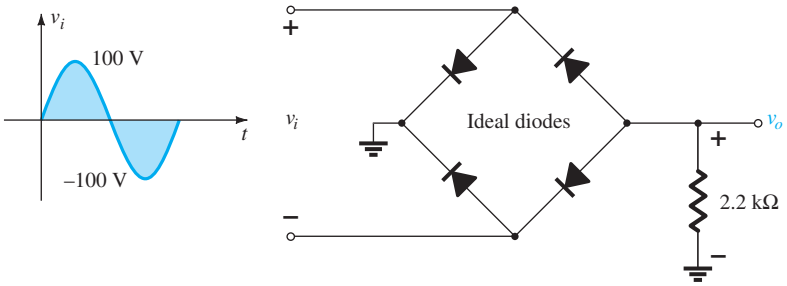


FIG. 2.173
Problem 29.

***30.** Sketch v_o for the network of Fig. 2.174 and determine the dc voltage available.

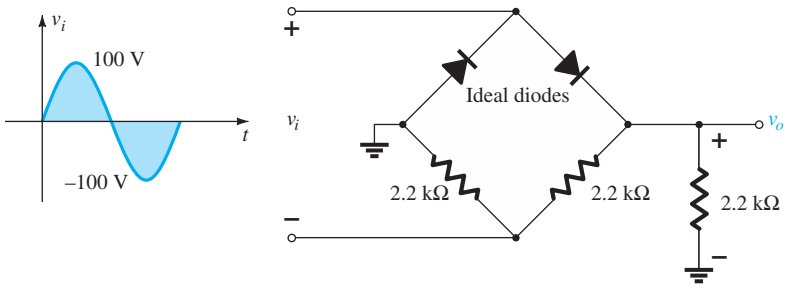


FIG. 2.174
Problem 30.

***31.** Sketch v_o for the network of Fig. 2.175 and determine the dc voltage available.

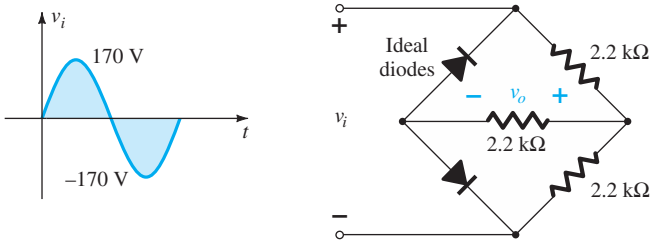


FIG. 2.175
Problem 31.

2.8 Clippers

32. Determine v_o for each network of Fig. 2.176 for the input shown.

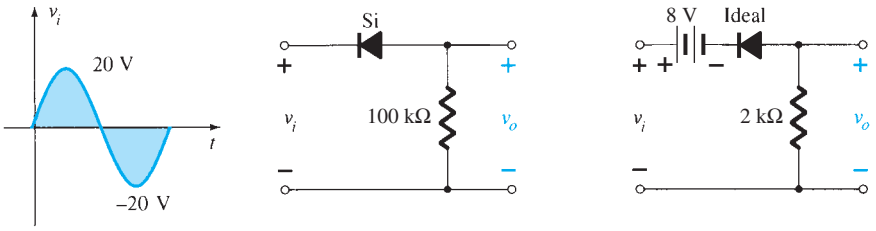


FIG. 2.176
Problem 32.

33. Determine v_o for each network of Fig. 2.177 for the input shown.

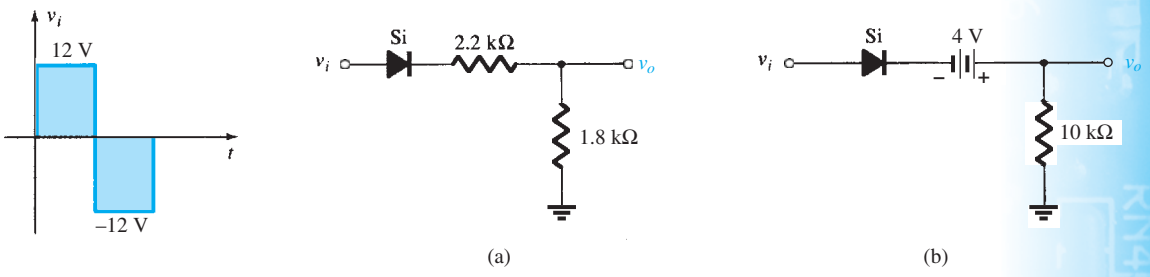


FIG. 2.177
Problem 33.

*34. Determine v_o for each network of Fig. 2.178 for the input shown.

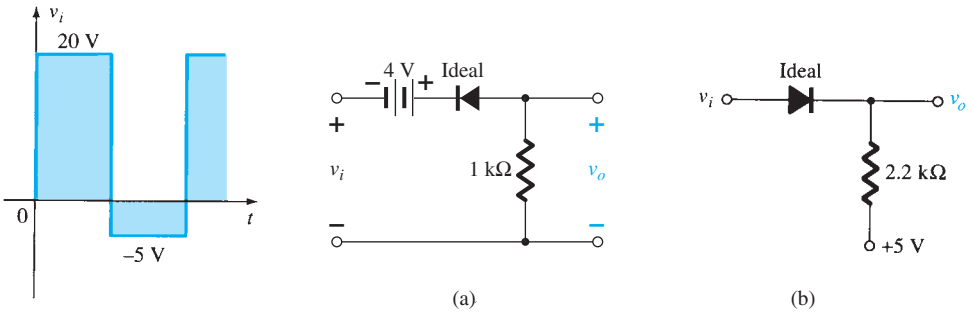


FIG. 2.178
Problem 34.

*35. Determine v_o for each network of Fig. 2.179 for the input shown.

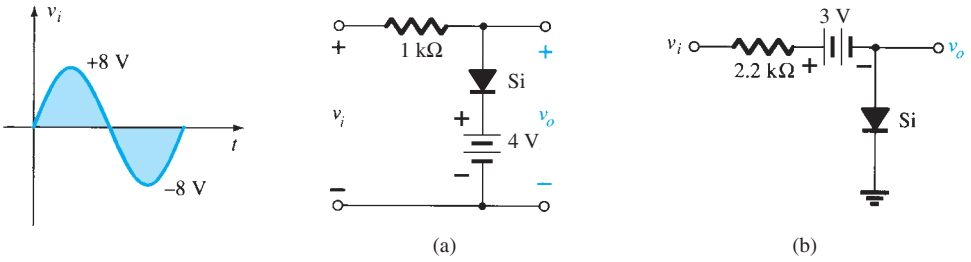


FIG. 2.179
Problem 35.

36. Sketch i_R and v_o for the network of Fig. 2.180 for the input shown.

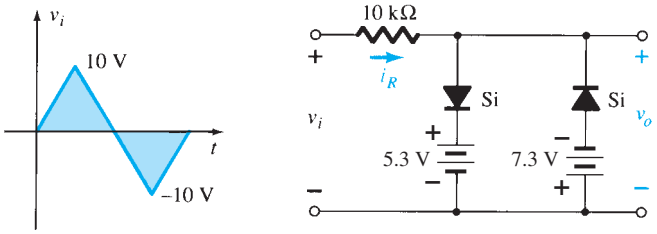


FIG. 2.180
Problem 36.

2.9 Clampers

37. Sketch v_o for each network of Fig. 2.181 for the input shown.

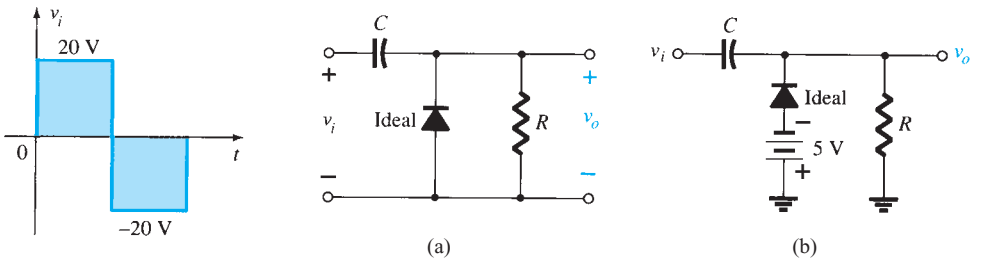


FIG. 2.181
Problem 37.

38. Sketch v_o for each network of Fig. 2.182 for the input shown.

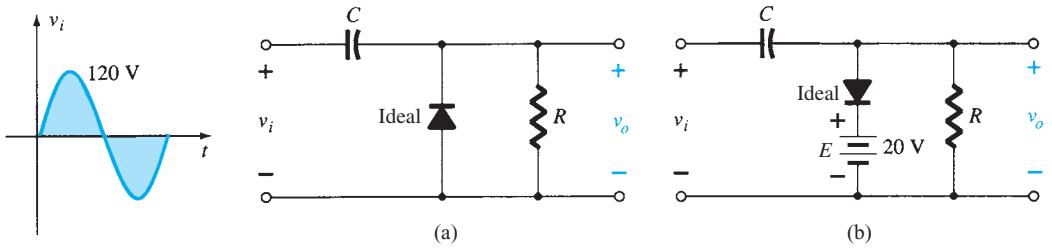


FIG. 2.182
Problem 38.

***39.** For the network of Fig. 2.183:

a. Calculate 5τ.

b. Compare 5τ to half the period of the applied signal.

c. Sketch v_o.

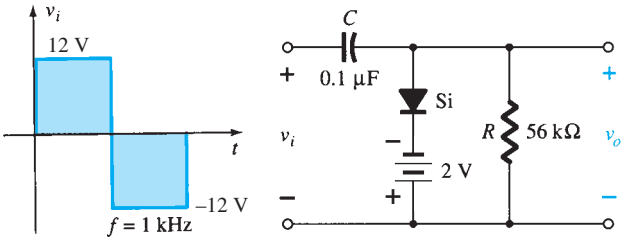


FIG. 2.183
Problem 39.

***40.** Design a clamper to perform the function indicated in Fig. 2.184.

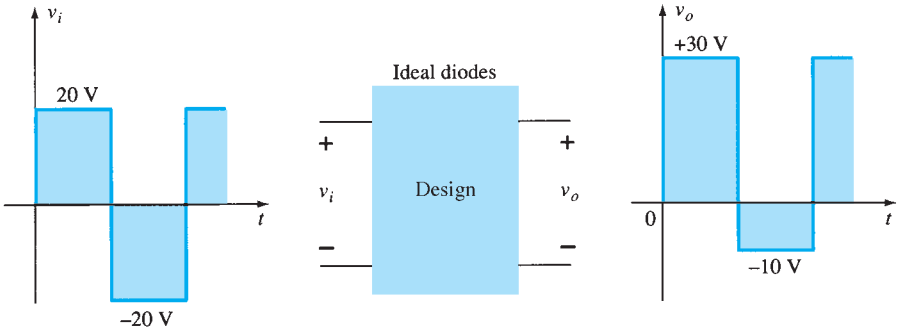


FIG. 2.184
Problem 40.

***41.** Design a clamper to perform the function indicated in Fig. 2.185.

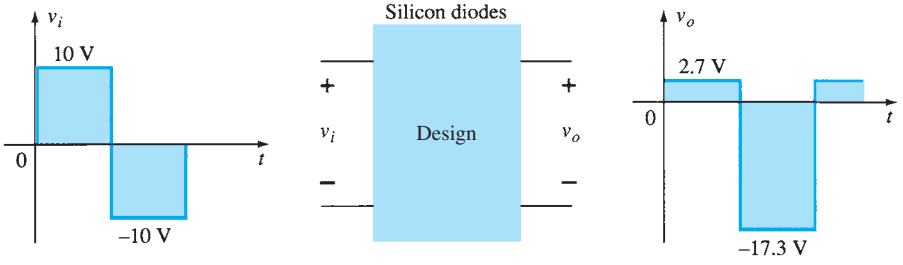


FIG. 2.185
Problem 41.

2.10 Zener Diodes

*42. **a.** Determine V_L, I_L, I_Z, and I_R for the network of Fig. 2.186 if $R_L = 180\ \Omega$.
b. Repeat part (a) if $R_L = 470\ \Omega$.
c. Determine the value of R_L that will establish maximum power conditions for the Zener diode.
d. Determine the minimum value of R_L to ensure that the Zener diode is in the "on" state.

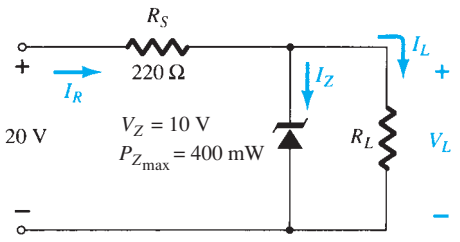


FIG. 2.186
Problem 42.

*43. **a.** Design the network of Fig. 2.187 to maintain V_L at 12 V for a load variation (I_L) from 0 mA to 200 mA. That is, determine R_S and V_Z.
b. Determine $P_{Z\,max}$ for the Zener diode of part (a).

*44. For the network of Fig. 2.188, determine the range of V_i that will maintain V_L at 8 V and not exceed the maximum power rating of the Zener diode.

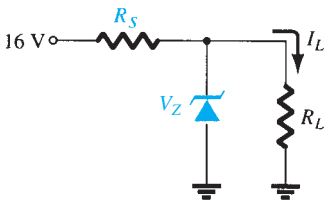


FIG. 2.187
Problem 43.

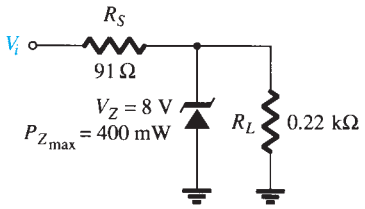


FIG. 2.188
Problems 44 and 52.

45. Design a voltage regulator that will maintain an output voltage of 20 V across a 1-kΩ load with an input that will vary between 30 V and 50 V. That is, determine the proper value of R_S and the maximum current I_{ZM}.

46. Sketch the output of the network of Fig. 2.145 if the input is a 50-V square wave. Repeat for a 5-V square wave.

2.11 Voltage-Multiplier Circuits

47. Determine the voltage available from the voltage doubler of Fig. 2.123 if the secondary voltage of the transformer is 120 V (rms).

48. Determine the required PIV ratings of the diodes of Fig. 2.123 in terms of the peak secondary voltage V_m.

2.14 Computer Analysis

49. Perform an analysis of the network of Fig. 2.156b using PSpice Windows.

50. Perform an analysis of the network of Fig. 2.161b using PSpice Windows.

51. Perform an analysis of the network of Fig. 2.162 using PSpice Windows.

52. Perform a general analysis of the Zener network of Fig. 2.188 using PSpice Windows.

53. Repeat Problem 49 using Multisim.

54. Repeat Problem 50 using Multisim.

55. Repeat Problem 51 using Multisim.

56. Repeat Problem 52 using Multisim.