APPENDIX

A PROBABLE VALUES OF GENERAL PHYSICAL CONSTANTS†

Constant	Symbol	Value
Electronic charge	q	1.602×10^{-19} C
Electronic mass	m	9.109×10^{-31} kg
Ratio of charge to mass of an electron	q/m	1.759×10^{11} C/kg
Mass of atom of unit atomic weight (hypothetical)	.....	1.660×10^{-27} kg
Mass of proton	m_p	1.673×10^{-27} kg
Ratio of proton to electron mass	m_p/m	1.837×10^{3}
Planck's constant	h	6.626×10^{-34} J-s
Boltzmann constant	$\bar{k}$	1.381×10^{-23} J/°K
	k	8.620×10^{-5} eV/°K
Stefan-Boltzmann constant	σ	5.670×10^{-8} W/(m^2)(°K^4)
Avogadro's number	N_A	6.023×10^{23} molecules/mole
Gas constant	R	8.314 J/(deg)(mole)
Velocity of light	c	2.998×10^{8} m/s
Faraday's constant	F	9.649×10^{3} C/mole
Volume per mole	V_o	2.241×10^{-2} m^3
Acceleration of gravity	g	9.807 m/s^2
Permeability of free space	μ_o	1.257×10^{-6} H/m
Permittivity of free space	ϵ_o	8.849×10^{-12} F/m

† E. A. Mechtly, "The International System of Units: Physical Constants and Conversion Factors," National Aeronautics and Space Administration, NASA SP-7012, Washington, D.C., 1964.

APPENDIX

B

CONVERSION FACTORS AND PREFIXES

1 ampere (A)	= 1 C/s
1 angstrom unit (Å)	= 10^{-10} m
	= 10^{-4} μm
1 atmosphere pressure	= 760 mm Hg
1 coulomb (C)	= 1 A-s
1 electron volt (eV)	= 1.60×10^{-19} J
1 farad (F)	= 1 C/V
1 foot (ft)	= 0.305 m
1 gram-calorie	= 4.185 J
giga (G)	= $\times 10^{9}$
1 henry (H)	= 1 V-s/A
1 hertz (Hz)	= 1 cycle/s
1 inch (in.)	= 2.54 cm
1 joule (J)	= 10^{7} ergs
	= 1 W-s
	= 6.25×10^{18} eV
	= 1 N-m
	= 1 C-V
kilo (k)	= $\times 10^{3}$
1 kilogram (kg)	= 2.205 lb
1 kilometer (km)	= 0.622 mile
1 lumen	= 0.0016 W (at 0.55 μm)
1 lumen per square foot	= 1 ft-candle (fc)
mega (M)	= $\times 10^{6}$
1 meter (m)	= 39.37 in.
micro (μ)	= $\times 10^{-6}$
1 micron	= 10^{-6} m
	= 1 μm
1 mil	= 10^{-3} in.
	= 25 μm
1 mile	= 5,280 ft
	= 1.609 km
milli (m)	= $\times 10^{-3}$
nano (n)	= $\times 10^{-9}$
1 newton (N)	= 1 kg-m/s^2
pico (p)	= $\times 10^{-12}$
1 pound (lb)	= 453.6 g
1 tesla (T)	= 1 Wb/m^2
1 ton	= 2,000 lb
1 volt (V)	= 1 W/A
1 watt (W)	= 1 J/s
1 weber (Wb)	= 1 V-s
1 weber per square meter (Wb/m^2)	= 10^{4} gauss

APPENDIX

C PROBLEMS

CHAPTER 1

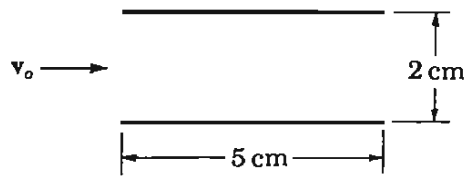
1-1 (*a*) The distance between the plates of a plane-parallel capacitor is 1 cm. An electron starts at rest at the negative plate. If a direct voltage of 1,000 V is applied, how long will it take the electron to reach the positive plate?
(*b*) What is the magnitude of the force which is exerted on the electron at the beginning and at the end of its path?
(*c*) What is its final velocity?
(*d*) If a 60-Hz sinusoidal voltage of peak value 1,000 V is applied, how long will the time of transit be? Assume that the electron is released with zero velocity at the instant of time when the applied voltage is passing through zero. HINT: Expand the sine function into a power series. Thus $\sin \theta = \theta - \theta^3/3! + \theta^5/5! - \cdots$.

1-2 The plates of a parallel-plate capacitor are d m apart. At $t = 0$ an electron is released at the bottom plate with a velocity v_o (meters per second) normal to the plates. The potential of the top plate with respect to the bottom is $-V_m \sin \omega t$.
(*a*) Find the position of the electron at any time t.
(*b*) Find the value of the electric field intensity at the instant when the velocity of the electron is zero.

1-3 An electron is released with zero initial velocity from the lower of a pair of horizontal plates which are 3 cm apart. The accelerating potential between these plates increases from zero linearly with time at the rate of 10 V/μs. When the electron is 2.8 cm from the bottom plate, a reverse voltage of 50 V replaces the linearly rising voltage.
(*a*) What is the instantaneous potential between the plates at the time of the potential reversal?
(*b*) With which electrode does the electron collide?
(*c*) What is the time of flight?
(*d*) What is the impact velocity of the electron?

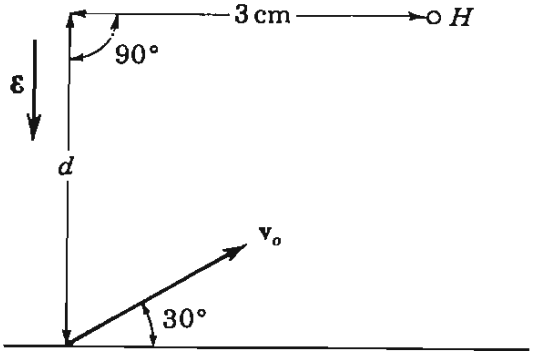
1-4 A 100-eV hydrogen ion is released in the center of the plates, as shown in the figure. The voltage between the plates varies linearly from 0 to 50 V in 10^{-7} s and then drops immediately to zero and remains at zero. The separation between the plates is 2 cm. If the ion enters the region between the plates at

time $t = 0$, how far will it be displaced from the X axis upon emergence from between the plates?



Prob. 1-4

1-5 Electrons are projected into the region of constant electric field intensity of magnitude 5×10^3 V/m that exists vertically. The electron-emitting device makes an angle of 30° with the horizontal. It ejects the electrons with an energy of 100 eV.



Prob. 1-5

(*a*) How long does it take an electron leaving the emitting device to pass through a hole *H* at a horizontal distance of 3 cm from the position of the emitting device? Refer to the figure. Assume that the field is downward.
(*b*) What must be the distance *d* in order that the particles emerge through the hole?
(*c*) Repeat parts *a* and *b* for the case where the field is upward.

1-6 (*a*) An electron is emitted from an electrode with a negligible initial velocity and is accelerated by a potential of 1,000 V. Calculate the final velocity of the particle.
(*b*) Repeat the problem for the case of a deuterium ion (heavy hydrogen ion—atomic weight 2.01) that has been introduced into the electric field with an initial velocity of 10^5 m/s.

1-7 An electron having an initial kinetic energy of 10^{-16} J at the surface of one of two parallel-plane electrodes and moving normal to the surface is slowed down by the retarding field caused by a 400-V potential applied between the electrodes.
(*a*) Will the electron reach the second electrode?
(*b*) What retarding potential would be required for the electron to reach the second electrode with zero velocity?

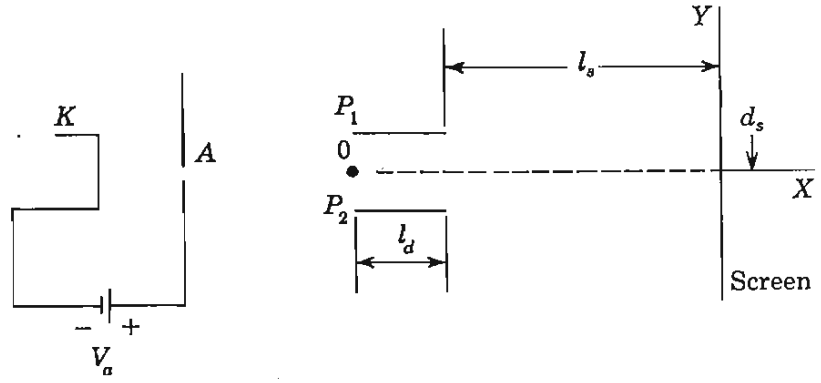
1-8 In a certain plane-parallel diode the potential V is given as a function of the distance x between electrodes by the equation

$$V = kx^{\frac{4}{3}}$$

where k is a constant.

(*a*) Find an expression for the time it will take an electron that leaves the electrode with the lower potential with zero initial velocity to reach the electrode with the higher potential, a distance d away.
(*b*) Find an expression for the velocity of this electron.

1-9 The essential features of the displaying tube of an oscilloscope are shown in the accompanying figure. The voltage difference between K and A is V_a and between P_1 and P_2 is V_p. Neither electric field affects the other one. The electrons are emitted from the electrode K with initial zero velocity, and they pass through a hole in the middle of electrode A. Because of the field between P_1 and P_2 they change direction while they pass through these plates and, after that, move with constant velocity toward the screen S. The distance between plates is d.



Prob. 1-9

(*a*) Find the velocity v_x of the electrons as a function of V_a as they cross A.
(*b*) Find the Y-component of velocity v_y of the electrons as they come out of the field of plates P_1 and P_2 as a function of V_p, l_d, d, and v_x.
(*c*) Find the distance from the middle of the screen (d_s), when the electrons reach the screen, as a function of tube distances and applied voltages.
(*d*) For $V_a = 1.0$ kV, and $V_p = 10$ V, $l_d = 1.27$ cm, $d = 0.475$ cm, and $l_s = 19.4$ cm, find the numerical values of v_x, v_y, and d_s.
(*e*) If we want to have a deflection of $d_s = 10$ cm of the electron beam, what must be the value of V_a?

1-10 A diode consists of a plane emitter and a plane-parallel anode separated by a distance of 0.5 cm. The anode is maintained at a potential of 10 V negative with respect to the cathode.
(*a*) If an electron leaves the emitter with a speed of 10^6 m/s, and is directed toward the anode, at what distance from the cathode will it intersect the potential-energy barrier?
(*b*) With what speed must the electron leave the emitter in order to be able to reach the anode?

1-11 A particle when displaced from its equilibrium position is subject to a linear restoring force $f = -kx$, where x is the displacement measured from the equilibrium position. Show by the energy method that the particle will execute periodic vibrations with a maximum displacement which is proportional to the square root of the total energy of the particle.

1-12 A particle of mass m is projected vertically upward in the earth's gravitational field with a speed v_o.
(*a*) Show by the energy method that this particle will reverse its direction at the height of $v_o^2/2g$, where g is the acceleration of gravity.
(*b*) Show that the point of reversal corresponds to a "collision" with the potential-energy barrier.

1-13 (*a*) Prove Eq. (1-13).
(*b*) For the hydrogen atom show that the possible radii in meters are given by

$$r = \frac{h^2 \epsilon_o n^2}{\pi m q^2}$$

where n is any integer but not zero. For the ground state ($n = 1$) show that the radius is 0.53 Å.

1-14 Show that the time for one revolution of the electron in the hydrogen atom in a circular path about the nucleus is

$$T = \frac{m^{\frac{1}{2}} q^2}{4\sqrt{2}\,\epsilon_o (-W)^{\frac{3}{2}}}$$

where the symbols are as defined in Sec. 1-4.

1-15 For the hydrogen atom show that the reciprocal of the wavelength (called the *wave number*) of the spectral lines is given, in waves per meter, by

$$\frac{1}{\lambda} = R\left(\frac{1}{{n_2}^2} - \frac{1}{{n_1}^2}\right)$$

where n_1 and n_2 are integers, with n_1 greater than n_2, and $R = mq^4/8\epsilon_o^2 h^3 c = 1.10 \times 10^7\ \text{m}^{-1}$ is called the *Rydberg constant.*

If $n_2 = 1$, this formula gives a series of lines in the ultraviolet, called the *Lyman series.* If $n_2 = 2$, the formula gives a series of lines in the visible, called the *Balmer series.* Similarly, the series for $n_2 = 3$ is called the *Paschen series.* These predicted lines are observed in the hydrogen spectrum.

1-16 Show that Eq. (1-14) is equivalent to Eq. (1-11).

1-17 (*a*) A photon of wavelength 1,026 Å is absorbed by hydrogen, and two other photons are emitted. If one of these is the 1,216 Å line, what is the wavelength of the second photon?
(*b*) If the result of bombardment of the hydrogen was the presence of the fluorescent lines 18,751 and 1,026 Å, what wavelength must have been present in the bombarding radiation?

1-18 The seven lowest energy levels of sodium vapor are 0, 2.10, 3.19, 3.60, 3.75, 4.10, and 4.26 eV. A photon of wavelength 3,300 Å is absorbed by an atom of the vapor.
(*a*) What are all the possible fluorescent lines that may appear?
(*b*) If three photons are emitted and one of these is the 11,380-Å line, what are the wavelengths of the other two photons?
(*c*) Between what energy states do the transitions take place in order to produce these lines?

1-19 (*a*) With what speed must an electron be traveling in a sodium-vapor lamp in order to excite the yellow line whose wavelength is 5,893 Å?
(*b*) What should be the frequency of a photon in order to excite the same yellow line?
(*c*) What would happen if the frequency of the photon was 530 or 490 THz (T = Tera = 10^{12})?
(*d*) What should be the minimum frequency of the photon in order to ionize an unexcited atom of sodium vapor?
(*e*) What should be the minimum speed of an electron in order to ionize an unexcited atom of sodium vapor? Ionization of sodium vapor: 5.12 eV.

1-20 An x-ray tube is essentially a high-voltage diode. The electrons from the hot filament are accelerated by the plate supply voltage so that they fall upon the anode with considerable energy. They are thus able to effect transitions among the tightly bound electrons of the atoms in the solid of which the target (the anode) is constructed.
(*a*) What is the minimum voltage that must be applied across the tube in order to produce x-rays having a wavelength of 0.5 Å?
(*b*) What is the minimum wavelength in the spectrum of an x-ray tube across which is maintained 60 kV?

1-21 Argon resonance radiation corresponding to an energy of 11.6 eV falls upon sodium vapor. If a photon ionizes an unexcited sodium atom, with what speed is the electron ejected? The ionization potential of sodium is 5.12 eV.

1-22 A radio transmitter radiates 1,000 W at a frequency of 10 MHz.
(*a*) What is the energy of each radiated quantum in electron volts?
(*b*) How many quanta are emitted per second?
(*c*) How many quanta are emitted in each period of oscillation of the electromagnetic field?
(*d*) If each quantum acts as a particle, what is its momentum?

1-23 What is the wavelength of (*a*) a mass of 1 kg moving with a speed of 1 m, s, (*b*) an electron which has been accelerated from rest through a potential difference of 10 V?

1-24 Classical physics is valid as long as the physical dimensions of the system are much larger than the De Broglie wavelength. Determine whether the particle is classical in each of the following cases:
(*a*) An electron accelerated through a potential of 300 V in a device whose dimensions are of the order of 1 cm.
(*b*) An electron in the electron beam of a cathode-ray tube (anode-cathode voltage = 25 kV).
(*c*) The electron in a hydrogen atom.

1-25 A photon of wavelength 1,216 Å excites a hydrogen atom which is at rest. Calculate
(*a*) The photon momentum imparted to the atom.
(*b*) The energy corresponding to this momentum and imparted to the hydrogen atom.
(*c*) The ratio of the energy found in part *b* to the energy of the photon. HINT: Use conservation of momentum.

CHAPTER 2

2-1 Prove that the concentration n of free electrons per cubic meter of a metal is given by

$$n = \frac{dv}{AM} = \frac{A_o dv \times 10^3}{A}$$

where d = density, kg/m^3
v = valence, free electrons per atom
A = atomic weight
M = weight of atom of unit atomic weight, kg (Appendix A)
A_o = Avogadro's number, molecules/mole

2-2 The specific density of tungsten is 18.8 g/cm^3, and its atomic weight is 184.0. Assume that there are two free electrons per atom. Calculate the concentration of free electrons.

2-3 (*a*) Compute the conductivity of copper for which $\mu = 34.8$ cm^2/V-s and $d = 8.9$ g/cm^3. Use the result of Prob. 2-1.
(*b*) If an electric field is applied across such a copper bar with an intensity of 10 V/cm, find the average velocity of the free electrons.

2-4 Compute the mobility of the free electrons in aluminum for which the density is 2.70 g/cm^3 and the resistivity is 3.44×10^{-6} Ω-cm. Assume that aluminum has three valence electrons per atom. Use the result of Prob. 2-1.

2-5 The resistance of No. 18 copper wire (diameter = 1.03 mm) is 6.51 Ω per 1,000 ft. The concentration of free electrons in copper is 8.4×10^{28} electrons/m^3. If the current is 2 A, find the (*a*) drift velocity, (*b*) mobility, (*c*) conductivity.

2-6 (*a*) Determine the concentration of free electrons and holes in a sample of germanium at 300°K which has a concentration of donor atoms equal to 2×10^{14} atoms/cm^3 and a concentration of acceptor atoms equal to 3×10^{14} atoms/cm^3. Is this p- or n-type germanium? In other words, is the conductivity due primarily to holes or to electrons?
(*b*) Repeat part *a* for equal donor and acceptor concentrations of 10^{15} atoms/cm^3. Is this p- or n-type germanium?
(*c*) Repeat part *a* for donor concentration of 10^{16} atoms/cm^3 and acceptor concentration 10^{14} atoms/cm^3.

2-7 (*a*) Find the concentration of holes and of electrons in p-type germanium at 300°K if the conductivity is 100 $(\Omega\text{-cm})^{-1}$.
(*b*) Repeat part *a* for n-type silicon if the conductivity is 0.1 $(\Omega\text{-cm})^{-1}$.

2-8 (*a*) Show that the resistivity of intrinsic germanium at 300°K is 45 Ω-cm.
(*b*) If a donor-type impurity is added to the extent of 1 atom per 10^8 germanium atoms, prove that the resistivity drops to 3.7 Ω-cm.

2-9 (*a*) Find the resistivity of intrinsic silicon at 300°K.
(*b*) If a donor-type impurity is added to the extent of 1 atom per 10^8 silicon atoms, find the resistivity.

2-10 Consider intrinsic germanium at room temperature (300°K). By what percent does the conductivity increase per degree rise in temperature?

2-11 Repeat Prob. 2-10 for intrinsic silicon.

2-12 Repeat Prob. 2-6*a* for a temperature of 400°K, and show that the sample is essentially intrinsic.

2-13 A sample of germanium is doped to the extent of 10^{14} donor atoms/cm^3 and 7×10^{13} acceptor atoms/cm^3. At the temperature of the sample the resistivity of pure (intrinsic) germanium is 60 Ω-cm. If the applied electric field is 2 V/cm, find the total conduction current density.

2-14 (*a*) Find the magnitude of the Hall voltage V_H in an *n*-type germanium bar used in Fig. 2-10, having majority-carrier concentration $N_D = 10^{17}$/cm^3. Assume $B_z = 0.1$ Wb/m^2, $d = 3$ mm, and $\mathcal{E}_x = 5$ V/cm.
(*b*) What happens to V_H if an identical *p*-type germanium bar having $N_A = 10^{17}$/cm^3 is used in part *a*?

2-15 The Hall effect is used to determine the mobility of holes in a *p*-type silicon bar used in Fig. 2-10. Assume the bar resistivity is 200,000 Ω-cm, the magnetic field $B_z = 0.1$ Wb/m^2, and $d = w = 3$ mm. The measured values of the current and Hall voltage are 10 μA and 50 mV, respectively. Find μ_p.

2-16 A certain photosurface has a spectral sensitivity of 6 mA/W of incident radiation of wavelength 2,537 Å. How many electrons will be emitted photoelectrically by a pulse of radiation consisting of 10,000 photons of this wavelength?

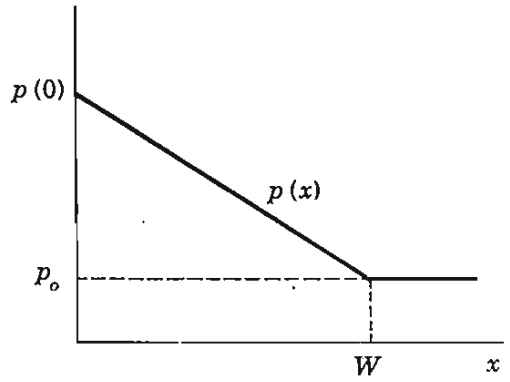
2-17 (*a*) Consider the situation depicted in Fig. 2-13 with the light turned on. Show that the equation of conservation of charge is

$$\frac{dp}{dt} + \frac{p}{\tau} = \frac{\bar{p}}{\tau}$$

where the time axis in Fig. 2-13 is shifted to t'.
(*b*) Verify that the concentration is given by the equation

$$p = \bar{p} + (p_o - \bar{p})e^{-t/\tau}$$

2-18 The hole concentration in a semiconductor specimen is shown.
(*a*) Find an expression for and sketch the hole current density $J_p(x)$ for the case in which there is no externally applied electric field.



Prob. 2-18

(*b*) Find an expression for and sketch the built-in electric field that must exist if there is to be no net hole current associated with the distribution shown.
(*c*) Find the value of the potential between the points $x = 0$ and $x = W$ if $p(0)/p_o = 10^3$.

2-19 Given a 20 Ω-cm n-type germanium bar with material lifetime of 100 μs, cross section of 1 mm², and length of 1 cm. One side of the bar is illuminated with 10^{15} photons/s. Assume that each incident photon generates one electron-hole pair and that these are distributed uniformly throughout the bar. Find the bar resistance under continuous light excitation at room temperature.

2-20 (*a*) Consider an open-circuited graded semiconductor as in Fig. 2-17*a*. Verify the Boltzmann equation for electrons [Eq. (2-61)].
(*b*) For the step-graded semiconductor of Fig. 2-17*b* verify the expression for the contact potential V_o given in Eq. (2-63), starting with $J_n = 0$.

2-21 (*a*) Consider the step-graded germanium semiconductor of Fig. 2-17*b* with $N_D = 10^3 N_A$ and with N_A corresponding to 1 acceptor atom per 10^8 germanium atoms. Calculate the contact difference of potential V_o at room temperature.
(*b*) Repeat part *a* for a silicon p-n junction.

CHAPTER 3

3-1 (*a*) The resistivities of the two sides of a step-graded germanium diode are 2 Ω-cm (p side) and 1 Ω-cm (n side). Calculate the height E_o of the potential-energy barrier.
(*b*) Repeat part *a* for a silicon p-n junction.

3-2 (*a*) Sketch logarithmic and linear plots of carrier concentration vs. distance for an abrupt silicon junction if $N_D = 10^{15}$ atoms/cm³ and $N_A = 10^{16}$ atoms/cm³. Give numerical values for ordinates. Label the n, p, and depletion regions.
(*b*) Sketch the space-charge electric field and potential as a function of distance for this case (Fig. 3-1).

3-3 Repeat Prob. 3-2 for an abrupt germanium junction.

3-4 (*a*) Consider a p-n diode operating under low-level injection so that $p_n \ll n_n$. Assuming that the minority current is due entirely to diffusion, verify that the electric field in the n side is given by

$$\mathcal{E}(x) = \frac{I + (D_n/D_p - 1)I_{pn}(x)}{qn\mu_n A}$$

(*b*) Using this value of $\mathcal{E}$, find the next approximation to the drift hole current and show that it may indeed be neglected compared with the diffusion hole current.
(*c*) Sketch the following currents as a function of distance in the n side: (i) total diode current; (ii) minority-carrier current; (iii) majority diffusion current; (iv) majority drift current; (v) total majority-carrier current.

3-5 Starting with Eq. (3-5) for I_{pn} and the corresponding expression for I_{np}, prove that the ratio of hole to electron current crossing a p-n junction is given by

$$\frac{I_{pn}(0)}{I_{np}(0)} = \frac{\sigma_p L_n}{\sigma_n L_p}$$

where $\sigma_p(\sigma_n)$ = conductivity of $p(n)$ side. Note that this ratio depends upon the ratio of the conductivities. For example, if the p side is much more heavily

doped than the n side, the hole current will be much larger than the electron current crossing the junction.

3-6 (*a*) Prove that the reverse saturation current in a p-n diode is given by

$$I_o = Aq\left(\frac{D_p}{L_pN_D} + \frac{D_n}{L_nN_A}\right)n_i^2$$

(*b*) Starting with the expression for I_o found in part *a*, verify that the reverse saturation current is given by

$$I_o = AV_T\frac{b\sigma_i^2}{(1+b)^2}\left(\frac{1}{L_p\sigma_n} + \frac{1}{L_n\sigma_p}\right)$$

where $\sigma_n(\sigma_p)$ = conductivity of $n(p)$ side
σ_i = conductivity of intrinsic material
$b = \mu_n/\mu_p$

3-7 (*a*) Using the result of Prob. 3-6, find the reverse saturation current for a germanium p-n junction diode at room temperature, 300°K. The cross-sectional area is 4.0 mm², and

$$\sigma_p = 1.0\ (\Omega\text{-cm})^{-1} \qquad \sigma_n = 0.1\ (\Omega\text{-cm})^{-1} \qquad L_n = L_p = 0.15\ \text{cm}$$

Other physical constants are given in Table 2-1.
(*b*) Repeat part *a* for a silicon p-n junction diode. Assume $L_n = L_p = 0.01$ cm and $\sigma_n = \sigma_p = 0.01\ (\Omega\text{-cm})^{-1}$.

3-8 Find the ratio of the reverse saturation current in germanium to that in silicon, using the result of Prob. 3-6. Assume $L_n = L_p = 0.1$ cm and $\sigma_n = \sigma_p = 1.0\ (\Omega\text{-cm})^{-1}$ for germanium, whereas the corresponding values are 0.01 cm and $0.01\ (\Omega\text{-cm})^{-1}$ for silicon. See also Table 2-1.

3-9 (*a*) For what voltage will the reverse current in a p-n junction germanium diode reach 90 percent of its saturation value at room temperature?
(*b*) What is the ratio of the current for a forward bias of 0.05 V to the current for the same magnitude of reverse bias?
(*c*) If the reverse saturation current is 10 μA, calculate the forward currents for voltages of 0.1, 0.2, and 0.3 V, respectively.

3-10 (*a*) Evaluate η in Eq. (3-9) from the slope of the plot in Fig. 3-8 for $T = 25$°C. Draw the best-fit line over the current range 0.01 to 10 mA.
(*b*) Repeat for $T = -55$ and 150°C.

3-11 (*a*) Calculate the anticipated factor by which the reverse saturation current of a germanium diode is multiplied when the temperature is increased from 25 to 80°C.
(*b*) Repeat part *a* for a silicon diode over the range 25 to 150°C.

3-12 It is predicted that, for germanium, the reverse saturation current should increase by $0.11°C^{-1}$. It is found experimentally in a particular diode that at a reverse voltage of 10 V, the reverse current is 5 μA and the temperature dependence is only $0.07°C^{-1}$. What is the leakage resistance shunting the diode?

3-13 A diode is mounted on a chassis in such a manner that, for each degree of temperature rise above ambient, 0.1 mW is thermally transferred from the diode

to its surroundings. (The "thermal resistance" of the mechanical contact between the diode and its surroundings is 0.1 mW/°C.) The ambient temperature is 25°C. The diode temperature is not to be allowed to increase by more than 10°C above ambient. If the reverse saturation current is 5.0 μA at 25°C and increases at the rate $0.07°C^{-1}$, what is the maximum reverse-bias voltage which may be maintained across the diode?

3-14 A silicon diode operates at a forward voltage of 0.4 V. Calculate the factor by which the current will be multiplied when the temperature is increased from 25 to 150°C. Compare the result with the plot of Fig. 3-8.

3-15 An ideal germanium p-n junction diode has at a temperature of 125°C a reverse saturation current of 30 μA. At a temperature of 125°C find the dynamic resistance for a 0.2 V bias in (*a*) the forward direction, (*b*) the reverse direction.

3-16 Prove that for an alloy p-n junction (with $N_A \ll N_D$), the width W of the depletion layer is given by

$$W = \left(\frac{2\epsilon\mu_p V_j}{\sigma_p}\right)^{\frac{1}{2}}$$

where V_j is the junction potential under the condition of an applied diode voltage V_d.

3-17 (*a*) Prove that for an alloy silicon p-n junction (with $N_A \ll N_D$), the depletion-layer capacitance in picofarads per square centimeter is given by

$$C_T = 2.9 \times 10^{-4}\left(\frac{N_A}{V_j}\right)^{\frac{1}{2}}$$

(*b*) If the resistivity of the p material is 3.5 Ω-cm, the barrier height V_o is 0.35 V, the applied reverse voltage is 5 V, and the cross-sectional area is circular of 40 mils diameter, find C_T.

3-18 (*a*) For the junction of Fig. 3-10, find the expression for the $\mathcal{E}$ and V as a function of x in the n-type side for the case where N_A and N_D are of comparable magnitude. HINT: Shift the origin of x so that $x = 0$ at the junction.
(*b*) Show that the total barrier voltage is given by Eq. (3-21) multiplied by $N_A/(N_A + N_D)$ and with $W = W_p + W_n$.
(*c*) Prove that $C_T = [qN_AN_D\epsilon/2(N_A + N_D)]^{\frac{1}{2}}V^{-\frac{1}{2}}$.
(*d*) Prove that $C_T = \epsilon A/(W_p + W_n)$.

3-19 Reverse-biased diodes are frequently employed as electrically controllable variable capacitors. The transition capacitance of an abrupt junction diode is 20 pF at 5 V. Compute the decrease in capacitance for a 1.0-V increase in bias.

3-20 Calculate the barrier capacitance of a germanium p-n junction whose area is 1 mm by 1 mm and whose space-charge thickness is 2×10^{-4} cm. The dielectric constant of germanium (relative to free space) is 16.

3-21 The zero-voltage barrier height at an alloy-germanium p-n junction is 0.2 V. The concentration N_A of acceptor atoms in the p side is much smaller than the concentration of donor atoms in the n material, and $N_A = 3 \times 10^{20}$ atoms/m^3. Calculate the width of the depletion layer for an applied reverse voltage of (*a*) 10 V and (*b*) 0.1 V and (*c*) for a forward bias of 0.1 V. (*d*) If the cross-

sectional area of the diode is 1 mm², evaluate the space-charge capacitance corresponding to the values of applied voltage in (*a*) and (*b*).

3-22 (*a*) Consider a grown junction for which the uncovered charge density ρ varies linearly with distance. If $\rho = ax$, prove that the barrier voltage V_j is given by

$$V_j = \frac{aW^3}{12\epsilon}$$

(*b*) Verify that the barrier capacitance C_T is given by Eq. (3-23)

3-23 Given a forward-biased silicon diode with $I = 1$ mA. If the diffusion capacitance is $C_D = 1\ \mu$F, what is the diffusion length L_p? Assume that the doping of the p side is much greater than that of the n side.

3-24 The derivation of Eq. (3-28) for the diffusion capacitance assumes that the p side is much more heavily doped than the n side, so that the current at the junction is entirely due to holes. Derive an expression for the total diffusion capacitance when this approximation is not made.

3-25 (*a*) Prove that the maximum electric field $\mathcal{E}_m$ at a step-graded junction with $N_A \gg N_D$ is given by

$$\mathcal{E}_m = \frac{2V_j}{W}$$

(*b*) It is found that Zener breakdown occurs when $\mathcal{E}_m = 2 \times 10^7$ V/$m \equiv \mathcal{E}_z$. Prove that Zener voltage V_z is given by

$$V_z = \frac{\epsilon \mathcal{E}_z^2}{2qN_D}$$

Note that the Zener breakdown voltage can be controlled by controlling the concentration of donor ions.

3-26 (*a*) Zener breakdown occurs in germanium at a field intensity of 2×10^7 V/m. Prove that the breakdown voltage is $V_Z = 51/\sigma_p$, where σ_p is the conductivity of the p material in $(\Omega\text{-cm})^{-1}$. Assume that $N_A \ll N_D$.

(*b*) If the p material is essentially intrinsic, calculate V_Z.

(*c*) For a doping of 1 part in 10^8 of p-type material, the resistivity drops to 3.7 Ω-cm. Calculate V_Z.

(*d*) For what resistivity of the p-type material will $V_Z = 1$ V?

3-27 (*a*) Two p-n germanium diodes are connected in series opposing. A 5-V battery is impressed upon this series arrangement. Find the voltage across each junction at room temperature. Assume that the magnitude of the Zener voltage is greater than 5 V.

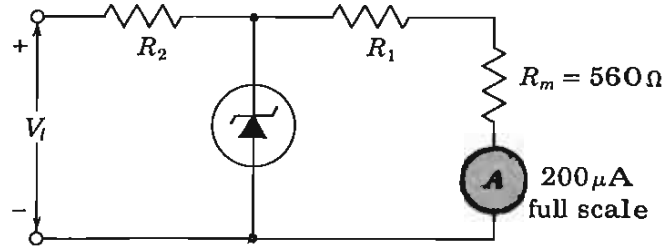
Note that the result is independent of the reverse saturation current. Is it also independent of temperature?

HINT: Assume that reverse saturation current flows in the circuit, and then justify this assumption.

(*b*) If the magnitude of the Zener voltage is 4.9 V, what will be the current in the circuit? The reverse saturation current is 5 μA.

3-28 The Zener diode can be used to prevent overloading of sensitive meter movements without affecting meter linearity. The circuit shown represents a dc

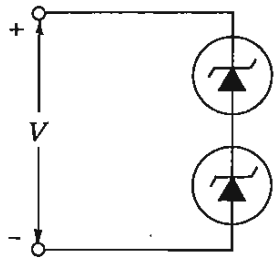
voltmeter which reads 20 V full scale. The meter resistance is 560 Ω, and $R_1 + R_2 = 99.5$ K. If the diode is a 16-V Zener, find R_1 and R_2 so that, when $V_i > 20$ V, the Zener diode conducts and the overload current is shunted away from the meter.



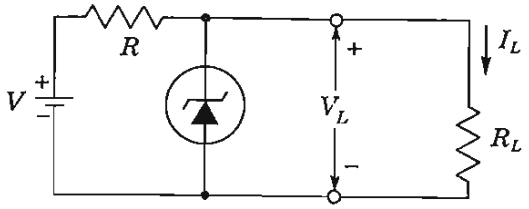
Prob. 3-28

3-29 A series combination of a 15-V avalanche diode and a forward-biased silicon diode is to be used to construct a zero-temperature-coefficient voltage reference. The temperature coefficient of the silicon diode is −1.7 mV/°C. Express in percent per degree centigrade the required temperature coefficient of the Zener diode.

3-30 The saturation currents of the two diodes are 1 and 2 μA. The breakdown voltages of the diodes are the same and are equal to 100 V.
(*a*) Calculate the current and voltage for each diode if $V = 90$ V and $V = 110$ V.
(*b*) Repeat part *a* if each diode is shunted by a 10-MΩ resistor.



Prob. 3-30



Prob. 3-31

3-31 (*a*) The avalanche diode regulates at 50 V over a range of diode currents from 5 to 40 mA. The supply voltage $V = 200$ V. Calculate R to allow voltage regulation from a load current $I_L = 0$ up to I_{max}, the maximum possible value of I_L. What is I_{max}?
(*b*) If R is set as in part *a* and the load current is set at $I_L = 25$ mA, what are the limits between which V may vary without loss of regulation in the circuit?

3-32 (*a*) Consider a tunnel diode with $N_D = N_A$ and with the impurity concentration corresponding to 1 atom per 10^3 germanium atoms. At room temperature calculate (i) the height of the potential-energy barrier under open-circuit conditions (the contact potential energy), (ii) the width of the space-charge region.
(*b*) Repeat part *a* if the semiconductor is silicon instead of germanium.

3-33 The photocurrent I in a *p-n* junction photodiode as a function of the distance x of the light spot from the junction is given in Fig. 3-22. Prove that the slopes

of ln I versus x are $-1/L_p$ and $-1/L_n$, respectively, on the n and p sides. Note that L_p represents the diffusion length for holes in the n material.

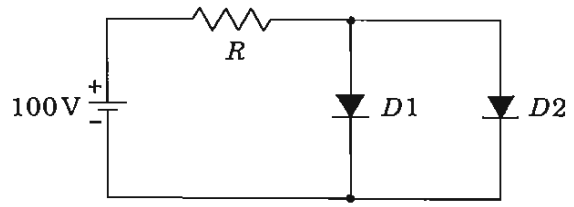
3-34 (a) For the type LS 223 photovoltaic cell whose characteristics are given in Fig. 3-23, plot the power output vs. the load resistance R_L.
(b) What is the optimum value of R_L?

CHAPTER 4

4-1 (a) In the circuit of Prob. 3-27, the Zener breakdown voltage is 2.0 V. The reverse saturation current is 5 μA. If the silicon diode resistance could be neglected, what would be the current?
(b) If the ohmic resistance is 100 Ω, what is the current?
NOTE: Answer part b by plotting Eq. (3-9) and drawing a load line. Verify your answer analytically by a method of successive approximations.

4-2 A p-n germanium junction diode at room temperature has a reverse saturation current of 10 μA, negligible ohmic resistance, and a Zener breakdown voltage of 100 V. A 1-K resistor is in series with this diode, and a 30-V battery is impressed across this combination. Find the current (a) if the diode is forward-biased, (b) if the battery is inserted into the circuit with the reverse polarity. (c) Repeat parts a and b if the Zener breakdown voltage is 10 V.

4-3 Each diode is described by a linearized volt-ampere characteristic, with incremental resistance r and offset voltage V_γ. Diode $D1$ is germanium with $V_\gamma =$ 0.2 V and $r = 20$ Ω, whereas $D2$ is silicon with $V_\gamma = 0.6$ V and $r = 15$ Ω. Find the diode currents if (a) $R = 10$ K, (b) $R = 1$ K.



Prob. 4-3

4-4 The photodiode whose characteristics are given in Fig. 3-21 is in series with a 30-V supply and a resistance R. If the illumination is 3,000 fc, find the current for (a) $R = 0$, (b) $R = 50$ K, (c) $R = 100$ K.

4-5 (a) For the application in Sec. 4-3, plot the voltage across the diode for one cycle of the input voltage v_i. Let $V_m = 2.4$ V, $V_\gamma = 0.6$ V, $R_f = 10$ Ω, and $R_L = 100$ Ω.
(b) By direct integration find the average value of the diode voltage and the load voltage. Note that these two answers are numerically equal and explain why.

4-6 Calculate the break region over which the dynamic resistance of a diode is multiplied by a factor of 1,000.

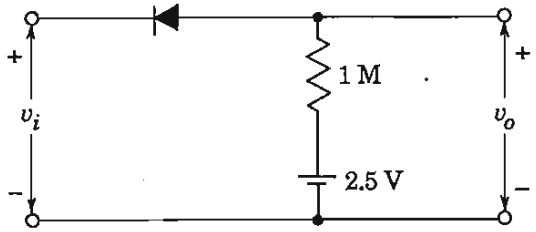
4-7 For the diode clipping circuit of Fig. 4-9a assume that $V_R = 10$ V, $v_i = 20 \sin \omega t$, and that the diode forward resistance is $R_f = 100$ Ω while $R_r = \infty$ and $V_\gamma = 0$. Neglect all capacitances. Draw to scale the input and output waveforms and

label the maximum and minimum values if (*a*) $R = 100\ \Omega$, (*b*) $R = 1$ K, and (*c*) $R = 10$ K.

4-8 Repeat Prob. 4-7 for the case where the reverse resistance is $R_r = 10$ K.

4-9 In the diode clipping circuit of Fig. 4-9*a* and *d*, $v_i = 20 \sin \omega t$, $R = 1$ K, and $V_R = 10$ V. The reference voltage is obtained from a tap on a 10-K divider connected to a 100-V source. Neglect all capacitances. The diode forward resistance is 50 Ω, $R_r = \infty$, and $V_\gamma = 0$. In both cases draw the input and output waveforms to scale. Which circuit is the better clipper? HINT: Apply Thévenin's theorem to the reference-voltage divider network.

4-10 A symmetrical 5-kHz square wave whose output varies between +10 and −10 V is impressed upon the clipping circuit shown. Assume $R_f = 0$, $R_r = 2$ M, and

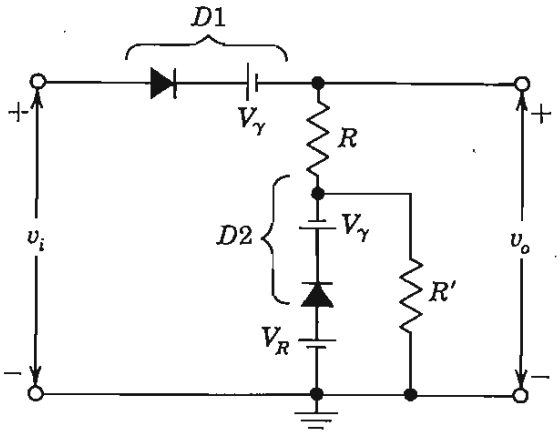


Prob. 4-10

$V_\gamma = 0$. Sketch the steady-state output waveform, indicating numerical values of the maximum, minimum, and constant portions.

4-11 For the clipping circuits shown in Fig. 4-9*b* and *d* derive the transfer characteristic v_o versus v_i, taking into account R_f and V_γ and considering $R_r = \infty$.

4-12 The clipping circuit shown employs temperature compensation. The dc voltage source V_γ represents the diode offset voltage; otherwise the diodes are assumed to be ideal with $R_f = 0$ and $R_r = \infty$.



Prob. 4-12

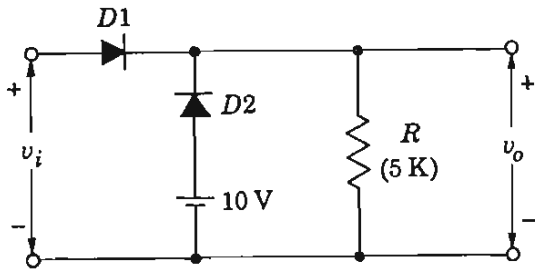
(*a*) Sketch the transfer curve v_o versus v_i.

(*b*) Show that the maximum value of the input voltage v_i so that the current in *D*2 is always in the forward direction is

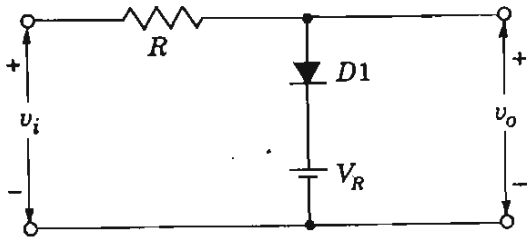
$$v_{i,\max} = V_R + \frac{R}{R'}(V_R - V_\gamma)$$

(*c*) What is the temperature dependence of the point on the input waveform at which clipping occurs?

4-13 (*a*) In the clipping circuit shown, *D*2 compensates for temperature variations. Assume that the diodes have infinite back resistance, a forward resistance of 50 Ω, and a break point at the origin ($V_\gamma = 0$). Calculate and plot the transfer characteristic v_o against v_i. Show that the circuit has an extended break point, that is, two break points close together.



Prob. 4-13



Prob. 4-14

(*b*) Find the transfer characteristic that would result if *D*2 were removed and the resistor *R* were moved to replace *D*2.

(*c*) Show that the double break of part *a* would vanish and only the single break of part *b* would appear if the diode forward resistances were made vanishingly small in comparison with *R*.

4-14 (*a*) In the peak clipping circuit shown, add another diode *D*2 and a resistor *R*′ in a manner that will compensate for drift with temperature.

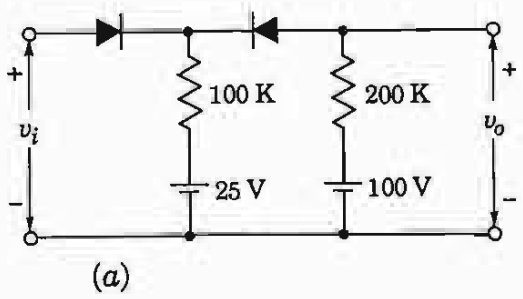
(*b*) Show that the break point of the transmission curve occurs at V_R. Assume $R_r \gg R \gg R_f$.

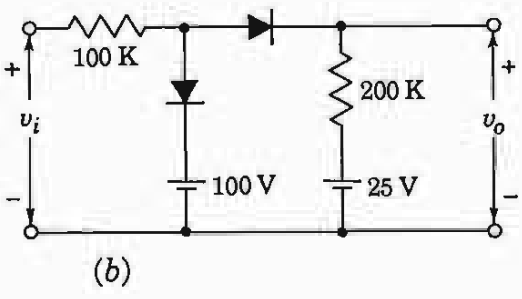
(*c*) Show that if *D*2 is always to remain in conduction it is necessary that

$$v_i < v_{i,\max} = V_R + \frac{R}{R'}(V_R - V_\gamma)$$

4-15 (*a*) The input voltage v_i to the two-level clipper shown in part *a* of the figure varies linearly from 0 to 150 V. Sketch the output voltage v_o to the same time scale as the input voltage. Assume ideal diodes.

(*b*) Repeat (*a*) for the circuit shown in part *b* of the figure.

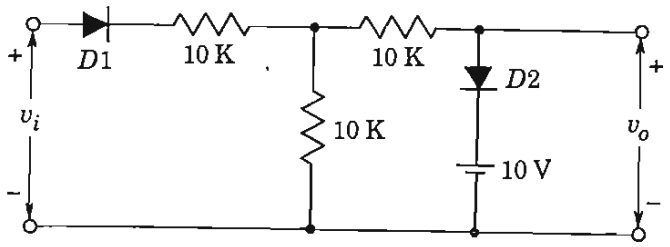




Prob. 4-15

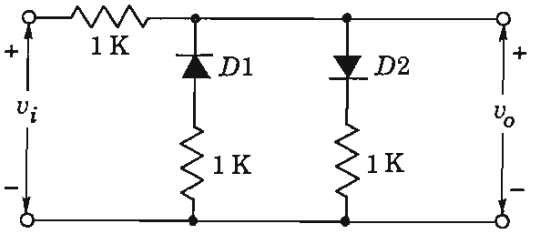
4-16 The circuit of Fig. 4-10*a* is used to "square" a 10-kHz input sine wave whose peak value is 50 V. It is desired that the output voltage waveform be flat for 90 percent of the time. Diodes are used having a forward resistance of 100 Ω and a backward resistance of 100 K.
(*a*) Find the values of V_{R1} and V_{R2}.
(*b*) What is a reasonable value to use for R?

4-17 (*a*) The diodes are ideal. Write the transfer characteristic equations (v_o as a function of v_i).
(*b*) Plot v_o against v_i, indicating all intercepts, slopes, and voltage levels.
(*c*) Sketch v_o if $v_i = 40 \sin \omega t$. Indicate all voltage levels.



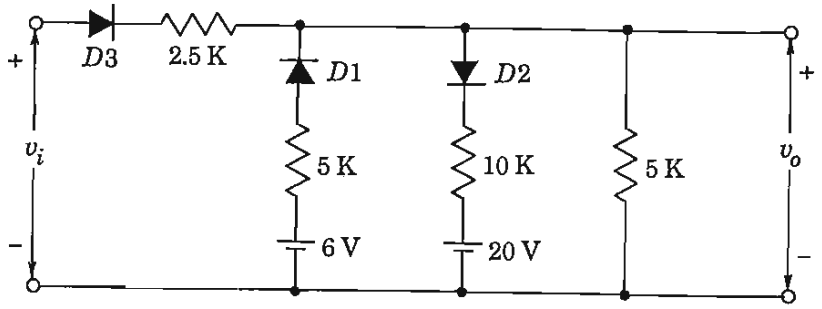
Prob. 4-17

4-18 (*a*) Repeat Prob. 4-17 for the circuit shown.
(*b*) Repeat for the case where the diodes have an offset voltage $V_\gamma = 1$ V.



Prob. 4-18

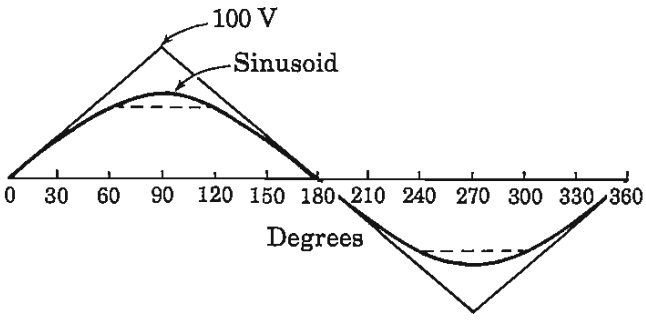
4-19 Assume that the diodes are ideal. Make a plot of v_o against v_i for the range of v_i from 0 to 50 V. Indicate all slopes and voltage levels. Indicate, for each region, which diodes are conducting.



Prob. 4-19

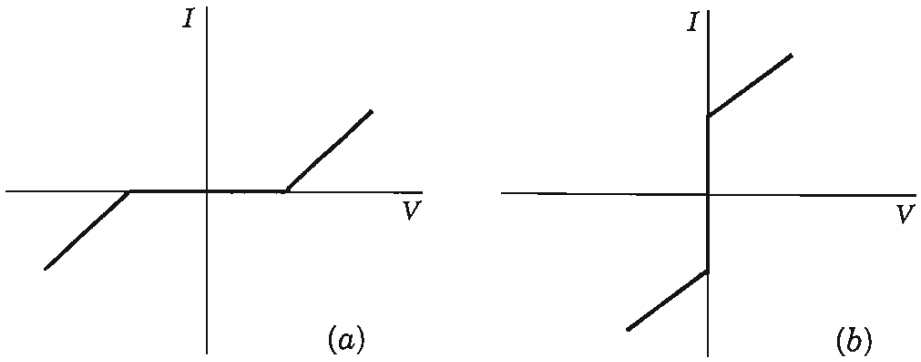
4-20 The triangular waveform shown is to be converted into a sine wave by using clipping diodes. Consider the dashed waveform sketched as a first approximation to the sinusoid. The dashed waveform is coincident with the sinusoid at 0°,

30°, 60°, etc: Devise a circuit whose output is this broken-line waveform when the input is the triangular waveform. Assume ideal diodes and calculate the values of all supply voltages and resistances used. The peak value of the sinusoid is 50 V.



Prob. 4-20

4-21 Construct circuits which exhibit terminal characteristics as shown in parts *a* and *b* of the figure.



Prob. 4-21

4-22 The diode-resistor comparator of Fig. 4-13 is connected to a device which responds when the comparator output attains a level of 0.1 V. The input is a ramp which rises at the rate 10 V/μs. The germanium diode has a reverse saturation current of 1 μA. Initially, $R = 1$ K and the 0.1-V output level is attained at a time $t = t_1$. If we now set $R = 100$ K, what will be the corresponding change in t_1? $V_R = 0$.

4-23 For the four-diode sampling gate of Fig. 4-14 consider that v_s is at its most negative value, say, $v_s = -V_s$. Then verify that the expressions for $V_{n,\min}$ and $V_{c,\min}$ given in Eqs. (4-7) and (4-8) remain valid.

4-24 A balancing voltage divider is inserted between $D3$ and $D4$ in Fig. 4-14 so as to give zero output voltage for zero input. If the divider is assumed to be set at its midpoint, if its total resistance is R, and if R and R_f are both much less than R_c or R_L, show that

$$V_{c,\min} = V_s\left(2 + \frac{R_c}{R_L}\right)\left(1 + \frac{R}{4R_f}\right)$$

4-25 (*a*) Explain qualitatively the operation of the sampling gate shown. The supply voltage V is constant. The control voltage v_c is the square wave of Fig. 4-14*b*. Assume ideal diodes with $V_\gamma = 0$, $R_f = 0$, and $R_r = \infty$. HINT: When $v_c = V_c$, the diodes $D1$ and $D2$ conduct (if $V > V_{\min}$) and $D3$ and $D4$ are OFF. If $v_c = -V_n$, then $D3$ and $D4$ conduct and $D1$ and $D2$ are OFF.

Verify the following relationships:

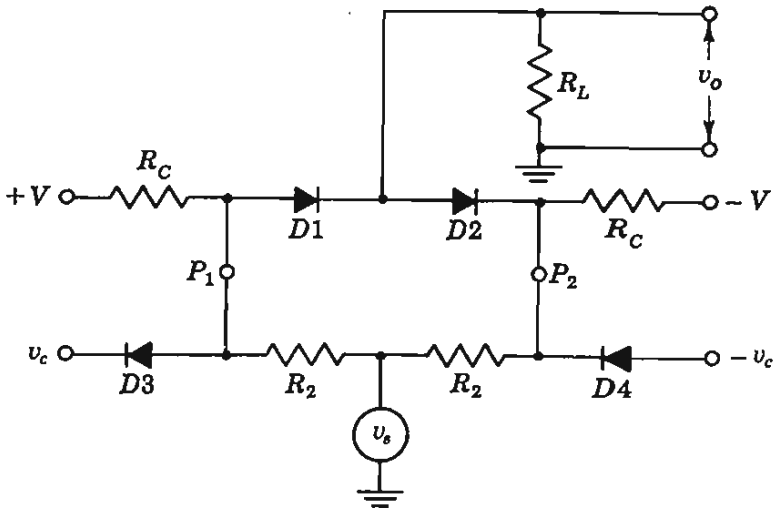
(*b*) $$V_{\min} = \frac{R_c}{R_2}\frac{R_1}{R_1 + 2R_L}V_s$$

where $R_1 = R_c \| R_2$.

(*c*) $$A = \frac{v_o}{v_s} = \frac{2R_L}{R_2}\frac{R_1}{R_1 + 2R_L}$$

(*d*) $$V_{n,\min} = V_s\frac{R_c}{R_c + R_2} - V\frac{R_2}{R_c + R_2}$$

(*e*) $$V_{c,\min} = AV_s$$



Prob. 4-25

4-26 A diode whose internal resistance is 20 Ω is to supply power to a 1,000-Ω load from a 110-V (rms) source of supply. Calculate (*a*) the peak load current, (*b*) the dc load current, (*c*) the ac load current, (*d*) the dc diode voltage, (*e*) the total input power to the circuit, (*f*) the percentage regulation from no load to the given load.

4-27 Show that the maximum dc output power $P_{dc} \equiv V_{dc}I_{dc}$ in a half-wave single-phase circuit occurs when the load resistance equals the diode resistance R_f.

4-28 The efficiency of rectification η_r is defined as the ratio of the dc output power $P_{dc} \equiv V_{dc}I_{dc}$ to the input power $P_i = (1/2\pi)\int_0^{2\pi} v_i i \, d\alpha$.

(*a*) Show that, for the half-wave-rectifier circuit,

$$\eta_r = \frac{40.6}{1 + R_f/R_L} \%$$

(*b*) Show that, for the full-wave rectifier, η_r has twice the value given in part *a*.

4-29 Prove that the regulation of both the half-wave and the full-wave rectifier is given by

$$\% \text{ regulation} = \frac{R_f}{R_L} = 100\%$$

4-30 (*a*) Prove Eqs. (4-21) and (4-22) for the dc voltage of a full-wave-rectifier circuit.
(*b*) Find the dc voltage across a diode by direct integration.

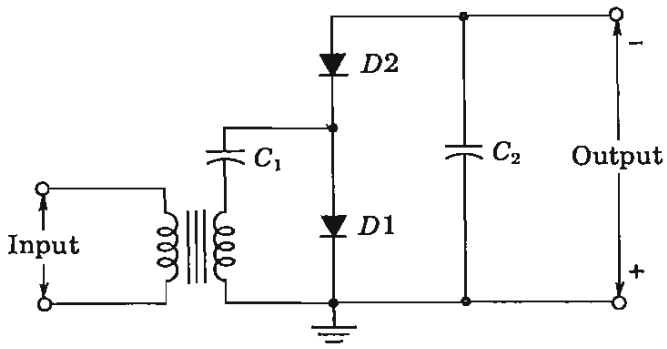
4-31 A full-wave single-phase rectifier consists of a double-diode vacuum tube, the internal resistance of each element of which may be considered to be constant and equal to 500 Ω. These feed into a pure resistance load of 2,000 Ω. The secondary transformer voltage to center tap is 280 V. Calculate (*a*) the dc load current, (*b*) the direct current in each tube, (*c*) the ac voltage across each diode, (*d*) the dc output power, (*e*) the percentage regulation.

4-32 In the full-wave single-phase bridge, can the transformer and the load be interchanged? Explain carefully.

4-33 A 1-mA dc meter whose resistance is 10 Ω is calibrated to read rms volts when used in a bridge circuit with semiconductor diodes. The effective resistance of each element may be considered to be zero in the forward direction and infinite in the inverse direction. The sinusoidal input voltage is applied in series with a 5-K resistance. What is the full-scale reading of this meter?

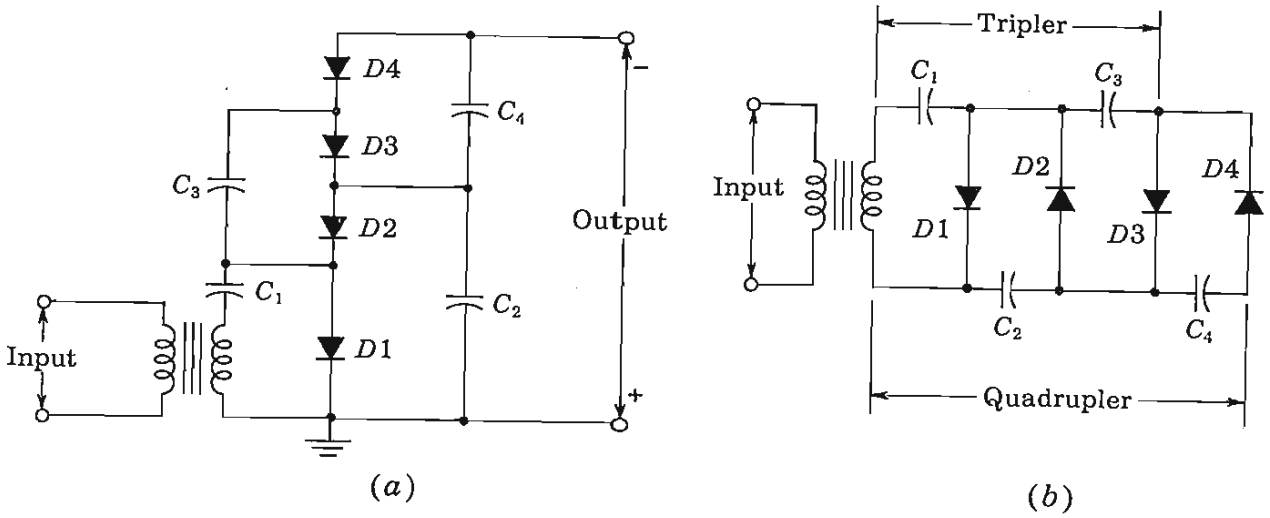
4-34 The circuit shown is a half-wave voltage doubler. Analyze the operation of this circuit. Calculate (*a*) the maximum possible voltage across each capacitor, (*b*) the peak inverse voltage of each diode. Compare this circuit with the bridge voltage doubler of Fig. 4-22. In this circuit the output voltage is negative with respect to ground. Show that if the connections to the cathode and anode of each diode are interchanged, the output voltage will be positive with respect to ground.

Prob. 4-34



4-35 The circuit of Prob. 4-34 can be extended from a doubler to a quadrupler by adding two diodes and two capacitors as shown. In the figure, parts *a* and *b* are alternative ways of drawing the same circuit.

(*a*) Analyze the operation of this circuit.
(*b*) Answer the same questions as asked in Prob. 4-34.
(*c*) Generalize the circuit of this and of Prob. 4-34 so as to obtain n-fold multiplication when n is any even number. In particular, sketch the circuit for sixfold multiplication.
(*d*) Show that n-fold multiplication, with n odd, can also be obtained provided that the output is properly chosen.



Prob. 4-35

4-36 A single-phase full-wave rectifier uses a semiconductor diode. The transformer voltage is 35 V rms to center tap. The load consists of a 40-μF capacitance in parallel with a 250-Ω resistor. The diode and the transformer resistances and leakage reactance may be neglected.
(*a*) Calculate the cutout angle.
(*b*) Plot to scale the output voltage and the diode current as in Fig. 4-25. Determine the cutin point graphically from this plot, and find the peak diode current corresponding to this point.
(*c*) Repeat parts *a* and *b*, using a 160-μF instead of a 40-μF capacitance.

CHAPTER 5

5-1 (*a*) Show that for an n-p-n silicon transistor of the alloy type in which the resistivity ρ_B of the base is much larger than that of the collector, the punch-through voltage V is given by $V = 6.1 \times 10^3 W_B^2/\rho_B$, where V is in volts, ρ_B in ohm-centimeters, and W in mils. For punch-through, $W = W_B$ in Fig. 5-8*a*.
(*b*) Calculate the punch-through voltage if $W = 1$ μm and $\rho_B = 0.5$ Ω-cm.

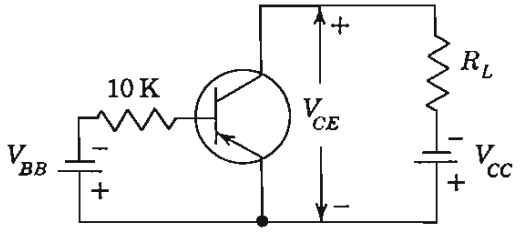
5-2 The transistor of Fig. 5-3*a* has the characteristics given in Figs. 5-6 and 5-7. Let $V_{CC} = 6$ V, $R_L = 200$ Ω, and $I_E = 15$ mA.
(*a*) Find I_C and V_{CB}.

(*b*) Find V_{EB} and V_L.
(*c*) If I_E changes by $\Delta I_E = 10$ mA symmetrically around the point of part *a* and with constant V_{CB}, find the corresponding change in I_C.

5-3 The CB transistor used in the circuit of Fig. 5-3*a* has the characteristics given in Figs. 5-6 and 5-7. Let $I_C = -20$ mA, $V_{CB} = -4$ V, and $R_L = 200\ \Omega$.
(*a*) Find V_{CC} and I_E.
(*b*) If the supply voltage V_{CC} decreases from its value in part *a* by 2 V while I_E retains its previous value, find the new values of I_C and V_{CB}.

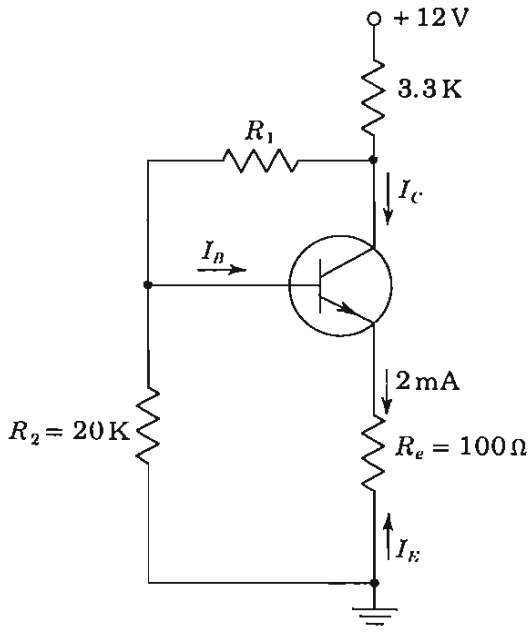
5-4 The CE transistor used in the circuit shown has the characteristics given in Figs. 5-10 and 5-11.
(*a*) Find V_{BB} if $V_{CC} = 10$ V, $V_{CE} = -1$ V, and $R_L = 250\ \Omega$.
(*b*) If $V_{CC} = 10$ V, find R_L so that $I_C = -20$ mA and $V_{CE} = -4$ V. Find V_{BB}.

Prob. 5-4



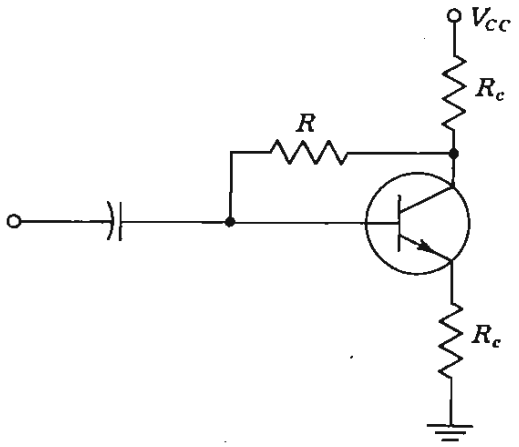
5-5 If $\alpha = 0.98$ and $V_{BE} = 0.7$ V, find R_1 in the circuit shown for an emitter current $I_E = -2$ mA. Neglect the reverse saturation current.

Prob. 5-5



5-6 (*a*) Find R_c and R_b in the circuit of Fig. 5-12*a* if $V_{CC} = 10$ V and $V_{BB} = 5$ V, so that $I_C = 10$ mA and $V_{CE} = 5$ V. A silicon transistor with $\beta = 100$, $V_{BE} = 0.7$ V, and negligible reverse saturation current is under consideration.
(*b*) Repeat part *a* if a 100-Ω emitter resistor is added to the circuit.

5-7 In the circuit shown, $V_{CC} = 24$ V, $R_c = 10$ K, and $R_e = 270$ Ω. If a silicon transistor is used with $\beta = 45$ and if $V_{CE} = 5$ V, find R. Neglect the reverse saturation current.

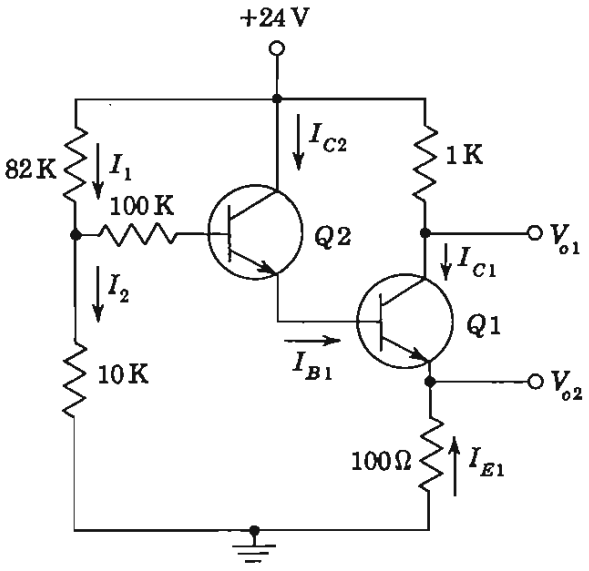


Prob. 5-7

5-8 For the circuit shown, transistors $Q1$ and $Q2$ operate in the active region with $V_{BE1} = V_{BE2} = 0.7$ V, $\beta_1 = 100$, and $\beta_2 = 50$. The reverse saturation currents may be neglected.

(*a*) Find the currents I_{B2}, I_1, I_2, I_{C2}, I_{B1}, I_{C1}, and I_{E1}.

(*b*) Find the voltages V_{o1} and V_{o2}.



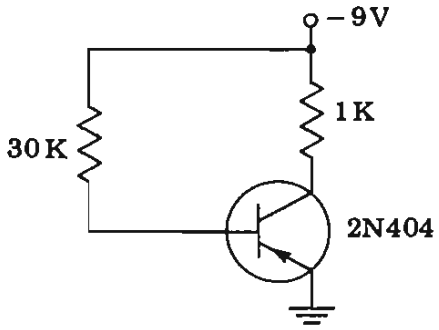
Prob. 5-8

5-9 (*a*) The reverse saturation current of the germanium transistor in Fig. 5-13 is 2 μA at room temperature (25°C) and increases by a factor of 2 for each temperature increase of 10°C. The bias $V_{BB} = 5$ V. Find the maximum allowable value for R_B if the transistor is to remain cut off at a temperature of 75°C.

(*b*) If $V_{BB} = 1.0$ V and $R_B = 50$ K, how high may the temperature increase before the transistor comes out of cutoff?

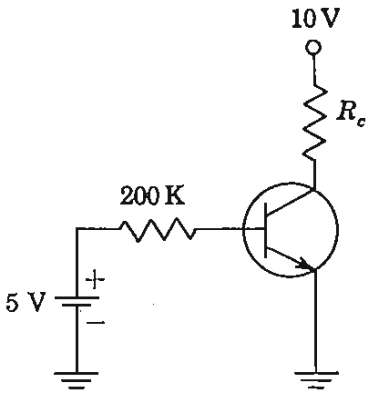
5-10 From the characteristic curves for the type 2N404 transistor given in Fig. 5-14, find the voltages V_{BE}, V_{CE}, and V_{BC} for the circuit shown.

Prob. 5-10



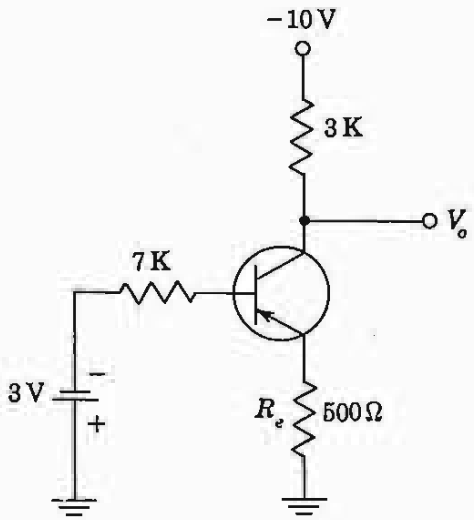
5-11 A silicon transistor with $V_{BE,sat} = 0.8$ V, $\beta = h_{FE} = 100$, $V_{CE,sat} = 0.2$ V is used in the circuit shown. Find the minimum value of R_c for which the transistor remains in saturation.

Prob. 5-11

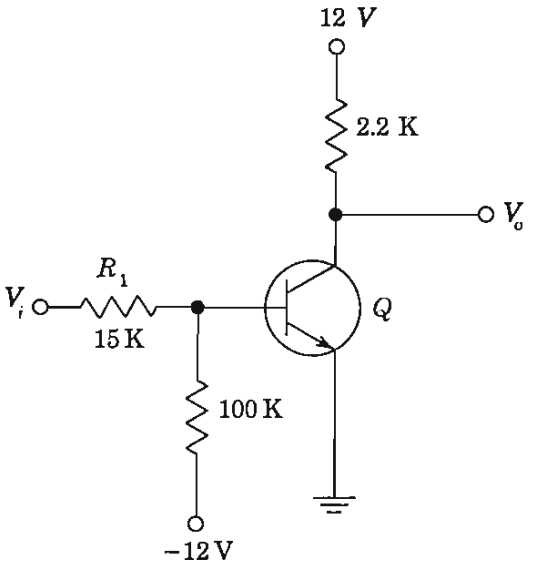


5-12 For the circuit shown, assume $\beta = h_{FE} = 100$.
(*a*) Find if the silicon transistor is in cutoff, saturation, or in the active region.
(*b*) Find V_o.
(*c*) Find the minimum value for the emitter resistor R_e for which the transistor operates in the active region.

Prob. 5-12

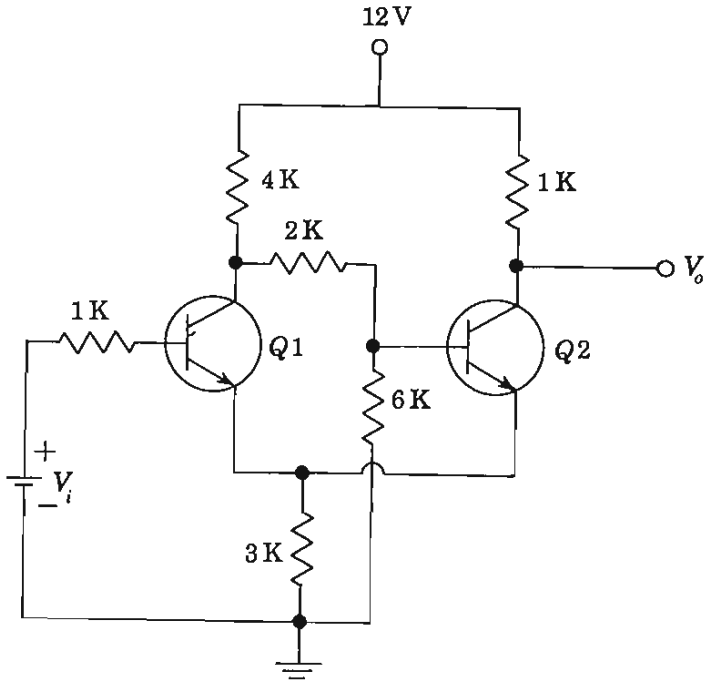


5-13 If the silicon transistor used in the circuit shown has a minimum value of $\beta = h_{FE}$ of 30 and if $I_{CBO} = 10$ nA at 25°C:
(*a*) Find V_o for $V_i = 12$ V and show that Q is in saturation.
(*b*) Find the minimum value of R_1 for which the transistor in part *a* is in the active region.
(*c*) If $R_1 = 15$ K and $V_i = 1$ V, find V_o and show that Q is at cutoff.
(*d*) Find the maximum temperature at which the transistor in part *c* remains at cutoff.



Prob. 5-13

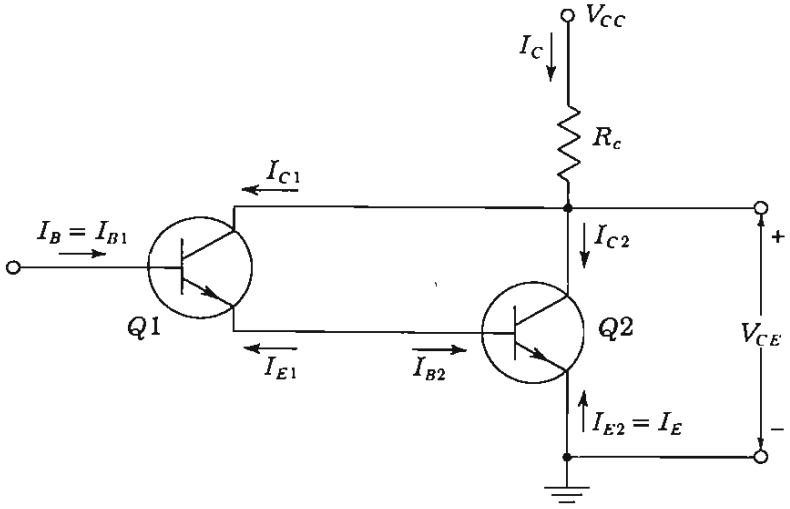
5-14 Silicon transistors with $h_{FE} = 100$ are used in the circuit shown. Neglect the reverse saturation current.
(*a*) Find V_o when $V_i = 0$ V. Assume $Q1$ is OFF and justify the assumption.
(*b*) Find V_o when $V_i = 6$ V. Assume $Q2$ is OFF and justify this assumption.



Prob. 5-14

5-15 For the circuit shown, $\alpha_1 = 0.98$, $\alpha_2 = 0.96$, $V_{CC} = 24$ V, $R_c = 120\ \Omega$, and $I_E = -100$ mA. Neglecting the reverse saturation currents, determine (*a*) the currents I_{C1}, I_{B1}, I_{E1}, I_{C2}, I_{B2}, and I_C; (*b*) V_{CE}; (*c*) I_C/I_B, I_C/I_E.

Prob. 5-15



5-16 Derive from Eqs. (5-24) and (5-25) the explicit expressions for I_C and I_E in terms of V_C and V_E.

5-17 (*a*) Derive Eqs. (5-29) and (5-30).
(*b*) Derive Eq. (5-31).

5-18 Draw the Ebers-Moll model for an *n-p-n* transistor.

5-19 (*a*) Show that the exact expression for the CE output characteristics of a *p-n-p* transistor is

$$V_{CE} = V_T \ln \frac{\alpha_I}{\alpha_N} + V_T \ln \frac{I_{CO} + \alpha_N I_B - I_C(1 - \alpha_N)}{I_{EO} + I_B + I_C(1 - \alpha_I)}$$

(*b*) Show that this reduces to Eq. (5-31) if $I_B \gg I_{EO}$ and $I_B \gg I_{CO}/\alpha_N$.

5-20 (*a*) A transistor is operating in the cutoff region with both the emitter and collector junctions reverse-biased by at least a few tenths of a volt. Prove that the currents are given by

$$I_E = \frac{I_{EO}(1 - \alpha_N)}{1 - \alpha_N \alpha_I}$$

$$I_C = \frac{I_{CO}(1 - \alpha_I)}{1 - \alpha_N \alpha_I}$$

(*b*) Prove that the emitter-junction voltage required just to produce cutoff ($I_E = 0$ and the collector back-biased) is

$$V_E = V_T \ln (1 - \alpha_N)$$

5-21 (*a*) Find the collector current for a transistor when both emitter and collector junctions are reverse-biased. Assume $I_{CO} = 5\ \mu$A, $I_{EO} = 3.57\ \mu$A, and $\alpha_N = 0.98$.
(*b*) Find the emitter current I_E under the same conditions as in part *a*.

5-22 Show that the emitter volt-ampere characteristic of a transistor in the active region is given by

$$I_E \approx I_S \epsilon^{V_E/V_T}$$

where $I_S = -I_{EO}/(1 - \alpha_N\alpha_I)$. Note that this characteristic is that of a p-n junction diode.

5-23 (*a*) Given an n-p-n transistor for which (at room temperature) $\alpha_N = 0.98$, $I_{CO} = 2\ \mu A$, and $I_{EO} = 1.6\ \mu A$. A common-emitter connection is used, and $V_{CC} = 12$ V and $R_L = 4.0$ K. What is the minimum base current required in order that the transistor enter its saturation region?
(*b*) Under the conditions in part *a*, find the voltages across each junction between each pair of terminals if the base-spreading resistance $r_{bb'}$ is neglected.
(*c*) Repeat part *b* if the base current is 200 μA.
(*d*) How are the above results modified if $r_{bb'} = 250\ \Omega$?

5-24 Plot the emitter current vs. emitter-to-base voltage for a transistor for which $\alpha_N = 0.98$, $I_{CO} = 2\ \mu A$, and $I_{EO} = 1.6\ \mu A$ if (*a*) $V_C = 0$, (*b*) V_C is back-biased by more than a few tenths of a volt. Neglect the base-spreading resistance.

5-25 Plot carefully to scale the common-emitter characteristic I_C/I_B versus V_{CE} for a transistor with $\alpha_N = 0.90 = \alpha_I$.

5-26 Show that

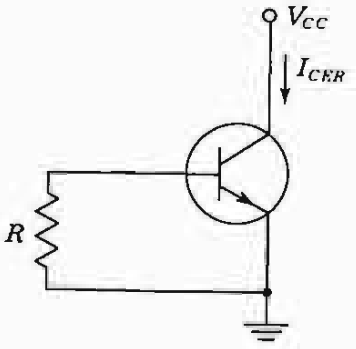
$$I_{CES} = \frac{I_{CO}}{1 - \alpha_N\alpha_I} \qquad I_{CEO} = \frac{I_{CO}}{1 - \alpha_N}$$

5-27 A common method of calculating α_N and α_I is by measurement of I_{CO}, I_{CEO}, and I_{CES}. Show that

$$(a)\ \alpha_N = \frac{I_{CEO} - I_{CO}}{I_{CEO}} \qquad (b)\ \alpha_I = \frac{1 - I_{CO}/I_{CES}}{1 - I_{CO}/I_{CEO}}$$

5-28 The collector leakage current is measured as shown in the figure, with the emitter grounded and a resistor R connected between base and ground. If this current is designated as I_{CER}, show that

$$I_{CER} = \frac{I_{CO}(1 + I_{EO}R/V_T)}{1 - \alpha_N\alpha_I + (I_{EO}R/V_T)(1 - \alpha_N)}$$



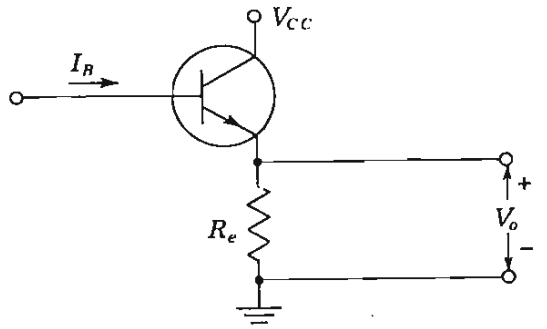
Prob. 5-28

5-29 For the circuit shown, verify that $V_o = V_{CC}$ when

$$I_B = \frac{V_{CC}}{R_e}\left(1 + \frac{\alpha_N}{\alpha_I}\frac{1 - \alpha_I}{1 - \alpha_N}\right) = \frac{V_{CC}}{R_e}\left(1 + \frac{\beta_N}{\beta_I}\right)$$

Under these conditions the base current exceeds the emitter current.

Prob. 5-29

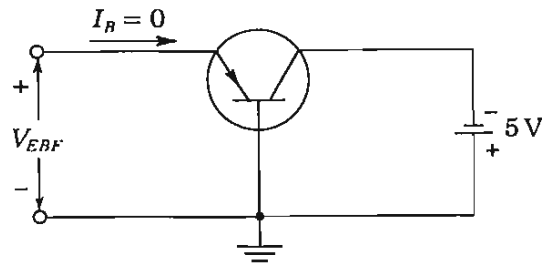


5-30 For the circuit shown, prove that the floating emitter-to-base voltage is given by

$$V_{EBF} = V_T \ln (1 - \alpha_N)$$

Neglect $r_{bb'}$.

Prob. 5-30

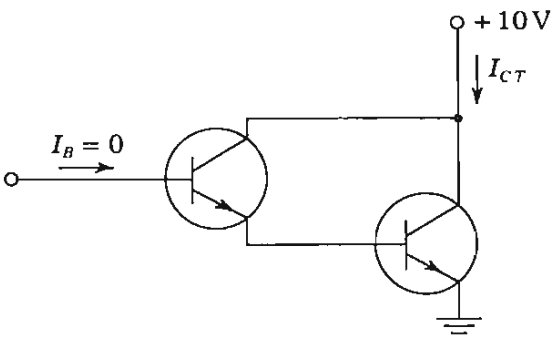


5-31 For the "floating-base" connection shown, prove that

$$I_{CT} = \frac{2 - \alpha_N}{(1 - \alpha_N)^2} I_{CO}$$

Assume that the transistors are identical.

Prob. 5-31



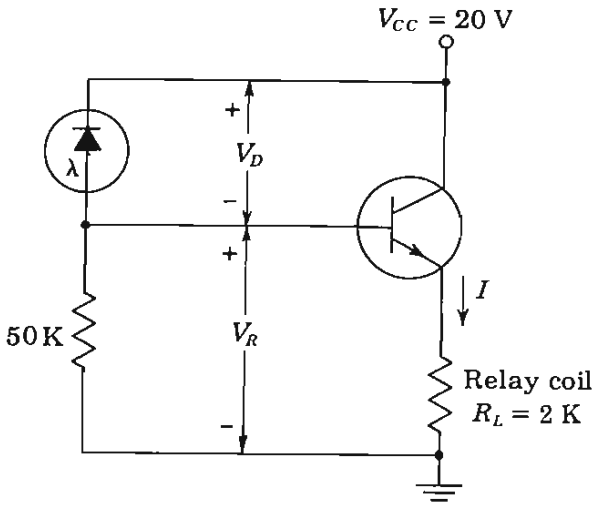
5-32 (*a*) Show that if the collector junction is reverse-biased with $|V_{CB}| \gg V_T$, the voltage V_{BE} is related to the base current by

$$V_{BE} = I_B\left(r_{bb'} + \frac{R_E}{1 - \alpha_N}\right) + \left\{\frac{I_{CO}R_E}{1 - \alpha_N} + V_T \ln\left[1 + \frac{I_B(1 - \alpha_N\alpha_I)}{I_{EO}(1 - \alpha_N)} + \frac{\alpha_N(1 - \alpha_I)}{\alpha_I(1 - \alpha_N)}\right]\right\}$$

where $r_{bb'}$ is the base-spreading resistance, and R_E is the emitter-body resistance. (*b*) Show that $V_{BE} = I_B(r_{bb'} + R_E) + V_T(1 + I_B/I_E)$ if the collector is open-circuited.

5-33 A transistor is operated at a forward emitter current of 2 mA and with the collector open-circuited. Find (*a*) the junction voltages V_C and V_E, (*b*) the collector-to-emitter voltage V_{CE}. Assume $I_{CO} = 2\ \mu A$, $I_{EO} = 1.6\ \mu A$, $\alpha_N = 0.98$. Is the transistor operating in saturation, at cutoff, or in the active region?

5-34 Photodiode 1N77 (Fig. 3-21) is used in the circuit shown. R_L represents the coil resistance of a relay for which the current required to close the relay is 6 mA. The transistor used is silicon with $V_{BE} = 0.7$ V and $h_{FE} = 100$.



Prob. 5-34

(*a*) Find the voltage V_D at which switching of the relay occurs.
(*b*) Find the minimum illumination required to close the relay.
(*c*) If the relay coil is placed directly in series with the phototransistor of Fig. 5-25 across 20 V, find the illumination intensity required to close the relay.

CHAPTER 6

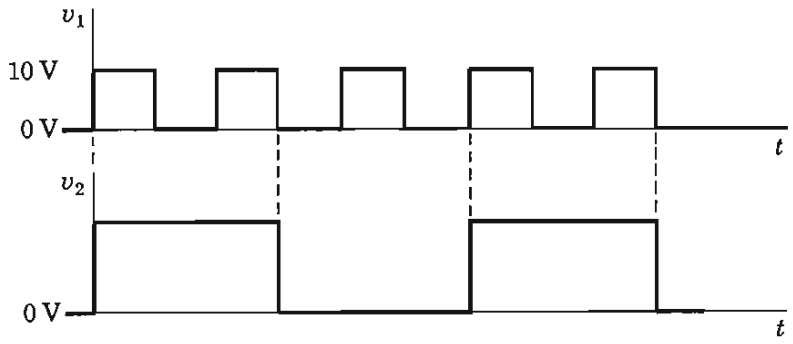
6-1 Convert the following decimal numbers to binary form: (*a*) 671, (*b*) 325, (*c*) 152.

6-2 The parameters in the diode OR circuit of Fig. 6-3 are $V(0) = +12$ V, $V(1) = -2$ V, $R_s = 600\ \Omega$, $R = 10$ K, $R_f = 0$, $R_r = \infty$, and $V_\gamma = 0.6$ V. Calculate the output levels if one input is excited and if (*a*) $V_R = +12$ V, (*b*) $V_R = +10$ V, (*c*) $V_R = +14$ V, and (*d*) $V_R = 0$ V. For which of these cases is the OR function

satisfied (except possibly for a shift in level between input and output)? (*e*) Repeat part *a* if three inputs are excited.

6-3 Consider a two-input positive-logic diode OR gate (Fig. 6-3 with the diodes reversed) and with $V_R = 0$. The inputs are the square waves v_1 and v_2 indicated. Sketch the output waveform if the ratio of the amplitude of v_2 to v_1 is (*a*) 2 and (*b*) $\frac{1}{2}$. Assume ideal diodes ($R_f = 0$, $R_r = \infty$, and $V_\gamma = 0$) and $R_s = 0$.

Prob. 6-3



6-4 Consider two signals, a 1-kHz sine wave and a 10-kHz square wave of zero average value, applied to the OR circuit of Fig. 6-3 with $V_R = 0$. Draw the output waveform if the sine-wave amplitude (*a*) exceeds the square-wave amplitude, (*b*) is less than the square-wave amplitude.

6-5 Consider a two-input positive-logic diode AND circuit (Fig. 6-5) with $V_R = 15$ V, $R = 10$ K, $R_s = 1$ K. Assume ideal diodes and neglect all capacitances. A square wave v_i, extending from -5 to $+5$ V with respect to ground, is applied simultaneously to both inputs. (*a*) Sketch the output v_o and calculate the maximum and minimum voltages with respect to ground. (*b*) If $v_1 = v_i$ and $v_2 = -v_i$, calculate the voltage levels of v_o and plot.

6-6 (*a*) Using a clamping diode draw an AND diode gate whose output is V' when there is no coincidence, and $V(1)$ when there is. Assume that $V_R \geq V(1)$ and that positive logic is used.

(*b*) Find the minimum required value of V' and the maximum number of inputs if the rated current of the catching diode is I_m.

6-7 (*a*) Indicate how to modify the circuit of Prob. 6-5 so that the minimum voltage is zero.

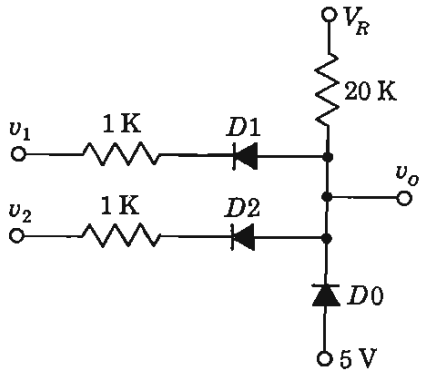
(*b*) Repeat parts *a* and *b* of Prob. 6-5 assuming maximum rated current of the catching diode 5 mA.

(*c*) Find the maximum number of inputs if rated current of catching diode is 50 mA.

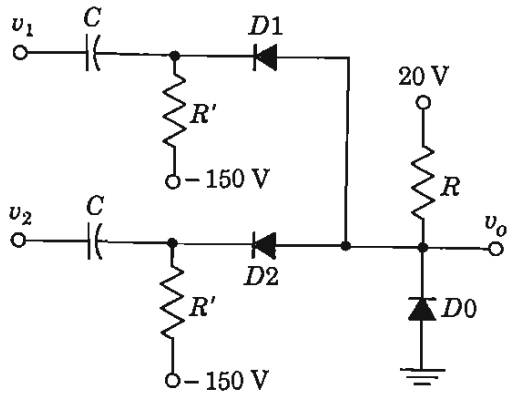
6-8 Consider a two-input positive-logic diode AND circuit (Fig. 6-5*b*) with $V_R = 10$ V, $R = 10$ K, and $R_s = 0$. Assume ideal diodes and neglect capacitances. The input waveforms are v_1 and v_2 sketched in Prob. 6-3. Sketch the output waveform if the ratio of the amplitude of v_2 to v_1 is (*a*) 2, (*b*) 1, and (*c*) $\frac{1}{2}$. Repeat part *b* if $R_s = 1$ K.

6-9 The binary input levels for the AND circuit shown are $V(0) = 0$ V and $V(1) = 25$ V. Assume ideal diodes. If $v_1 = V(0)$ and $v_2 = V(1)$, then v_o is to be at 5 V. However, if $v_1 = v_2 = V(1)$, then v_o is to rise above 5 V.

(*a*) What is the maximum value of V_R which may be used?
(*b*) If $V_R = 20$ V, what is v_o at a coincidence [$v_1 = v_2 = V(1)$]? What are the diode currents?
(*c*) Repeat part *b* if $V_R = 40$ V.



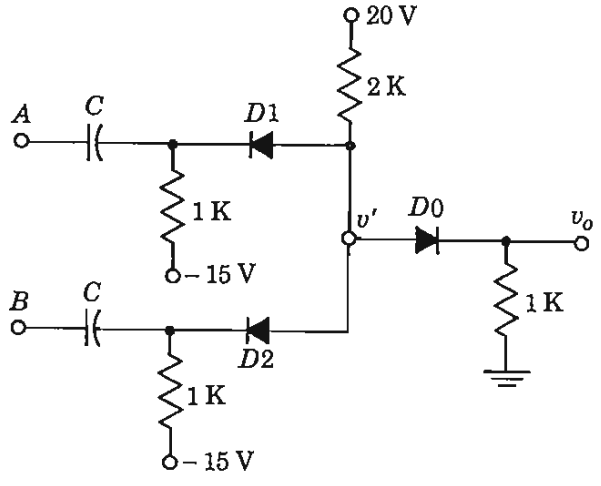
Prob. 6-9



Prob. 6-10

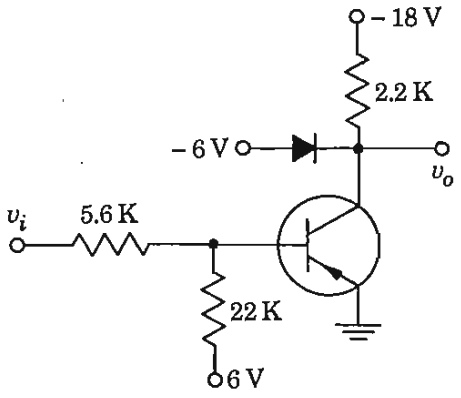
6-10 The two-input-diode AND circuit shown uses diodes with $R_f = 500\ \Omega$, $R_r = \infty$, and $V_\gamma = 0$. The quiescent current in *D*0 is 6 mA, and the currents in *D*1 and *D*2 are each 4 mA
(*a*) Calculate the quiescent output voltage v_o and the values of R and R'.
(*b*) Calculate the output voltage when one input diode is cut off. Calculate this result approximately by assuming that the currents through R and the remaining input diode do not change. Also, calculate the result exactly.
(*c*) Assume that diode *D*0 is omitted, that the currents in *D*1 and *D*2 remain 4 mA each, and that the output v_o is the same as that found in part *a*. Find R and R'.
(*d*) If the conditions are as indicated in part *c* but one of the diodes is cut off, find the output voltage v_o. Compare with the result in part *b* when *D*0 acts as a clamp.

6-11 Find v_o and v' if (*a*) there are no pulses at either *A* or *B*, (*b*) there is a 30-V positive pulse at *A* or *B*, and (*c*) there are positive pulses at both *A* and *B*. (*d*) What is the minimum pulse amplitude which must be applied in order that the circuit operate properly? Assume ideal diodes.



Prob. 6-11

6-12 (*a*) Verify that the circuit shown is an inverter by calculating the output levels corresponding to input levels of 0 and −6 V. What minimum value of h_{FE} is required? Neglect junction saturation voltages and assume an ideal diode.
(*b*) If the reverse collector saturation current at 25°C is 5 μA, what is the maximum temperature at which this inverter will operate properly?



Prob. 6-12

6-13 For the circuit shown in Fig. 6-7, $V_{CC} = 8$ V, $V_{BB} = 8$ V, $V_{EE} = 0$, and $R_c = 2.2$ K. The inverter is to operate properly in the temperature range −25 to 125°C. The silicon transistor used has $(h_{FE})_{\min} = 65$ at 25°C, 55 at −25°C, 85 at 125°C, and $I_{CBO} = 5$ nA at 25°C. The desired logic levels are $V(1) = 8 \pm 2$ V, $V(0) = 0.2 \pm 0.2$ V.
(*a*) Find the maximum value of R_1 if $R_2 = 100$ K.
(*b*) If the desired logic levels are $V(1) = 4 \pm 1$ V and $V(0) = 0.2 \pm 0.2$ V, what modification should you make to this circuit?

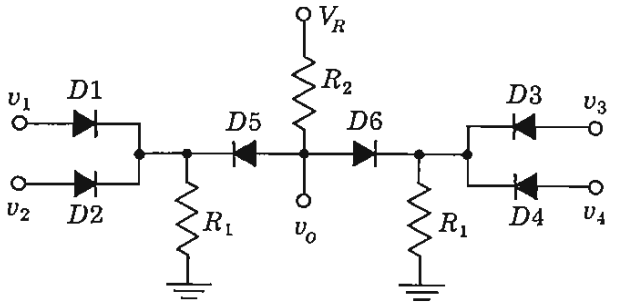
6-14 A half adder is a combination of OR and AND gates. It has two inputs and two outputs and the following truth table:

Input 1	Input 2	Output 1	Output 2
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Draw the logic block diagram for a half adder.

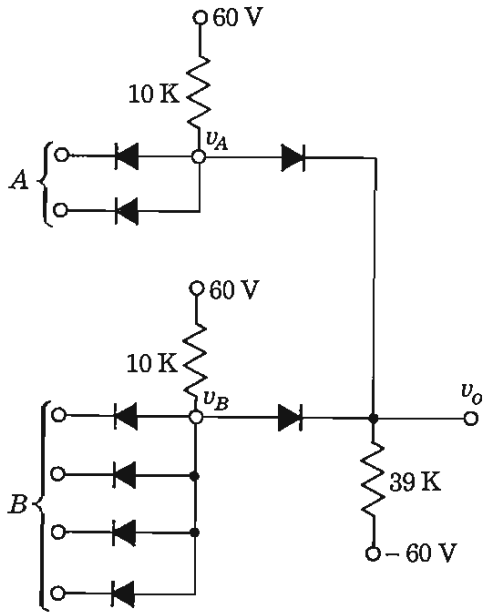
6-15 The four inputs v_1, v_2, v_3, and v_4 are voltages from zero-impedance sources whose values are either $V(0) = 10$ V or $V(1) = 20$ V. The diodes are ideal. $V_R = 25$ V, $R_1 = 5$ K, and $R_2 = 10$ K.
(*a*) If $v_1 = v_2 = 10$ V and $v_3 = v_4 = 20$ V, find v_o and the currents in each diode.
(*b*) If $v_1 = v_3 = 10$ V and $v_2 = v_4 = 20$ V, find v_o and the currents in each diode.
(*c*) Sketch in block-diagram form the logic performed by this circuit.
(*d*) Verify that in order for the circuit to operate properly the following inequality must be satisfied:

$$R_2 > \frac{V_R - V(0)}{V(0)} R_1$$



Prob. 6-15

6-16 (*a*) In block-diagram form indicate the logic performed by the diode system shown. The input levels are $V(0) = -8$ V and $V(1) = +2$ V. Neglect source resistance and assume that the diodes are ideal. Justify your answer by calculating the voltages v_A, v_B, and v_o (and indicating which diodes are conducting) under the following circumstances: (i) all inputs are at $V(0)$; (ii) some but not all inputs in A are at $V(1)$ and all inputs in B are at $V(0)$; (iii) all inputs in A are at $V(1)$ and some inputs in B are at $V(1)$; and (iv) all inputs are at $V(1)$.
(*b*) If the 10-K resistance were increased, at what maximum value would the circuit no longer operate in the manner described above?
(*c*) Indicate how to modify the circuit so that the output levels are -5 and 0 V, respectively.



Prob. 6-16

6-17 (*a*) Verify De Morgan's law [Eq. (6-27)] in a manner analogous to that given in the text in connection with the proof of Eq. (6-25).
(*b*) Prove Eq. (6-27) by constructing a truth table for each side and verifying that these two tables have the same outputs.

6-18 Verify the auxiliary Boolean identities in Table 6-4 (page 174).

6-19 Using Boolean algebra, verify
(*a*) $\overline{\bar{A} + B} + \overline{\bar{A} + \bar{B}} = A$
(*b*) $AB + AC + B\bar{C} = AC + B\bar{C}$
HINT: Multiply the first term on the left-hand side by $C + \bar{C} = 1$.
(*c*) $\overline{AB + BC + C\bar{A}} = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A}$

6-20 Using Boolean algebra, verify
(*a*) $(A + B)(B + C)(C + A) = AB + BC + CA$
(*b*) $(A + B)(\bar{A} + C) = AC + \bar{A}B$
(*c*) $AB + \bar{B}\bar{C} + A\bar{C} = AB + \bar{B}\bar{C}$
HINT: A term may be multiplied by $B + \bar{B} = 1$.

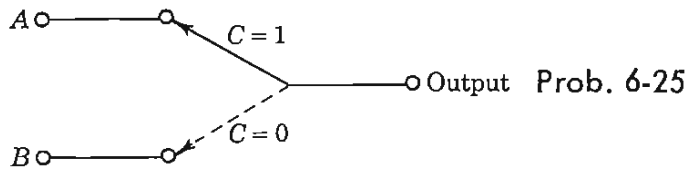
6-21 Given two N-bit characters which are available in parallel form. Indicate in block-diagram form a system whose output is 1 if and only if *all* corresponding bits are equal, that is, only if the two characters are equal.

6-22 A, B, and C represent the presence of pulses. The logic statement "A or B and C" can have two interpretations. Which are they? In block-diagram form draw the circuit to perform each of the two logic operations.

6-23 A circuit has three input and one output terminals. The output is 1 if any two of the three inputs are 1 and is 0 for any other combination of inputs. Draw a block diagram of this logic circuit.

6-24 In block-diagram form draw a circuit to perform the following logic: If pulses A_1, A_2, and A_3 occur simultaneously or if pulses B_1 and B_2 occur simultaneously, an output pulse is delivered, provided that pulse C does not occur at the same time. No output is to be obtained if A_1, A_2, A_3, B_1, and B_2 occur simultaneously.

6-25 A single-pole double-throw switch is to be simulated with AND, OR, and INHIBITOR circuits. Call the two signal inputs A and B. A third input C receives the switching instructions in the form of a code: 1 (a pulse is present) or 0 (no pulse exists). It is desired that $C = 1$ set the switch to A and $C = 0$ set the switch to B, as indicated schematically. In block-diagram form show the circuit for this switch.



Prob. 6-25

6-26 In block-diagram form draw a circuit which satisfies simultaneously the conditions *a*, *b*, and *c* as follows:
(*a*) The output is excited if any pair of inputs A_1, A_2, and A_3 is excited, provided that B is also excited.
(*b*) The output is 1 if any one (and only one) of the inputs A_1, A_2, or A_3 is 1, provided that $B = 0$.
(*c*) No output is excited if A_1, A_2, and A_3 are simultaneously excited.

6-27 (*a*) For the illustrative NAND gate of Fig. 6-19*a* calculate the minimum value of h_{FE} taking junction voltages into account.
(*b*) What is the maximum noise voltage (superimposed upon the logic level) which will still permit the circuit to operate properly? Consider the following two cases: (i) a complete coincidence and (ii) all inputs but one in the 1 state.
(*c*) What is the maximum value of the source resistance which will still permit proper circuit operation? Assume a 0.7-V drop across a conducting diode.

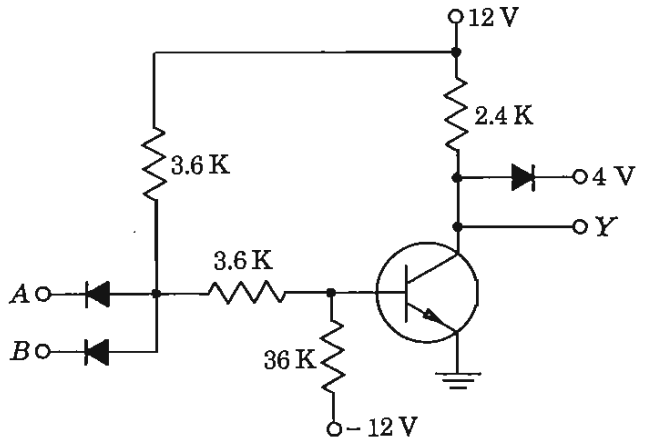
6-28 The circuit shown uses silicon diodes and a silicon transistor. The input A or B is obtained from the output Y of a similar gate.

(a) What are the logic levels? Take junction voltages into account.

(b) Verify that the circuit satisfies the NAND operation. Assume $h_{FE,\min} = 15$.

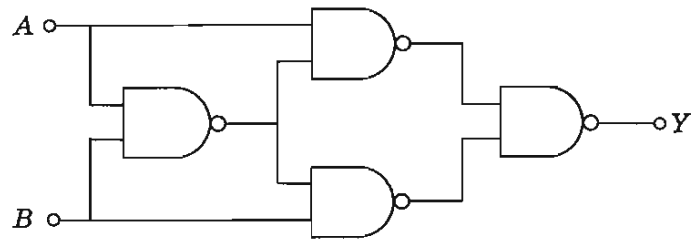
(c) What is the maximum allowable value of I_{CBO}?

(d) Now neglect junction voltages and I_{CBO} and verify that the circuit satisfies the NOR operation.



Prob. 6-28

6-29 Verify that the circuit shown is an EXCLUSIVE OR.

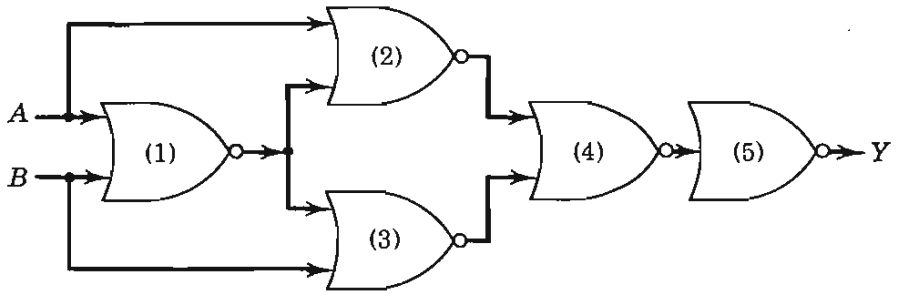


Prob. 6-29

6-30 Verify that the NOR-NOR topology is equivalent to an OR-AND system.

6-31 Verify that the logic operations OR, AND, and NOT may be implemented by using only NOR gates.

6-32 What logic operation is performed by the circuit shown, which consists of interconnected NOR gates?

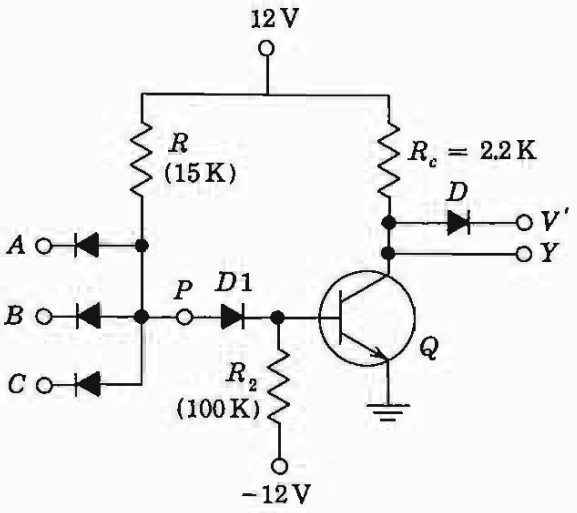


Prob. 6-32

6-33 (*a*) Implement the EXCLUSIVE OR gate using (i) NOR gates, (ii) NAND gates.
(*b*) Repeat part *a* for the half adder of Prob. 6-14.

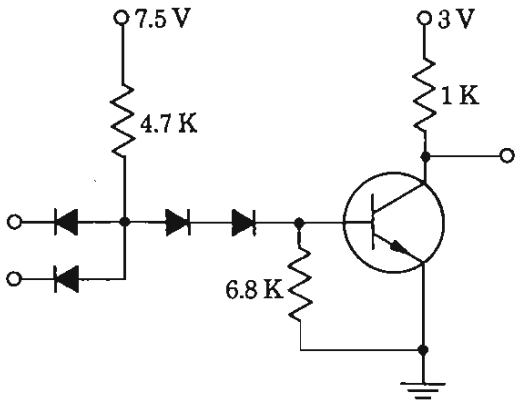
6-34 (*a*) The discrete-components circuit of a DTL gate shown uses a silicon transistor with worst-case values of $V_{BE,sat} = 1.0$ V and $V_{CE,sat} = 0.5$ V. The voltage across any silicon diode (when conducting) is 0.7 V. Assume that $D1$ consists of two diodes in series. The circuit parameters are $V_{CC} = V_{BB} = 12$ V, $R = 15$ K, $R_2 = 100$ K, and $R_c = 2.2$ K. The inputs to this switch are obtained from the outputs of similar gates. Verify that the circuit functions as a positive NAND. In particular, for proper operation, calculate the minimum value of the clamping voltage V' and h_{FE}.
(*b*) Will the circuit operate properly if $D1$ is (i) a single diode or (ii) three diodes in series?
(*c*) Replace $D1$ by a 15-K resistance and repeat part *a*. Compare the binary levels in part *a* and *c*.
(*d*) What is the maximum allowed fan-in, assuming that the diodes are ideal? What is a practical limitation on fan-in?

Prob. 6-34



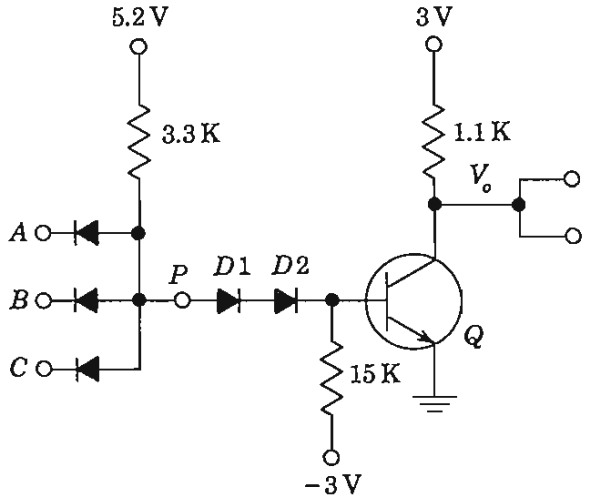
6-35 The DTL shown uses silicon devices with $V_{BE,sat} = 0.8$ V, $V_{CE,sat} = 0.2$ V, $V_\gamma = 0.5$ V, and the drop across a conducting diode = 0.7 V. The inputs to this switch are obtained from the outputs of similar gates.

Prob. 6-35



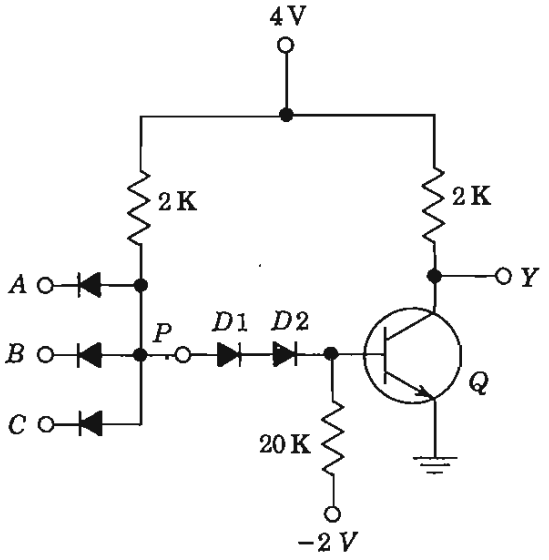
(*a*) Verify that the circuit functions as a positive NAND and calculate $h_{FE,\min}$. Assume that the transistor is essentially cut off if the base-to-emitter voltage is at least 0.1 V smaller than the cutin voltage V_γ.
(*b*) Assume that the diode reverse saturation current is equal to the transistor reverse saturation collector current. Find $I_{CBO,\max}$.
(*c*) If all inputs are high, what is the magnitude of noise voltage at the input which will cause the gate to malfunction?
(*d*) Repeat part *c* if at least one input is low.

6-36 (*a*) Analyze the DTL circuit shown. Use the voltage drops given in Prob. 6-35.
(*b*) Find $h_{FE,\min}$ if two similar gates are to be driven by this circuit.
(*c*) Find the noise margins.



Prob. 6-36

6-37 (*a*) Analyze the DTL circuit shown. Use the voltage drops given in Prob. 6-35.
(*b*) If $h_{FE} = 25$, calculate the fan-out N.
(*c*) For a fan-out of 10 and assuming a diode reverse saturation current of 15 μA, what is $V(1)$?



Prob. 6-37

6-38 The positive DTL NAND gate of Prob. 6-39 is to operate properly in the temperature range −50 to 160°C. The silicon transistor has $h_{FE,\min} = 50$ at −50°C, $h_{FE,\min} = 65$ at 25°C, and $h_{FE,\min} = 100$ at 160°C. The reverse saturation collector current of the transistor at 25°C is $I_{CBO} = 0.5$ nA, and it equal to the reverse saturation current of the silicon diode. The maximum current rating of the transistor is 50 mA. The gate will be used in a system with power supply voltage of 5 V, and the allowed variation in $V(1)$ is ± 0.5 V. The desired absolute value of the noise margin is 1.5 V and the desired fanout is 10. The transistor is considered OFF if $V_{BE} \leq 0.4$ V.

(*a*) Calculate the minimum required number of diodes between P and the base of the transistor.

(*b*) Calculate the maximum value of R_2.

(*c*) For the values found in (*a*) and (*b*) determine the range of values that R_c can take.

(*d*) Using the middle value of R_c found in part (*c*), specify the range of values that R_1 can take.

6-39 For the integrated positive DTL NAND gate shown, prove that

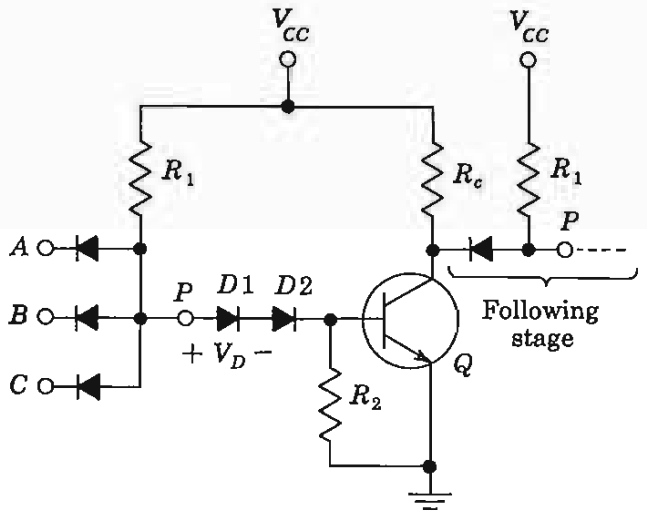
(*a*) The maximum number of diodes that can be used is given by $n_{\max} = (V_{CC} - V_{BE,\text{sat}})/V_D$, where V_D is the voltage drop across a diode.

(*b*) The maximum fan-out is given by

$$N_{\max} \approx h_{FE} - h_{FE}\left(n + \frac{R_1}{R_2}\right)\frac{V_D}{V_{CC}} - \frac{R_1}{R_c}\left(1 + \frac{V_D}{V_{CC}}\right)$$

Assume that $V_{BE,\text{sat}} \approx V_D$ and $V_{CC} - V_D \gg V_{CE,\text{sat}}$.

Prob. 6-39

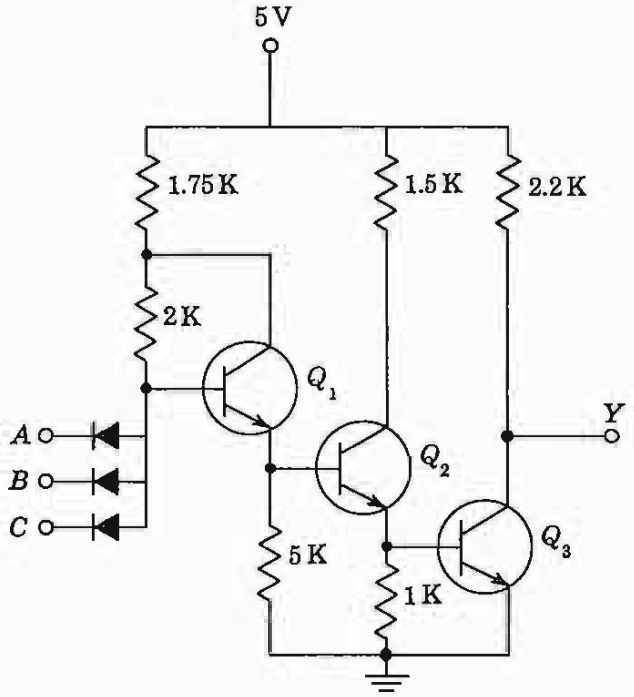


6-40 For the modified integrated positive DTL NAND of Fig. 6-24 specify h_{FE} and the maximum current rating in order to have a fan-out of 50.

6-41 For the integrated positive DTL gate shown

(*a*) Verify its function as a NAND gate and specify the state of each transistor when at least one input is low and also at a coincidence.

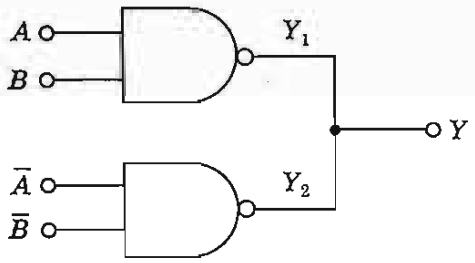
(*b*) For $h_{FE,\min} = 30$, calculate the fan-out of this gate. The inputs of this gate are obtained from the outputs of similar gates, and its output drives similar gates.



Prob. 6-41

6-42 In the integrated positive DTL NAND gate of Fig. 6-24 a Schottky diode is fabricated between base and collector to prevent the transistor $Q2$ from saturating. The anode of the Schottky diode is at the base and the drop across the diode when conducting is 0.4 V (Sec. 7-13).
(*a*) Explain why the transistor $Q2$ does not go into saturation.
(*b*) Verify the operation of the gate as a NAND gate and calculate noise margins.
(*c*) Find the logic levels and maximum fan-out if the inputs of this gate are obtained from similar gates and outputs drive similar gates and $h_{FE} = 30$.

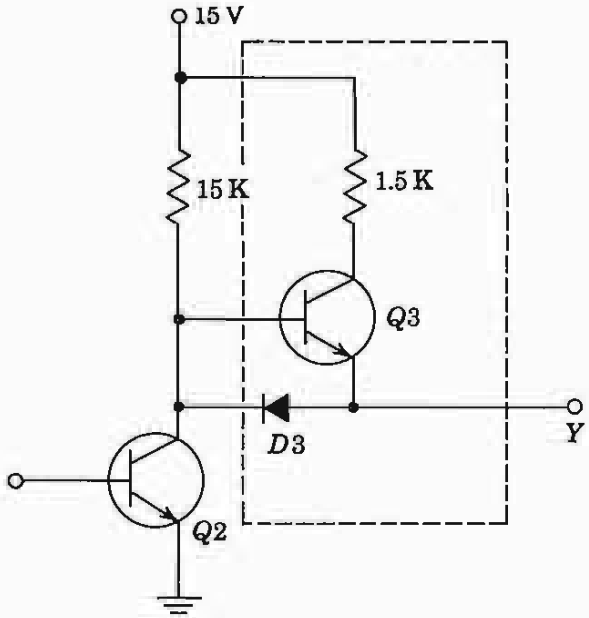
6-43 Verify that this wired circuit performs the EXCLUSIVE OR function.



Prob. 6-43

6-44 (*a*) For the high-threshold logic NAND gate of Fig. 6-26, if V_2 of the diode is 6.9 V, verify that this circuit functions as a positive NAND and calculate $h_{FE,\min}$. The inputs of this gate are obtained from the output of similar gates.
(*b*) Calculate noise margins.
(*c*) Calculate the fan-out of this gate if $h_{FE,\min} = 40$.

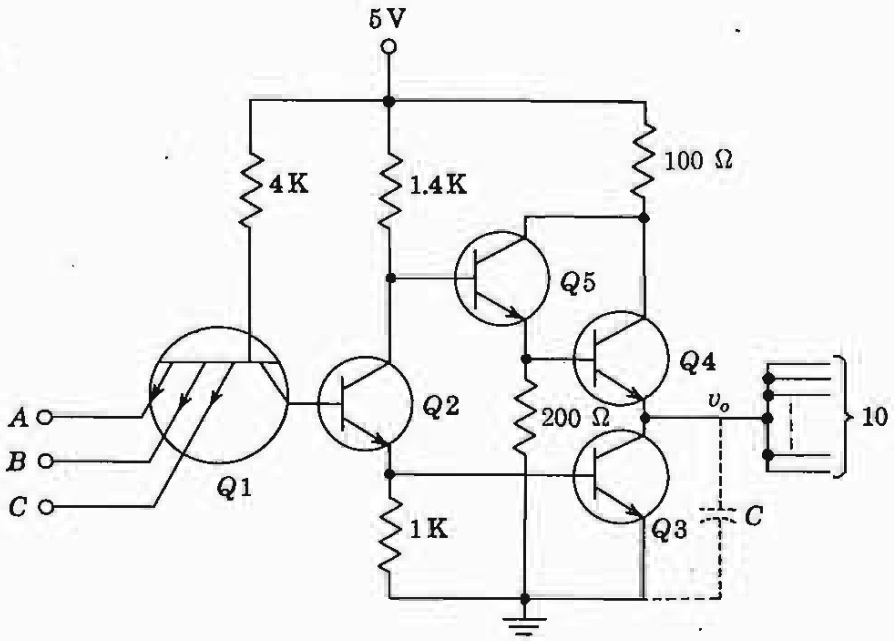
6-45 If the output in Fig. 6-26 is capacitively loaded (by C), then the rise time as Y goes from its low to its high state will be long because of the high load resistance (15 K) of $Q2$. To reduce this time constant the active pull-up circuit indicated in the dashed block is added across the 15-K resistor.
(*a*) Explain how the circuit works.
(*b*) Why not simply replace 15 K by 1.5 K?



Prob. 6-45

6-46 (*a*) For the IC positive TTL NAND gate shown in Fig. 6-27, calculate $h_{FE,\min}$ for proper operation of the circuit.
(*b*) Calculate noise margins.
(*c*) Calculate the fan-out if $h_{FE,\min} = 30$.

6-47 For the IC positive NAND TTL gate shown, if the inputs are obtained from the outputs of similar gates and $h_{FE,\min}$ of the transistors is 30, verify its operation as a NAND gate when the fan-out is 10.
(*a*) At coincidence, find the state of each transistor and all currents and voltages of the circuit.
(*b*) Repeat part *a* if at least one input is low.
(*c*) Find the logic levels.
(*d*) Calculate the peak current drawn from the supply during the transient.
(*e*) Calculate maximum fan-out for proper operation of the gate.



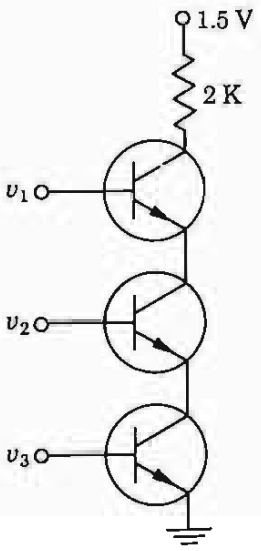
Prob. 6-47

6-48 For an RTL IC positive NOR gate prove that the maximum fan-out can be approximated by the formula

$$N_{\max} = h_{FE,\min} - h_{FE,\min}\frac{0.6}{V_{CC}} - \frac{R_b}{R_c}$$

6-49 The inputs of the RTL IC positive NOR gate shown in Fig. 6-29 are obtained from the outputs of similar gates and the outputs drive similar gates. If the supply voltage of the system is 5 V and the temperature range for proper operation of the gate is -50 to 150°C, calculate the maximum permissible values of the resistances. Assume $h_{FE} = 30$ at -50°C, $I_{CBO} = 10$ nA at 25°C, and the desired fan-out is 10.

6-50 Verify that the DCTL circuit shown with the fan-in transistors in series satisfies the NAND operation. Assume that for the silicon transistors, $V_{CE,\text{sat}} = 0.2$ V and $V_{BE,\text{sat}} = 0.8$ V. Calculate the collector currents in each transistor when all inputs are high. The input to each base is taken from the output of a similar gate.



Prob. 6-50

CHAPTER 7

7-1 (*a*) Verify that Eq. (7-3) meets the stated boundary conditions.
(*b*) Verify that Eq. (7-5) satisfies the diffusion equation (7-2) and that it meets the stated boundary conditions.

7-2 A silicon wafer is uniformly doped with phosphorus to a concentration of 10^{15} cm^{-3}. Refer to Table 2-1 on page 29. At room temperature (300°K) find
(*a*) The percentage of phosphorus by weight in the wafer.
(*b*) The conductivity and resistivity.
(*c*) The concentration of boron, which, if added to the phosphorus-doped wafer, would halve the conductivity.

7-3 (*a*) Using the data of Fig. 7-8, calculate the percent maximum concentration of arsenic (atoms per cubic centimeter) that can be achieved in solid silicon. The

concentration of pure silicon may be calculated from the data in Table 2-1 on page 29.

(*b*) Repeat part *a* for gold.

7-4 (*a*) How long would it take for a fixed amount of phosphorus distributed over one surface of a 25-μm-thick silicon wafer to become substantially uniformly distributed throughout the wafer at 1300°C? Consider that the concentration is sufficiently uniform if it does not differ by more than 10 percent from that at the surface.

(*b*) Repeat part *a* for gold, given that the diffusion coefficient of gold in silicon is 1.5×10^{-6} cm^2/s at 1300°C.

7-5 Show that the junction depth x_j resulting from a Gaussian impurity diffusion into an oppositely doped material of background concentration N_{BC} is given by

$$x_j = \left(2Dt \ln \frac{Q^2}{N_{BC}^2 \pi Dt}\right)^{\frac{1}{2}}$$

7-6 A uniformly doped *n*-type silicon substrate of 0.1 Ω-cm resistivity is to be subjected to a boron diffusion with constant surface concentration of 4.8×10^{18} cm^{-3}. The desired junction depth is 2.7 μm.

(*a*) Calculate the impurity concentration for the boron diffusion as a function of distance from the surface.

(*b*) How long will it take if the temperature at which this diffusion is conducted is 1100°C?

(*c*) An *n-p-n* transistor is to be completed by diffusing phosphorus at a surface concentration of 10^{21} cm^{-3}. If the new junction is to be at a depth of 2 μm, calculate the concentration for the phosphorus diffusion as a function of distance from the surface.

(*d*) Plot the impurity concentrations (log scale) vs. distance (linear scale) for parts *a* and *c*, assuming that the boron stays put during the phosphorus diffusion. Indicate emitter, base, and collector on your plot.

(*e*) If the phosphorus diffusion takes 30 min, at what temperature is the apparatus operated?

7-7 List in order the steps required in fabricating a monolithic silicon integrated transistor by the epitaxial-diffused method. Sketch the cross section after each oxide growth. Label materials clearly. No buried layer is required.

7-8 Sketch *to scale* the cross section of a monolithic transistor fabricated on a 5-mil-thick silicon substrate. HINT: Refer to Sec. 7-1 and Figs. 7-12 and 7-13 for typical dimensions.

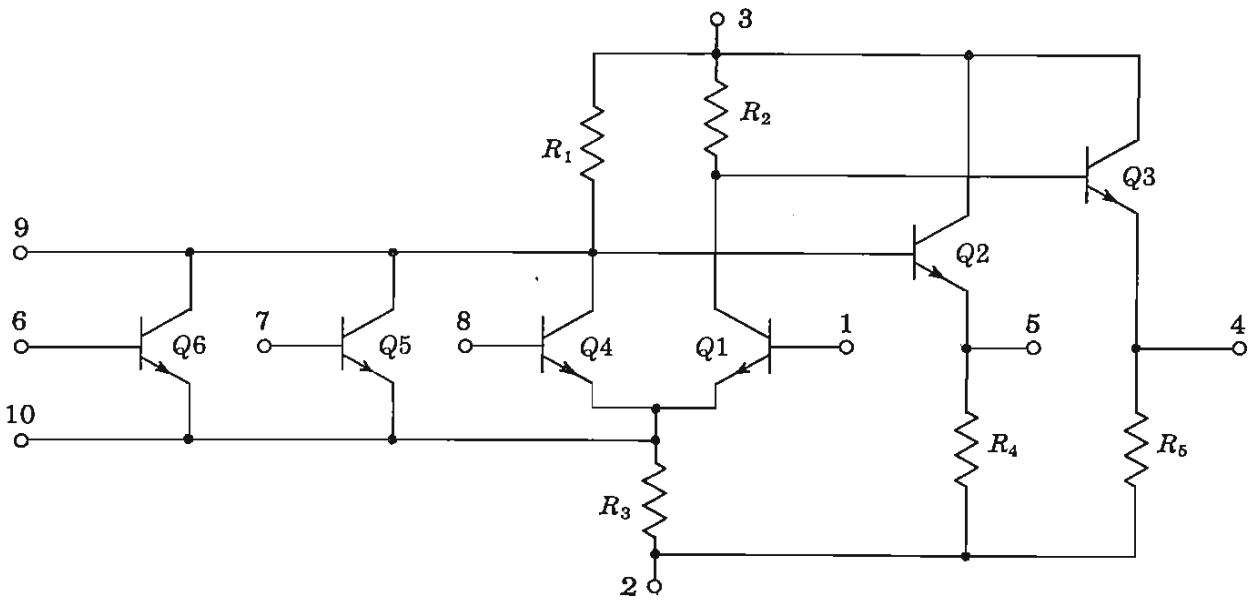
7-9 Sketch the five basic diode connections (in circuit form) for the monolithic integrated circuits. Which will have the lowest forward voltage drop? Highest breakdown voltage?

7-10 If the base sheet resistance can be held to within ± 10 percent and resistor line widths can be held to ± 0.1 mil, plot approximate tolerance of a diffused resistor as a function of line width w in mils over the range $0.5 \leq w \leq 5.0$. (Neglect contact-area and contact-placement errors.)

7-11 A 1-mil-thick silicon wafer has been doped uniformly with phosphorus to a concentration of 10^{16} cm^{-3}, plus boron to a concentration of 2×10^{15} cm^{-3}. Find its sheet resistance.

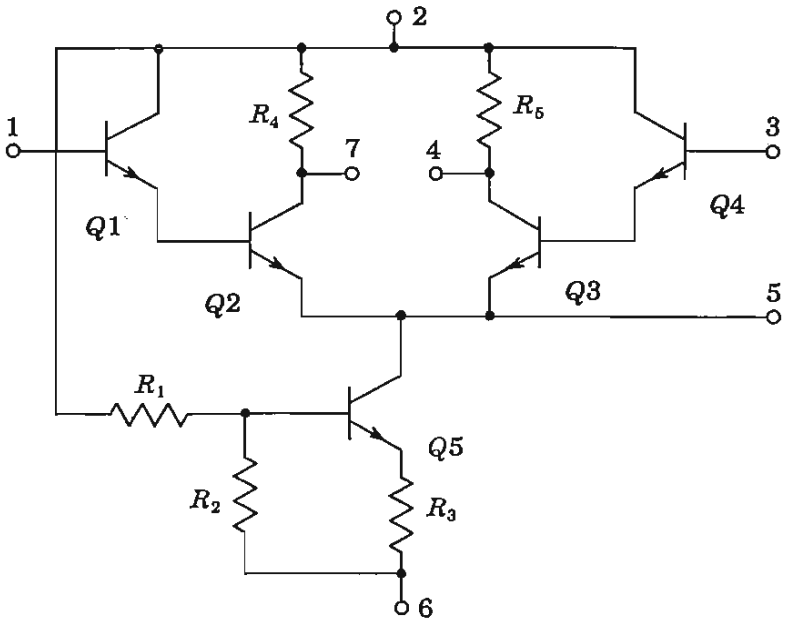
7-12 (*a*) Calculate the resistance of a diffused crossover 4 mils long, 1 mil wide, and 2 μm thick, given that its sheet resistance is 2.2 Ω/square.
(*b*) Repeat part *a* for an aluminum metalizing layer 0.5 μm thick of resistivity 2.8×10^{-6} Ω-cm. Note the advantage of avoiding diffused crossovers.

7-13 (*a*) What is the minimum number of isolation regions required to realize in monolithic form the logic gate shown?
(*b*) Draw a monolithic layout of the gate in the fashion of Fig. 7-25*b*.



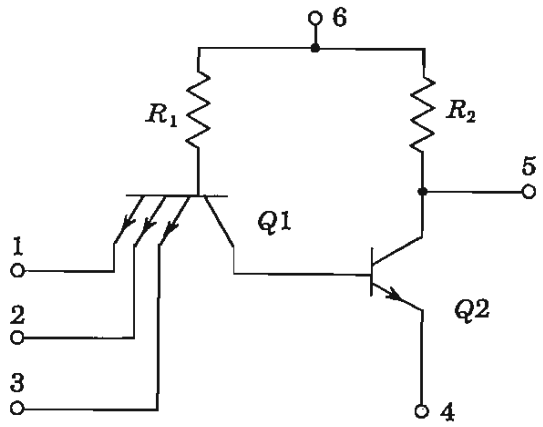
Prob. 7-13

7-14 Repeat Prob. 7-13 for the difference amplifier shown.



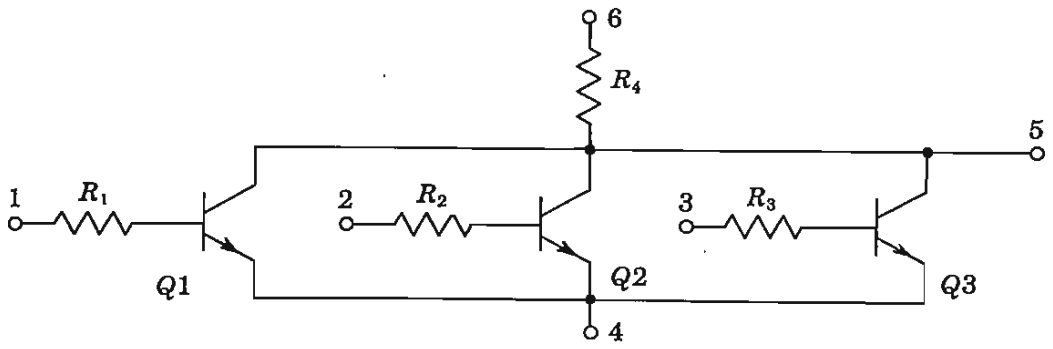
Prob. 7-14

7-15 For the circuit shown, find (*a*) the *minimum* number, (*b*) the *maximum* number, of isolation regions.



Prob. 7-15

7-16 For the circuit shown, (*a*) find the minimum number of isolation regions, and (*b*) draw a monolithic layout in the fashion of Fig. 7-26, given that (i) $Q1$, $Q2$, and $Q3$ should be single-base-stripe, 1- by 2-mil emitter, transistors, (ii) $R_1 = R_2 = R_3 = 400\ \Omega$, $R_4 = 600\ \Omega$. Use 1-mil-wide resistors.

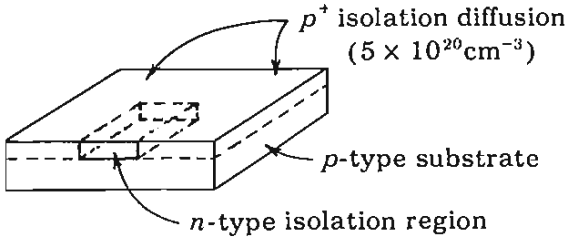


Prob. 7-16

7-17 An integrated junction capacitor has an area of 1,000 mils^2 and is operated at a reverse barrier potential of 1 V. The acceptor concentration of 10^{15} atoms/cm^3 is much smaller than the donor concentration. Calculate the capacitance.

7-18 A thin-film capacitor has a capacitance of 0.4 pF/mil^2. The relative dielectric constant of silicon dioxide is 3.5. What is the thickness of the SiO_2 layer in angstroms?

7-19 The *n*-type epitaxial isolation region shown is 8 mils long, 6 mils wide, and 1 mil thick and has a resistivity of 0.1 Ω-cm. The resistivity of the *p*-type substrate is 10 Ω-cm. Find the parasitic capacitance between the isolation region and the substrate under 5-V reverse bias. Assume that the sidewalls contribute 0.1 pF/mil^2.



Prob. 7-19

NOTE: *In the problems that follow, indicate your answer by giving the letter of the statement you consider correct.*

7-20 The typical number of diffusions used in making epitaxial-diffused silicon integrated circuits is (*a*) 1, (*b*) 2, (*c*) 3, (*d*) 4, (*e*) 5.

7-21 The "buried layer" in an integrated transistor is (*a*) p^+ doped, (*b*) located in the base region, (*c*) n^+ doped, (*d*) used to reduce the parasitic capacitance.

7-22 Epitaxial growth is used in integrated circuits (ICs)
(*a*) To grow selectively single-crystal p-doped silicon of one resistivity on a p-type substrate of a different resistivity.
(*b*) To grow single-crystal n-doped silicon on a single-crystal p-type substrate.
(*c*) Because it yields back-to-back isolating p-n junctions.
(*d*) Because it produces low parasitic capacitance.

7-23 Silicon dioxide (SiO_2) is used in ICs
(*a*) Because it facilitates the penetration of diffusants.
(*b*) Because of its high heat conduction.
(*c*) To control the location of diffusion and to protect and insulate the silicon surface.
(*d*) To control the concentration of diffusants.

7-24 The p-type substrate in a monolithic circuit should be connected to
(*a*) The most positive voltage available in the circuit.
(*b*) The most negative voltage available in the circuit.
(*c*) Any dc ground point.
(*d*) Nowhere, i.e., be left floating.

7-25 Monolithic integrated circuit systems offer greater reliability than discrete-component systems because
(*a*) There are fewer interconnections.
(*b*) High-temperature metalizing is used.
(*c*) Electric voltages are low.
(*d*) Electric elements are closely matched.

7-26 The collector-substrate junction in the epitaxial collector structure is, approximately,
(*a*) A step-graded junction.
(*b*) A linearly graded junction.
(*c*) An exponential junction.
(*d*) None of the above.

7-27 The sheet resistance of a semiconductor is
(*a*) An undesirable parasitic element.
(*b*) An important characteristic of a diffused region, especially when used to form diffused resistors.

(*c*) A characteristic whose value determines the required area for a given value of integrated capacitance.
(*d*) A parameter whose value is important in a thin-film resistance.

7-28 Isolation in ICs is required.
(*a*) To make it simpler to test circuits.
(*b*) To protect the components from mechanical damage.
(*c*) To protect the transistor from possible "thermal runaway."
(*d*) To minimize electrical interaction between circuit components.

7-29 Almost all resistors are made in a monolithic IC
(*a*) During the emitter diffusion.
(*b*) While growing the epitaxial layer.
(*c*) During the base diffusion.
(*d*) During the collector diffusion.

7-30 Increasing the yield of an integrated circuit
(*a*) Reduces individual circuit cost.
(*b*) Increases the cost of each good circuit.
(*c*) Results in a lower number of good chips per wafer.
(*d*) Means that more transistors can be fabricated on the same size wafer.

7-31 In a monolithic-type IC
(*a*) All isolation problems are eliminated.
(*b*) Resistors and capacitors of any value may be made.
(*c*) All components are fabricated into a single crystal of silicon.
(*d*) Each transistor is diffused into a separate isolation region.

7-32 The main purpose of the metalization process is
(*a*) To interconnect the various circuit elements
(*b*) To protect the chip from oxidation.
(*c*) To act as a heat sink.
(*d*) To supply a bonding surface for mounting the chip.

CHAPTER 8

NOTE: *Unless otherwise specified, all transistors in these problems are identical, and the numerical values of their h parameters are given in Table* 8-2. *Also assume that all capacitances are arbitrarily large.*

8-1 (*a*) Using Fig. 8-6*b* write the input and output equations.
(*b*) Draw the hybrid model for a CB transistor and write the input and output equations.

8-2 (*a*) Describe how to obtain h_{ic} from the CE input characteristics.
(*b*) Repeat part *a* for h_{rc}. Explain why this procedure, although correct in principle, is inaccurate in practice.

8-3 The transistor whose input characteristics are shown in Fig. 8-2 is biased at $V_{CE} = -8$ V and $I_B = -300\ \mu$A.
(*a*) Compute graphically h_{fe} and h_{oe} at the quiescent point specified above.
(*b*) Using the *h* parameters computed in part *a*, calculate h_{fb} and h_{ob}.

8-4 Justify the statement in the footnote to Table 8-3. HINT: Draw a CE transistor circuit with a signal voltage V_s between base and ground. Now interchange *B* and *E* and observe the resulting configuration.

8-5 (*a*) Find the CC h parameters in terms of the CE h parameters.
(*b*) Find the CE h parameters in terms of the CC parameters.

8-6 (*a*) Find the h_{rb} in terms of the CE h parameters.
(*b*) Find h_{ie} in terms of the CB h parameters.

8-7 (*a*) Show that the exact expression for h_{fe} in terms of the CB hybrid parameters is

$$h_{fe} = -\frac{h_{fb}(1 - h_{rb}) + h_{ib}h_{ob}}{(1 + h_{fb})(1 - h_{rb}) + h_{ob}h_{ib}}$$

(*b*) From this exact formula obtain the approximate expression for h_{fe}.
(*c*) Show that the exact expression for h_{fb} in terms of the CE hybrid parameters is

$$h_{fb} = -\frac{h_{fe}(1 - h_{re}) + h_{ie}h_{oe}}{(1 + h_{fe})(1 - h_{re}) + h_{oe}h_{ie}}$$

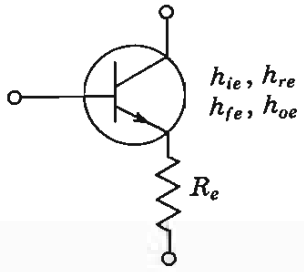
(*d*) From this exact formula obtain the approximate expression for h_{fb}.

8-8 For the circuit shown, verify that the modified h parameters (indicated by primes) are

(*a*) $h'_{ie} \approx h_{ie} + \dfrac{(1 + h_{fe})R_e}{1 + h_{oe}R_e}$ (*b*) $h'_{re} = \dfrac{h_{re} + h_{oe}R_e}{1 + h_{oe}R_e}$

(*c*) $h'_{fe} = \dfrac{h_{fe} - h_{oe}R_e}{1 + h_{oe}R_e}$ (*d*) $h'_{oe} = \dfrac{h_{oe}}{1 + h_{oe}R_e}$

(*e*) To what do these expressions reduce if $h_{oe}R_e \ll 1$?

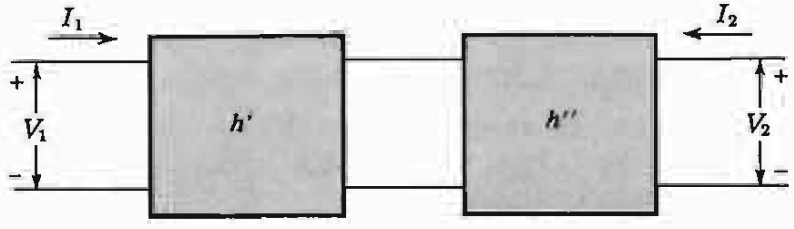


Prob. 8-8

8-9 Show that the overall h parameters of the accompanying two-stage cascaded amplifier are

(*a*) $h_{11} = h'_{11} - \dfrac{h'_{12}h'_{21}}{1 + h'_{22}h''_{11}}h''_{11}$ (*b*) $h_{12} = \dfrac{h'_{12}h''_{12}}{1 + h'_{22}h''_{11}}$

(*c*) $h_{21} = -\dfrac{h'_{21}h''_{21}}{1 + h'_{22}h''_{11}}$ (*d*) $h_{22} = h''_{22} - \dfrac{h''_{12}h''_{21}}{1 + h'_{22}h''_{11}}h'_{22}$



Prob. 8-9

8-10 Show that the overall h parameters for the composite transistor shown are

(*a*) $h_{ie} = h_{ie1} + \dfrac{(1 - h_{re1})(1 + h_{fe1})h_{ie2}}{1 + h_{oe1}h_{ie2}}$

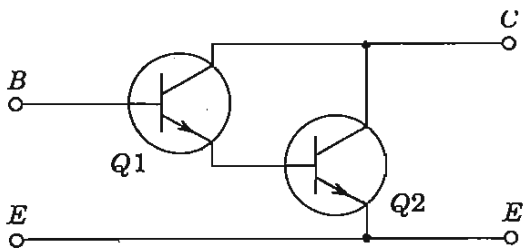
(*b*) $h_{fe} = h_{fe1} + \dfrac{(h_{fe2} - h_{oe1}h_{ie2})(1 + h_{fe1})}{1 + h_{oe1}h_{ie2}}$

(*c*) $h_{oe} = h_{oe2} + \dfrac{(1 + h_{fe2})(1 - h_{re2})h_{oe1}}{1 + h_{oe1}h_{ie2}}$

(*d*) $h_{re} = h_{re2} + \dfrac{(h_{ie2}h_{oe1} + h_{re1})(1 - h_{re2})}{1 + h_{oe1}h_{ie2}}$

(*e*) Obtain numerical values for the h parameters of the composite transistor by assuming identical transistors $Q1$ and $Q2$ and using Table 8-2.

Prob. 8-10



8-11 Given a single-stage transistor amplifier with the h parameters specified in Table 8-2, calculate A_I, A_V, A_{Vs}, R_i, and R_o for the CC transistor configuration, with $R_s = R_L = 10$ K. Check your results with Fig. 8-16.

8-12 (*a*) Draw the equivalent circuit for the CE and CC configurations subject to the restriction that $R_L = 0$. Show that the input impedances of the two circuits are identical.

(*b*) Draw the circuits for the CE and CC configurations subject to the restriction that the input is open-circuited. Show that the output impedances of the two circuits are identical.

8-13 For any single-transistor amplifier prove that

$$R_i = \frac{h_i}{1 - h_r A_V}$$

8-14 Prove that

$$Y_o = h_o \left(\frac{R_s + R_{i\infty}}{R_s + R_{io}} \right)$$

where $R_{i\infty} \equiv R_i$ for $R_L = \infty$, and $R_{io} \equiv R_i$ for $R_L = 0$.

8-15 (*a*) For a CE configuration, what is the maximum value of R_L for which R_i differs by no more than 10 percent of its value at $R_L = 0$? Use the transistor parameters given in Table 8-2.

(*b*) What is the maximum value of R_s for which R_o differs by no more than 10 percent of its value for $R_s = 0$?

(*c*) For the CB configuration, what is the maximum value of R_L for which R_i does not exceed 50 Ω?

8-16 Consider an emitter follower and show that as $R_e \to \infty$

(*a*) $R_i \to h_{ie} + \dfrac{1 + h_{fe}}{h_{oe}} \approx \dfrac{1}{h_{ob}}$

Explain the result physically.

(*b*) $1 - A_V \approx \dfrac{h_{ie}h_{oe}}{1 + h_{fe}}$

Evaluate A_V using the *h*-parameter values given in Table 8-2.

8-17 For the emitter follower with $R_s = 0.5$ K and $R_L = 5$ K, calculate A_I, R_i, A_V, A_{Vs}, R_o. Assume $h_{fe} = 50$, $h_{ie} = 1$ K, $h_{oe} = 25$ μA/V.

8-18 (*a*) Design an emitter follower having $R_i = 500$ K and $R_o = 20$ Ω. Assume $h_{fe} = 50$, $h_{ie} = 1$ K, $h_{oe} = 25$ μA/V.

(*b*) Find A_I and A_V for the emitter follower of part *a*.

(*c*) Find R_i and the necessary R_L so that $A_V = 0.999$.

8-19 For the transistor circuit in Fig. 8-12 show that

(*a*) $(A_{Is})_{max} = -h_f$, if $R_L = 0$ and $R_s = \infty$.

(*b*) $R_i = h_i$, if $R_L = 0$.

(*c*) $R_i = \dfrac{h_ih_o - h_rh_f}{h_o}$, if $R_L = \infty$.

(*d*) $(A_{Vs})_{max} = -\dfrac{h_f}{h_ih_o - h_rh_f}$, if $R_L = \infty$ and $R_s = 0$.

(*e*) $R_o = \dfrac{h_i}{h_ih_o - h_rh_f}$, if $R_s = 0$.

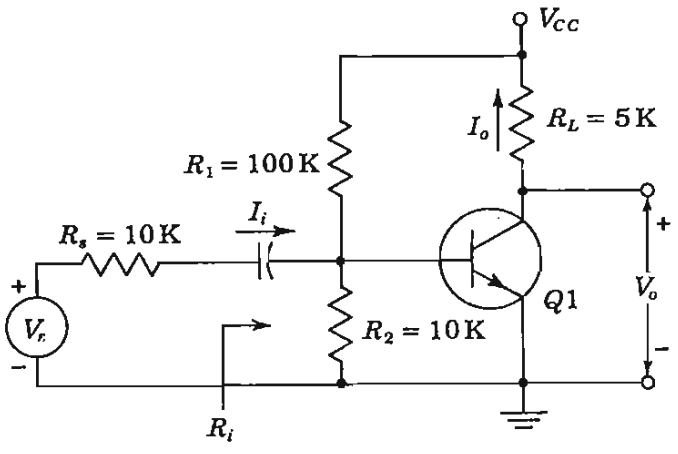
(*f*) $R_o = \dfrac{1}{h_o}$, if $R_s = \infty$.

8-20 Using the *h*-parameter values given in Table 8-2, calculate $(A_{Is})_{max}$, R_i, $(A_{Vs})_{max}$, and R_o derived in Prob. 8-19 (*a*) for a CE connection, (*b*) for a CB connection, (*c*) for a CC connection. Compare your answers with the values in Fig. 8-16.

8-21 Find the output impedance Z_o for the example in Sec. 8-6 by evaluating the current I_a drawn from an auxiliary voltage source V_a impressed across the output terminals (with zero input voltage and $R_L = \infty$). Then $Z_o = V_a/I_a$.

8-22 Find the voltage gain A_V for the example in Sec. 8-6 directly as the ratio V_o/V_i (without finding A_I or Z_i).

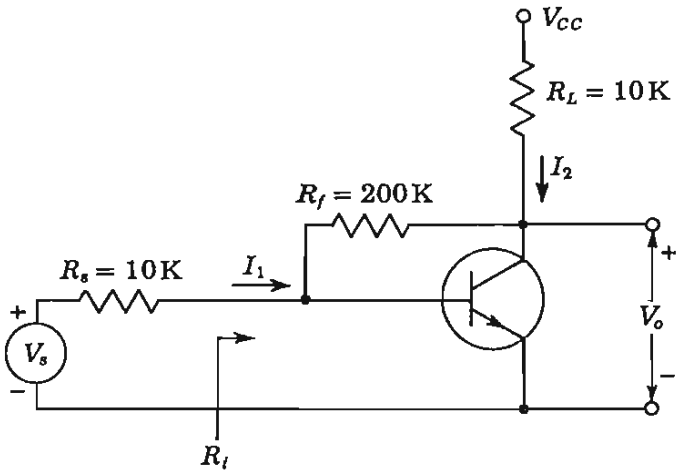
8-23 The transistor amplifier shown uses a transistor whose *h* parameters are given in Table 8-2. Calculate $A_I = I_o/I_i$, A_V, A_{Vs}, R_o, and R_i.



Prob. 8-23

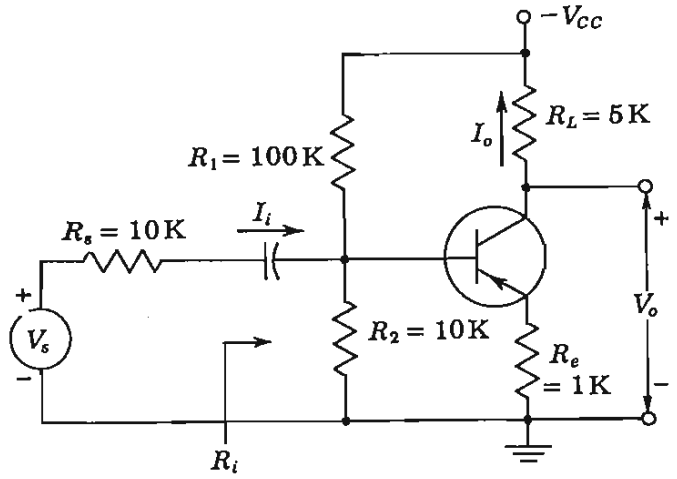
8-24 (*a*) In the circuit shown, find the input impedance R_i in terms of the CE h parameters, R_L and R_e. HINT: Follow the rules given in Sec. 8-10.
(*b*) If $R_L = R_e = 1$ K and the h parameters are as given in Table 8-2, what is the value of R_i?

Prob. 8-24



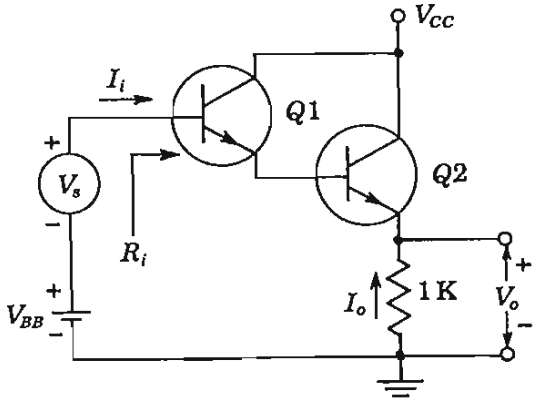
8-25 For the amplifier shown, using a transistor whose parameters are given in Table 8-2, compute $A_I = I_o/I_i$, A_V, A_{V_s}, and R_i. HINT: Follow the rules given in Sec. 8-10.

Prob. 8-25

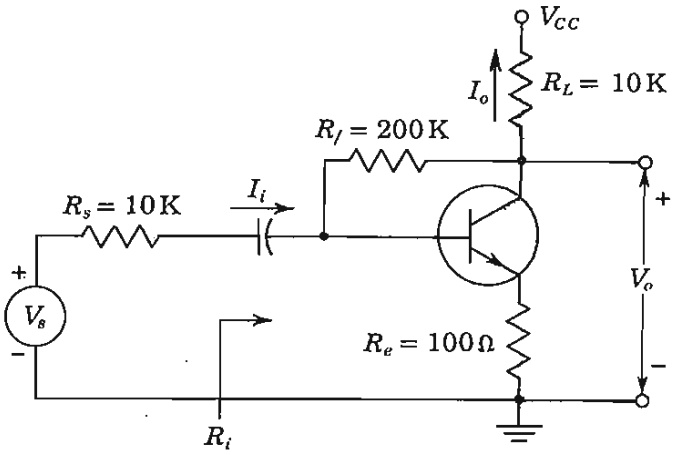


8-26 (*a*) Calculate R_i, A_V, and $A_I = -I_o/I_i$ for the circuit shown. Use the h-parameter values given in Table 8-2. HINT: Follow the rules given in Sec. 8-10.
(*b*) Repeat part *a* using the results in Prob. 8-10.

Prob. 8-26



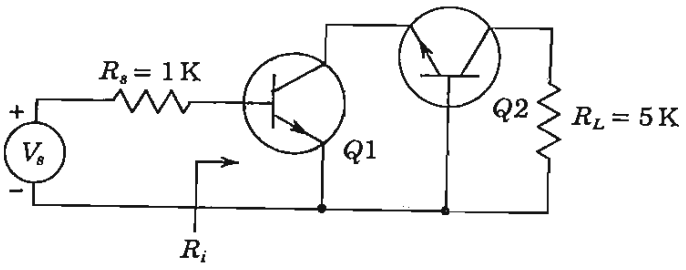
8-27 For the circuit shown, with the transistor parameters specified in Table 8-2, calculate $A_I = I_o / I_i$, A_V, A_{Vs}, and R_i. HINT: Follow the rules given in Sec. 8-10.



Prob. 8-27

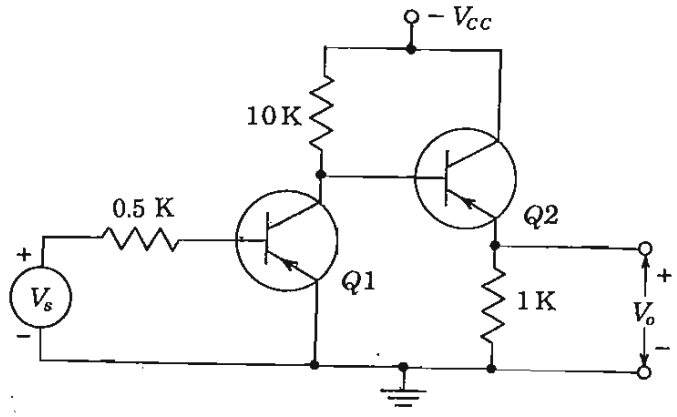
8-28 Repeat Prob. 8-24 by applying the dual of Miller's theorem.

8-29 (*a*) For the two-transistor amplifier circuit shown (supply voltages are not indicated) calculate A_I, A_V, A_{Vs}, and R_i. The transistors are identical, and their parameters are given in Table 8-2. HINT: Follow rules given in Sec. 8-10. (*b*) Repeat part *a* using the results given in Prob. 8-9.



Prob. 8-29

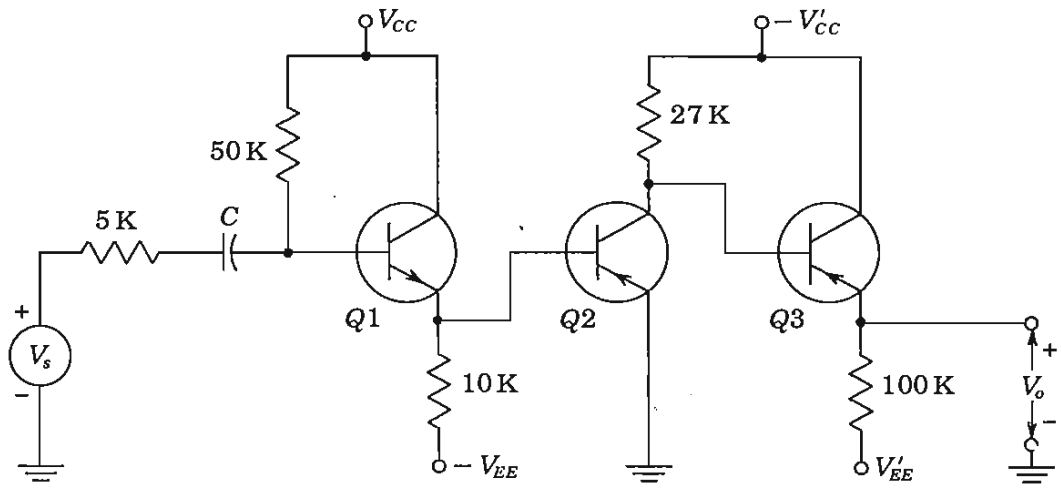
8-30 (*a*) Find the voltage gain A_{Vs} of the amplifier shown. Assume $h_{ie} = 1{,}000\ \Omega$, $h_{re} = 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 10^{-4}$ A/V. (*b*) Find R_o'.



Prob. 8-30

8-31 The three-stage amplifier shown contains identical transistors. Calculate the voltage gain of each stage and the overall voltage gain V_o/V_s. See note on page 809.

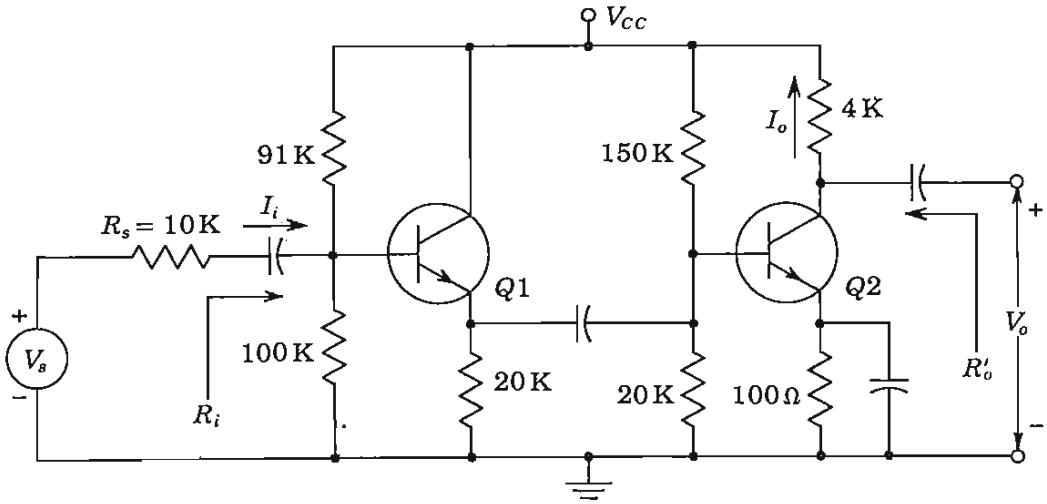
Prob. 8-31



8-32 (*a*) For the two-stage cascade shown, compute the input and output impedances and the individual and overall voltage and current gains, using the exact procedure of Sec. 8-12. See note on page 809.

(*b*) Repeat part *a* using the approximate formulas in Table 8-7.

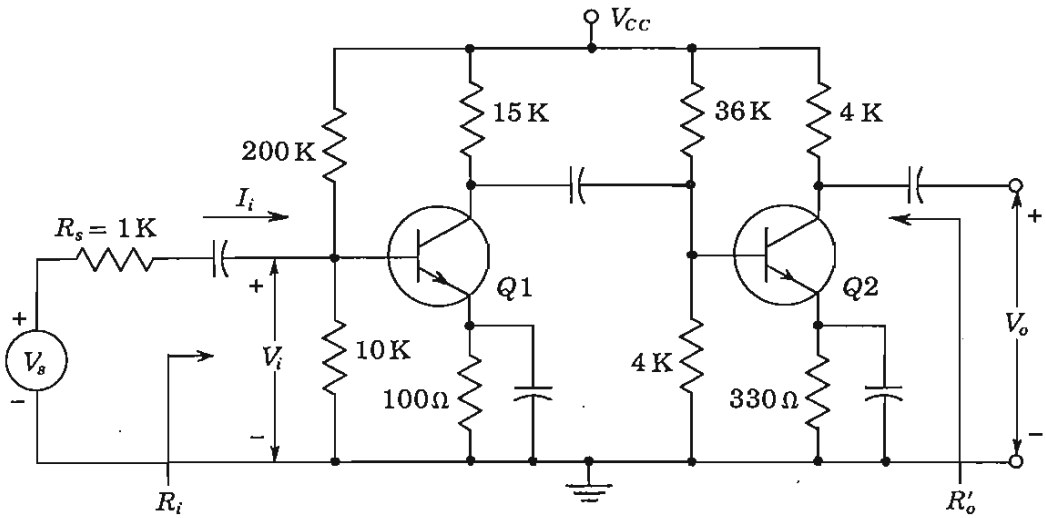
Prob. 8-32



8-33 (*a*) Compute A_I, A_V, A_{V_s}, R_i, and R'_o for the two-stage cascade shown, using the exact procedure of Sec. 8-12. See note on page 809.

(*b*) Repeat part *a* using the approximate formulas in Table 8-7.

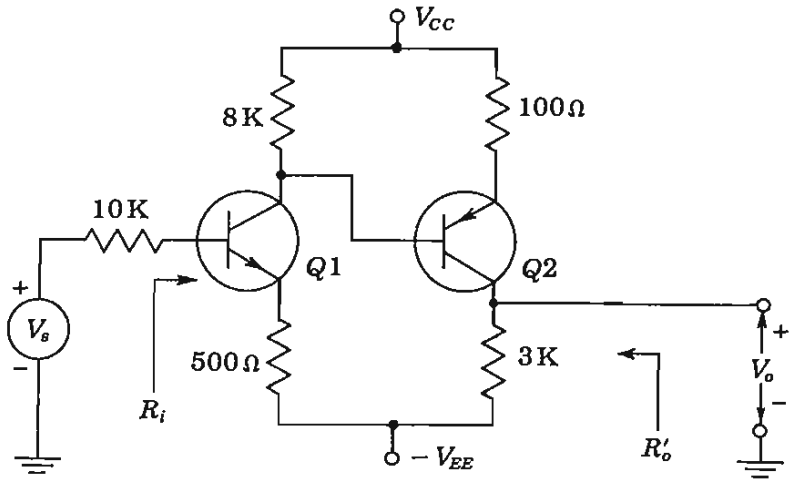
Prob. 8-33



8-34 For a CB connection derive the simplified expressions given in Table 8-7 and prove that they are in error by less than 10 percent from the exact formulas.

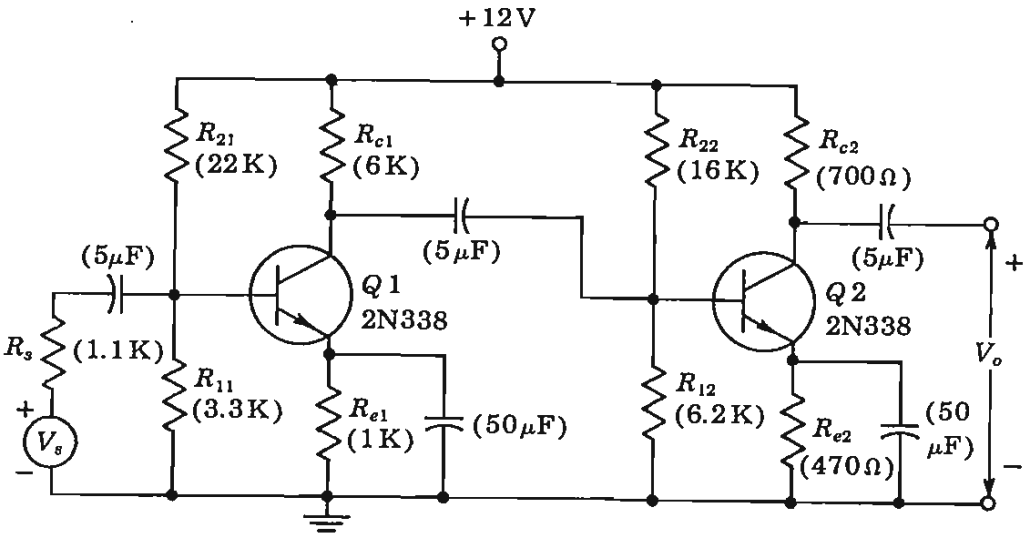
8-35 (*a*) Consider a CB connection with $R_s = 2$ K and $R_L = 4$ K. Find the exact and approximate values of A_I, A_V, A_{Vs}, R_i, and R_o'.
(*b*) Repeat part *a* for the CE connection.
(*c*) Repeat part *a* for the CC connection. See note on page 809.

8-36 For the circuit shown, compute A_I, A_V, A_{Vs}, R_i, and R_o'. See note on page 809.



Prob. 8-36

8-37 For the two-stage amplifier shown calculate A_V, A_{VS}, R_i, and R_o'. Neglect the effect of all capacitances. See note on page 809.



Prob. 8-37

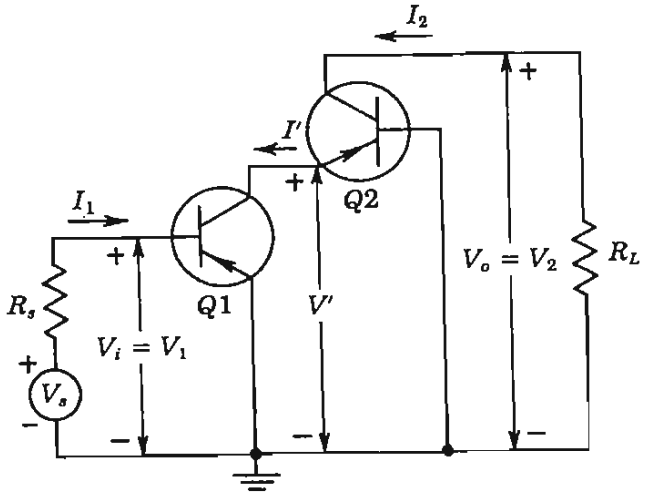
8-38 In the circuit of Prob. 8-27 change R_L to 4 K. Find A_V and A_{Vs} by using Miller's theorem.

8-39 The cascode transistor configuration consists of a CE stage $Q1$ in series with a CB stage $Q2$ (the collector current of $Q1$ equals the emitter current of $Q2$). Verify that the cascode combination acts like a single CE transistor with negli-

gible internal feedback and very small output conductance for an open-circuited input. In other words, verify that

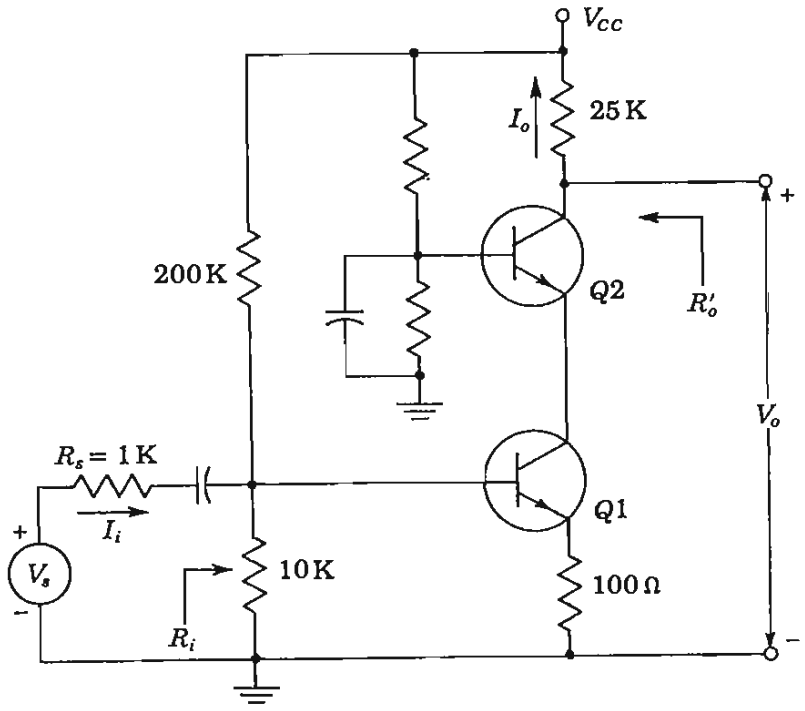
$$h_{11} \approx h_{ie} \qquad h_{21} \approx h_{fe} \qquad h_{22} \approx h_{ob} \qquad h_{12} \approx h_{re}h_{rb}$$

Prob. 8-39

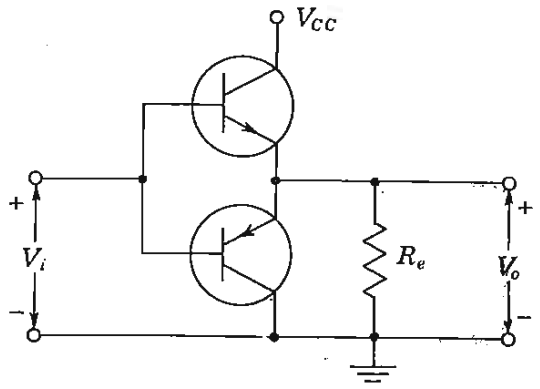


8-40 Calculate $A_I = I_o/I_i$, A_V, A_{Vs}, R_i, and R_o' for the cascode circuit shown. See note on page 809. HINT: Use results of Prob. 8-39.

Prob. 8-40

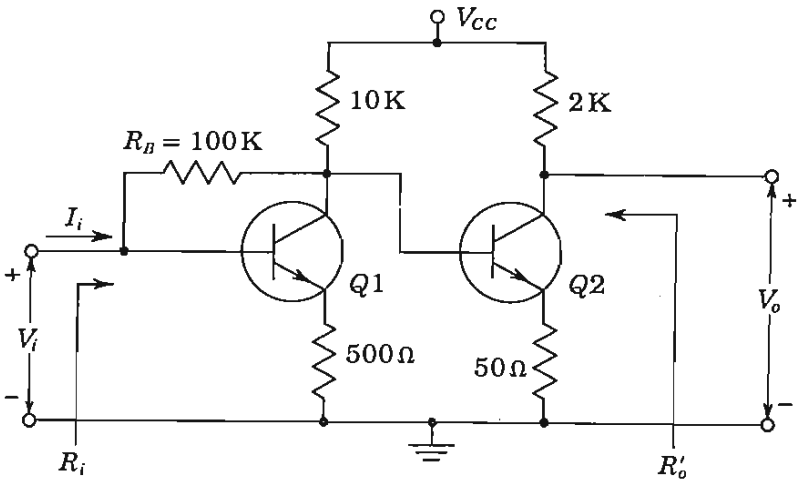


8-41 The circuit shown is an amplifier using a *p-n-p* and an *n-p-n* transistor in parallel. The two transistors have identical characteristics. Find the expression for the voltage gain and the input resistance of the amplifier, using the simplified hybrid model.



Prob. 8-41

8-42 For the two-stage cascade shown, find A_I, A_V, R_i, and R_o'. See note on page 809.

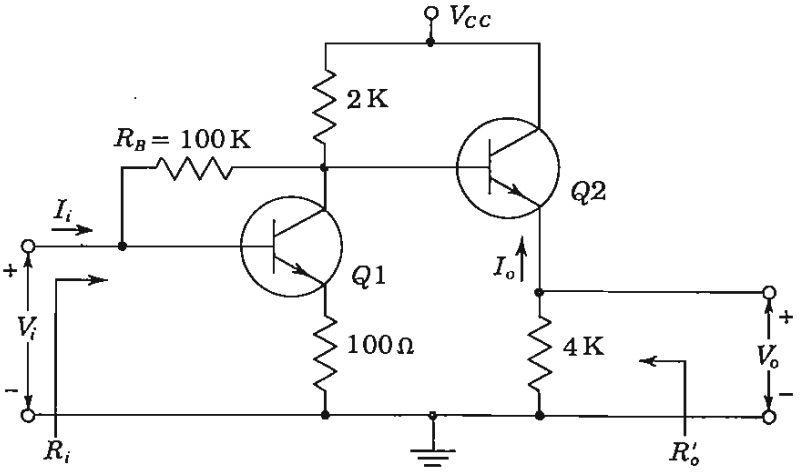


Prob. 8-42

8-43 Design a two-stage cascade using the configuration of Prob. 8-42, with R_B = 100 K, to meet the following specifications (see note on page 809):

$125 \geq A_V \geq 100$ $\quad$ $10\text{ K} \geq R_i \geq 5\text{ K}$ $\quad$ $R_o' \leq 3\text{ K}$

8-44 For the two-stage cascade shown, calculate A_I, A_V, R_i, and R_o'. See note on page 809.



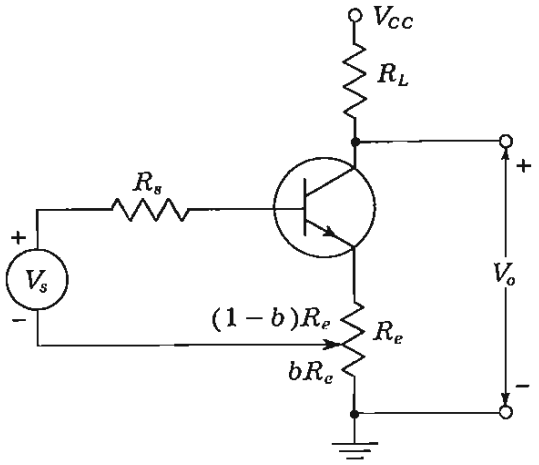
Prob. 8-44

8-45 Design a two-stage amplifier using the configuration of Prob. 8-44, with $R_B = 100$ K, to meet the following specifications (see note on page 809):

$$|A_V| \geq 15 \qquad R_i \geq 2 \text{ K} \qquad R_o' \leq 100\ \Omega$$

8-46 For the circuit shown, find the voltage gain V_o/V_s and input impedance as a function of R_s, b, R_e, and R_L. Assume that $h_{oe}(R_e + R_L) \leq 0.1$.

Prob. 8-46



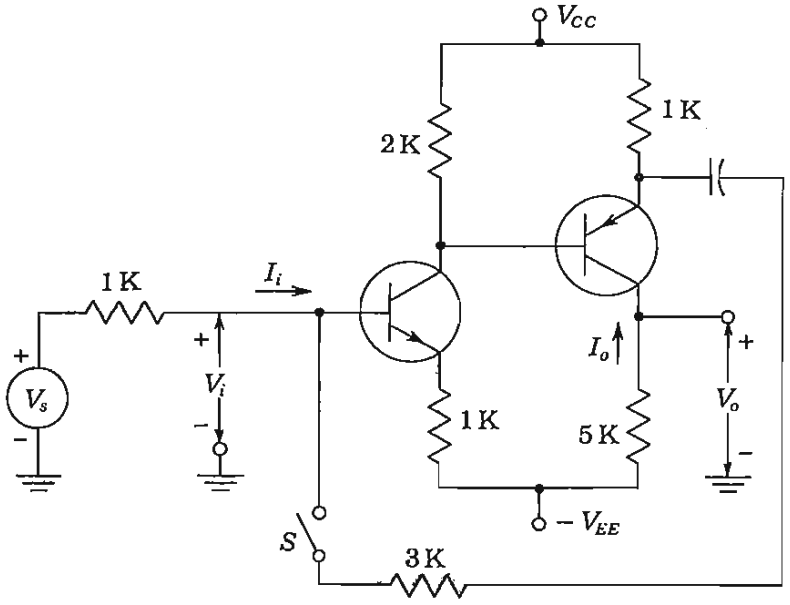
8-47 Using the exact expressions of Eq. (8-67) for A_I and Eq. (8-68) for R_i, calculate the output resistance R_o in Fig. 8-28*a* as the ratio of open-circuit voltage V to short-circuit current I. Verify that R_o is given by Eq. (8-70). HINT: Note that $V = \lim_{R_L \to \infty} A_V V_s$.

8-48 The amplifier shown is made up of an n-p-n and a p-n-p transistor. The h parameters of the two transistors are identical, and are given as $h_{ie} = 1$ K, $h_{fe} = 100$, $h_{oe} = 0$, and $h_{re} = 0$.

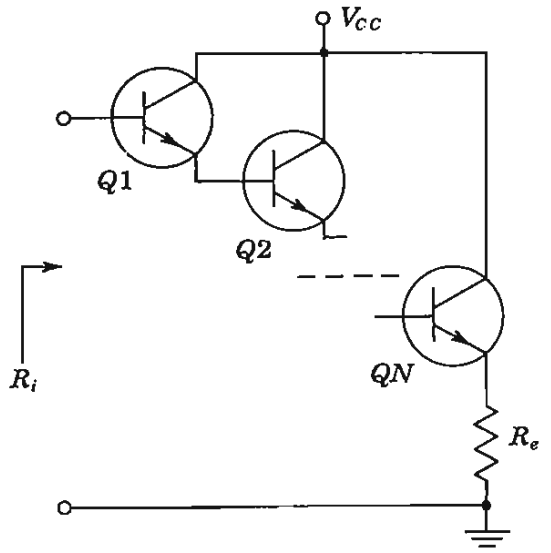
(*a*) With the switch open, find $A_V = V_o/V_i$.

(*b*) With the switch closed, find (with the aid of Miller's theorem) A_V, A_{Vs}, R_i, and $A_I \equiv -I_o/I_i$.

Prob. 8-48



8-49 The cascade configuration shown is known as the tandem emitter follower. Find the input resistance R_i if $h_{ie} = h_{re} = h_{oe} = 0$, and h_{fe} is the same for each of the transistors $Q1$ to QN.

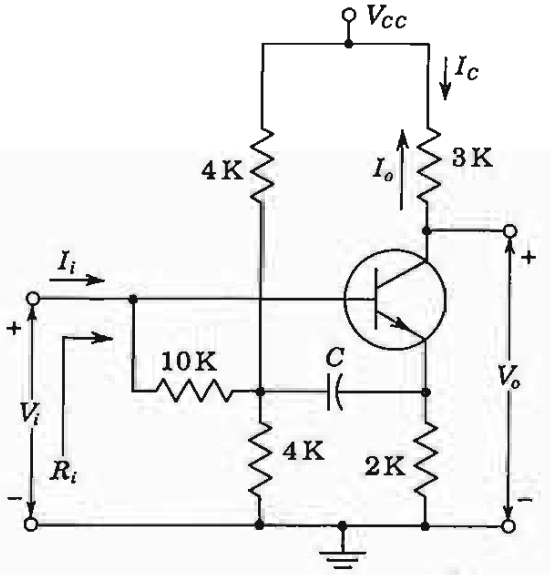


Prob. 8-49

8-50 (*a*) Verify Eq. (8-80) for the voltage gain of a Darlington emitter follower.
(*b*) Verify Eq. (8-81) for the output resistance.

8-51 Verify Eq. (8-84).

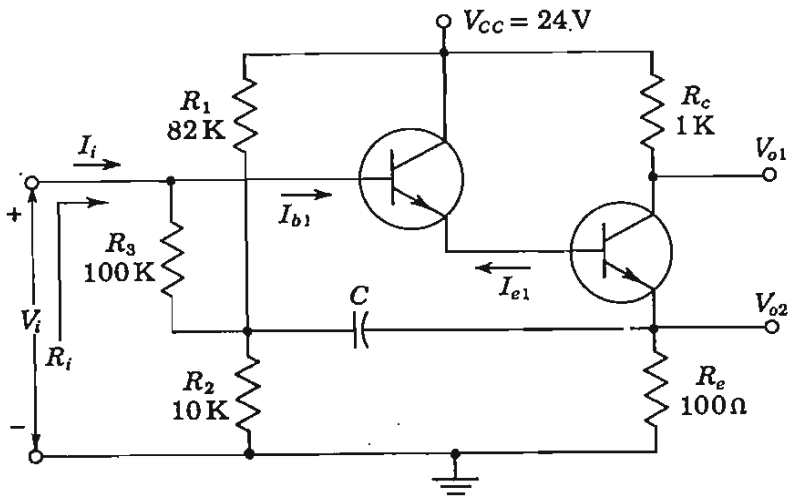
8-52 For the bootstrap circuit shown, calculate $A_I \equiv I_o/I_i$, R_i, and A_V. The transistor parameters are $h_{ie} = 2$ K, $h_{fe} = 100$, $1/h_{oe} = 40$ K, and $h_{re} = 2.5 \times 10^{-4}$.



Prob. 8-52

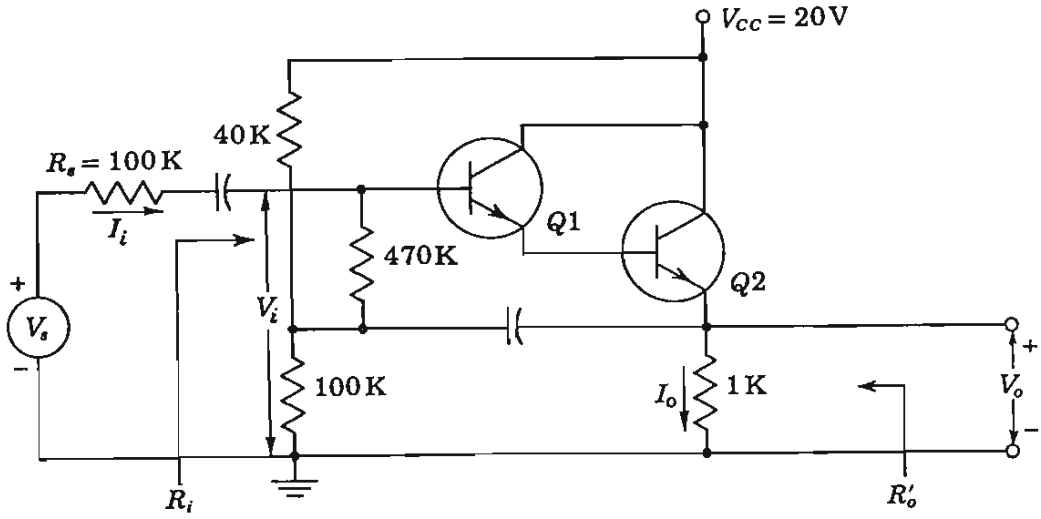
8-53 The bootstrapped Darlington pair uses identical transistors with the following h parameters; $h_{ie} = 1$ K, $h_{re} = 2.5 \times 10^{-4}$, $h_{oe} = 2.5 \times 10^{-5}$ A, V, and $h_{fe} = 100$. Find I_{e1}/I_{b1}, V_{o2}/V_i, R_i, and V_{o1}/V_i.

Prob. 8-53



8-54 Calculate A_I, A_V, R_i, and R_o' for the circuit shown. See note on page 809.

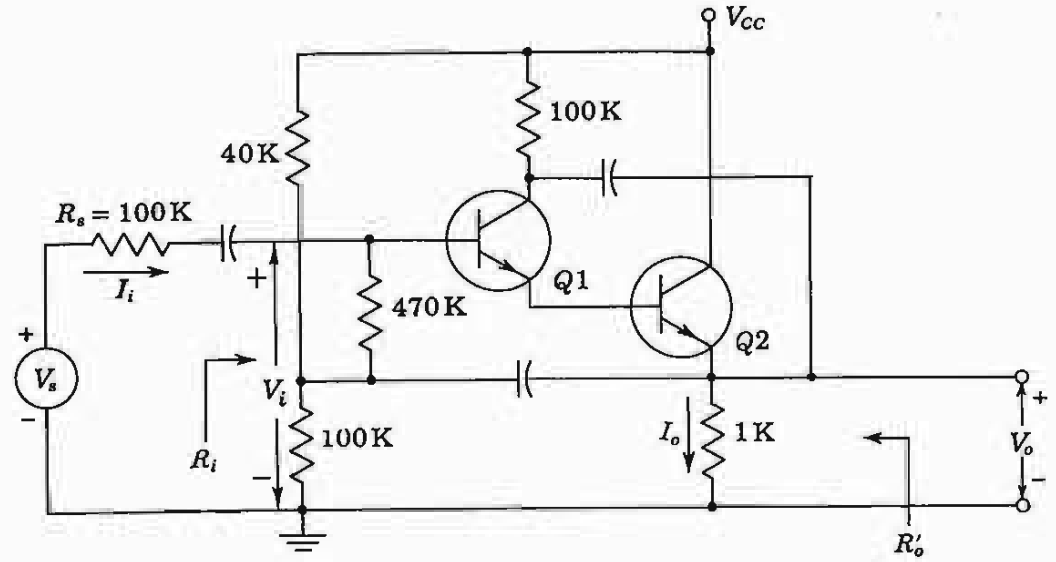
Prob. 8-54



8-55 Calculate R_i and A_V for the circuit shown in Fig. 8-32, with $R_{c1} = 100$ K and $R_{e2} = 1$ K.

8-56 For the circuit shown, find A_V, A_{Vs}, $A_I = I_o/I_i$, R_i, and R_o'. See note on page 809.

Prob. 8-56



CHAPTER 9

9-1 (*a*) Determine the quiescent currents and the collector-to-emitter voltage for a silicon transistor with $\beta = 50$ in the self-biasing arrangement of Fig. 9-5. The circuit component values are $V_{CC} = 20$ V, $R_c = 2$ K, $R_e = 0.1$ K, $R_1 = 100$ K, and $R_2 = 5$ K.

(*b*) Repeat (*a*) for a germanium transistor.

9-2 A *p-n-p* germanium transistor is used in the self-biasing arrangement of Fig. 9-5. The circuit component values are $V_{CC} = 4.5$ V, $R_c = 1.5$ K, $R_e = 0.27$ K, $R_2 = 2.7$ K, and $R_1 = 27$ K. If $\beta = 44$

(*a*) Find the quiescent point.

(*b*) Recalculate these values if the base-spreading resistance of 690 Ω is taken into account.

9-3 A *p-n-p* silicon transistor is used in a common-collector circuit (Fig. 9-5 with $R_c = 0$). The circuit component values are $V_{CC} = 3.0$ V, $R_e = 1$ K, $R_1 = R_2 = 5$ K. If $\beta = 44$

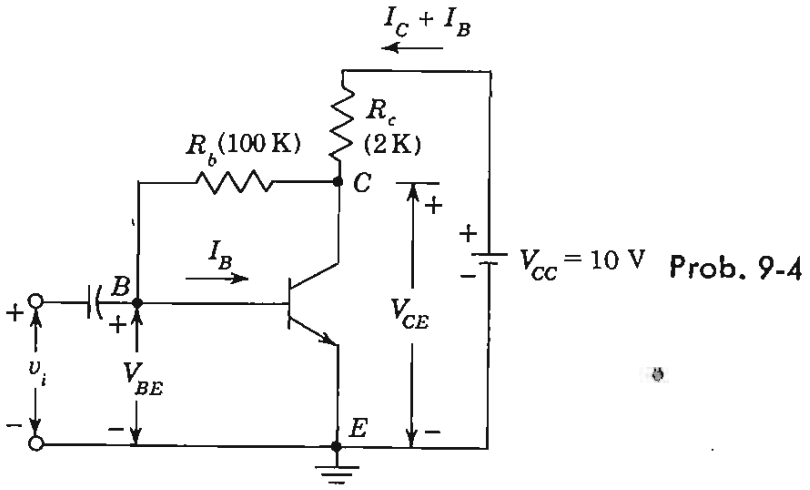
(*a*) Find the quiescent point.

(*b*) Recalculate these values, taking the base-spreading resistance of 690 Ω into account.

9-4 For the circuit shown

(*a*) Calculate I_B, I_C, and V_{CE} if a silicon transistor is used with $\beta = 50$.

(*b*) Specify a value for R_b so that $V_{CE} = 7$ V.



Prob. 9-4

9-5 (*a*) Verify Eq. (9-13).

(*b*) Show that S may be put in the form

$$S = \frac{G_e + G_1 + G_2}{G_e/(1 + \beta) + G_1 + G_2}$$

where the G's are the conductances corresponding to the R's shown in Fig. 9-5*a*.

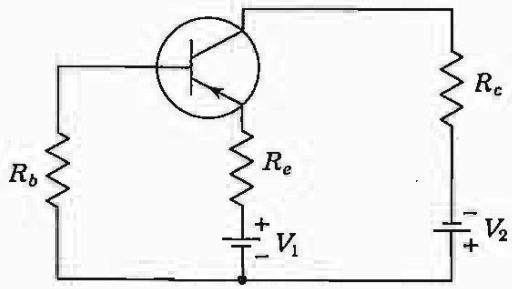
(*c*) Show that for the circuit of Prob. 9-4, S is given by

$$S = \frac{\beta + 1}{1 + \beta R_c/(R_c + R_b)}$$

9-6 (*a*) Find the stability factor S for the circuit of Prob. 9-1.
(*b*) Repeat (*a*) for the circuit of Prob. 9-2.
(*c*) Repeat (*a*) for the circuit of Prob. 9-3.

9-7 For the two-battery transistor circuit shown, prove that the stabilization factor S is given by

$$S = \frac{1 + \beta}{1 + \beta R_b'/(R_e + R_b)}$$

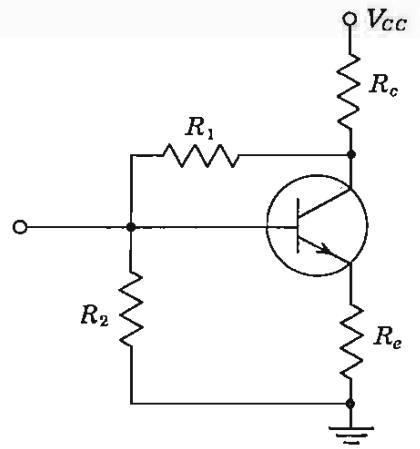


Prob. 9-7

9-8 Assume that a silicon transistor with $\beta = 50$, $V_{BE,\text{active}} = 0.7$, $V_{CC} = 22.5$ V, and $R_c = 5.6$ K is used in Fig. 9-5*a*. It is desired to establish a Q point at $V_{CE} = 12$ V, $I_C = 1.5$ mA, and stability factor $S \leq 3$. Find R_e, R_1, and R_2.

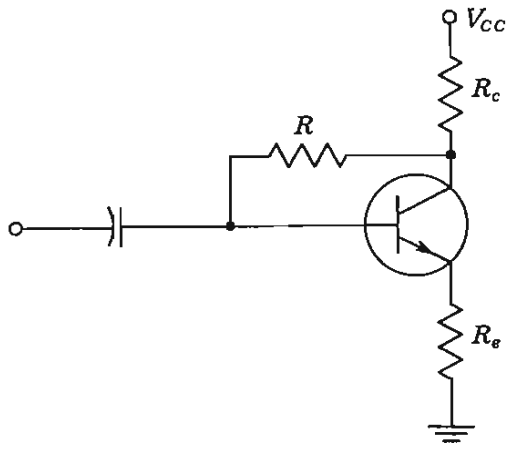
9-9 (*a*) A germanium transistor is used in the self-biasing arrangement of Fig. 9-5 with $V_{CC} = 16$ V and $R_c = 1.5$ K. The quiescent point is chosen to be $V_{CE} = 8$ V and $I_C = 4$ mA. A stability factor $S = 12$ is desired. If $\beta = 50$, find R_1, R_2, and R_e.
(*b*) Repeat part *a* for $S = 3$.

9-10 Determine the stability factor S for the circuit shown.



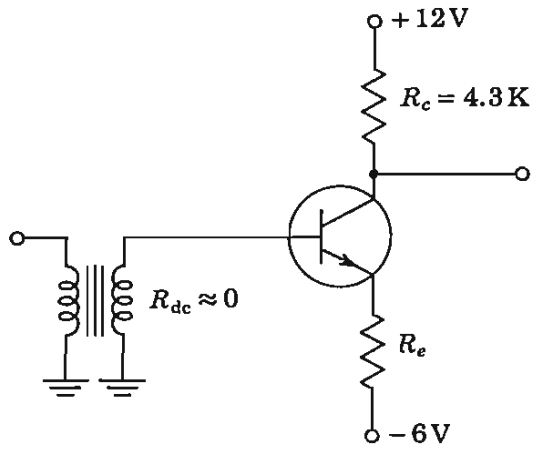
Prob. 9-10

9-11 In the circuit shown, $V_{CC} = 24$ V, $R_c = 10$ K, and $R_e = 270$ Ω. If a silicon transistor is used with $\beta = 45$ and if under quiescent conditions $V_{CE} = 5$ V, determine (*a*) R, (*b*) the stability factor S.



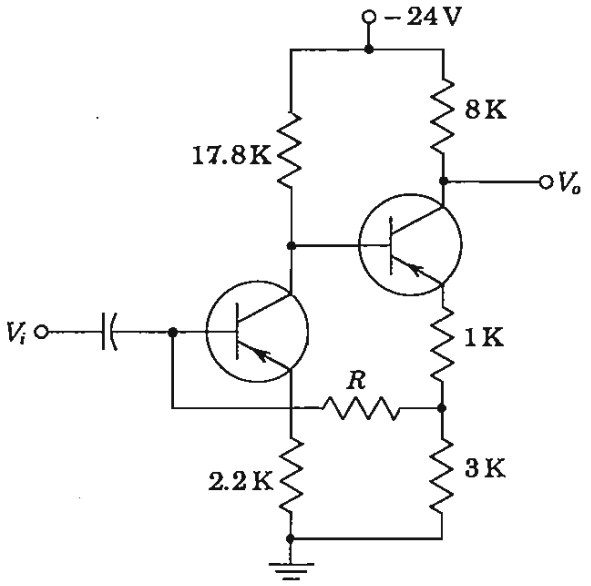
Prob. 9-11

9-12 In the transformer-coupled amplifier stage shown, $V_{BE} = 0.7$ V, $\beta = 50$, and the quiescent voltage is $V_{CE} = 4$ V. Determine (*a*) R_c, (*b*) the stability factor S.



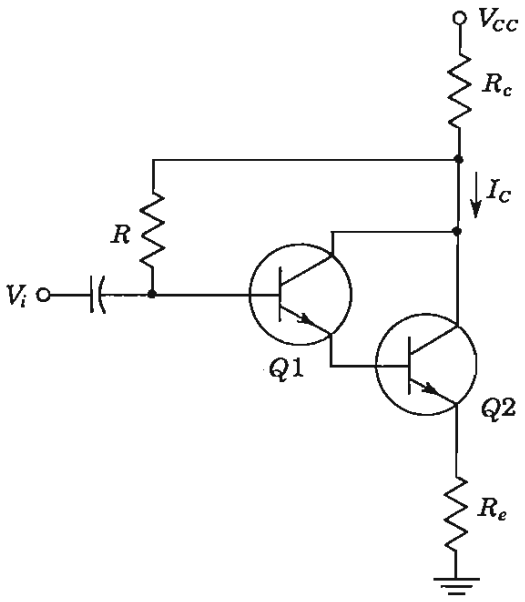
Prob. 9-12

9-13 In the two-stage circuit shown, assume $\beta = 100$ for each transistor.
(*a*) Determine R so that the quiescent conditions are $V_{CE1} = -4$ V and $V_{CE2} = -6$ V.
(*b*) Explain how quiescent-point stabilization is obtained. Assume $V_{BE} = 0.2$ V.



Prob. 9-13

9-14 In the Darlington stage shown, $V_{CC} = 24$ V, $\beta_1 = 24$, $\beta_2 = 39$, $V_{BE} = 0.7$, $R_c = 330\ \Omega$, and $R_e = 120\ \Omega$. If at the quiescent point $V_{CE2} = 6$ V, determine (*a*) R, (*b*) the stability factor defined as $S \equiv dI_C/dI_{CO1}$.



Prob. 9-14

9-15 (*a*) Prove that for the circuit of Fig. 9-5*b* the stability factor S' is given by

$$S' = \frac{-S}{R_b + R_e} \times \frac{\beta}{\beta + 1}$$

(*b*) Derive Eq. (9-22).

9-16 For the bias arrangement given in Prob. 9-4 prove that

$$S' = \frac{-\beta S}{1 + \beta} \times \frac{1}{R_c + R_b}$$

$$S'' = \frac{I_C}{\beta} \times \frac{S}{\beta + 1}$$

where S is the stabilization factor of this circuit.

9-17 If in Eq. (9-11) we do not assume $\beta \gg 1$ so that V' is now a function of β, verify that Eq. (9-22) is given by

$$S'' = \frac{(I_C - I_{CO})S}{\beta(1 + \beta)}$$

9-18 If in Eq. (9-11) we do not assume $\beta \gg 1$, so that V' is now a function of β, verify that Eq. (9-27) is given by

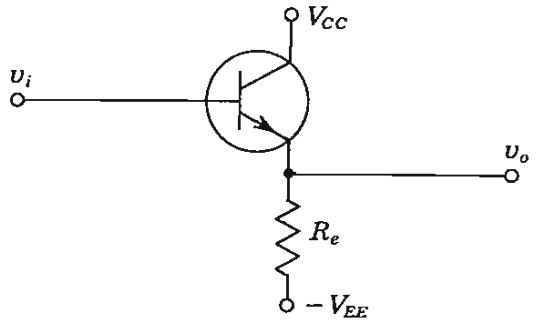
$$S'' = \frac{(I_{C1} - I_{CO1})S_2}{(\beta_1)(1 + \beta_2)}$$

HINT: Write the expression for $(I_{C2} - I_{CO2})'(I_{C1} - I_{CO1})$ and then subtract unity from both sides of the equation.

9-19 In the circuit of Fig. 9-5, let $R_c = 5.6$ K, $R_e = 1$ K, $R_1 = 90$ K, $R_2 = 10$ K, $I_C = 1.5$ mA at 25°C. Using the transistor of Table 9-1, find I_C at +175 and −65°C.

9-20 Repeat Prob. 9-19 for the transistor of Table 9-2 at +75 and −65°C.

9-21 In the emitter-follower circuit shown, $R_e = 1$ K and V_{CC} and V_{EE} are adjusted to give $I_C = 1.5$ mA at 25°C. Using the transistor of Table 9-1, find I_C at +175 and −65°C. Compare the results with those of Prob. 9-19.



Prob. 9-21

9-22 Repeat Prob. 9-21 for the transistor of Table 9-2 at +75 and −65°C. Compare these results with those of Prob. 9-20.

9-23 For the self-bias circuit of Fig. 9-5*a*, $R_e = 1$ K and $R_b = R_1 \| R_2 = 7.75$ K. The collector supply voltage and R_c are adjusted to establish a collector current of 1.5 mA at 25°C. Determine the variation of I_C in the temperature range −65 to +175°C when the silicon transistor of Table 9-1 is used.

9-24 Repeat Prob. 9-23 for the range −65 to +75°C when the germanium transistor of Table 9-2 is used.

9-25 Design the emitter-follower circuit shown in Prob. 9-21 using the silicon transistor type 2N3565 to meet the specifications of the illustrative example on page 298.

9-26 Two identical silicon transistors with $\beta = 48$, $V_{BE} = 0.7$ V at $T = 25$°C, $V_{CC} = 20.7$ V, $R_1 = 10$ K, and $R_c = 5$ K are used in Fig. 9-11*a*.
(*a*) Find the currents I_{B1}, I_{B2}, I_{C1}, and I_{C2} at $T = 25$°C.
(*b*) Find I_{C2} at $T = 175$°C when $\beta = 98$ and $V_{BE} = 0.3$ V. HINT: Assume $I_{B1} = I_{B2}$.

9-27 For the biasing arrangement of Fig. 9-10 and assuming that the reverse saturation currents of the diode and the transistor are equal, prove that

$$S = 1$$

$$S' = -\frac{\beta}{R_1}$$

$$S'' = \frac{\Delta(I_C - I_{CO})}{\Delta\beta} = \frac{I_{C1} - I_{CO1}}{\beta_1}$$

9-28 (*a*) For the self-bias circuit of Fig. 9-9, the operating point is $I_C = 1.5$ mA at 25°C, $R_e = 1$ K, $R_b = 7.75$ K, $V_{DD} = 15$ V, and $V_{D,ON} = 0.7$ V, find the maximum value of R_d for proper operation.

(*b*) For the circuit of part *a* determine the variation of I_C in the temperature range −65 for 175°C when the silicon transistor of Table 9-1 is used.

9-29 Prove Eq. (9-38).

9-30 (*a*) The circuit of Prob. 9-19 is modified by the addition of a thermistor as in Fig. 9-12. Find R_T, I_T, and V_{CE} for the modified circuit if $I_C = 1.5$ mA and $V_{CC} = 27.5$ V.
(*b*) It is desired that as the temperature changes from 25 to 175°, the variation of I_C be +0.4 mA. Calculate the temperature coefficient of the thermistor.

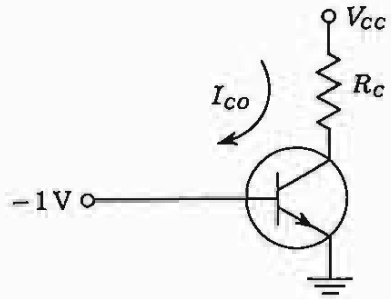
9-31 (*a*) Calculate the thermal resistance for the 2N338 transistor for which the manufacturer specifies $P_{C,\max} = 125$ mW at 25°C free-air temperature and maximum junction temperature $T_j = 150$°C.
(*b*) What is the junction temperature if the collector dissipation is 75 mW?

9-32 Show that the load line tangent to the constant-power-dissipation hyperbola of Fig. 9-14 is bisected by the tangency point, that is, $AC = BC$.

9-33 The transistor used in the circuit is at cutoff.
(*a*) Show that runaway will occur for values of I_{CO} in the range

$$\frac{V_{CC} - \sqrt{V_{CC}^2 - 8R_c/0.07\Theta}}{4R_c} \leq I_{CO} \leq \frac{V_{CC} + \sqrt{V_{CC}^2 - 8R_c/0.07\Theta}}{4R_c}$$

(*b*) Show that if runaway is not destructive, the collector current I_{CO} after runaway can never exceed $I_{CO} = V_{CC}/2R_c$.



Prob. 9-33

9-34 A germanium transistor with $\Theta = 250$°C/W, $I_{CO} = 10$ μA at 25°C, $R_c = 1$ K, and $V_{CC} = 30$ V is used in the circuit of Prob. 9-33.
(*a*) Find I_{CO} at the point of runaway.
(*b*) Find the ambient temperature at which runaway will occur.

CHAPTER 10

10-1 The drain resistance R_d of an *n*-channel FET with the source grounded is 2 K. The FET is operating at a quiescent point $V_{DS} = 10$ V, and $I_{DS} = 3$ mA, and its characteristics are given in Fig. 10-3.
(*a*) To what value must the gate voltage be changed if the drain current is to change to 5 mA?

(*b*) To what value must the drain voltage be changed if the drain current is to be brought back to its previous value? The gate voltage is maintained constant at the value found in part *a*.

10-2 For a *p*-channel silicon FET with $a = 2 \times 10^{-4}$ cm and channel resistivity $\rho = 10\ \Omega$-cm
(*a*) Find the pinch-off voltage.
(*b*) Repeat (*a*) for a *p*-channel germanium FET with $\rho = 2\ \Omega$-cm.

10-3 (*a*) Plot the transfer characteristic curve of an FET as given by Eq. (10-8), with $I_{DSS} = 10$ mA and $V_P = -4$ V.
(*b*) The magnitude of the slope of this curve at $V_{GS} = 0$ is g_{mo} and is given by Eq. (10-17). If the slope is extended as a tangent, show that it intersects the V_{GS} axis at the point $V_{GS} = V_P/2$.

10-4 (*a*) Show that the transconductance g_m of a JFET is related to the drain current I_{DS} by

$$g_m = \frac{2}{|V_P|}\sqrt{I_{DSS}I_{DS}}$$

(*b*) If $V_P = -4$ V and $I_{DSS} = 4$ mA, plot g_m versus I_{DS}.

10-5 Show that for small values of V_{GS} compared with V_P, the drain current is given approximately by $I_D \approx I_{DSS} + g_{mo}V_{GS}$.

10-6 (*a*) For the FET whose characteristics are plotted in Fig. 10-3, determine r_d and g_m graphically at the quiescent point $V_{DS} = 10$ V and $V_{GS} = -1.5$ V. Also evaluate μ.
(*b*) Determine $r_{d,\text{ON}}$ for $V_{GS} = 0$.

10-7 (*a*) Verify Eq. (10-15).
(*b*) Starting with the definitions of g_m and r_d, show that if two identical FETs are connected in parallel, g_m is doubled and r_d is halved. Since $\mu = r_d g_m$, then μ remains unchanged.
(*c*) If the two FETs are not identical, show that

$$\frac{1}{r_d} = \frac{1}{r_{d1}} + \frac{1}{r_{d2}}$$

and that

$$\mu = \frac{\mu_1 r_{d2} + \mu_2 r_{d1}}{r_{d1} + r_{d2}}$$

10-8 Given the transfer characteristic of an FET, explain clearly how to determine g_m at a specified quiescent point.

10-9 (*a*) Using Eq. (10-18), prove that the load conductance of a MOSFET is given by

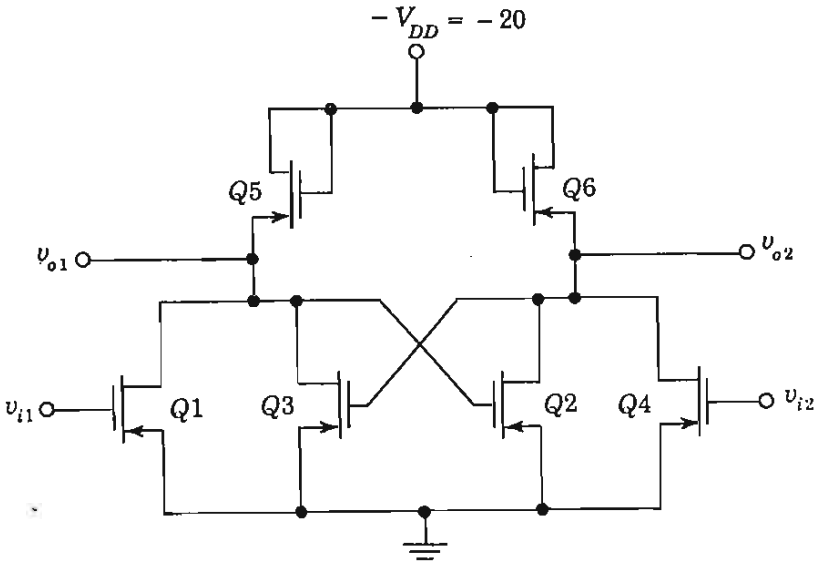
$$g_L = g_{do}\left(1 - \frac{V_{DS}}{V_T}\right) \qquad \text{where } g_{do} = \frac{2I_{DSS}}{|V_T|}$$

(*b*) Prove that $g_L = g_m$ for a JFET. HINT: Use Eq. (10-8).

10-10 Draw the circuit of a MOSFET negative AND gate and explain its operation.

10-11 Consider the FLIP-FLOP circuit shown. Assume $V_T = V_{ON} = 0$ and $|V_{DD}| \gg V_T$.
(*a*) Assume $v_{i1} = v_{i2} = 0$. Verify that the circuit has two possible stable states; either $v_{o1} = 0$ and $v_{o2} = -V_{DD}$ or $v_{o1} = -V_{DD}$ and $v_{o2} = 0$.
(*b*) Show that the state of the FLIP-FLOP may be changed by momentarily allowing one of the inputs to go to $-V_{DD}$; in other words by applying a negative input pulse.

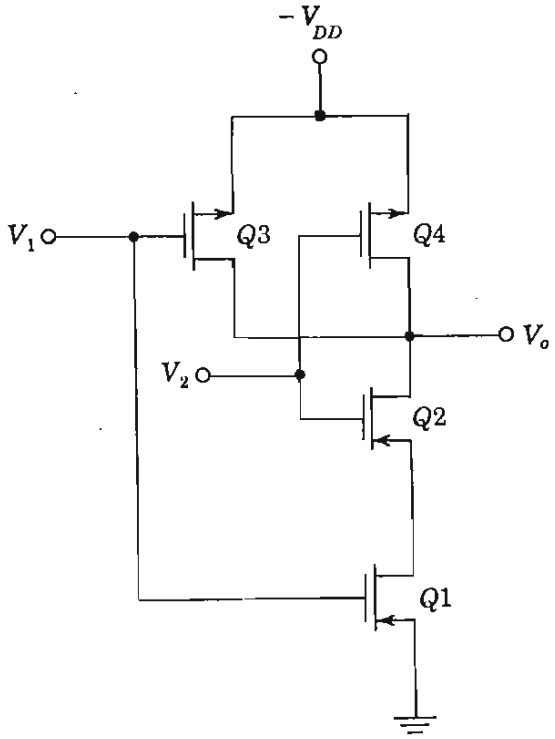
Prob. 10-11



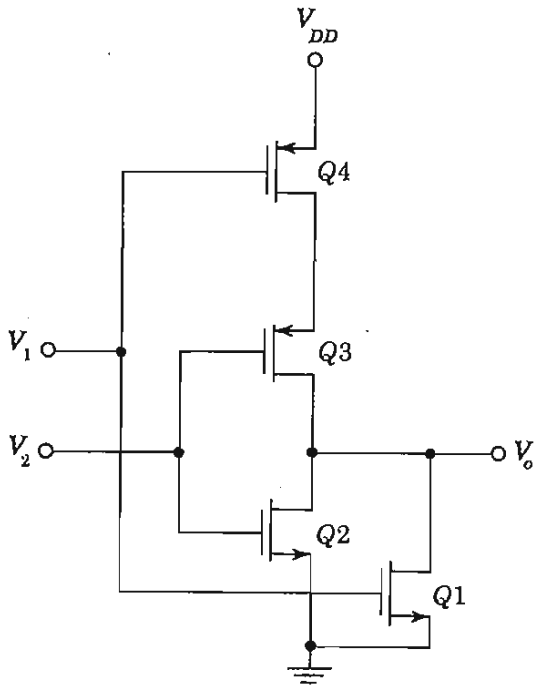
10-12 Draw a CMOS inverter using positive logic.

10-13 (*a*) The complementary MOS negative NAND gate is indicated. Explain its operation.
(*b*) Draw the corresponding positive NAND gate.

Prob. 10-13



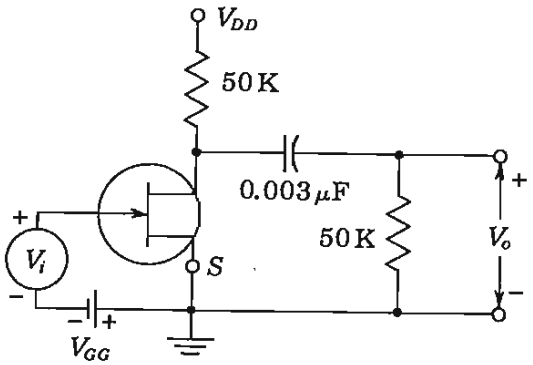
10-14 The circuit of a CMOS positive NOR gate is indicated. Explain its operation.



Prob. 10-14

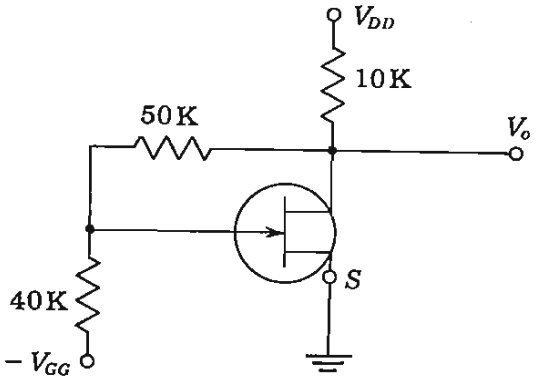
10-15 Draw a MOSFET circuit satisfying the logic equation. $Y = \overline{A + BC}$, where Y is the output corresponding to the three inputs A, B, and C.

10-16 (*a*) Calculate the voltage gain $A_V = V_o/V_i$ at 1 kHz for the circuit shown. The FET parameters are $g_m = 2$ mA/V and $r_d = 10$ K. Neglect capacitances. (*b*) Repeat part *a* if the capacitance 0.003 μF is taken under consideration.



Prob. 10-16

10-17 If an input signal V_i is impressed between gate and ground, find the amplification $A_V = V_o/V_i$. Apply Miller's theorem to the 50-K resistor. The FET parameters are $\mu = 30$ and $r_d = 5$ K. Neglect capacitances.

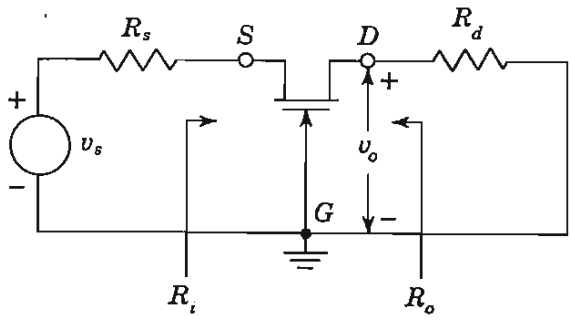


Prob. 10-17

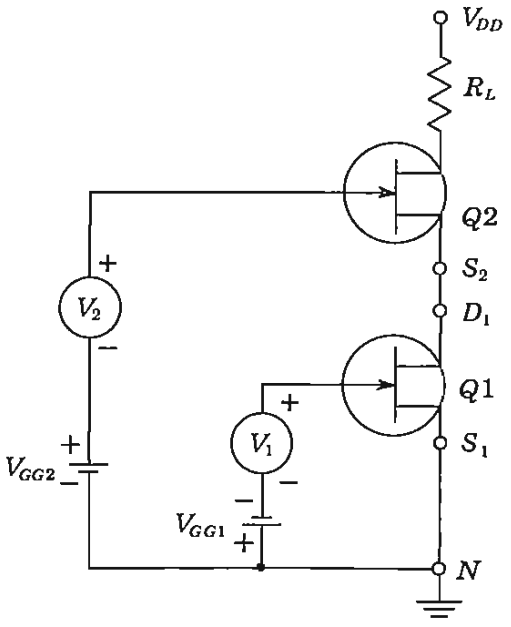
10-18 If in Prob. 10-17 the signal V_i is impressed in series with the 40-K resistor (instead of from gate to ground), find $A_V = V_o/V_i$.

10-19 The circuit shown is called common-gate amplifier. For this circuit find (*a*) the voltage gain, (*b*) the input impedance, (*c*) the output impedance. Power supplies are omitted for simplicity. Neglect capacitances.

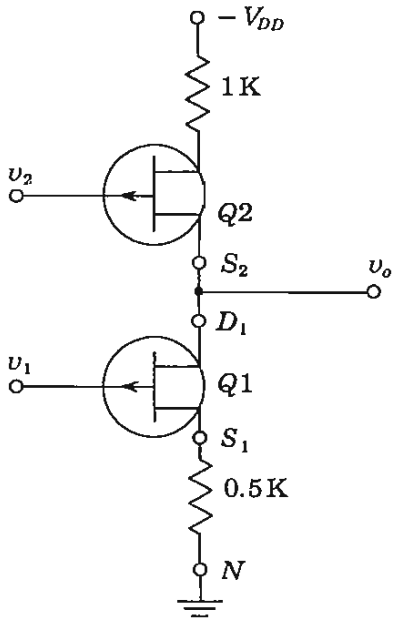
Prob. 10-19



10-20 Find an expression for the signal voltage across R_L. The two FETs are identical, with parameters μ, r_d, and g_m. HINT: Use the equivalent circuits in Fig. 10-22 at S_2 and D_1.



Prob. 10-20



Prob. 10-21

10-21 Each FET shown has the parameters r_d = 10 K and g_m = 2 mA/V. Using the equivalent circuits in Fig. 10-22 at S_2 and D_1, find the gain (*a*) v_o/v_1 if $v_2 = 0$, (*b*) v_o/v_2 if $v_1 = 0$.

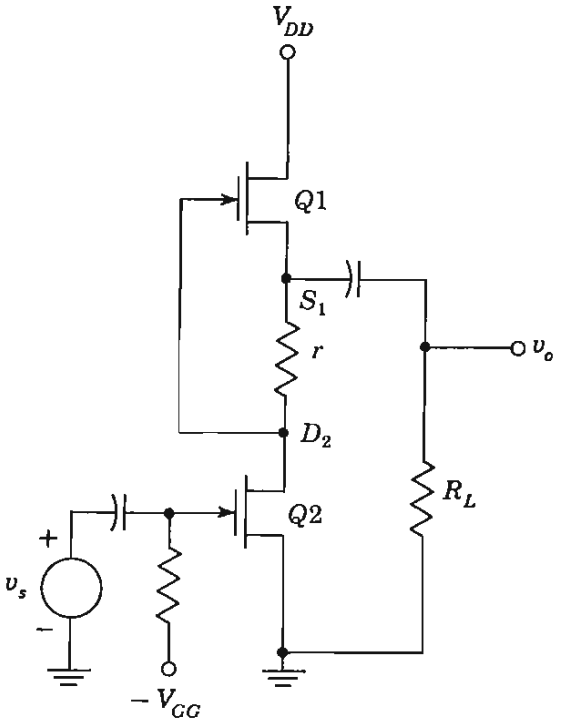
10-22 (*a*) Prove that the magnitude of the signal current is the same in both FETs provided that

$$r = \frac{1}{g_m} + \frac{2R_L}{\mu}$$

Neglect the reactance of the capacitors.

(*b*) If r is chosen as in part *a*, prove that the voltage gain is given by

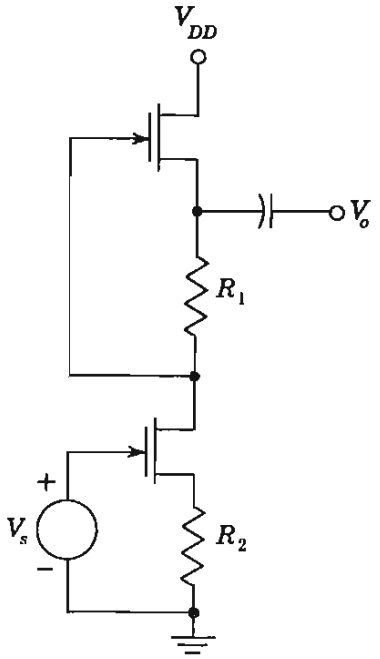
$$A = \frac{-\mu^2}{\mu + 1} \frac{R_L}{R_L + r_d/2}$$



Prob. 10-22

10-23 (*a*) If $R_1 = R_2 = R$ and the two FETs have identical parameters, verify that the voltage amplification is $V_o/V_s = -\mu/2$ and the output impedance is $\frac{1}{2}[r_d + (\mu + 1)R]$.

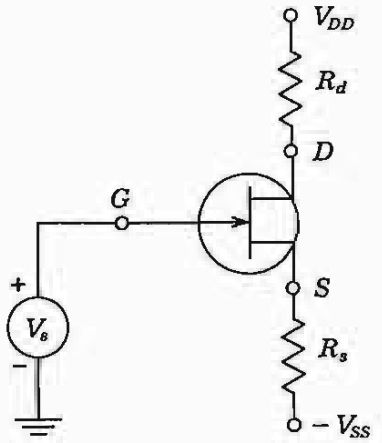
(*b*) Given $r_d = 62$ K, $\mu = 10$, $R_1 = 2$ K, and $R_2 = 1$ K. Find the voltage gain and the output impedance.



Prob. 10-23

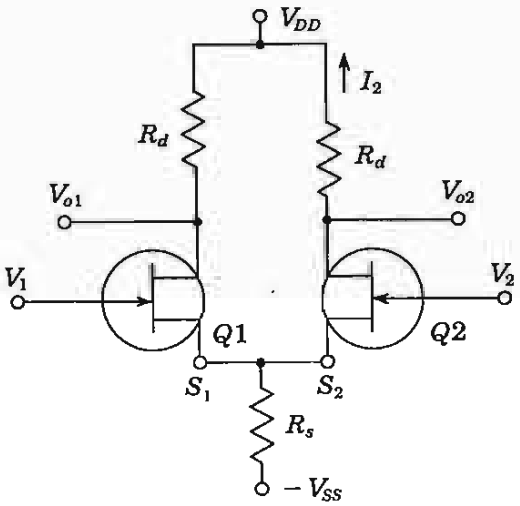
10-24 (*a*) If in the amplifier stage shown the positive supply voltage V_{DD} changes by $\Delta V_{DD} = v_a$, how much does the drain-to-ground voltage change?
(*b*) How much does the source-to-ground voltage change under the conditions in part *a*?
(*c*) Repeat parts *a* and *b* if V_{DD} is constant but V_{SS} changes by $\Delta V_{SS} = v_s$.

Prob. 10-24



10-25 If in the circuit shown $V_2 = 0$, then this circuit becomes a source-coupled phase inverter, since $V_{o1} = -V_{o2}$. Solve for the current I_2 by drawing the equivalent circuit, looking into the source of $Q1$ (Fig. 10-22). Then replace $Q2$ by the equivalent circuit, looking into its drain. The source resistance R_s may be taken as arbitrarily large.

Prob. 10-25

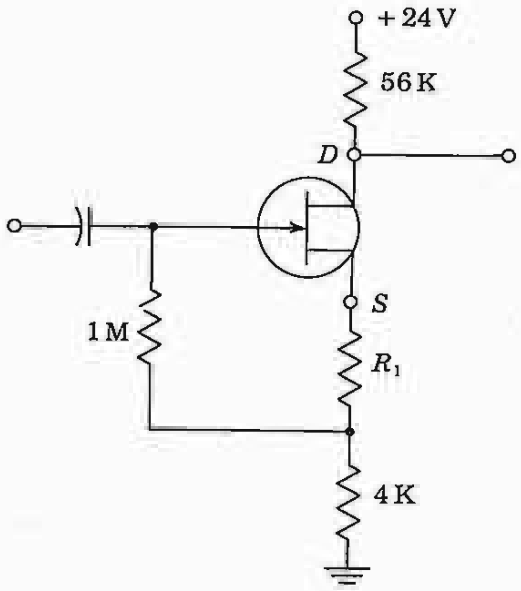


10-26 In the circuit of Prob. 10-25, assume that $V_2 = 0$, $R_d = r_d = 10$ K, $R_s = 1$ K, and $\mu = 19$. If the output is taken from the drain of $Q2$, find (*a*) the voltage gain, (*b*) the output impedance. HINT: Use the equivalent circuits in Fig. 10-22.

10-27 In the circuit of Prob. 10-25, $V_2 \neq V_1$, $R_d = 30$ K, $R_s = 2$ K, $\mu = 19$, and $r_d = 10$ K. Find (*a*) the voltage gains A_1 and A_2 defined by $V_{o2} = A_1V_1 + A_2V_2$. HINT: Use the equivalent circuits in Fig. 10-22. (*b*) If R_s is arbitrarily large, show that $A_2 = -A_1$. Note that the circuit now behaves as a difference amplifier.

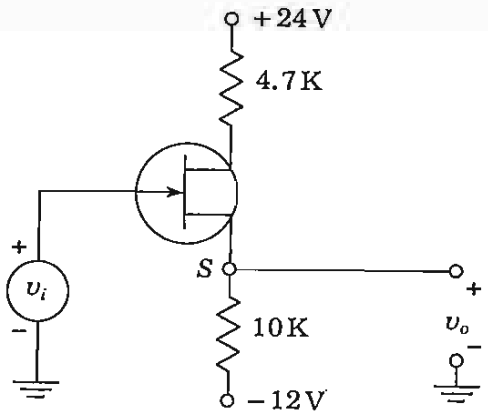
10-28 The CS amplifier stage shown in Fig. 10-23 has the following parameters: $R_d = 12$ K, $R_g = 1$ M, $R_s = 470\ \Omega$, $V_{DD} = 30$ V, C_s is arbitrarily large, $I_{DSS} = 3$ mA, $V_P = -2.4$ V, and $r_d \gg R_d$. Determine (*a*) the gate-to-source bias voltage V_{GS}, (*b*) the drain current I_D, (*c*) the quiescent voltage V_{DS}, (*d*) the small-signal voltage gain A_v.

10-29 The amplifier stage shown uses an *n*-channel FET having $I_{DSS} = 1$ mA, $V_P = -1$ V. If the quiescent drain-to-ground voltage is 10 V, find R_1.

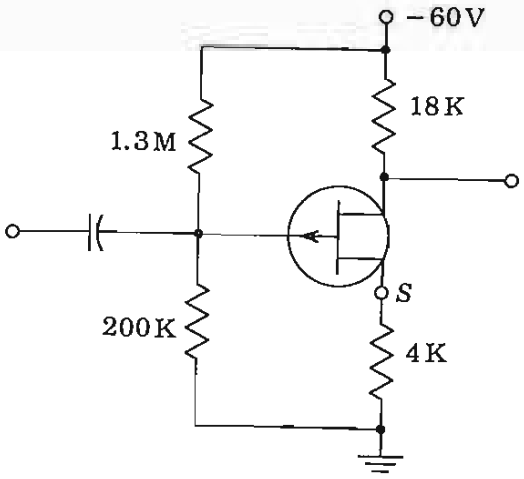


Prob. 10-29

10-30 The FET shown has the following parameters: $I_{DSS} = 5.6$ mA and $V_P = -4$ V.
(*a*) If $v_i = 0$, find v_o.
(*b*) If $v_i = 10$ V, find v_o.
(*c*) If $v_o = 0$, find v_i.
NOTE: v_i and v_o are constant voltages (and not small-signal voltages).



Prob. 10-30



Prob. 10-31

10-31 If $|I_{DSS}| = 4$ mA, $V_P = 4$ V, calculate the quiescent values of I_D, V_{GS}, and V_{DS}.

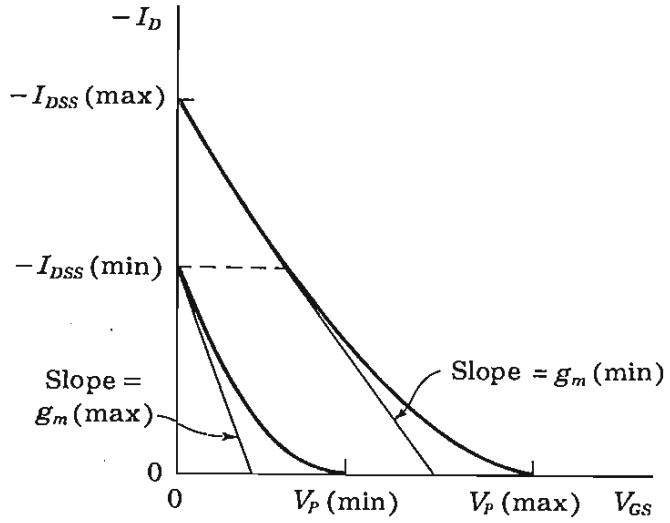
10-32 In the figure shown, two extreme transfer characteristics are indicated. The values of $V_{P,\max}$ and $V_{P,\min}$ are difficult to determine accurately. Hence these values are calculated from the experimental values of $I_{DSS,\max}$, $I_{DSS,\min}$, $g_{m,\max}$, and $g_{m,\min}$. Note that g_m is the slope of the transfer curve and that both $g_{m,\max}$ and $g_{m,\min}$ are measured at a drain current corresponding to $I_{DSS,\min}$. Verify that

(a) $V_{P,\max} = -\dfrac{2}{g_{m,\min}} (I_{DSS,\max} I_{DSS,\min})^{\frac{1}{2}}$

(b) $V_{P,\min} = -\dfrac{2I_{DSS,\min}}{g_{m,\max}}$

(c) If for a given FET, $I_{DSS,\min} = 2$ mA, $I_{DSS,\max} = 6$ mA, $g_{m,\min} = 1.5$ mA/V, and $g_{m,\max} = 3$ mA/V, evaluate $V_{P,\max}$ and $V_{P,\min}$.

Prob. 10-32

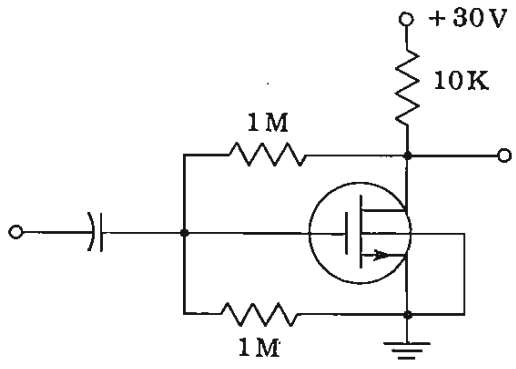


10-33 The drain current in milliamperes of the enhancement-type MOSFET shown is given by

$$I_D = 0.2(V_{GS} - V_P)^2$$

in the region $V_{DS} \geq V_{GS} - V_P$. If $V_P = +3$ V, calculate the quiescent values I_D, V_{GS}, and V_{DS}.

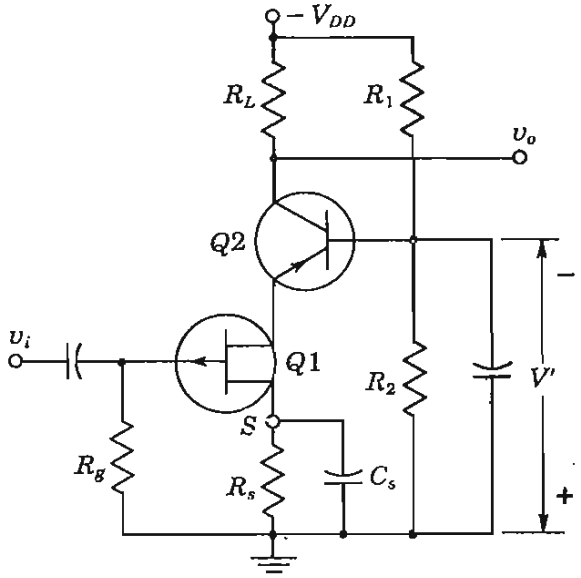
Prob. 10-33



10-34 Show that if $R_L \ll 1/h_{ob2}$, the voltage gain of the hybrid cascode amplifier stage shown is given to a very good approximation by

$$A_V = g_m h_{fb} R_L$$

where g_m is the FET transconductance.

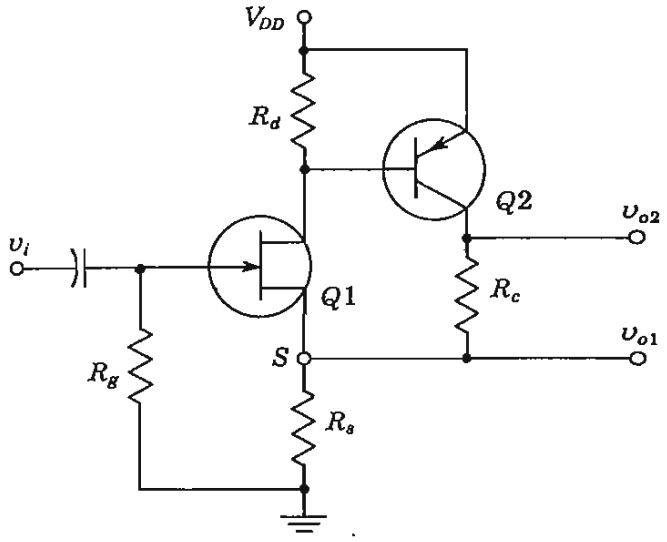


Prob. 10-34

10-35 If $h_{ie} \ll R_d$, $h_{ie} \ll r_d$, $h_{fe} \gg 1$, and $\mu \gg 1$ for the circuit, show that

(a) $A_{V1} = \dfrac{v_{o1}}{v_i} \approx \dfrac{g_m h_{fe} R_s}{1 + g_m h_{fe} R_s}$ (b) $A_{V2} = \dfrac{v_{o2}}{v_i} \approx \dfrac{g_m h_{fe}(R_s + R_c)}{1 + g_m h_{fe} R_s}$

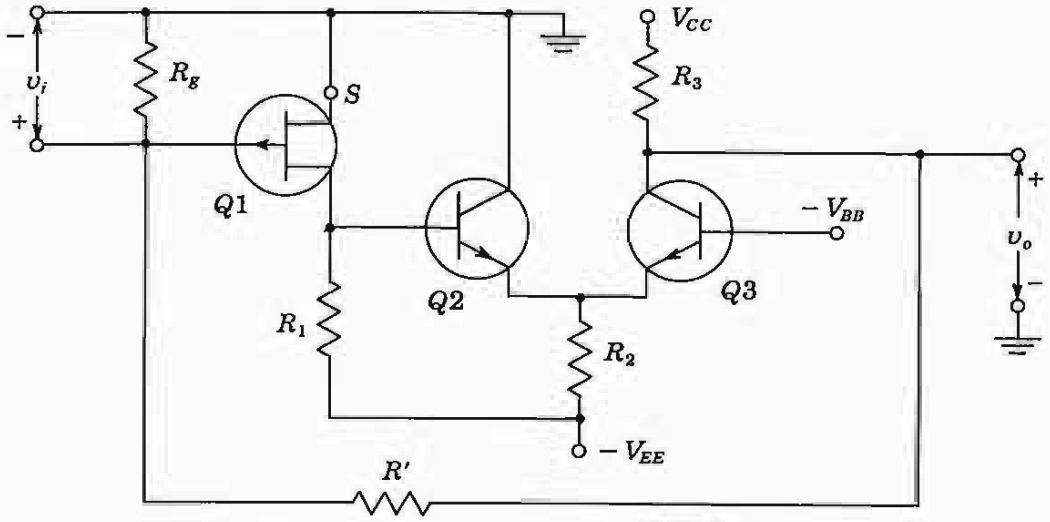
where g_m is the FET transconductance.



Prob. 10-35

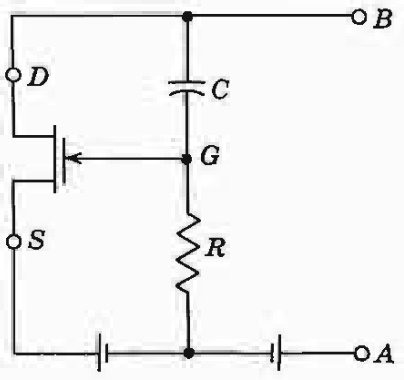
10-36 If $r_d \gg R_1$, $R_2 \gg h_{ib3}$, $1/h_{oe2} \gg h_{ib3}$, $R' \gg R_3$, and $1/h_{ob3} \gg R_3$, show that the voltage gain at low frequencies is given by

$$A_o = \frac{v_o}{v_i} = g_m(1 + h_{fe2})h_{fb3} \frac{R_1 R_3}{R_1 + h_{ie2} + h_{ib3}(1 + h_{fe2})}$$



Prob. 10-36

10-37 In the circuit shown, the FET is used as an adjustable impedance element by varying the dc bias, and thereby the g_m of the FET.
(*a*) Assume that there is a generator V between the terminals A and B. Draw the equivalent circuit. Neglect interelectrode capacitances.



Prob. 10-37

(*b*) Show that the input admittance between A and B is

$$Y_i = Y_d + (1 + g_m R) Y_{CR}$$

where Y_d is the admittance corresponding to r_d, and Y_{CR} is the admittance corresponding to R and C in series.
(*c*) If $g_m R \gg 1$, show that the effective input capacitance is

$$C_i = \frac{g_m \alpha}{\omega(1 + \alpha^2)}$$

and the effective input resistance is

$$R_i = \frac{(1 + \alpha^2) r_d}{1 + \alpha^2(1 + \mu)}$$

where $\alpha \equiv \omega C R$.

(*d*) At a given frequency, show that the maximum value of C_i (as either C or R is varied) is obtained when $\alpha = 1$, and

$$(C_i)_{\max} = \frac{g_m}{2\omega}$$

Also show that the value of R_i corresponding to this C_i is

$$(R_i)_{\max} = \frac{2r_d}{2 + \mu}$$

which, for $\mu \gg 2$, reduced to $(R_i)_{\max} = 2/g_m$.

10-38 Solve Prob. 10-37 if the capacitance C is replaced by an inductance L.

10-39 (*a*) A MOSFET connected in the CS configuration works into a 100-K resistive load. Calculate the complex voltage gain and the input admittance of the system for frequencies of 100 and 100,000 Hz. Take the interelectrode capacitances into consideration. The MOSFET parameters are $\mu = 100$, $r_d = 40$ K, $g_m = 2.5$ mA/V, $C_{gs} = 4.0$ pF, $C_{ds} = 0.6$ F, and $C_{gd} = 2.4$ pF. Compare these results with those obtained when the interelectrode capacitances are neglected. (*b*) Calculate the input resistance and capacitance.

10-40 Calculate the input admittance of an FET at 10^3 and 10^6 Hz when the total drain circuit impedance is (*a*) a resistance of 50 K, (*b*) a capacitive reactance of 50 K at each frequency. Take the interelectrode capacitances into consideration. The FET parameters are $\mu = 20$, $r_d = 10$ K, $g_m = 2.0$ mA/V, $C_{gs} = 3.0$ pF, $C_{ds} = 1.0$ pF, and $C_{gd} = 2.0$ pF. Express the results in terms of the input resistance and capacitance.

10-41 (*a*) Starting with the circuit model of Fig. 10-31, verify Eq. (10-37) for the voltage gain of the source follower, taking interelectrode capacitances into account.
(*b*) Verify Eq. (10-39) for the input admittance.
(*c*) Verify Eq. (10-40) for the output admittance.
HINT: For part *c*, set $V_i = 0$ and impress an external voltage V_o from S to N; the current drawn from V_o divided by V_o is Y_o.

10-42 Starting with the circuit model of Fig. 10-8, show that, for the *CG* amplifier stage with $R_s = 0$ and $C_{ds} = 0$,

(*a*) $A_V = \dfrac{(g_m + g_d)R_d}{1 + R_d(g_d + j\omega C_{gd})}$ (*b*) $Y_i = g_m + g_d(1 - A_V) + j\omega C_{sg}$

(*c*) Repeat (*a*), taking the source resistance R_s into account.
(*d*) Repeat (*b*), taking the source resistance R_s into account.

10-43 (*a*) For the source follower with $g_m = 2$ mA/V, $R_s = 100$ K, $r_d = 50$ K, and with each internode capacitance 3 pF, find the frequency at which the reactive component of the output admittance equals the resistive component.
(*b*) At the frequency found in part *a* calculate the gain and compare it with the low-frequency value.

CHAPTER 11

11-1 Show that at low frequencies the hybrid-Π model with $r_{b'c}$ and r_{cc} taken as infinite reduces to the approximate CE h-parameter model.

11-2 (*a*) Consider the hybrid-Π circuit at low-frequencies, so that C_c and C_c may be neglected. Omit none of the other elements in the circuit. If the load resistance is $R_L = 1/g_L$, prove that

$$K \equiv \frac{V_{cc}}{V_{b'e}} = \frac{-g_m + g_{b'c}}{g_{b'c} + g_{ce} + g_L}$$

HINT: Use the theorem that the voltage between C and E equals the short-circuit current times the impedance seen between C and E, with the input voltage $V_{b'e}$ shorted [Eq. (8-36)].
(*b*) Using Miller's theorem, draw the equivalent circuit between C and E. Applying KCL to this network, show that the above value of K is obtained.
(*c*) Using Miller's theorem, draw the equivalent circuit between B and E. Prove that the current gain under load is

$$A_I = \frac{g_L}{(g_{b'c} + g_{b'e})/K - g_{b'c}}$$

(*d*) Using the results of parts *a* and *c* and the relationships between the hybrid-Π and the h parameters, prove that

$$A_I = \frac{-h_{fe}}{1 + h_{oe}R_L}$$

which is the result [Eq. (8-18)] obtained directly from the low-frequency h-parameter model. HINT: Neglect $g_{b'c}$ compared with g_m or $g_{b'e}$ in A_I and in K. Justify these approximations.

11-3 The following low-frequency parameters are known for a given transistor at $I_C = 10$ mA, $V_{CE} = 10$ V, and at room temperature.

$h_{ie} = 500\ \Omega$ $\quad h_{oe} = 10^{-5}$ A/V

$h_{fe} = 100$ $\quad h_{re} = 10^{-4}$

At the same operating point, $f_T = 50$ MHz and $C_{ob} = 3$ pF, compute the values of all the hybrid-Π parameters.

11-4 Given the following transistor measurements made at $I_C = 5$ mA, $V_{CE} = 10$ V, and at room temperature:

$h_{fe} = 100$ $\quad h_{ie} = 600\ \Omega$

$[A_{ie}] = 10$ at 10 MHz $\quad C_c = 3$ pF

Find f_β, f_T, C_e, $r_{b'e}$, and $r_{bb'}$.

11-5 A silicon p-n-p transistor has an $f_T = 400$ MHz. What is the base thickness?

11-6 Given a germanium p-n-p transistor whose base width is 10^{-4} cm. At room temperature and for a dc emitter current of 2 mA, find (a) the emitter diffusion capacitance, (b) f_T.

11-7 (a) At low frequencies the CE current gain β is related to the CB current gain α by

$$\alpha = \frac{\beta}{1 + \beta}$$

Assuming that this relationship remains valid at high frequencies and using

$$\beta = -A_i = \frac{\beta_o}{1 + j(f/f_\beta)}$$

show that α is given by

$$\alpha = \frac{\alpha_o}{1 + j(f/f_\alpha)}$$

where

$$\alpha_o = \frac{h_{fe}}{1 + h_{fe}} \quad \text{and} \quad f_\alpha = \frac{f_\beta}{1 - \alpha_o}$$

(b) Using the results of part a, verify that, for $\alpha_o \approx 1$, $f_\alpha \approx f_\beta h_{fe}$.
(c) Verify that

$$A_i = \frac{-\alpha_o}{1 - \alpha_o + jf/f_\alpha}$$

(d) To account for "excess phase" replace α_o by $\alpha_o \epsilon^{-jmf/f_\alpha}$. Prove that f_T, the frequency at which $|A_i| = 1$, is given implicitly by

$$1 + x^2 = 2\alpha_o(\cos mx - x \sin mx)$$

where $x = f_T/f_\alpha$.
(e) If $mx \ll 1$, expand the trigonometric functions and prove that

$$f_T \approx \frac{\alpha_o f_\alpha}{[1 + 2\alpha_o(m + m^2/2)]^{\frac{1}{2}}}$$

(f) If $\alpha_o = 1$ and $m = 0.2$, show that $f_T = f_\alpha/1.2$.

11-8 (a) Redraw the CE hybrid-II equivalent circuit with the base as the common terminal and the output terminals, collector and base, short-circuited. Taking account of typical values of the transistor parameters, show that C_c, $r_{b'c}$, and r_{ce} may be neglected.
(b) Using the circuit in part a, prove that the CB short-circuit current gain is

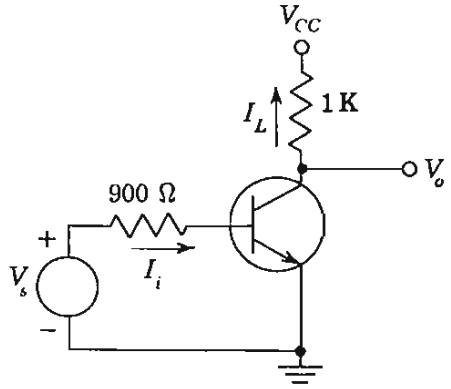
$$A_{ib} = \frac{g_m}{g_{b'e} + g_m + j\omega C_e} = \frac{\alpha_o}{1 + jf/f_\alpha}$$

where

$$\alpha_o = \frac{h_{fe}}{1 + h_{fe}} \quad \text{and} \quad f_\alpha = \frac{g_m}{2\pi C_e \alpha_o} \approx \frac{f_\beta}{1 - \alpha_o}$$

11-9 The hybrid-Π parameters of the transistor used in the circuit shown are given in Sec. 11-1. Using Miller's theorem and the approximate analysis, compute
(*a*) The upper 3-dB frequency of the current gain $A_I = I_L/I_i$.
(*b*) The magnitude of the voltage gain $A_{V_s} = V_o/V_s$ at the frequency of part *a*.

Prob. 11-9



11-10 Consider a single-stage CE transistor amplifier with the load resistor R_L shunted by a capacitance C_L.
(*a*) Prove that the internal voltage gain $K = V_{ce}/V_{b'e}$ is

$$K \approx \frac{-g_m R_L}{1 + j\omega(C_c + C_L)R_L}$$

(*b*) Prove that the 3-dB frequency is given by

$$f_H \approx \frac{1}{2\pi(C_c + C_L)R_L}$$

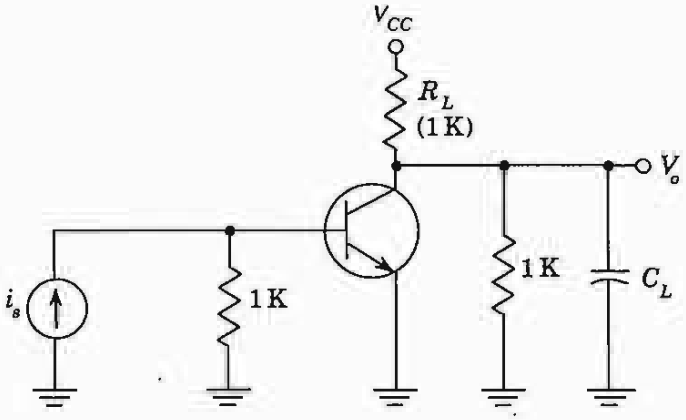
provided that the following condition is satisfied:

$$g_{b'e}R_L(C_c + C_L) \gg C_e + C_c(1 + g_m R_L)$$

11-11 For a single-stage CE transistor amplifier whose hybrid-Π parameters have the average values given in Sec. 11-1, what value of source resistance R_s will give a 3-dB frequency f_H which is (*a*) half the value for $R_s = 0$, (*b*) twice the value for $R_s = \infty$? Do these values of R_s depend upon the magnitude of the load R_L? Use Miller's theorem and the approximate analysis.

11-12 A single-stage CE amplifier is measured to have a voltage-gain bandwidth f_H of 5 MHz with $R_L = 500\ \Omega$. Assume $h_{fe} = 100$, $g_m = 100$ mA/V, $r_{bb'} = 100\ \Omega$, $C_c = 1$ pF, and $f_T = 400$ MHz.
(*a*) Find the value of the source resistance that will give the required bandwidth.
(*b*) With the value of R_s found in part *a*, find the midband voltage gain V_o/V_s.
HINT: Use the approximate analysis.

11-13 The hybrid-Π parameters of the transistor used in the circuit shown are given in Sec. 11-1. The input to the amplifier is an abrupt current step 0.2 mA in magnitude. Find the output voltage as a function of time (*a*) if $C_L = 0$. Neglect the output time constant. (*b*) If $C_L = 0.1\ \mu$F. Neglect the input time constant.



Prob. 11-13

11-14 (*a*) Verify the nodal equations for the single-stage CE amplifier of Sec. 11-8.
(*b*) Obtain Eq. (11-37) for the voltage gain V_o/V_s.

11-15 (*a*) Verify the values of K_1, s_o, s_1, and s_2 given in Sec. 11-8 for the CE stage of Fig. 11-10.
(*b*) Evaluate the gain at zero frequency.
(*c*) Evaluate the magnitude of the gain at 2 MHz and check with Fig. 11-11.
(*d*) Evaluate the phase of the gain at 2 MHz and check with Fig. 11-11.

11-16 (*a*) From the circuit of Fig. 11-12 (and not assuming that $|K| \gg 1$), prove that

$$K = \frac{-g_m R_L + j\omega C_c R_L}{1 + j\omega C_c R_L}$$

Why may the term $j\omega C_c R_L$ be neglected in the numerator but not in the denominator?
(*b*) The Miller admittance in the output circuit is given by

$$Y_o = j\omega C_c \left(1 - \frac{1}{K}\right)$$

Prove that this represents a capacitance C_o in parallel with a resistance R_o given by

$$C_o = C_c \frac{1 + g_m R_L}{g_m R_L} \qquad R_o = \frac{-g_m}{\omega^2 C_c^2}$$

Note that R_o is negative.
(*c*) Evaluate C_o and R_o at the 3-dB frequency of 3.0 MHz and verify that the effective output time constant remains $R_L C_c$ (approximately). Assume $g_m = 50$ mA/V, $R_L = 2$ K, $C_c = 100$ pF, and $C_c = 3$ pF.

11-17 Verify Eq. (11-54).

11-18 (*a*) Verify the nodal equations in Sec. 11-10 for the emitter follower.
(*b*) Find the gain V_e/V_s as a function of s.

11-19 Delete all capacitors from the emitter-follower equivalent circuit of Fig. 11-14*b*. Find (*a*) the input impedance and (*b*) the output impedance and (*c*) show that these results are consistent with the low-frequency equivalent circuits of Fig. 8-25.

11-20 (*a*) For the emitter follower of Fig. 11-14 at high frequencies, obtain $K = V_{e'}/V_i'$ and (with $g \equiv g_m + g_{b'e}$) verify that

$$K = \frac{gR_L}{1 + gR_L} \frac{1 + j\omega(C_{e'}/g)}{1 + j\omega\left(\frac{C_L + C_e}{1 + gR_L}\right) R_L}$$

(*b*) If $gR_L \gg 1$ and $C_L \gg C_e$, show that

$$K \approx \frac{1}{1 + jf/f_H}$$

where

$$f_H = \frac{1}{2\pi} \frac{g}{C_L + C_e} = \frac{1}{2\pi} \frac{g_m + g_{b'e}}{C_L + C_e}$$

CHAPTER 12

12-1 (*a*) To show the effect of phase shift on the image seen on a cathode-ray screen, consider the following example: The sinusoidal voltages applied to both sets of plates should be equal in phase and magnitude so that the maximum displacement in either direction on the screen is 2 in. Because of frequency distortion in the horizontal amplifier, the phase of the horizontal voltage is shifted 5° but the magnitude is changed inappreciably. Plot to scale the image that actually appears on the screen, and compare with the image that would be seen if there were no phase shift.
(*b*) If the phase shift in both amplifiers were the same, what would be seen on the cathode-ray screen?

12-2 The input to an amplifier consists of a voltage made up of a fundamental signal and a second-harmonic signal of half the magnitude and in phase with the fundamental. Plot the resultant.

The output consists of the same magnitude of each component, but with the second harmonic shifted 90° (on the fundamental scale). This corresponds to perfect frequency response but bad phase-shift response. Plot the output and compare it with the input waveshape.

12-3 The bandwidth of an amplifier extends from 20 Hz to 20 kHz. Find the frequency range over which the voltage gain is down less than 1 dB from its midband value. Assume that the low- and high-frequency response is given by Eqs. (12-1) and (12-5) multiplied by a constant A_{Vo}.

12-4 Prove that over the range of frequencies from $10f_L$ to $0.1f_H$ the voltage amplification is constant to within 0.5 percent and the phase shift to within ± 0.1 rad. Make the same assumption as in Prob. 12-3.

12-5 (*a*) Show that the Bode magnitude plot for a two-pole transfer function is equal to the sum of the magnitude plots of each pole considered separately.
(*b*) Repeat part *a* for the Bode phase plot.

12-6 Sketch the idealized Bode amplitude and phase plots for a transfer function with one zero f_z and one pole f_p if (*a*) $f_p < f_z$ and (*b*) $f_p > f_z$.

12-7 Consider a transfer characteristic with two poles such that $f_{p2} = 4f_{p1}$.
(*a*) Plot the idealized and true Bode magnitude curves. Obtain the actual 3-dB frequency graphically.
(*b*) Plot the idealized and true Bode phase curves.

12-8 Repeat Prob. 12-7 for poles at $f_{p2} = 2f_{p1}$.

12-9 Consider the transfer function given in Eq. (12-1) which has one pole and a zero at $f = 0$. Draw the piecewise linear Bode plots for the pole, the zero, and the resultant for (*a*) amplitude, (*b*) phase.

12-10 An ideal 1-μs pulse is fed into an amplifier. Plot the output if the bandpass is (*a*) 10 MHz, (*b*) 1.0 MHz, (*c*) 0.1 MHz. Assume $f_L = 0$ and a single-pole amplifier.

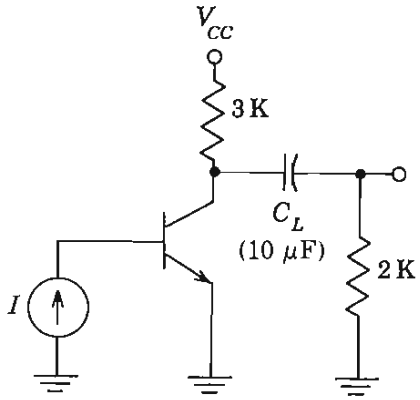
12-11 (*a*) Prove that the response of a two-stage (identical and noninteracting) low-pass amplifier to a unit step is

$$v_o = A_o^2[1 - (1 + x)\epsilon^{-x}]$$

where A_o is the midband voltage gain and $x \equiv t/RC$.
(*b*) For $t \ll RC$, show that the output varies quadratically with time.

12-12 In Prob. 12-11, let the upper 3-dB frequency of a single stage be f_H and the rise time of the two stages in cascade be t_r. Show that $f_H t_r = 0.53$.

12-13 (*a*) For the transistor *CE* stage shown with $1/h_{oe} \approx \infty$, calculate the percentage tilt in the output if the input current I is a 100-Hz square wave.
(*b*) What is the lowest-frequency square wave which will suffer less than 1 percent tilt?



Prob. 12-13

12-14 Consider a transfer function with n poles and k zeros. Assume that all the zeros occur at much higher frequencies than the poles. Verify that the 3-dB frequency is given by Eq. (12-25).

12-15 The transfer function V_o/V_s of an amplifier has n poles $s_1, s_2, \ldots, s_n$ and k zeros $s_{z1}, s_{z2}, \ldots, s_{zk}$, as follows:

$$\frac{V_o}{V_s} = \frac{K(s - s_{z1})(s - s_{z2}) \cdots (s - s_{zk})}{(s - s_1)(s - s_2) \cdots (s - s_n)}$$

If the zeros are of much higher frequencies than the poles, show that
(*a*) An approximate expression for the high 3-dB frequency f_H^* is given by

$$\frac{1}{f_H^*} \approx \sqrt{\frac{1}{f_1^2} + \frac{1}{f_2^2} + \cdots + \frac{1}{f_n^2}}$$

(*b*) An expression which gives a more accurate result is

$$\frac{1}{f_H^*} \approx 1.1 \sqrt{\frac{1}{f_1^2} + \frac{1}{f_2^2} + \cdots + \frac{1}{f_n^2}}$$

Verify this, using Eq. (12-26) for the case of
(i) Two identical poles $f_1 = f_2$.
(ii) Three identical poles $f_1 = f_2 = f_3$.
Show that the error is within 10 percent.

12-16 Consider a transfer function with poles at 1 MHz and 2 MHz. Assume all other poles and zeros are much larger than 2 MHz. Calculate the high 3-dB frequency. Compare your result with the approximate value obtained from Eq. (12-31).

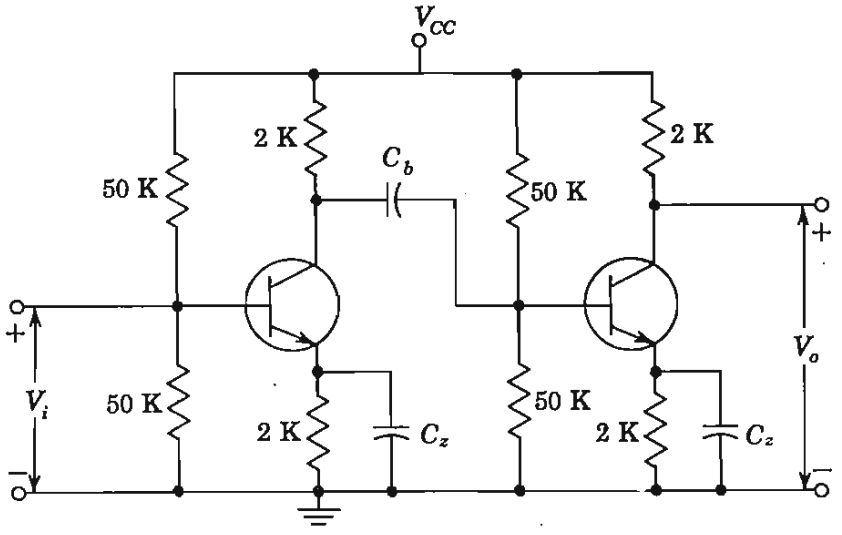
12-17 If two cascaded single-pole stages have very unequal bandpasses, show that the combined bandwidth is essentially that of the smaller. Assume noninteracting stages.

12-18 Three identical cascaded stages have an overall upper 3-dB frequency of 20 kHz and a lower 3-dB frequency of 20 Hz. What are f_L and f_H of each stage? Assume noninteracting stages.

12-19 It is desired that the voltage gain of an *RC*-coupled amplifier at 60 Hz should not decrease by more than 10 percent from its midband value. Show that the coupling capacitance C must be at least equal to $5.5/R'$, where $R' = R_o' + R_i'$ is expressed in kilohms, and C in microfarads.

12-20 The parameters of the transistors in the circuit shown are $h_{fe} = 50$, $h_{ie} = 1.1$ K, $h_{re} = h_{oe} = 0$. Find (*a*) the midband gain, (*b*) the value of C_b necessary to give a lower 3-dB frequency of 20 Hz. Assume that C_z represents a short-circuit at this frequency. (*c*) Find the value of C_b necessary to ensure less than 10 percent tilt for a 100-Hz square-wave input.

Prob. 12-20



12-21 A two-stage FET RC-coupled amplifier has the following parameters: $g_m = 10$ mA/V, $r_d = 5.5$ K, $R_d = 10$ K, and $R_g = 0.5$ M for each stage. Assume C_s in Fig. 12-11b to be arbitrarily large.
(a) What must be the value of C_b in order that the frequency characteristic of each stage be flat within 1 dB down to 10 Hz?
(b) Repeat part a if the overall gain of both stages is to be down 1 dB at 10 Hz.
(c) What is the overall midband voltage gain?

12-22 A three-stage RC-coupled amplifier uses field-effect transistors (Fig. 12-11b), with the following parameters: $g_m = 2.6$ mA/V, $r_d = 7.7$ K, $R_d = 10$ K, $R_g = 0.1$ M, $C_b = 0.005\ \mu$F, and $C_s = \infty$. Evaluate (a) the overall midband voltage gain in decibels, (b) f_L of each individual stage, (c) the overall lower 3-dB frequency.

12-23 Plot the idealized Bode *phase* characteristic corresponding to the amplitude response of Fig. 12-15 [Eq. (12-39)].

12-24 (a) Show that the relative voltage gain of an amplifier with an emitter resistor R_e bypassed by a capacitor C_z may be expressed in the form

$$\frac{A_V}{A_o} = \frac{1 + j\omega R_e C_z}{B + j\omega R_e C_z}$$

where $B = 1 + R'/R$, $R' = R_e(1 + h_{fe})$, and $R = R_s + h_{ie}$.
(b) Prove that the lower 3-dB frequency is

$$f_L = \frac{\sqrt{B^2 - 2}}{2\pi R_e C_z}$$

What is the physical meaning of the condition $B < \sqrt{2}$?
(c) If $B^2 \gg 2$, show that $f_L \approx f_p$, the pole frequency as defined in Eq. (12-40).

12-25 In the circuit of Fig. 12-14a, let $R_s = 500\ \Omega$; $R_1 = R_2 = 50$ K; $R_c = R_e = 2$ K; $h_{ie} = 1.1$ K; $h_{fe} = 50$; $h_{re} = h_{oe} = 0$; $C_b = 5\ \mu$F.
(a) Neglecting the effects of C_z, find f_L for the transistor stage.
(b) Neglecting the effects of C_b, find expressions for f_p and f_o due to C_z alone.
(c) Find a value of C_z for which f_L is virtually unaffected by the presence of the emitter bypass capacitor.

12-26 Find the percentage tilt in the output of a transistor stage caused by a capacitor C_z bypassing an emitter resistor R_e. Use the following method: If V is the magnitude of the input step, then from Fig. 12-14 (and using lowercase letters for instantaneous values),

$$v_o = -h_{fe} i_b R_c = -h_{fe} R_c \frac{V - v_{en}}{R}$$

where $R \equiv R_s + h_{ie}$. Take as a first approximation $v_{en} = 0$. Calculate the corresponding current, and assuming that all the emitter current passes through C_z, calculate v_{en}, and then show that

$$v_o = -\frac{h_{fe} R_c V}{R}\left[1 - \frac{(1 + h_{fe})t}{RC_z}\right]$$

From this result verify Eq. (12-43).

12-27 Show that the low-frequency voltage gain of the FET stage shown with $r_d \gg R_L + R_s$ is given by

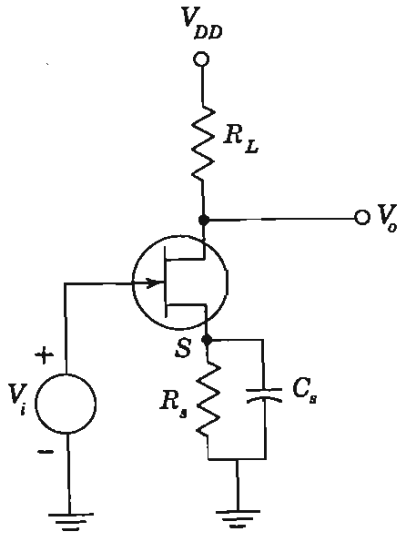
(*a*) $$\frac{A_V}{A_o} = \frac{1}{1 + g_m R_s} \frac{1 + jf/f_o}{1 + jf/f_p}$$

where

$$A_o \equiv -g_m R_L \qquad f_o \equiv \frac{1}{2\pi C_s R_s} \qquad f_p = \frac{1 + g_m R_s}{2\pi C_s R_s}$$

(*b*) If $g_m R_s \gg 1$ and $g_m = 5$ mA/V, find C_s so that a 50-Hz square-wave input will suffer no more than 10 percent tilt.

Prob. 12-27



12-28 Verify that the transfer function of the two-stage interacting amplifier of Fig. 12-19 is given by Eq. (12-48).

12-29 Verify Eq. (12-50).

12-30 Justify Eq. (12-52).

12-31 (*a*) Find the noise bandwidth B_n for an amplifier for which $A_{Vo} = 1, f_L = 0$ Hz, and

$$|A_V(f)| = \frac{1}{\sqrt{1 + (f/f_H)^2}}$$

(*b*) Compute B_n if $f_H = 10$ kHz.

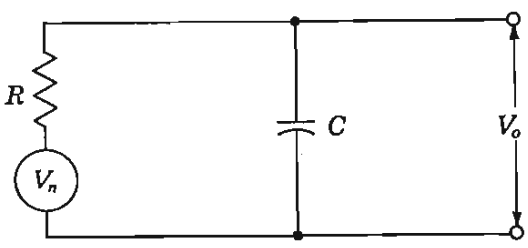
12-32 (*a*) Find the mean-square value V_o^2 of the output noise voltage for the circuit shown. The circle represents a generator supplying Johnson noise to the RC combination.

(*b*) Prove that

$$\tfrac{1}{2}CV_o^2 = \tfrac{1}{2}\bar{k}T$$

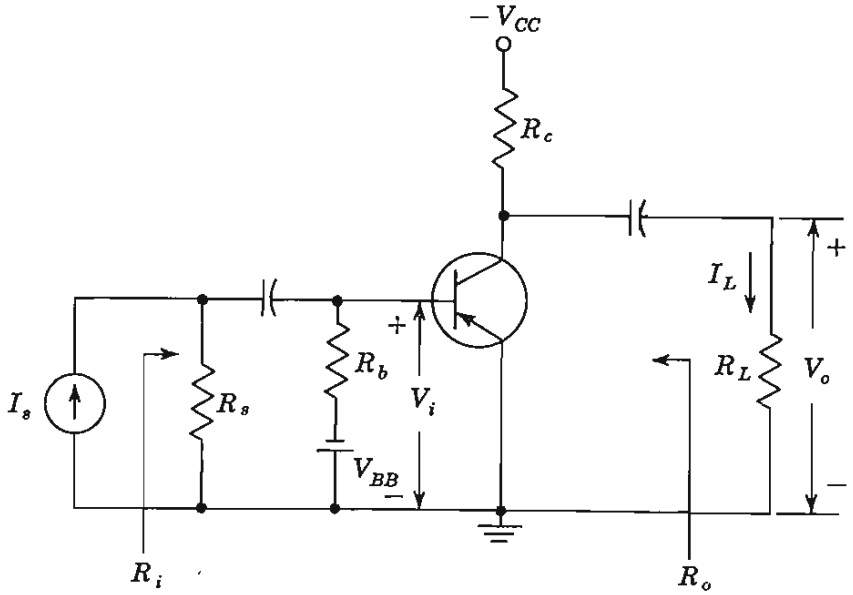
This result is known as the *equipartition theorem.*

Prob. 12-32



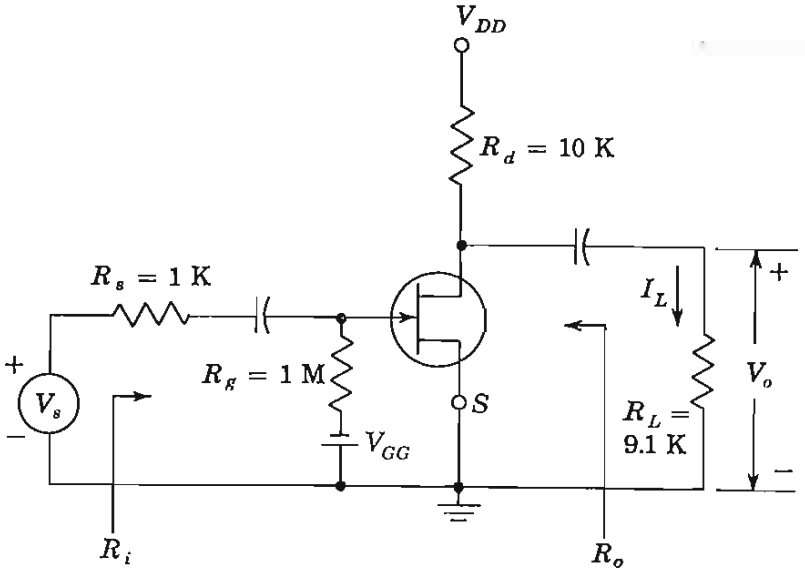
CHAPTER 13

13-1 For the circuit shown, with $R_c = 4$ K, $R_L = 4$ K, $R_b = 20$ K, $R_s = 1$ K, and the transistor parameters given in Table 8-2, find
(*a*) The current gain $I_L/I_s = A_I$.
(*b*) The voltage gain V_o/V_s, where $V_s \equiv I_s R_s$.
(*c*) The transconductance $I_L/V_s = G_M$.
(*d*) The transresistance $V_o/I_s = R_M$.
(*e*) The input resistance seen by the source.
(*f*) The output resistance seen by the load.
Make reasonable approximations. Neglect all capacitive effects.



Prob. 13-1

13-2 Repeat Prob. 13-1 for the circuit shown, with $g_m = 5$ mA/V and $r_d = 100$ K. Note that $V_s \equiv I_s R_s$.

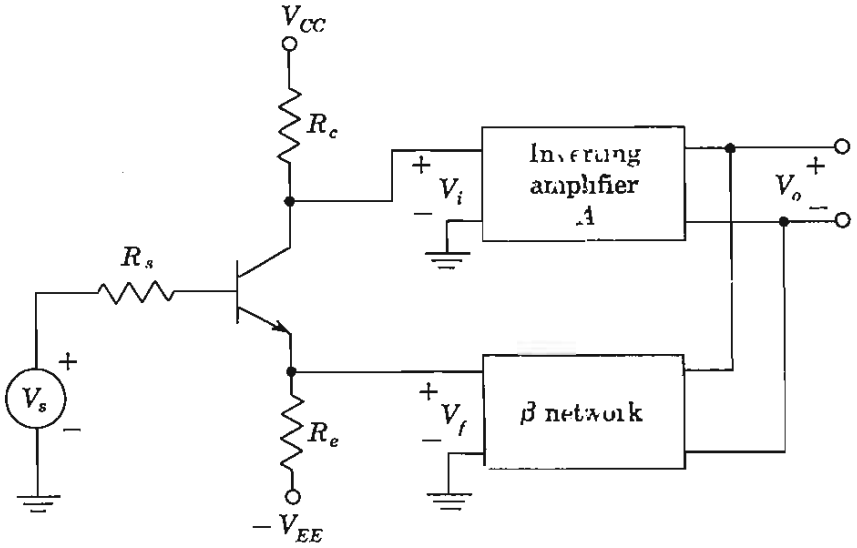


Prob. 13-2

13-3 (*a*) For the circuit shown, find the ac voltage V_i as a function of V_s and V_f. Assume that the inverting-amplifier input resistance is infinite, that $A = A_V =$

$-1{,}000$, $\beta = V_f/V_o = \frac{1}{100}$, $R_s = R_c = R_e = 1$ K, $h_{ie} = 1$ K, $h_{re} = h_{oc} = 0$, and $h_{fe} = 100$. (*b*) Find $A_{vf} = V_o/V_s = AV_i/V_s$.

Prob. 13-3



13-4 An amplifier consists of three identical stages connected in cascade. The output voltage is sampled and returned to the input in series opposing. If it is specified that the relative change dA_f/A_f in the closed-loop voltage gain A_f must not exceed Ψ_f, show that the minimum value of the open-loop gain A of the amplifier is given by

$$A = 3A_f \frac{|\Psi_1|}{|\Psi_f|}$$

where $\Psi_1 \equiv dA_1/A_1$ is the relative change in the voltage gain of each stage of the amplifier.

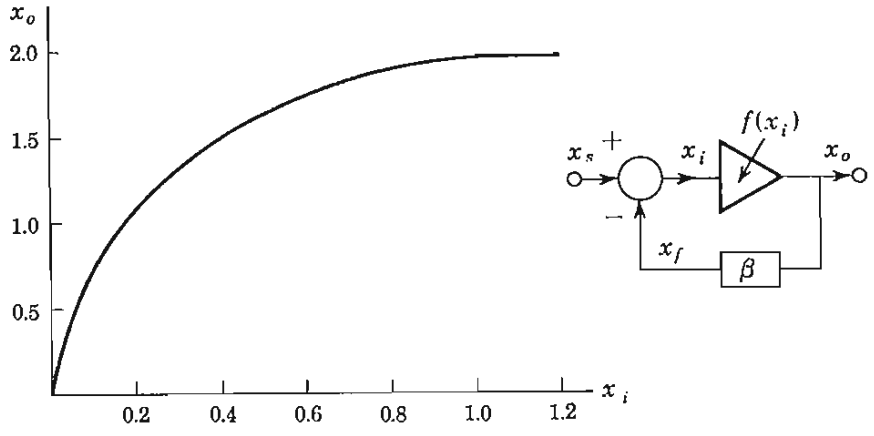
13-5 An amplifier with open-loop voltage gain $A_f = 1{,}000 \pm 100$ is available. It is necessary to have an amplifier whose voltage gain varies by no more than ± 0.1 percent.

(*a*) Find the reverse transmission factor β of the feedback network used.

(*b*) Find the gain with feedback.

13-6 The figure shows the transfer characteristic of a nonlinear amplifier. Negative feedback is applied to this amplifier as shown. Find the new transfer characteristic x_o versus x_s if (*a*) $\beta = 0.1$, (*b*) $\beta = 0.05$. Plot the two transfer characteristics on the same figure.

Prob. 13-6



13-7 An amplifier without feedback gives a fundamental output of 36 V with 7 percent second-harmonic distortion when the input is 0.028 V.
(*a*) If 1.2 percent of the output is fed back into the input in a negative voltage-series feedback circuit, what is the output voltage?
(*b*) If the fundamental output is maintained at 36 V but the second-harmonic distortion is reduced to 1 percent, what is the input voltage?

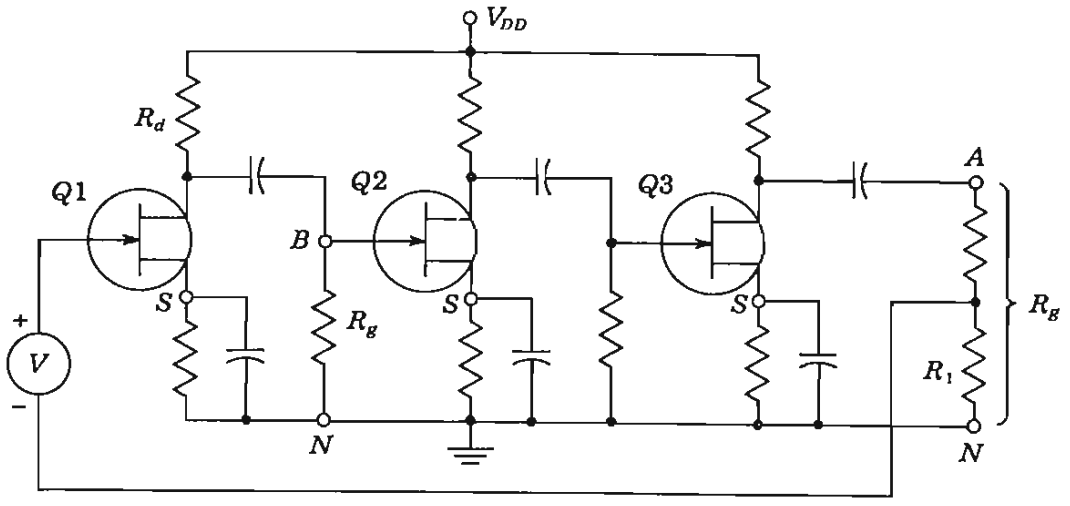
13-8 An amplifier with an open-loop voltage gain of 1,000 delivers 10 W of output power at 10 percent second-harmonic distortion when the input signal is 10 mV. If 40-dB negative voltage-series feedback is applied and the output power is to remain at 10 W, determine (*a*) the required input signal, (*b*) the percent harmonic distortion.

13-9 (*a*) Verify Eq. (13-16) for the input impedance of the current-series feedback amplifier.
(*b*) Repeat part (*a*) for Eq. (13-25) for the voltage-shunt amplifier.
(*c*) Verify Eq. (13-32) for the output impedance of the voltage-shunt feedback amplifier.
(*d*) Repeat part (*c*) for Eq. (13-38) for the current-series feedback amplifier.

13-10 The output impedance may be calculated as the ratio of the open-circuit voltage to the short-circuit current. Using this method, evaluate R_{of} and R'_{of} for (*a*) voltage-series feedback, (*b*) current-series feedback, (*c*) current-shunt feedback, and (*d*) voltage-shunt feedback.

13-11 The *h*-parameter model of a transistor can be considered to represent a feedback amplifier due to the presence of the h_{rc} source. Using feedback formulas, find (*a*) R_{if} and (*b*) $Y_{of} = 1/R_{of}$, representing the input and output resistances of a transistor stage taking h_{rc}, h_{oc}, and a source resistance R_s into account.

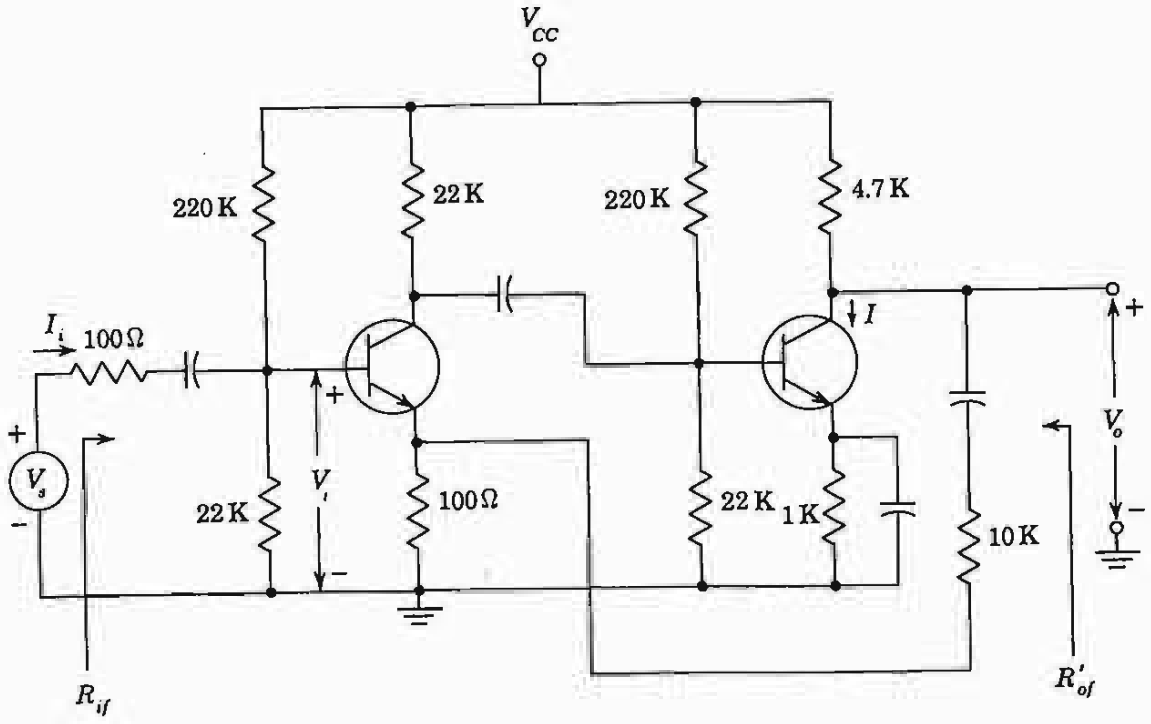
13-12 Assume that the parameters of the circuit are $r_d = 10$ K, $R_g = 1$ M, $R_1 = 40\ \Omega$, $R_d = 50$ K, and $g_m = 6$ mA/V. Neglect the reactances of all capacitors. Find the voltage gain and output impedance of the circuit at the terminals (*a*) *AN*, (*b*) *BN*.



Prob. 13-12

13-13 Prove that for voltage-series feedback, with $R_s = 0$, $A_{If} = A_I$. HINT: $A_V = A_I R_L / R_i$.

13-14 The transistors in the feedback amplifier shown are identical, and their h parameters are as given in Table 8-2. Make reasonable approximations whenever appropriate, and neglect the reactance of the capacitors. Calculate $R_{if} = V_s/I_i$, $A_{If} = -I/I_i$, $A'_{Vf} = V_o/V_i$, $A_{Vf} = V_o/V_s$, and R'_{of}.

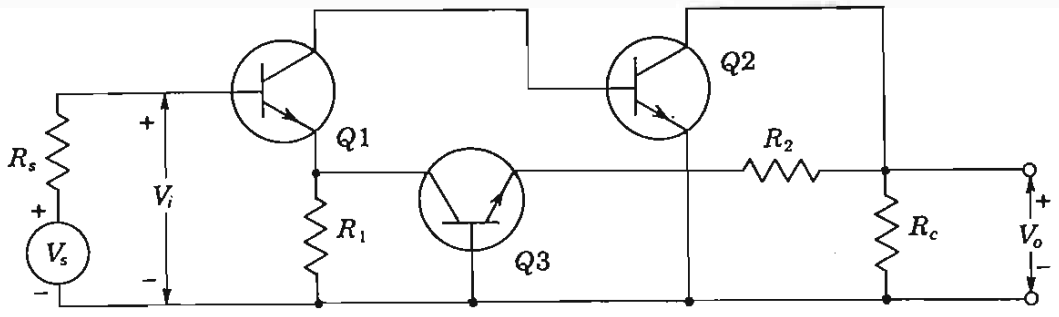


Prob. 13-14

13-15 A modified second-collector to first-emitter feedback pair is shown with dc biasing omitted for simplicity. All transistors are identical. Neglecting h_{re}, h_{rb}, h_{oe}, h_{ob} and assuming that $h_{fe} \gg 1$, $h_{fe}R_1 \gg R_s + h_{ie}$, and $R_2 \gg h_{ib3}$, show that

(*a*) The voltage gain $A_{Vf} = V_o/V_s \approx R_2/R_1$.

(*b*) The output resistance $R'_{of} \approx R_c \| (R_2/h_{fe})$.



Prob. 13-15

13-16 Consider the transistor stage of Fig. 13-16*a*.

(*a*) Neglecting h_{rc} and h_{oe} and assuming that $h_{fc} \gg 1$, show that the voltage gain is

$$A_{Vf} = \frac{V_o}{V_s} \approx \frac{-h_{fe}R_L}{R_s + h_{ie} + h_{fe}R_e}$$

(*b*) If the relative change dA_f/A_f of the voltage gain A_f must not exceed a specified value Ψ_f due to variations of h_{fe}, show that the minimum required value of the emitter resistor R_e is given by

$$R_e = \frac{R_s + h_{ie}}{h_{fe}} \left(\frac{dh_f/h_{fe}}{\Psi_f} - 1 \right)$$

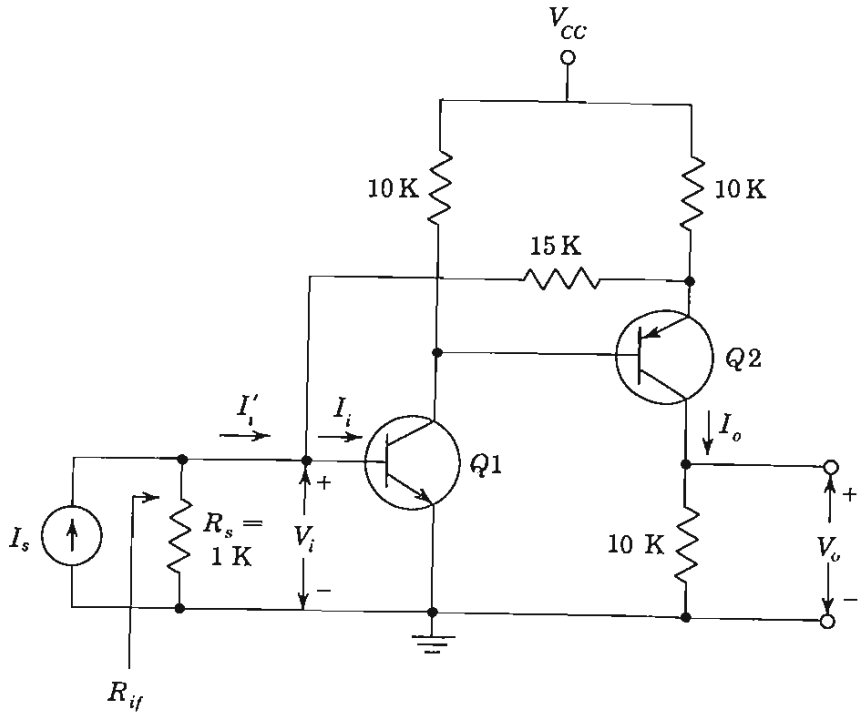
13-17 Solve the example in Sec. 13-11 on current-shunt feedback without using the feedback equations. Instead, apply Miller's theorem to the resistor R'. HINT: Assume the gain A'_V from V_{i1} to V_{e2} to be very large.

13-18 In the two-stage feedback amplifier shown, the transistors are identical and have the following parameters: $h_{fe} = 50$, $h_{ie} = 2$ K, $h_{re} = 0$, and $h_{oe} = 0$. Calculate

(*a*) $A_{If} = \dfrac{I_o}{I_s}$ (*b*) $R_{if} = \dfrac{V_i}{I_s}$ (*c*) $A'_{If} = \dfrac{I_o}{I'_i}$

(*d*) $A_{Vf} = \dfrac{V_o}{V_s}$ where $V_s = I_s R_s$

(*e*) Evaluate A_{Vf} from Eq. (13-70) and compare with the result obtained in part *d*.



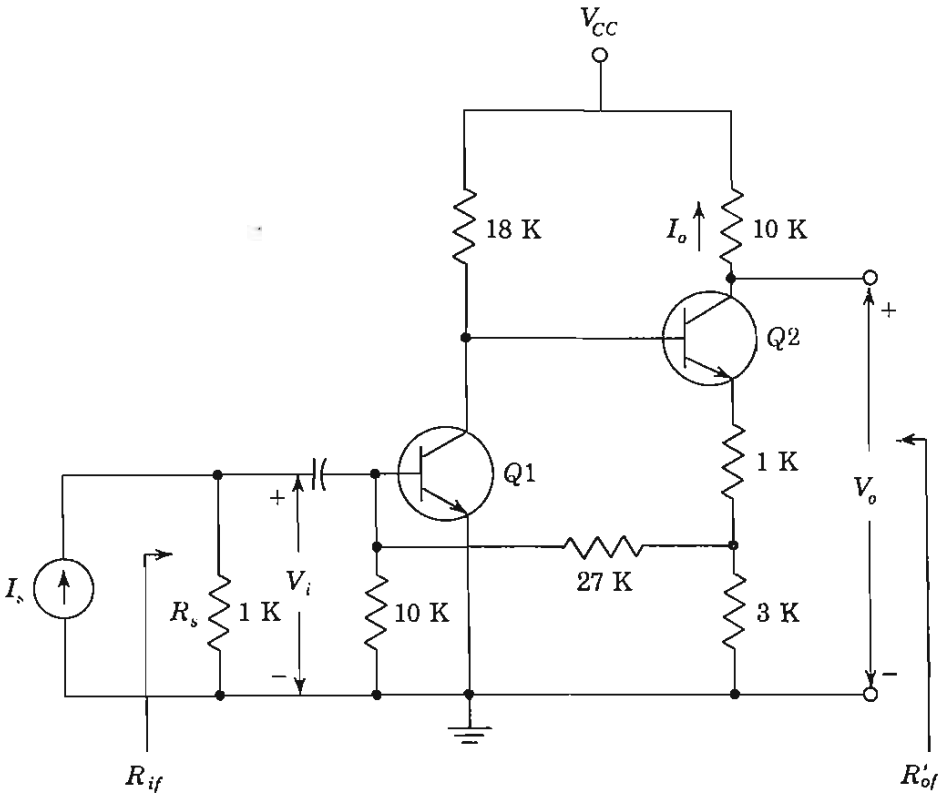
Prob. 13-18

13-19 For the circuit shown (and with the *h*-parameter values given in Prob. 13-18) find

(*a*) $A_{If} \equiv \dfrac{I_o}{I_s}$ (*b*) R_{if}

(*c*) $A_{Vf} \equiv \dfrac{V_o}{V_s}$ where $I_s \equiv \dfrac{V_s}{R_s}$

(*d*) $A'_{Vf} \equiv \dfrac{V_o}{V_i}$ (*e*) R'_{of}

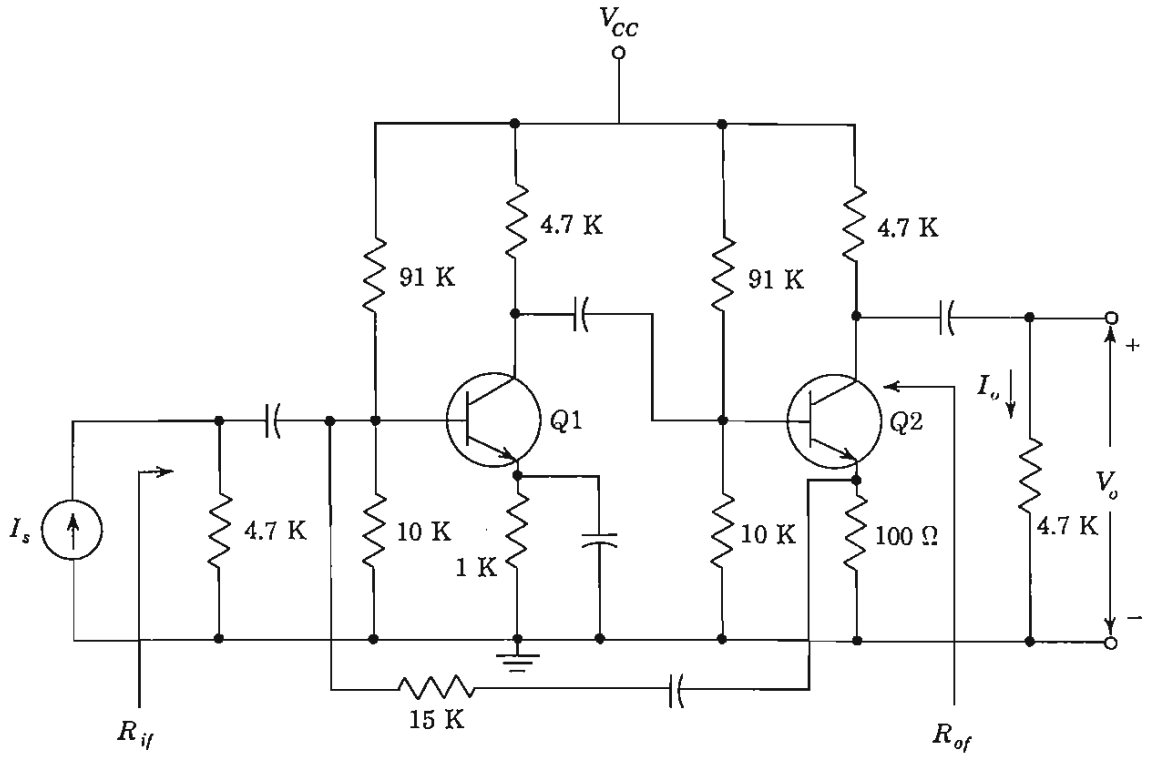


Prob. 13-19

13-20 The transistors in the feedback amplifier shown are identical, and their h parameters are given in Table 8-2. Make reasonable approximations where appropriate, and neglect the reactances of the capacitors. Calculate

(*a*) $A_{If} \equiv \dfrac{I_o}{I_s}$ (*b*) $A_{Vf} \equiv \dfrac{V_o}{V_s}$, where $V_s \equiv I_s R_s$

(*c*) R_{if} (*d*) R_{of}



Prob. 13-20

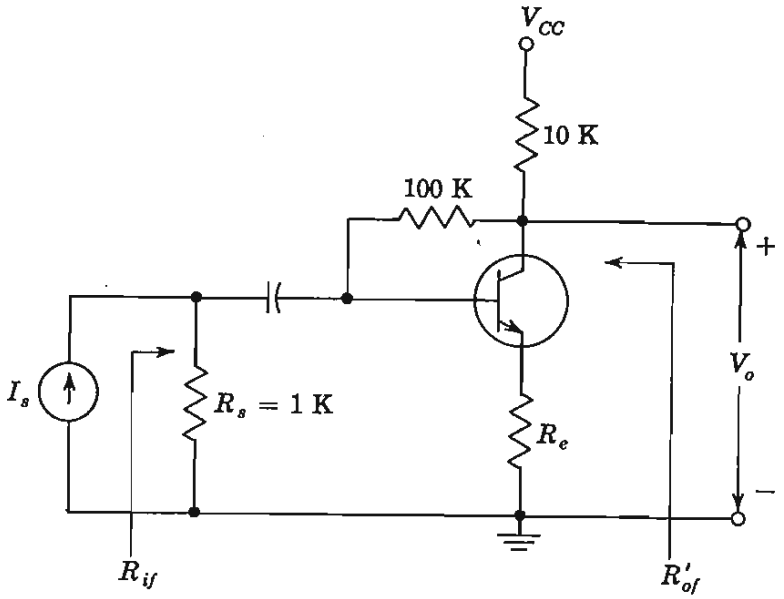
13-21 Let h_{fe} of $Q1$ and $Q2$ of Prob. 13-20 increase to 100. If all other parameters remain constant, repeat Prob. 13-20.

13-22 For the transistor feedback-amplifier stage shown, $h_{fe} = 100$, $h_{ie} = 1$ K, while h_{re} and h_{oe} are negligible. Determine with $R_e = 0$

(*a*) $R_{Mf} = \dfrac{V_o}{I_s}$ where $I_s = \dfrac{V_s}{R_s}$

(*b*) $A_{Vf} = \dfrac{V_o}{V_s}$ (*c*) R_{if} (*d*) R'_{of}

(*e*) Repeat the four preceding calculations if $R_e = 1$ K.

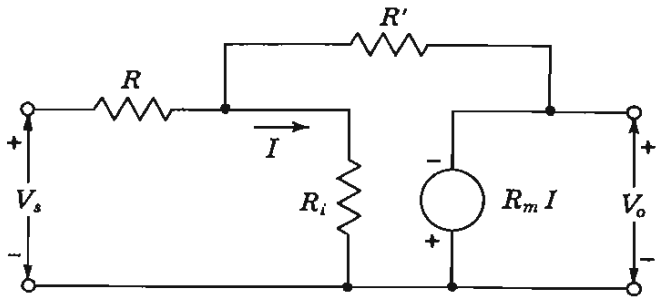


Prob. 13-22

13-23 Consider the illustrative example in Sec. 13-11 (current-shunt feedback) but with the output taken from the emitter of $Q2$. This configuration now represents voltage-shunt feedback and *not* current-shunt feedback. Analyze the circuit for (*a*) β; (*b*) R_M; (*c*) R_{Mf}; (*d*) A_{Vf}; (*e*) R_{if}; (*f*) R'_{of}.

13-24 For the circuit shown, prove that

$$A_{Vf} = \frac{V_o}{V_s} = -\frac{R'}{R}\,\frac{1}{1 + \dfrac{R'}{R_m}\left(\dfrac{R_i + R'}{R'} + \dfrac{R_i}{R}\right)}$$



Prob. 13-24

13-25 For the voltage-shunt feedback circuit in the example in Sec. (13-12), replace the transistor by the low-frequency approximate model ($h_{oc} = h_{rc} = 0$). Do *not* use feedback-analysis methods. Solve for A_{vf}, R_{if}, and R_{of} exactly. Compare with results obtained in Sec. 13-12.

CHAPTER 14

14-1 A single-stage *RC*-coupled amplifier with a midband voltage gain of 1,000 is made into a feedback amplifier by feeding 10 percent of its output voltage in series with the input opposing. Assume that the amplifier gain without feedback may be approximated at low frequencies by Eq. (12-2) and at high frequencies by Eq. (14-2).
(*a*) As the frequency is varied, to what value does the voltage gain of the amplifier without feedback fall before gain of the amplifier with feedback falls 3 dB?
(*b*) What is the ratio of the half-power frequencies with feedback to those without feedback?
(*c*) If $f_L = 20$ Hz and $f_H = 50$ kHz for the amplifier without feedback, what are the corresponding values after feedback has been added?

14-2 (*a*) Verify Eqs. (14-9) and (14-10) for A_f for the two-pole transfer gain.
(*b*) Verify that for $Q = Q_{\min}$, the roots are ω_1 and ω_2.

14-3 Verify Eqs. (14-14) and (14-16) for the transfer function of the circuit model of Fig. 14-4.

14-4 (*a*) Show that the two-pole closed-loop magnitude of the gain A_f is given by Eq. (14-18) as a function of frequency.
(*b*) Verify that the peak on the frequency response occurs at $\omega/\omega_o = \sqrt{1 - 2k^2}$ and has a value given by Eq. (14-20).

14-5 Plot the phase response (versus ω/ω_o) of a double-pole transfer function for $Q = 0.5, 1, 2, 5$.

14-6 Derive Eqs. (14-23), (14-24), (14-25), and (14-26), for the step response of the two-pole feedback amplifier. HINT: For the overdamped case, assume $k^2 \gg 1$ and expand $(1 - 1/k^2)^{\frac{1}{2}}$ in Taylor series.

14-7 Verify Eq. (14-27) for the positions x_m and magnitude y_m of the oscillatory-response maxima and minima.

14-8 Define the normalized settling time x_s to be the time at which the first peak (or dip) in Fig. 14-6 that is within the error band of $\pm P$ percent occurs. Show that the value of m corresponding to x_s is given by the smallest value of m that satisfies

$$100\epsilon^{-\pi km/(1-k^2)^{\frac{1}{2}}} \leq P$$

14-9 (*a*) Given a two-pole amplifier with corner frequencies at $\omega_1 = 1$Mrad/s and $\omega_2 = 0.2$Mrad/s. What are the maximum decibels of feedback which will give the fastest rise time without overshoot?
(*b*) What is the rise-time improvement for the condition in part *a*? In other words, find the ratio of the rise time for $k = 1$ to the rise time for zero feedback.

14-10 (*a*) For the amplifier in Prob. 14-9, find the maximum value of the loop gain for which the step-response overshoot will be 10 percent.
(*b*) At what time will the peak occur?
(*c*) Calculate the magnitude of the first minimum of the step response and the time at which it occurs.
(*d*) Verify that for $k = 0.707$ the maximum overshoot is 4.3 percent.

14-11 An amplifier has two poles on the negative real axis: $s_1 = -5\ \mu s^{-1}$, $s_2 = -15\ \mu s^{-1}$.
(*a*) Plot the root locus of the amplifier with negative feedback.
(*b*) Find the value of βA_o for which the maximum overshoot of the amplifier step response with feedback is 4.3 percent.

14-12 (*a*) If $k = 0.5$ ($Q = 1$), calculate the percent maximum overshoot in the step response for a two-pole feedback amplifier.
(*b*) If there is a 10 percent overshoot in the frequency response, what is the percent overshoot in the step response?

14-13 The roots of a closed-loop two-pole amplifier are $s_1 = -\sigma + j\omega$, $s_2 = -\sigma - j\omega$. Find the relationship between Q and $|\omega/\sigma|$.

14-14 For the three-pole feedback amplifier, verify Eq. (14-29) and show that

$$\omega_o{}^3 = \omega_1\omega_2\omega_3(1 + \beta A_o)$$

$$a_2 = \frac{\omega_1 + \omega_2 + \omega_3}{\omega_o}$$

$$a_1 = \frac{\omega_1\omega_2 + \omega_2\omega_3 + \omega_1\omega_3}{\omega_o{}^2}$$

14-15 (*a*) Consider a three-pole open-loop transfer function with all three poles at $s = -\omega_1$. Find an expression for the closed-loop gain.
(*b*) Show that as negative feedback is added, one pole s_{3f} moves along the negative real axis while the other two poles become complex conjugates and move toward the right-hand complex plane, as indicated in Fig. 14-8.
(*c*) Verify that the system is unstable for $|\beta A_o| > 8$; and that for $|\beta A_o| = 8$, the poles s_{2f} and s_{3f} are $\pm j\omega_1\sqrt{3}$ and $s_{1f} = -3\omega_1$.

14-16 Consider the amplifier with a transfer function $A(s) = A_1/[s(s + 3)^2]$.
(*a*) Find the value of βA_1 corresponding to the breakaway point (the point in the complex plane where the real poles become complex).
(*b*) Find the value of βA_1 for which the amplifier with negative feedback becomes unstable.
(*c*) Plot approximately the root locus.

14-17 Consider a transfer function with three poles s_1, s_2, s_3. Find s_1, s_2, s_3 knowing that

$$|s_1| = |s_2| = |s_3| = 1$$

and the Q of the complex pole pair (s_2, s_3) is 1.

14-18 An amplifier has the following transfer function:

$$A(s) = \frac{A_o \times 7.2 \times 10^{-4}}{(s + 0.02)(s + 0.09)(s + 0.4)}$$

Feedback is applied to this amplifier. Find the poles and βA_o if the Q of the complex pole pair is 1.

14-19 (*a*) Verify that a two-pole feedback amplifier *cannot* have a closed-loop dominant pole if $Q > 0.4$.
(*b*) Find an expression for the maximum value of βA_o for which a closed-loop dominant pole exists.
(*c*) Calculate βA_o for $n = 4$. What is the physical interpretation of this result?

14-20 Verify Eq. (14-33), using Eqs. (14-32) and (14-31).

14-21 Verify the expression for R_M in Eq. (14-34).

14-22 Verify the expression for G_M in Eq. (14-40).

14-23 For the voltage-series feedback pair in Sec. 14-8 verify that a dominant pole exists and that A_{Vf} can be approximated by Eq. (14-47).

14-24 Show that for the dominant-pole-amplifier polar plot in Fig. 14-18
(*a*) The upper semicircle of the plot is the locus of βA for negative frequencies.
(*b*) The lower semicircle corresponds to positive frequencies.
(*c*) The points corresponding to $f = \pm f_H$ are at the midpoints of the two semicircles.

14-25 Consider a feedback amplifier for which the gain at low frequencies without feedback is given by Eq. (12-2).
(*a*) Show that the polar plot of the loop gain is a circle in the right half of the complex βA plane, as in Fig. 14-18.
(*b*) Show that the upper semicircle corresponds to values of $f > 0$, and that the lower semicircle corresponds to values of $f < 0$.

14-26 Consider a two-pole feedback amplifier for which the gain without feedback is given by Eq. (14-8). Sketch the polar plot of the loop gain βA (β is a real constant and $f_2 = 10f_1$) for this amplifier, indicating
(*a*) The section of the plot corresponding to $f > 0$ and that corresponding to $f < 0$.
(*b*) The points on the plot corresponding to $f = 0$; $f = \pm\infty$; $f = f_1 = \omega_1/2\pi$; $f = f_2 = \omega_2/2\pi$.

14-27 Sketch the polar plot of the loop gain βA for a three-pole feedback amplifier with a dc gain (without feedback). $A_o = -1{,}000$, and open-loop poles at $f_1 = 0.5$ MHz, $f_2 = 1$ MHz, and $f_3 = 2$ MHz, under the following conditions:
(*a*) $\beta = -0.005$ (*b*) $\beta = -0.02$
In each case indicate whether or not the closed-loop amplifier is stable.
(*c*) What is the maximum value of β for which the amplifier is stable?

14-28 A three-pole feedback amplifier has a dc gain without feedback of -10^4. All three open-loop poles are at $f = 2$ MHz.
(*a*) What is the maximum value of β for which the amplifier is stable?
(*b*) Assume that one of the poles is shifted to $f_1 = 100$ kHz.
Using the value of β found in part *a*, what is the gain margin of the modified circuit?

14-29 Verify Eq. (14-53) for the transfer function of the pole-zero-compensation network.

14-30 Pole-zero compensation is used, but the zero f_z of the compensating network does not exactly equal the lowest pole f_1 of the uncompensated amplifier.
(*a*) Choose $f_z = 1.1f_1$ and sketch on log-log paper the function

$$A = \frac{1 + j(f/f_z)}{1 + j(f/f_1)}$$

(*b*) Repeat part *a* if $f_z = 0.9f_1$.

14-31 A three-pole amplifier without feedback has a dc gain of -10^3 and poles located at $f_1 = 1$ MHz, $f_2 = 10$ MHz, and $f_3 = 30$ MHz. Dominant-pole compensation is applied to this amplifier.
(*a*) Find the location of the dominant pole so that the open-loop gain is first constant and then falls at a rate of -20 dB per decade for frequencies $f \leq 1$ MHz.
(*b*) What is the maximum value of β for which this compensated amplifier is stable?

14-32 Pole-zero compensation is used with an amplifier which has -10^3 dc gain and three poles at $f_1 = 1$ MHz, $f_2 = 10$ MHz, and $f_3 = 200$ MHz. The zero of the pole-zero network is selected to cancel the 1-MHz pole of the uncompensated amplifier.
(*a*) Find the pole of the compensating network so that the amplifier is stable with a 45° phase margin when $\beta = -0.1$.
HINT: Let $-|\beta|A_v A'_V = \underline{/-135°}$ at $f = 10$ MHz.
(*b*) What is the bandwidth of the compensated amplifier with feedback?

14-33 Verify Eq. (14-60) for the feedback factor of the phase-shift network of Fig. 14-29, assuming that this network does not load the amplifier. Prove that the phase shift of V'_f/V_o is 180° for $\alpha^2 = 6$ and that at this frequency $\beta = \frac{1}{29}$.

14-34 (*a*) For the network of Prob. 14-33, show that the input impedance is given by

$$Z_i = R\,\frac{1 - 5\alpha^2 - j(6\alpha - \alpha^3)}{3 - \alpha^2 - j4\alpha}$$

(*b*) Show that the input impedance at the frequency of the oscillator, $\alpha = \sqrt{6}$, is $(0.83 - j2.70)R$.

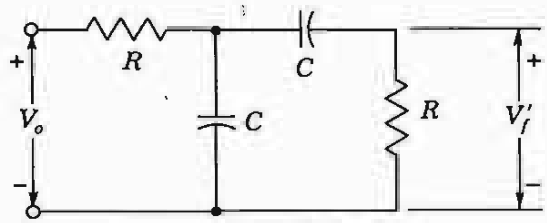
Note that if the frequency is varied by varying C, the input impedance remains constant. However, if the frequency is varied by varying R, the impedance is varied in proportion to R.

14-35 Design a phase-shift oscillator to operate at a frequency of 5 kHz. Use a MOSFET with $\mu = 55$ and $r_d = 5.5$ K. The phase-shift network is not to load down the amplifier.
(*a*) Find the minimum value of the drain-circuit resistance R_d for which the circuit will oscillate.
(*b*) Find the product RC.
(*c*) Choose a reasonable value for R, and find C.

14-36 (*a*) A two-stage FET oscillator uses the phase-shifting network shown. Prove that

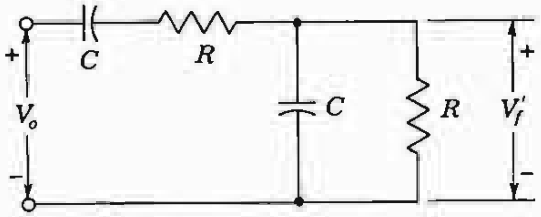
$$\frac{V_i}{V'_f} = \frac{1}{3 + j(\omega RC - 1/\omega RC)}$$

(*b*) Show that the frequency of oscillation is $f = 1/2\pi RC$ and that the gain must exceed 3.



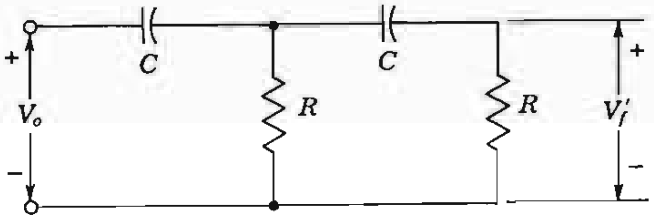
Prob. 14-36

14-37 (*a*) Find V_i/V_f' for the network shown.
(*b*) Sketch the circuit of a phase-shift FET oscillator, using this feedback network.
(*c*) Find the expression for the frequency of oscillation, assuming that the network does not load down the amplifier.
(*d*) Find the minimum gain required for oscillation.



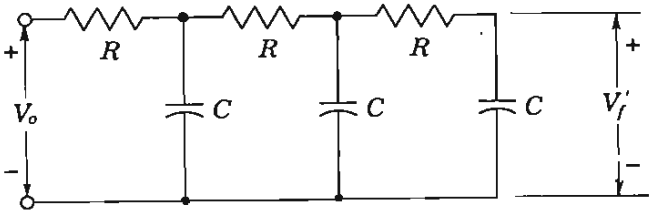
Prob. 14-37

14-38 Consider the two-section RC network shown. Find the V_i/V_f' function, and verify that it is not possible to obtain 180° phase shift with a finite attenuation.



Prob. 14-38

14-39 For the feedback network shown find (*a*) the transfer function, (*b*) the input impedance. (*c*) If this network is used in a phase-shift oscillator, find the frequency of oscillation and the minimum amplifier voltage gain. Assume that the network does not load down the amplifier.

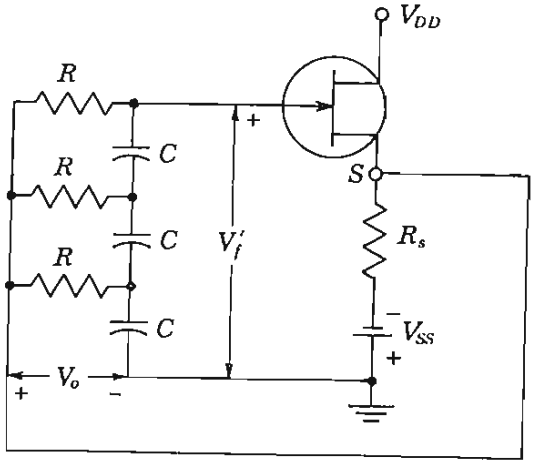


Prob. 14-39

14-40 Take into account the loading of the RC network in the phase-shift oscillator of Fig. 14-29a. If R_o is the output impedance of the amplifier (assume that C_s is arbitrarily large), prove that the frequency of oscillation f and the minimum gain A are given by

$$f = \frac{1}{2\pi RC}\frac{1}{\sqrt{6 + 4(R_o/R)}} \qquad A = 29 + 23\frac{R_o}{R} + 4\left(\frac{R_o}{R}\right)^2$$

14-41 For the FET oscillator shown, find (a) V_f'/V_o, (b) the frequency of oscillations, (c) the minimum gain of the source follower required for oscillations.



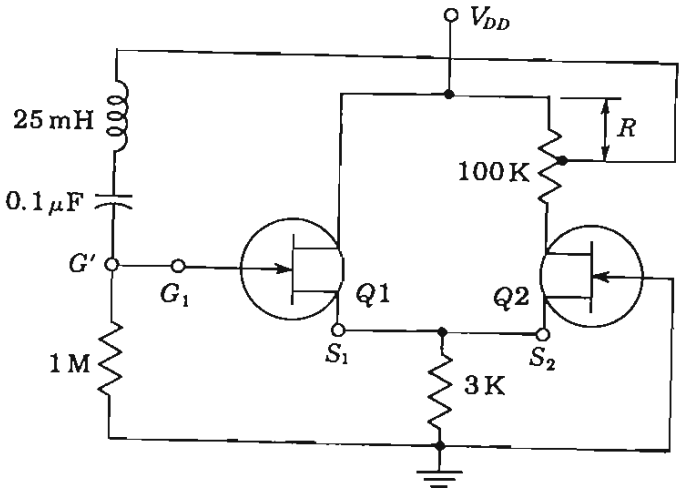
Prob. 14-41

14-42 Verify Eqs. (14-61) and (14-62) for the transistor phase-shift oscillator of Fig. 14-30.

14-43 Apply the Barkhausen criterion to the tuned-drain oscillator, and verify Eqs. (14-63) and (14-64).

14-44 (a) At what frequency will the circuit shown oscillate, if at all?
(b) Find the minimum value of R needed to sustain oscillations. The FETs are identical with $g_m = 1.6$ mA/V and $r_d = 44$ K.

HINT: Assume a voltage V from gate G_1 of $Q1$ to ground but with the point G' not connected to the gate G_1. Calculate the loop gain from the equivalent circuit, obtained by looking into each source.



Prob. 14-44

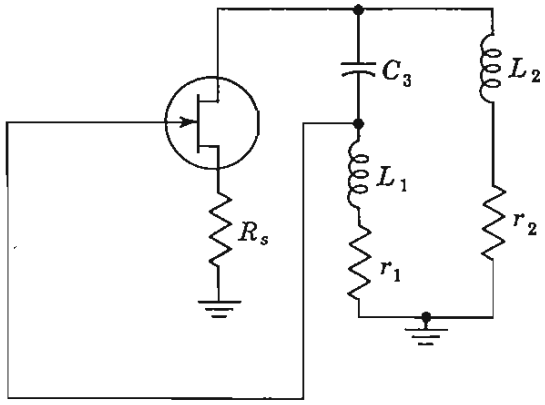
14-45 (*a*) Consider a Colpitts oscillator, using the circuit of Fig. 14-32 and taking into account the resistance r_3 in series with the inductor L_3. Show that the frequency of oscillation is given by

$$\omega^2 = \frac{1}{L_3}\left[\frac{1}{C_1} + \frac{1}{C_2}\left(1 + \frac{r_3}{R_o}\right)\right]$$

(*b*) If $r_3/R_o \ll 1$, show that the minimum amplifier gain required for oscillations is

$$A_v = \frac{C_1}{C_2} + \frac{C_2 + C_1}{L_3} R_o r_3$$

14-46 (*a*) Consider the Hartley oscillator circuit shown (with bias and power supplies omitted for simplicity). If the resistances of the inductors are r_1 and r_2, respectively, find the frequency of oscillation.
(*b*) Find the value of R_s for which the value of the loop gain will just equal unity.



Prob. 14-46

14-47 In the Wien bridge circuit of Fig. 14-34, add an inductor in series with R and C between points 2 and 3. Also, replace the parallel combination of R and C by a resistor R_3. Find the frequency of oscillation and the minimum gain of the amplifier if
(*a*) R_1 is infinite.
(*b*) R_1 is finite.

14-48 (*a*) Verify Eq. (14-75) for the reactance of a crystal.
(*b*) Prove that the ratio of the parallel- to series-resonant frequencies is given approximately by $1 + \frac{1}{2}C/C'$.
(*c*) If $C = 0.04$ pF and $C' = 2.0$ pF, by what percent is the parallel-resonant frequency greater than the series-resonant frequency?

14-49 A crystal has the following parameters: $L = 0.33$ H, $C = 0.065$ pF, $C' = 1.0$ pF, and $R = 5.5$ K.
(*a*) Find the series-resonant frequency.
(*b*) By what percent does the parallel-resonant frequency exceed the series-resonant frequency?
(*c*) Find the Q of the crystal.

CHAPTER 15

15-1 Verify Eqs. (15-2) and (15-3).

15-2 Find an expression for A_{Vf} in Fig. 15-3 by using feedback concepts. Show that this expression agrees with Eq. (15-2) if $A_v \gg R_o Y'$.

15-3 The amplifier shown uses an OP AMP with input resistance R_i, voltage gain $A_v < 0$, and zero output resistance. Assume also that the OP AMP is unilateral from input to output.

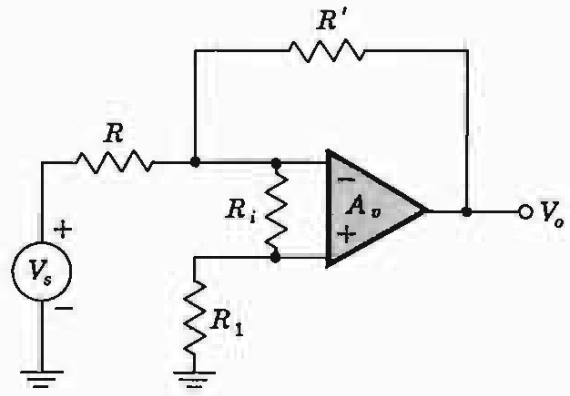
(*a*) Show that the amplifier satisfies the three fundamental assumptions of Sec. 13-2.

(*b*) Show that the transresistance of the amplifier without feedback is

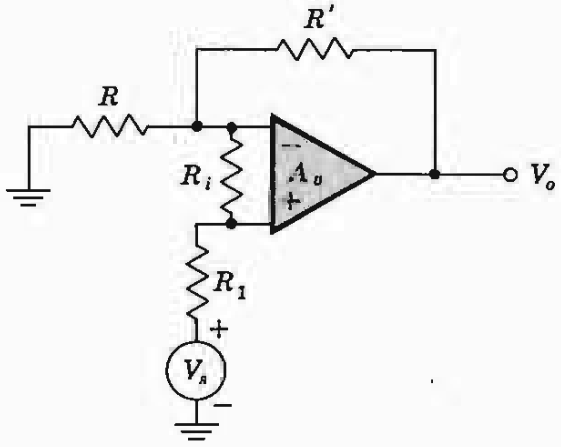
$$\frac{A_v R_i R R'}{RR' + (R_i + R_1)(R + R')}$$

(*c*) Show that

$$A_{Vf} = \frac{V_o}{V_s} = \frac{A_v R_i R'}{RR' + (R_i + R_1)(R + R') - A_v R_i R}$$



Prob. 15-3



Prob. 15-4

15-4 (*a*) Repeat Prob. 15-3 for the noninverting amplifier shown.

(*b*) Show that the voltage gain of the amplifier without feedback is

$$A_V = \frac{-A_v R_i (R + R')}{(R + R')(R_1 + R_i) + RR'}$$

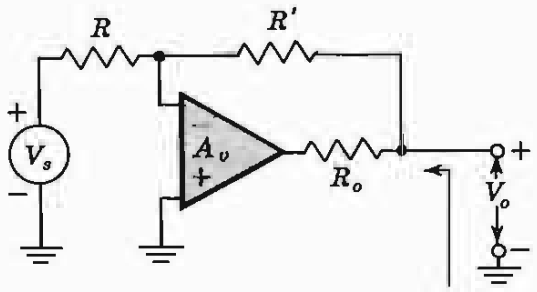
(*c*) Show that

$$A_{Vf} = \frac{-A_v R_i (R + R')}{RR' + (R_i + R_1)(R + R') - A_v R R_i} = \frac{V_o}{V_s}$$

15-5 For the circuit of this problem with $R_i = \infty$, show

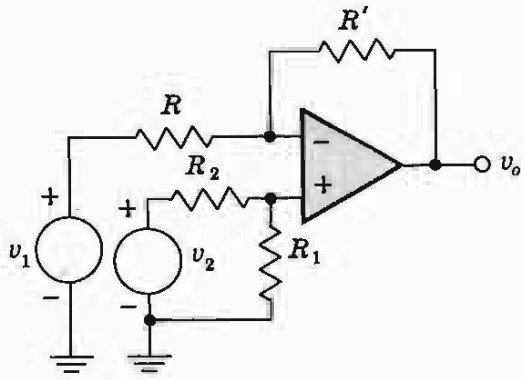
$$Y_{of} = \frac{1}{R_o}\left(1 - A_v \frac{R}{R + R'}\right) + \frac{1}{R + R'}$$

Prob. 15-5

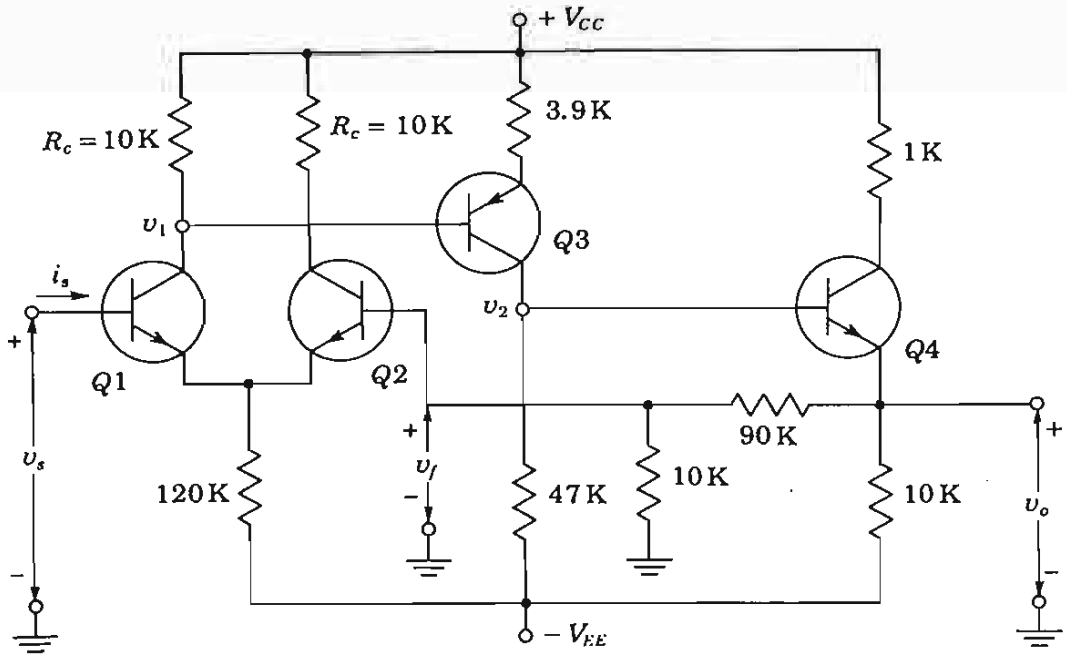


15-6 The circuit shown is a differential amplifier using an ideal OP AMP.
(*a*) Find the output voltage v_o.
(*b*) Show that the output corresponding to the common-mode voltage $v_c = \frac{1}{2}(v_1 + v_2)$ is equal to zero if $R'/R = R_1/R_2$. Find v_o in this case.
(*c*) Find the common-mode rejection ratio of the amplifier if $R'/R \neq R_1/R_2$.

Prob. 15-6



15-7 The circuit shown represents a dc feedback amplifier consisting of a differential input pair *Q*1-*Q*2 followed by two stages, *Q*3 and *Q*4.



Prob. 15-7

All transistors are identical, and their parameters are

$$h_{ie} = 1 \text{ K} \qquad h_{oe} = 10\ \mu\mho \qquad h_{re} = 2.5 \times 10^{-4} \qquad h_{fe} = 100$$

Make reasonable approximations resulting in errors of no more than 10 percent. Compute the following quantities at low frequencies.

(*a*) The difference gain A_d and common-mode gain A_c for the differential amplifier defined by the equation

$$v_1 = A_d(v_f - v_s) + A_c \frac{v_f + v_s}{2}$$

Make use of the symmetry of the circuit.

(*b*) v_2/v_1, v_o/v_2, and $A = v_o/v_1$. Assume that $Q2$ does not load the 10-K resistance.

(*c*) $A_V = v_o/v_s$. Compare this result with that obtained using the feedback factor β.

15-8 For the circuit of Fig. 15-6 assume that $R_s = 0$, $h_{oe}(R_c + 2R_e) \ll 1$, $h_{fe} \gg 1$, and $h_{ie} \ll 2R_e h_{fe}$.

(*a*) Verify that the common-mode rejection ratio is given by

$$\rho = \frac{h_{fe}R_e}{h_{ie}}$$

(*b*) If $r_{bb'} \ll r_{b'e}$ verify that $\rho = g_m R_e \approx V/2V_T$, where V is the quiescent voltage across R_e.

15-9 Draw the *h*-parameter model for the common-mode gain in a DIFF AMP. *Without* solving for A_c show from the circuit that A_c must be zero if $h_{fe}/h_{oe} = 2R_e$ [in agreement with Eq. (15-13)].

15-10 Verify Eqs. (15-13) and (15-14) for the difference amplifier.

15-11 Starting with Eq. (15-13) for A_d and assuming $R_s \ll h_{ic}$ and $r_{bb'} \ll r_{b'e}$, verify that

$$A_d = \frac{1}{2} g_m R_c \qquad \text{and} \qquad g_{md} = \frac{I_o}{4V_T}$$

15-12 (*a*) Show that the emitter volt-ampere characteristic of a transistor in the active region is given by

$$I_E \approx I_S \epsilon^{V_E/V_T}$$

where $I_S = -I_{EO}/(1 - \alpha_N \alpha_I)$.

(*b*) Verify Eq. (15-22) for the transfer characteristic of the DIFF AMP.

(*c*) Verify Eq. (15-23) for g_{md}.

15-13 (*a*) From Eq. (15-22), for the transfer characteristic of the DIFF AMP find the range $\Delta V = \Delta(V_{B1} - V_{B2})$ over which each collector current increases from 0.1 to 0.9 its peak value.

(*b*) Repeat part *a* for a collector-current variation from 50 to 99 percent of I_o.

(*c*) Compare your result with Fig. 15-9.

15-14 The differential amplifier of Fig. 15-8 is modified by putting two resistors R_e in series with the emitter lead of $Q1$ and $Q2$.

(*a*) Express $V_{B1} - V_{B2}$ as a function of $V_{BE1} - V_{BE2}$ and I_{C1}.
(*b*) Find the transfer characteristic I_{C1}/I_O versus $(V_{B1} - V_{B2})/V_T$ if $R_e = 50\ \Omega$ and $I_O = 2$ mA. Solve *graphically* by using Fig. 15-9 and part *a*.
(*c*) Find the transconductance

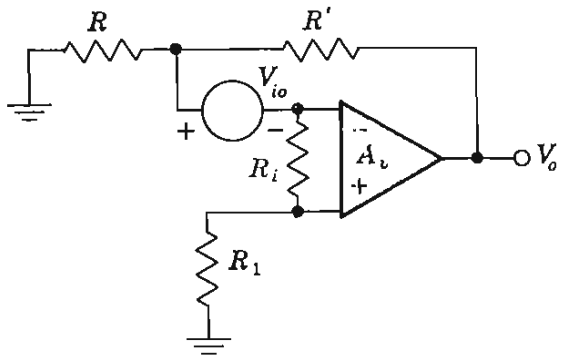
$$g'_{md} = \frac{dI_{C1}}{d(V_{B1} - V_{B2})}$$

evaluated at $V_{B1} = V_{B2}$.
(*d*) Express g'_{md} in terms of g_{md} given in Eq. (15-23).

15-15 (*a*) Calculate the common-mode rejection ratio ρ_1 for the first stage of the OP AMP in Fig. 15-11. Assume $1/h_{oe} = 100$ K and $h_{re} = 2.5 \times 10^{-4}$.
(*b*) Calculate ρ_2 for the second stage.
(*c*) What is the overall ρ (in decibels)?

15-16 The figure shows an inverting OP AMP with input resistance R_i and offset voltage V_{io}. Show that V_o is given by

$$V_o = \frac{-A_v R_i (R + R') V_{io}}{RR' + (R_i + R_1)(R + R') - RR_i A_v}$$



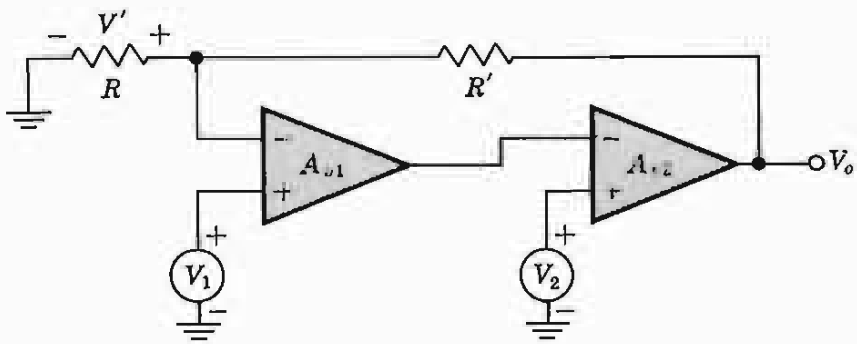
Prob. 15-16

15-17 For the amplifier shown, V_1 and V_2 represent undesirable voltages. Show that, if $R_i = \infty$, $R_o = 0$, and $A_{v1} < 0$ and $A_{v2} < 0$,

$$V_o = A_{v2}[A_{v1}(V' - V_1) - V_2] \qquad \text{where } V' = V_o \frac{R}{R + R'}$$

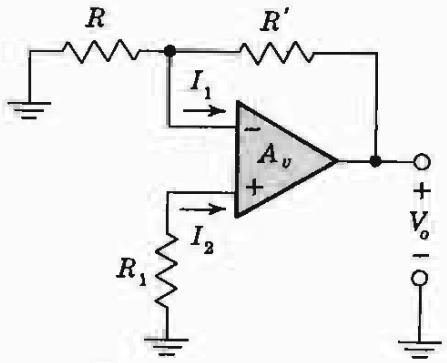
Show also that, if $A_{v2}A_{v1}R/(R + R') \gg 1$,

$$V_o = -\left(1 + \frac{R'}{R}\right)\left(V_1 + \frac{V_2}{A_{v1}}\right)$$

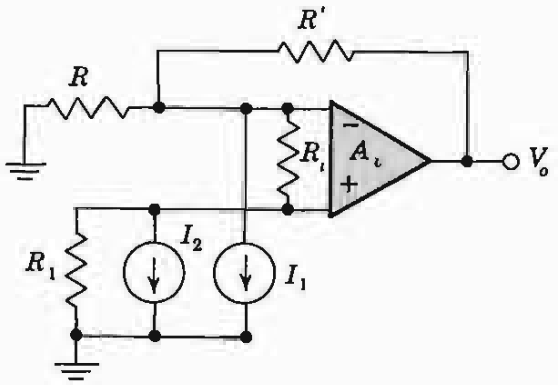


Prob. 15-17

15-18 Consider the circuit shown. An attempt is made to find a value of R_1 which minimizes the offset-current effects.
(*a*) First show that $V_o = 0$ if $I_1[RR'/(R + R')] = I_2R_1$.
(*b*) Conclude that $R_1 = RR'/(R + R')$ is the optimum value of R_1 if $I_1/I_2 \approx 1$. Find V_o in this case. Assume $R_o = 0$.



Prob. 15-18



Prob. 15-19

15-19 (*a*) For the amplifier shown (with $R_o = 0$) prove that
(i) The output voltage V_{o1} due to the bias current I_1 is

$$V_{o1} = \frac{-R'RR_iA_v}{(R_i + R_1)(R' + R) + RR' - A_vRR_i} I_1$$

(ii) The output voltage V_{o2} due to the bias current I_2 is

$$V_{o2} = \frac{R_iR_1(R + R')A_v}{(R + R')(R_1 + R_i) - A_vRR_i + RR'} I_2$$

(*b*) Show that if $I_1/I_2 \approx 1$, then $V_{o1} + V_{o2}$ is minimized by taking $R_1 = RR'/(R + R')$.

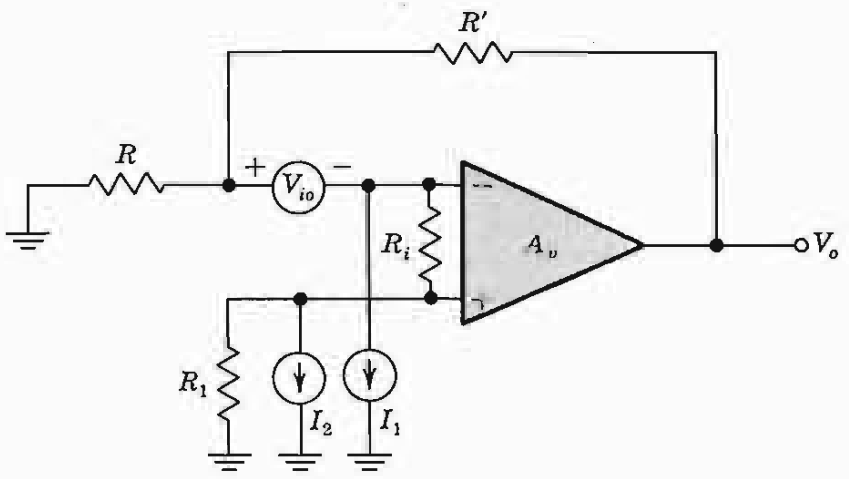
15-20 (*a*) Show that the gain A_{VfI} of the inverting OP AMP and the gain A_{VfNI} of the noninverting amplifier satisfy (assume $R_o = 0$)

$$\frac{A_{VfI}}{A_{VfNI}} = -\frac{R'}{R + R'}$$

HINT: Use the results of Probs. 15-3 and 15-4.
(*b*) Using (*a*), show that the input biasing currents I_1 and I_2 and the input offset voltage V_{io} produce an effective input error voltage V_{EI} on the inverting terminal equal to

$$V_{EI} = -I_1R + \frac{R + R'}{R'} R_1I_2 - V_{io}\frac{R + R'}{R'}$$

(*c*) Plot the curve $V_{EI} = f(R')$ for $R_1 = RR'/(R + R')$, $R = 1$ K, and typical values of V_{io} and $I_2 - I_1$ (Table 15-1).



Prob. 15-20

15-21 (*a*) Repeat part *b* of Prob. 15-20 and show that the input offset signals produce an effective input error voltage V_{ENI} on the noninverting terminal equal to

$$V_{ENI} = V_{io} - R_1 I_2 + I_1 \frac{RR'}{R + R'}$$

(*b*) Repeat parts *c* and *d* of Prob. 15-20.

15-22 Consider the inverting OP AMP of Prob. 15-20 with infinite open-loop gain and with an output-voltage swing of ±4.5 V.
(*a*) Plot the output voltage due to V_{io} as a function of R'/R.
(*b*) Plot the output voltage due to the biasing currents I_1 and I_2 as a function of R' (i) if $R_1 = RR'/(R + R')$, (ii) if $R_1 = 0$. Use typical values for the offset signals.

15-23 The input offset voltage V_{io} of an OP AMP is equal to 1 mV at 25°C. The input offset-voltage drift of this amplifier is equal to 5 μV/°C. Assume that the open-loop voltage gain is infinite. Using Prob. 15-16, find the output offset voltage at temperature $T = 100$°C if (i) $R'/R = 1$, (ii) $R'/R = 100$. At which temperature is the output offset voltage equal to 0.2 V if $R'/R = 200$?

15-24 (*a*) For the inverting OP AMP with $R_i = \infty$, draw the model of the amplifier without feedback but taking the loading of R' into account (Sec. 13-7). Refer to Fig. 15-2 with $Z = R$ and $Z' = R'$.
(*b*) Verify that $\beta = -1/R'$ and $R_M = A_V R_{11}$, where $R_{11} = R \| R'$.
(*c*) Verify that

$$A_{Vf} = \frac{R_{Mf}}{R} = \frac{R_M/R}{1 + \beta R_M}$$

and show that this expression reduces to Eq. (15-35).

15-25 (*a*) For the noninverting OP AMP of Fig. 15-4 with $R_i = \infty$, draw the model of the amplifier without feedback but taking the loading of R' into account.
(*b*) Verify that $\beta = R/(R + R')$.
(*c*) Find A_{Vf}.

15-26 Without using feedback-amplifier concepts, verify that A_{Vf} for the inverting OP AMP of Prob. 15-24 is given by Eq. (15-35).

15-27 Without using feedback concepts, verify that A_{vf} for the noninverting OP AMP of Prob. 15-25 is given by Eq. (15-38).

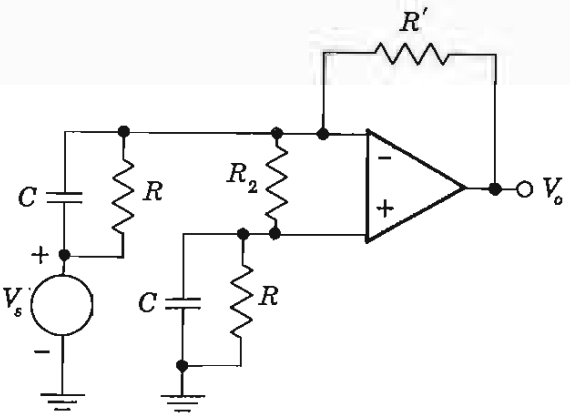
15-28 (*a*) The transfer function of an OP AMP has its first pole at 1 MHz and a low-frequency gain of 44 dB. Dominant-pole compensation is used for this OP AMP, and the gain of the compensated amplifier is zero dB at a frequency 1 MHz. Find the value f_d of the dominant pole.
(*b*) Repeat (*a*) if the low-frequency gain is 68 dB.

15-29 (*a*) In Fig. 15-11 find the resistance R_i seen between pins 9 and 10. Assume $1/h_{oc} = 100$ K and $h_{re} = 0$.
(*b*) A capacitor C_1 is connected between pins 9 and 10. For which value of C_1 is the first pole of the compensated amplifier equal to (i) $f_d = 200$ Hz, (ii) $f_d = 1$ kHz?

15-30 (*a*) Verify Eq. (15-41).
(*b*) Draw on the same figure the following Bode plots:
(i) Open-circuit voltage gain of the amplifier without compensation.
(ii) Open-circuit voltage gain of the amplifier if pole-zero cancellation is achieved, using Eq. (15-41).
In (i) assume that the amplifier has three poles.

15-31 In Prob. 15-30 the transfer function of the amplifier without compensation has three poles at 1, 4, and 40 MHz and a low-frequency open-loop gain of 72 dB.
(*a*) Find R_c and C_c as a function of R_1, R, R' if the gain of the compensated amplifier is zero dB at a frequency 4 MHz.
(*b*) Find R_c and C_c if $R_1 = RR'/(R + R')$, $R = 1$ K, and $R' \gg R$. Find also the bandwidth of the compensated amplifier without feedback.

15-32 (*a*) Show that pole-zero cancellation can be achieved by using the input circuit of the figure. Use the result of Prob. 15-3(*b*) and assume $R_i = \infty$.
(*b*) Draw the Bode plots of the open-loop gain for the compensated and the uncompensated amplifier. Assume that the OP AMP has three poles and that $R_2 \ll R$.



Prob. 15-32

15-33 Verify all the equations in Sec. 15-11 which relate to pole-zero cancellation using the Miller effect technique.

15-34 Verify Eq. (15-50) for the factor A introduced due to C' in Fig. 15-24.

15-35 The slew rate of an OP AMP is 6 V/μs when the closed-loop gain is unity. The amplified output signal is observed to be a pure sinusoid $v_o = V_m \cos \omega t$ provided the frequency of this signal does not exceed a certain limit.

Find the value of this limiting frequency before the output signal is distorted by the slew-rate limit if (*a*) $V_m = 1$ V, (*b*) $V_m = 10$ V.

CHAPTER 16

16-1 Design the circuit of Fig. 16-1 so that the output V_o (for a sinusoidal signal) is equal in magnitude to the input V_s and leads the input by 45°.

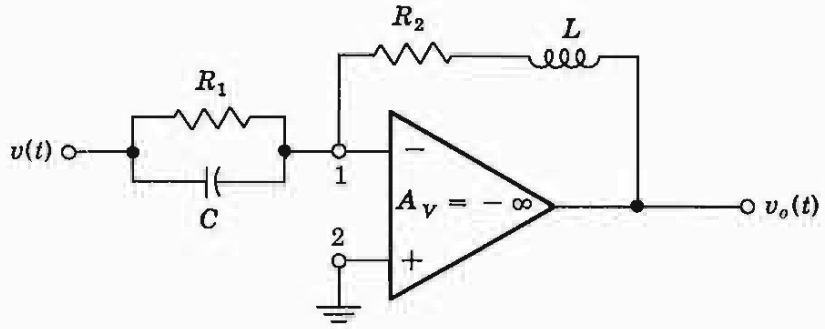
16-2 Consider the circuit of Fig. 16-1 with $A_V = -100$. If $Z = R$ and $Z' = -jX_C$ with $R = X_C$ at some specific frequency f, calculate the gain V_o/V_s as a complex number.

16-3 Given the operational amplifier circuit of Fig. 16-1 consisting of R and L in series for Z, and C for Z'. If the input voltage is a constant $v_s = V$, find the output v_o as a function of time. Assume an infinite open-loop gain.

16-4 For the given circuit, show that the output voltage is

$$-v_o = \frac{R_2}{R_1} v + \left(R_2 C + \frac{L}{R_1}\right)\frac{dv}{dt} + LC\frac{d^2v}{dt^2}$$

Prob. 16-4



16-5 Consider the operational amplifier circuit of Fig. 16-1 with Z consisting of a resistor R in parallel with a capacitor C, and Z' consisting of a resistor R'. The input is a sweep voltage $v = \alpha t$. Show that the output voltage v_o is a sweep voltage that starts with an initial step. Thus prove that

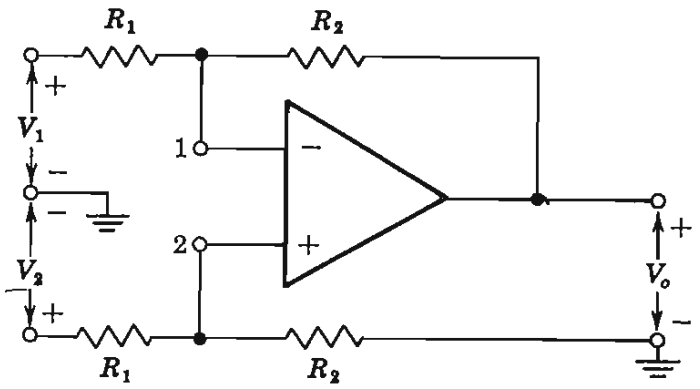
$$v_o = -\alpha R'C - \alpha \frac{R'}{R} t$$

Assume infinite open-loop gain.

16-6 Consider the operational amplifier circuit of Fig. 16-1 with Z consisting of a 100-K resistor and a series combination of a 50-K resistance with a 0.001-μF capacitance for Z'. If the capacitor is initially uncharged, and if at $t = 0$ the input voltage $v_s = 10\epsilon^{-t/\tau}$ with $\tau = 5 \times 10^{-4}$ s is applied, find $v_o(t)$.

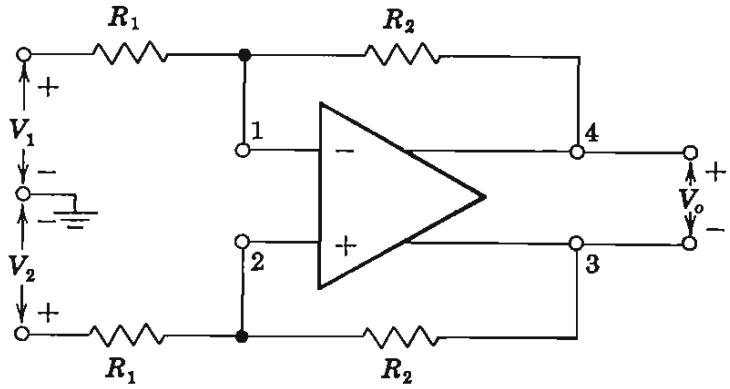
16-7 In Fig. 16-3*b* show that i_L is equal to $-v_s/R_2$ if $R_1/R_2 = R'/R_1$.

16-8 The differential input operational amplifier shown consists of a base amplifier of infinite gain. Show that $V_o = (R_2/R_1)(V_2 - V_1)$.



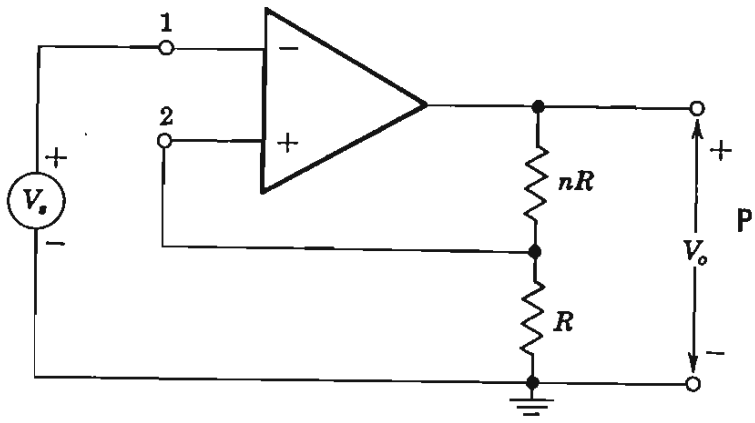
Prob. 16-8

16-9 Repeat Prob. 16-8 for the amplifier shown.



Prob. 16-9

16-10 For the base differential-input amplifier shown, assume infinite input resistance, zero output resistance, and finite differential gain $A_V = V_o/(V_1 - V_2)$.
(*a*) Obtain an expression for the gain $A_{Vf} = V_o/V_s$.
(*b*) Show that $\lim A_{Vf} = n + 1$, $A_V \to \infty$.



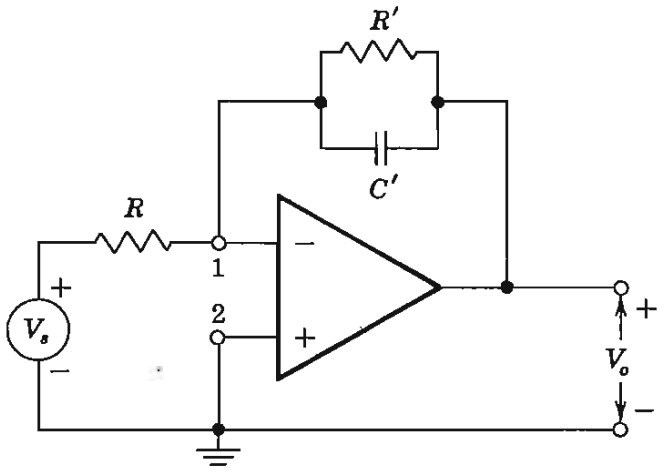
Prob. 16-10

16-11 Verify Eq. (16-6) for the bridge amplifier.

16-12 The circuit shown represents a low-pass dc-coupled amplifier. Assuming an

ideal operational amplifier determine (*a*) the high-frequency 3-dB point f_H; (*b*) the low-frequency gain $A_V = V_o/V_s$.

Prob. 16-12



16-13 (*a*) The input to the operational integrator of Fig. 16-10 is a step voltage of magnitude V. Show that the output is

$$v_o = A_V V(1 - \epsilon^{-t/RC(1-A_V)})$$

(*b*) Compare this result with the output obtained if the step voltage is impressed upon a simple RC integrating network (without the use of an operational amplifier). Show that for large values of RC, both solutions represent a voltage which varies approximately linearly with time. Verify that if $-A_V \gg 1$, the slope of the ramp output is approximately the same for both circuits. Also prove that the deviation from linearity for the amplifier circuit is $1/(1 - A_V)$ times that of the simple RC circuit.

16-14 Derive Eq. (16-13).

16-15 (*a*) The input to an operational differentiator whose open-loop gain $A_V \equiv A$ is infinite is a ramp voltage $v = \alpha t$. Show that the output is

$$v_o = \frac{A}{1 - A} \alpha RC(1 - \epsilon^{-t(1-A)/RC})$$

(*b*) Compare this result with that obtained if the same input is impressed upon a simple RC differentiating network (without the use of an amplifier). Show that, approximately, the same final constant output $RC\, dv/dt$ is obtained. Also show that the operational-amplifier output reaches this correct value of the differentiated input much more quickly than does the simple RC circuit.

16-16 Given an operational amplifier with Z consisting of R in series with C, and Z' consisting of R' in parallel with C'. The input is a step voltage of magnitude V. (*a*) Show by qualitative argument that the output voltage must start at zero, reach a maximum, and then again fall to zero.

(*b*) Show that if $R'C' \neq RC$, the output is given by

$$v_o = \frac{R'CV}{R'C' - RC}(\epsilon^{-t/RC} - \epsilon^{-t/R'C'})$$

16-17 Sketch an operational amplifier circuit having an input v and an output which is approximately $-5v - 3dv/dt$. Assume an ideal operational amplifier.

16-18 Sketch in block-diagram form a computer, using operational amplifiers, to solve the differential equation

$$\frac{dv}{dt} + 0.5v + 0.1 \sin \omega t = 0$$

An oscillator is available which will provide a signal sin ωt. Use only resistors and capacitors.

16-19 Set up a computer in block-diagram form, using operational amplifiers, to solve the following differential equation:

$$\frac{d^3y}{dt^3} + 2\frac{d^2y}{dt^2} - 4\frac{dy}{dt} + 2y = x(t)$$

where

$$y(0) = 0 \qquad \left.\frac{dy}{dt}\right|_{t=0} = -2 \qquad \text{and} \qquad \left.\frac{d^2y}{dt^2}\right|_{t=0} = 3$$

Assume that a generator is available which will provide the signal $x(t)$.

16-20 (*a*) Verify that the damping factor of each pair of complex poles of a Butterworth low-pass filter is given by $k = \cos \theta$, where θ is defined in Fig. 16-17.
(*b*) Define a damping factor k for the single pole at $s = -1$ which is consistent with Eq. (16-23).

16-21 Verify the entries in Table 16-1 for $n = 3$ by using Fig. 16-17*b*.

16-22 Using Eq. (16-22), show that the transfer function of a second-order Butterworth low-pass filter satisfies Eq. (16-19).

16-23 Use the value of $P_2(s)$ from Table 16-1 and verify that

$$P_2(s)P_2(-s)\Big|_{s=j\omega} = 1 + \omega^4$$

16-24 Use the values of $P_3(s)$ from Table 16-1 and verify that

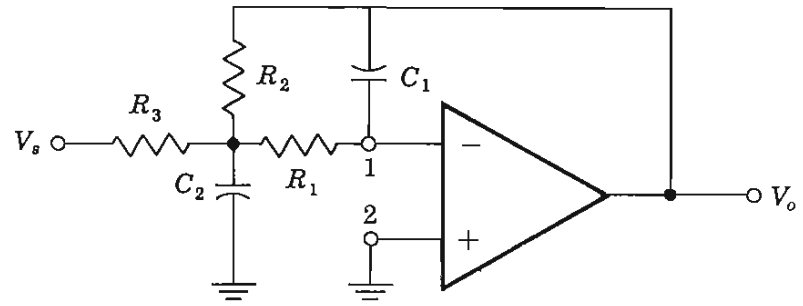
$$P_3(+s)P_3(-s)\Big|_{s=j\omega} = 1 + \omega^6$$

16-25 Show that the voltage gain $A_V(s) = V_o/V_s$ in Fig. 16-18*a* is given by Eq. (16-24). HINT: Use feedback principles.

16-26 Design an active sixth-order Butterworth low-pass filter with a cutoff frequency (or upper 3-dB frequency) of 1 kHz.

16-27 The circuit shown uses an ideal OP AMP.
(*a*) Find the voltage gain $A_V = V_o/V_s$, the damping factor k, and the cutoff frequency ω_o.
(*b*) Using this circuit. design a second-order Butterworth low-pass filter with $f_o = 1$ kHz and low-frequency voltage gain equal to -1.

Prob. 16-27



16-28 Define the z parameters of a two-port network by the following relations:

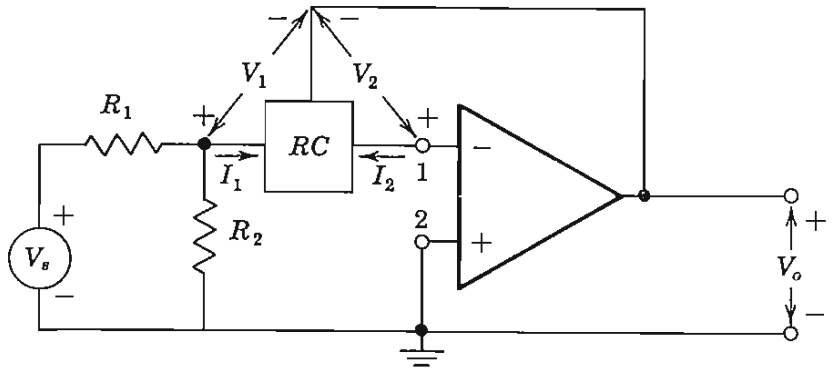
$$V_1 = z_{11}I_1 + z_{12}I_2$$
$$V_2 = z_{21}I_1 + z_{22}I_2$$

For the circuit shown prove that the voltage gain $A_V = V_o/V_s$ is given by

$$\frac{V_o}{V_s} = -\frac{R_2 z_{21}}{(R_1 + R_2)(z_{11} - z_{21}) + R_1 R_2}$$

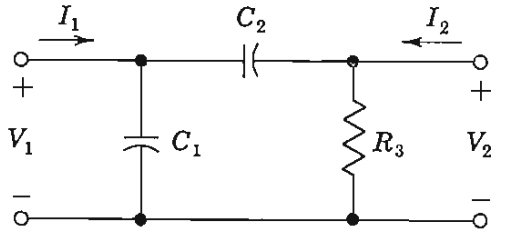
where z_{11} and z_{21} are the z parameters of the RC network.

Prob. 16-28



16-29 The network shown is the RC network of Prob. 16-28.
(*a*) Find the parameters z_{11} and z_{21} of this network.
(*b*) Find the voltage gain V_o/V_s of the amplifier in Prob. 16-28 if this RC network is used.

Prob. 16-29



16-30 Design a second-order active RC bandpass filter that has a midband voltage gain of 40 dB, center frequency of 100 Hz, and no specified bandwidth. However, the circuit must provide at least 20-dB rejection one decade from the center frequency and hold phase shift to $\pm 10°$ maximum for 10 percent change

from the center frequency. HINT: Use Fig. 16-22 to find Q and let $R_2 = \infty$, $R_1 = 1$ K.

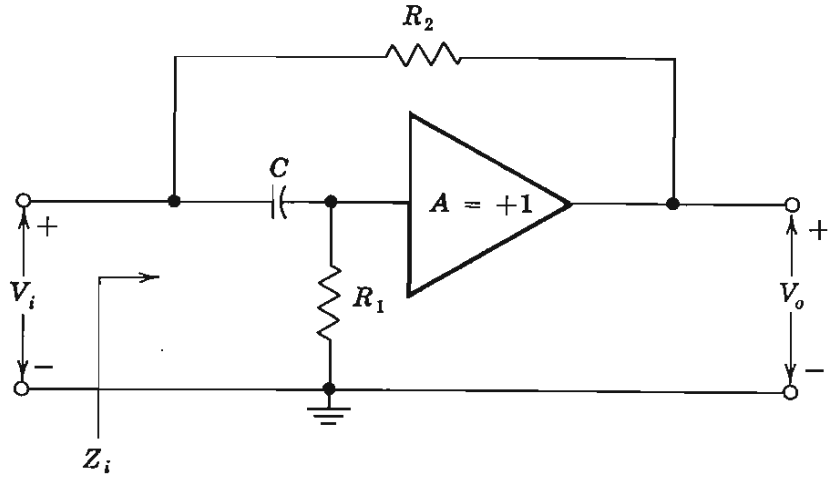
16-31 Design a bandpass RC active filter with midband voltage gain of 30, center frequency of 200 Hz, and $Q = 5$. HINT: Choose $C_1 = C_2 = 0.1\ \mu$F.

16-32 Design the resonant RLC bandpass filter of Fig. 16-21 with $f_o = 160$ Hz, 3-dB bandwidth $B = 16$ Hz, and minimum input resistance seen by the voltage source V_s of 1,000 Ω. Is this a practical circuit?

16-33 Verify Eq. (16-50) for the transfer function of the delay equalizer of Fig. 16-24*a*.

16-34 (*a*) Show that the circuit of the accompanying figure can simulate a grounded inductor if $R_1 > R_2$. In other words, show that the reactive part of the input impedance of this circuit is positive if $R_1 > R_2$.
(*b*) Find the frequency range in which the $Q = \omega L/R$ of the inductor is greater than unity.

Assume that the unity gain amplifier has infinite input resistance and zero output resistance.

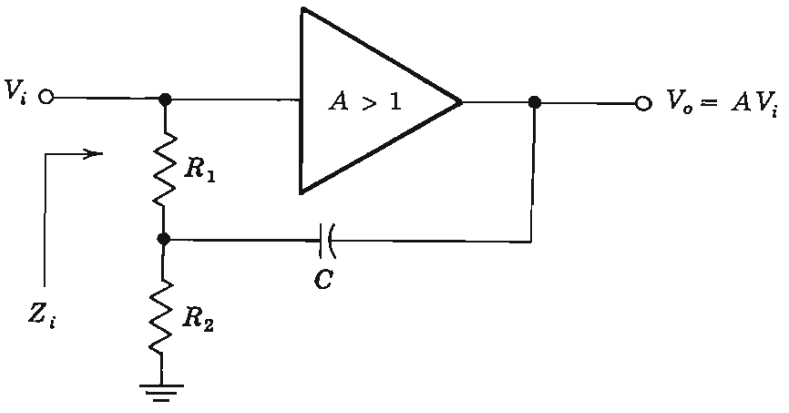


Prob. 16-34

16-35 (*a*) Show that the circuit of the given figure can simulate a grounded inductor if $A > 1$. In other words, show that the reactive part of Z_i is positive.
(*b*) Show that the real part of Z_i becomes zero ($Q = \infty$) at the frequency

$$\omega = \frac{1}{R_2 C}\sqrt{\frac{R_1 + R_2}{R_1(A - 1)}}$$

Assume that the input resistance of the amplifier of gain A is infinite.



Prob. 16-35

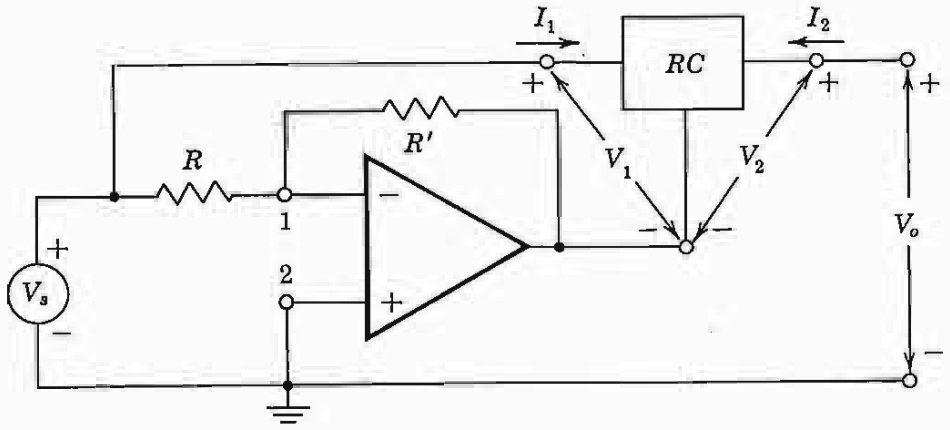
16-36 Using Fig. 16-27*b*, derive Eqs. (16-54) and (16-55).

16-37 Using Fig. 16-27*b*, derive Eqs. (16-57) and (16-58).

16-38 The figure shows a circuit using an ideal OP AMP and an *RC* two-port network. The *RC* two-port is defined in terms of its *y* parameters (Sec. 16-9). Show that the voltage gain $A_V = V_o/V_s$ is given by

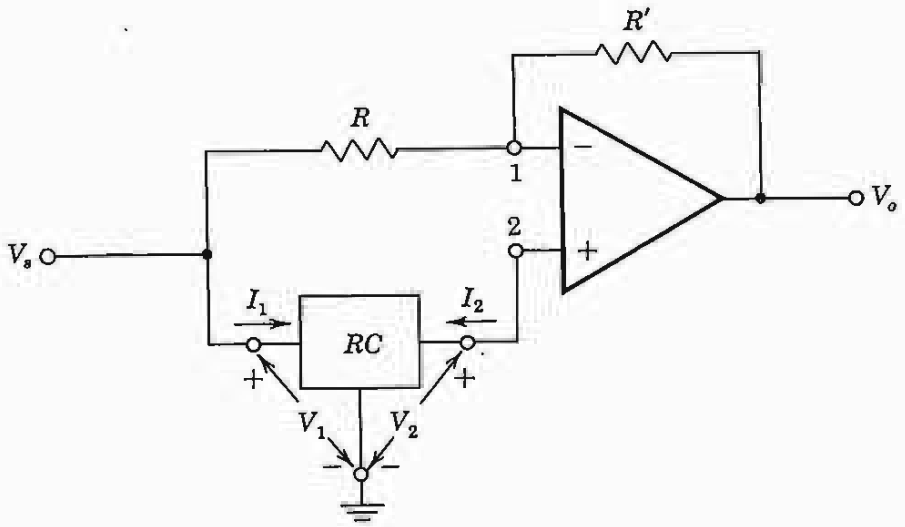
$$A_V = \frac{V_o}{V_s} = -\frac{y_{21}(1+k) + ky_{22}}{y_{22}} \qquad \text{where } k = \frac{R'}{R}$$

Prob. 16-38



16-39 Repeat Prob. 16-38 for the circuit shown. Show that the expression for $A_V = V_o/V_s$ is the same as in Prob. 16-38.

Prob. 16-39

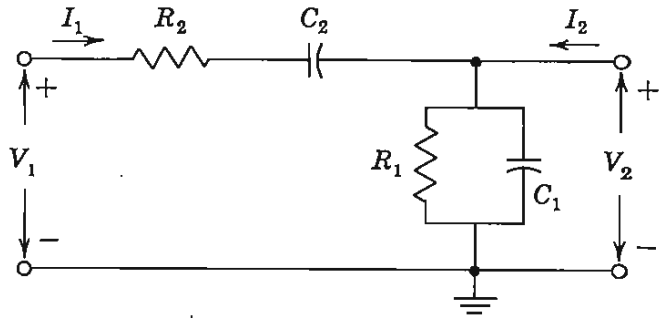


16-40 In Probs. 16-38 and 16-39 the *RC* two-port shown is used. (*a*) Find the parameters y_{21} and y_{22} of this two-port *RC* network. (*b*) Show that if

$$\frac{1}{k} = 2\left(\frac{R_2}{R_1} + \frac{C_1}{C_2}\right) + 1$$

then the two circuits are delay equalizers with transfer function

$$A_V = \frac{V_o}{V_s} = A_{Vo}\frac{(s - s_1)(s - s_2)}{(s + s_1)(s + s_2)}$$



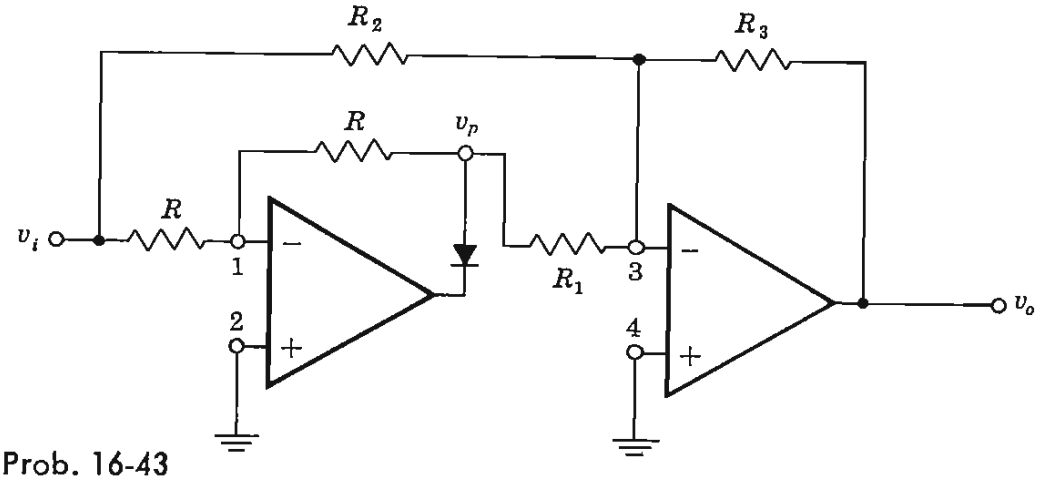
Prob. 16-40

16-41 Using the curve of Fig. 16-31 and assuming $V_{AGC} = 3.5$ V, with an audio modulating signal of 1.5 V peak to peak, calculate the modulation factor

$$k = \frac{V_{o,\max} - V_{o,\min}}{V_{o,\max}}$$

16-42 Derive Eq. (16-59) for the gain of the cascode video amplifier.

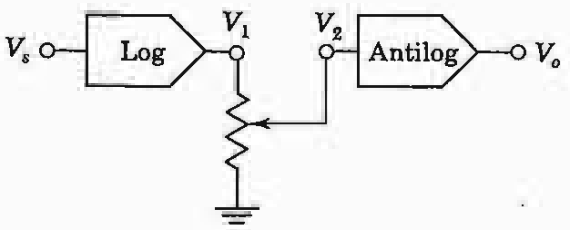
16-43 (*a*) Verify that the circuit shown gives full-wave rectification provided that $R_2 = 2R_1$.
(*b*) What is the peak value of the rectified output?
(*c*) Draw carefully the waveforms $v_i = 10 \sin \omega t$, v_p, and v_o if $R_3 = 2R_1$.



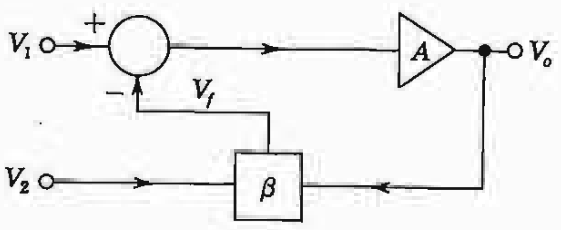
Prob. 16-43

16-44 If a waveform has a positive peak of magnitude V_1 and a negative peak of magnitude V_2, draw a circuit using two peak detectors whose output is equal to the peak-to-peak value $V_1 - V_2$.

16-45 Show that the given circuit can be used to raise the input V_s to an arbitrary power. Assume $V_1 = K_1 \ln K_2 V_s$, $V_o = K_3 \ln^{-1} K_4 V_2$, $V_2 = \alpha V_1$.



Prob. 16-45



Prob. 16-46

16-46 For the feedback circuit shown, the nonlinear feedback network β gives an output proportional to the product of the two inputs to this network, or $V_f = \beta V_2 V_o$. Prove that if $A = \infty$, then $V_o = K V_1 / V_2$, where K is a constant.

16-47 (*a*) With the results of Prob. 16-46, draw the block diagram of a system used to obtain the square root of the voltage V_s.
(*b*) What should be the value of β if it is required that $V_o = \sqrt{V_s}$?

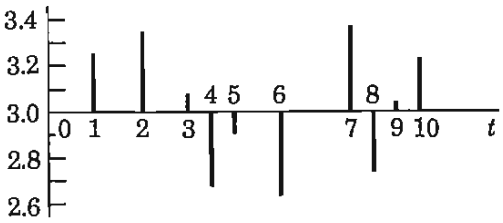
16-48 (*a*) Verify Eq. (16-78) for the pulse width of a monostable multivibrator.
(*b*) If $V_z \gg V_1$ and $\beta = 1/2$, what is T?

16-49 Verify Eq. (16-84) for the frequency of the triangle waveform.

16-50 The Schmitt trigger of Fig. 16-47 is modified to include two clamping Zener diodes across the output as in Fig. 16-45*a*. If $V_z = 4$ V and $A_v = 5{,}000$ and if the threshold levels desired are 6 ± 0.5 V, find (*a*) R_2/R_1, (*b*) the loop gain, and (*c*) V_R. (*d*) Is it possible to set the threshold voltage at a negative value? (*e*) In part (*a*) the ratio of R_2 to R_1 is obtained. What physical conditions determine the choice of the individual resistances?

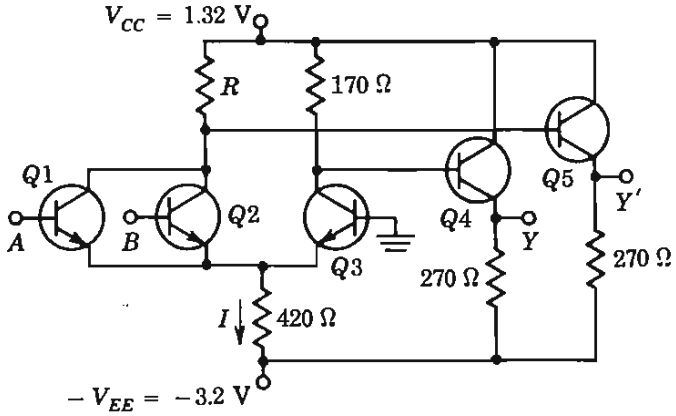
16-51 The input v_i to a Schmitt trigger is the set of pulses shown. Plot v_o versus time. Assume $V_1 = 3.2$ V, $V_2 = 2.8$ V, and $v_o = +5$ V at $t = 0$.

Prob. 16-51



16-52 (*a*) Calculate the logic levels at output Y of the ECL Texas Instruments gate shown. Assume that $V_{BE,\text{active}} = 0.7$ V. To find the drop across an emitter follower when it behaves as a diode assume a piecewise-linear diode model with $V_\gamma = 0.6$ and $R_f = 20\ \Omega$.
(*b*) Find the noise margin when the output Y is at $V(0)$ and also at $V(1)$.
(*c*) Verify that none of the transistors goes into saturation.
(*d*) Calculate R so that $Y' = \bar{Y}$.
(*e*) Find the average power taken from the power source.

Prob. 16-52



16-53 Verify that, if the outputs of two (or more) ECL gates are tied together as in Fig. 16-51, the OR function is satisfied.

16-54 (*a*) For the system in Fig. 16-51 obtain an expression for Y which contains three terms.
(*b*) If in Fig. 16-51 $\bar{Y}_1$ and $\bar{Y}_2$ are tied together, verify that the output is $Y = \bar{A}\bar{B} + \bar{C}\bar{D}$.

(*c*) If in Fig. 16-51 Y_1 and Y_2 are tied together and if the input to the lower ECL gate is $\bar{C}$ and $\bar{D}$ (instead of C and D), what is Y?

CHAPTER 17

17-1 Indicate how to implement S_n of Eq. (17-1) with AND, OR, and NOT gates.

17-2 Verify that the sum S_n in Eq. (17-1) for a full adder can be put in the form

$$S_n = A_n \oplus B_n \oplus C_{n-1}$$

17-3 (*a*) For convenience, let $A_n = A$, $B_n = B$, $C_{n-1} = C$, and $C_n = C^1$. Using Eq. (17-4) for C^1, verify Eq. (17-5) with the aid of the Boolean identities in Table 6-4; in other words, prove that

$$\bar{C}^1 = \bar{B}\bar{C} + \bar{C}\bar{A} + \bar{A}\bar{B}$$

(*b*) Evaluate $D \equiv (A + B + C)\bar{C}^1$ and prove that S_n in Eq. (17-1) is given by

$$S_n = D + ABC$$

17-4 (*a*) Verify that an EXCLUSIVE-OR gate is a true/complement unit.
(*b*) One input is A, the other (control) input is C, and the output is Y. Is $Y = A$ for $C = 1$ or $C = 0$?

17-5 For the system shown in Fig. 17-11*a*, verify the truth table in Fig. 17-11*b*.

17-6 (*a*) Make a truth table for a binary half subtractor A minus B (corresponding to the half adder of Fig. 17-3). Instead of a carry C, introduce a *borrow* P.
(*b*) Verify that the digit D is satisfied by an EXCLUSIVE-OR gate and that P follows the logic "B but not A."

17-7 Consider an 8-bit comparator. Justify the connections $C' = C_L$, $D' = D_L$, and $E' = E_L$ for the chip handling the more significant bits. HINT: Add 4 to each subscript in Fig. 17-14. Extend Eq. (17-12) for E and Eq. (17-13) for C to take all 8 bits into account.

17-8 (*a*) By means of a truth table verify the Boolean identity

$$Y = (A \oplus B) \oplus C = A \oplus (B \oplus C)$$

(*b*) Verify that $Y = 1(0)$ if an odd (even) number of variables equals 1. This result is *not* limited to three inputs, but is true for any number of inputs. It is used in Sec. 17-3 to construct a parity checker.

17-9 Construct the truth table for the EXCLUSIVE-OR tree of Fig. 17-15 for all possible inputs A, B, C, and D. Include $A \oplus B$ and $C \oplus D$ as well as the output Z. Verify that $Z = 1(0)$ for odd (even) parity.

17-10 (*a*) Draw the logic circuit diagram for an 8-bit parity check/generator system.
(*b*) Verify that the output is 0(1) for odd (even) parity.

17-11 (*a*) Verify that if $P' = 1$ in Fig. 17-15, this system is an even-parity check. In other words, demonstrate that with $P' = 1$, the output is $P = 0(1)$ for even (odd) parity of the inputs A, B, C, and D.
(*b*) Also verify that P generates the correct even-parity bit.

17-12 (*a*) Indicate an 8-bit parity checker as a block having 8 input bits (collectively designated A_1), an output P_1, and an input control P_1'. Consider a

second 8-bit unit with inputs A_2, output P_2, and control P_2'. Show how to cascade the two packages in order to check for odd parity of a 16-bit word. Verify that the system operates properly if $P_1' = 1$. Consider the four possible parity combinations of A_1 and A_2.

(*b*) Show how to cascade three units to obtain the parity of a 24-bit word. Should $P_1' = 0$ or 1 for odd parity?

(*c*) Show how to cascade units to obtain the parity of a 10-bit word.

17-13 Draw a logic diagram of a 4-to-10-line decoder using OR gates instead of AND gates.

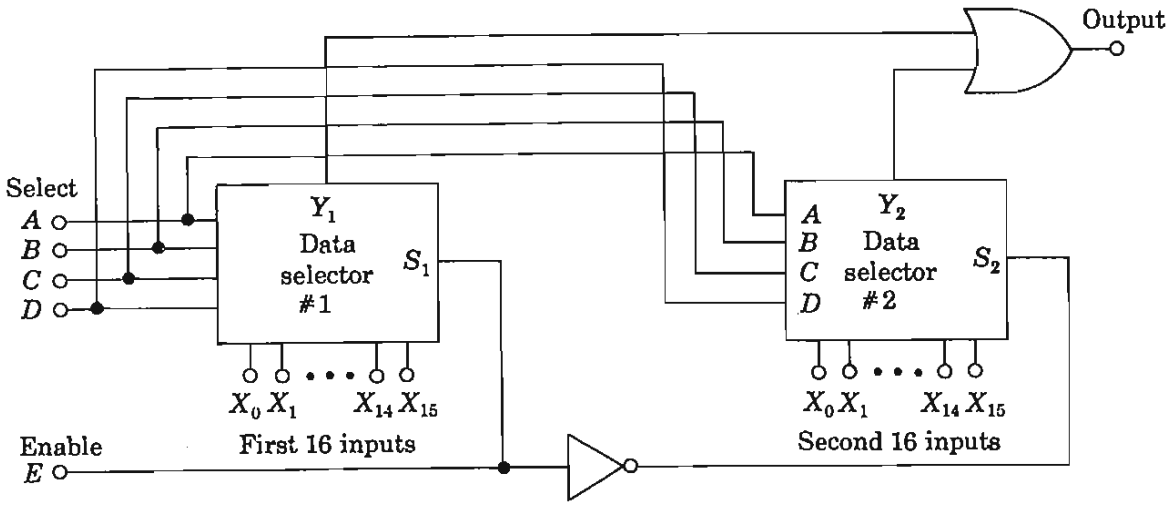
17-14 Draw a logic diagram for a 3-to-8-line decoder.

17-15 Explain how to convert a 4-to-10-line decoder unit into a 3-to-8-line decoder.

17-16 Draw a logic diagram for an 8-to-1-line multiplexer.

17-17 Write the Boolean expression for the output Y of a 4-to-1-line multiplexer with an enable input (Fig. 17-20).

17-18 The block diagram shows two data selectors being used to select 1 out of 32 data inputs. Explain the operation of the system.



Prob. 17-18

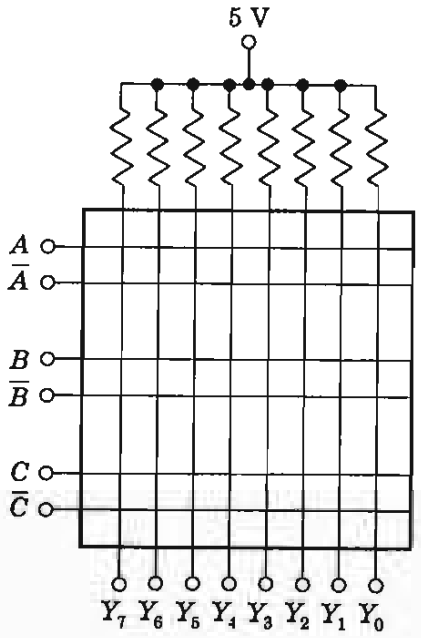
17-19 Design an encoder satisfying the following truth table, using a diode matrix.

Inputs				Outputs			
W_3	W_2	W_1	W_0	Y_3	Y_2	Y_1	Y_0
0	0	0	1	0	1	1	1
0	0	1	0	1	1	0	0
0	1	0	0	1	1	0	1
1	0	0	0	0	0	1	0

17-20 (*a*) Design an encoder, using multiple-emitter transistors, to satisfy the following truth table. (*b*) How many transistors are needed and how many emitters are there in each transistor?

Inputs			Outputs				
W_2	W_1	W_0	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	1	1	1	0	1	0
0	1	0	1	0	0	0	1
1	0	0	0	1	1	1	1

17-21 A block diagram of a three-input (A, B, and C) and eight-output (Y_0 to Y_7) decoder matrix is indicated. The bit Y_6 is to be 1 (5 V) if the input code is 110 corresponding to decimal 6. (*a*) Indicate how diodes are to be connected to line Y_6. (*b*) Repeat for Y_0, Y_1, and Y_7.



Prob. 17-21

17-22 (*a*) Write the expressions for Y_1 and Y_3 in the binary-to-Gray-code converter.
(*b*) Indicate how to implement the relationship for Y_1 with diodes.

17-23 (*a*) Give the relationships between the output and input bits for the Gray-to-binary-code translator for Y_1 and Y_2.
(*b*) Indicate how to implement the equation for Y_1 with transistors.

17-24 Minimize the number of terms in Eq. (17-23) and obtain Eq. (17-24).

17-25 (*a*) Write the sum-of-products canonical form for Y_4 of Table 17-5 for the seven-segment indicator code.
(*b*) Verify that this expression can be minimized to $Y_4 = A + C\bar{B}$.

17-26 How many AND, OR, and NOT gates are required if a three-input adder is implemented with an ROM? Compare these numbers with those used in a full-adder chip.

17-27 (*a*) Verify that it is not possible for both outputs in Fig. 17-27*a* to be in the same state.
(*b*) Verify that if $S = 0$ and $R = 1$ in Fig. 17-27*b*, the latch is reset to $Q = 0$.
(*c*) If $S = R = 0$, verify that the state of the latch is undetermined (it could be either $Q = 1$ or $Q = 0$).
(*d*) If $S = R = 1$, verify that both outputs would go to 1. Is this a valid situation?

17-28 Draw the logic diagram for an S-R FLIP-FLOP using AOI gates instead of NAND gates.

17-29 The excitation table for a J-K FLIP-FLOP is shown. An X in the table is to be interpreted to mean that it does not matter whether this entry is a 1 or a 0. It is referred to as a "don't care" condition. Thus the second row indicates that if the output is to change from 0 to 1, the J input must be 1, whereas K can be either 1 or 0. Verify this excitation table by referring to the truth table of Fig. 17-29*b*.

Q_n	Q_{n+1}	J_n	K_n
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

17-30 Verify that the J-K FLIP-FLOP truth table is satisfied by the difference equation

$$Q_{n+1} = J_n\bar{Q}_n + \bar{K}_nQ_n$$

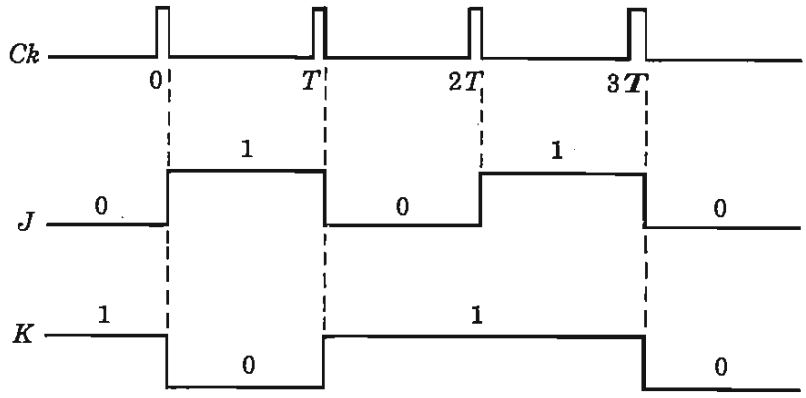
17-31 (*a*) For the J-K FLIP-FLOP of Fig. 17-30, verify that for $Cr = 1$, $Pr = 0$, and $Ck = 0$, the 1 state is preset independent of the values of J_n and K_n.
(*b*) Repeat part (*a*) for $Ck = 1$, provided that $J_n = K_n = 0$.
(*c*) Verify that $Cr = Pr = Ck = 0$ leads to an indeterminate state; i.e., it may be 0 or 1.

17-32 (*a*) Verify that there is no race-around difficulty in the J-K circuit of Fig. 17-30 for any data input combination except $J = K = 1$.
(*b*) Explain why the race-around condition does not exist (even for $J = K = 1$) provided that $t_p < \Delta t < T$.

17-33 (*a*) For the master-slave J-K FLIP-FLOP of Fig. 7-31 assume $Q = 1$, $\bar{Q} = 0$, $Ck = 1$, $K = 0$, and J arbitrary. What is Q_M?
(*b*) If K changes to 1, what is Q_M?
(*c*) If K returns to 0, what is Q_M? Note that Q_M does *not* return to its initial value. Hence K (and J) must not vary during the pulse.

17-34 The indicated waveforms J, K, and Ck are applied to a J-K FLIP-FLOP. Plot the output waveform for Q and $\bar{Q}$ lined up with respect to the clock pulses.

NOTE: Assume that the output $Q = 0$ when the first clock pulse is applied and that $Pr = Cl = 1$.



Prob. 17-34

17-35 (*a*) Verify that an *S-R* FLIP-FLOP is converted to a T type if S is connected to $\bar{Q}$ and R to Q.

(*b*) Verify that a D-type FLIP-FLOP becomes a T type if D is tied to $\bar{Q}$.

17-36 Augment the shift register of Fig. 17-34 with a four-input NOR gate whose output is connected to the *serial input* terminal. The NOR-gate inputs are Q_4, Q_3, Q_2, and Q_1.

(*a*) Verify that regardless of the initial state of each FLIP-FLOP, when power is applied, the register will assume correct operation as a ring counter after P clock pulses, where $P \leq 4$.

(*b*) If initially $Q_4 = 1$, $Q_3 = 1$, $Q_2 = 0$, $Q_1 = 0$, and $Q_0 = 1$, sketch the waveform at Q_0 for the first 16 pulses.

(*c*) Repeat part *b* if $Q_4 = 0$, $Q_3 = 1$, $Q_2 = 0$, $Q_1 = 0$, and $Q_0 = 0$.

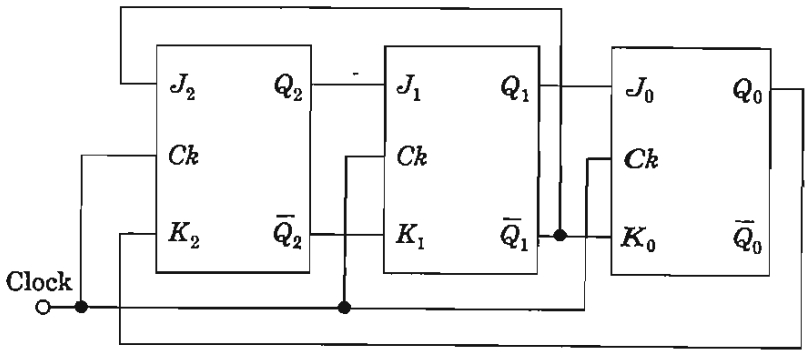
17-37 (*a*) Draw a waveform chart for the twisted-ring counter; i.e., indicate the waveforms Q_4, Q_3, Q_2, Q_1, and Q_0 for, say, 12 pulses. Assume that initially $Q_0 = Q_1 = Q_2 = Q_3 = Q_4 = 0$.

(*b*) Write the truth table after each pulse.

(*c*) By inspection of the table show that two-input AND gates can be used for decoding. For example, pulse 1 is decoded by $Q_4\bar{Q}_3$. Why?

17-38 (*a*) For the modified ring counter shown, assume that initially $Q_0 = 1$, $Q_1 = 0$, and $Q_2 = 0$. Make a table of the readings Q_0, Q_1, Q_2, J_2, and K_2 after each clock pulse. How many pulses are required before the system begins to operate as a divide-by-N counter? What is N?

(*b*) Repeat part (*a*) if initially $Q_0 = 1$, $Q_1 = 0$, and $Q_2 = 1$



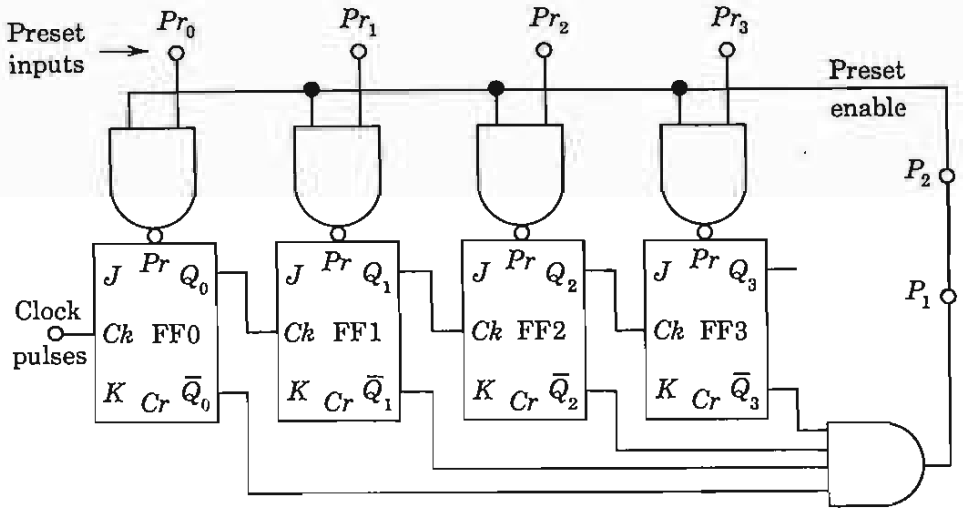
Prob. 17-38

17-39 A 50:1 ripple counter is desired. (*a*) How many FLIP-FLOPS are required? (*b*) If 4-bit FLIP-FLOPS are available on a chip, how many chips are needed? How are these interconnected?
(*c*) Indicate the feedback connections to the clear terminals.

17-40 (*a*) Indicate a divide-by-14 ripple-counter block diagram. Include a latch in the clear input.
(*b*) What are the inputs to the feedback NAND gate for a 153:1 ripple counter?

17-41 Consider the operation of the latch in Fig. 17-38. Make a table of the quantities Ck, Q_1, Q_3, P_1, $\overline{Ck}$, and $P_2 = Cr$ for the following conditions:
(*a*) Immediately after the tenth pulse.
(*b*) After the tenth pulse and assuming Q_1 has reset before Q_3.
(*c*) During the eleventh pulse.
(*d*) After the eleventh pulse.
This table should demonstrate that
(*a*) The tenth pulse sets the latch to clear the counter.
(*b*) The latch remains set until all FLIP-FLOPS are cleared.
(*c*) The positive edge of the eleventh pulse resets the latch so that $Cr = 1$.
(*d*) The negative edge of the eleventh pulse initiates the new counting cycle.

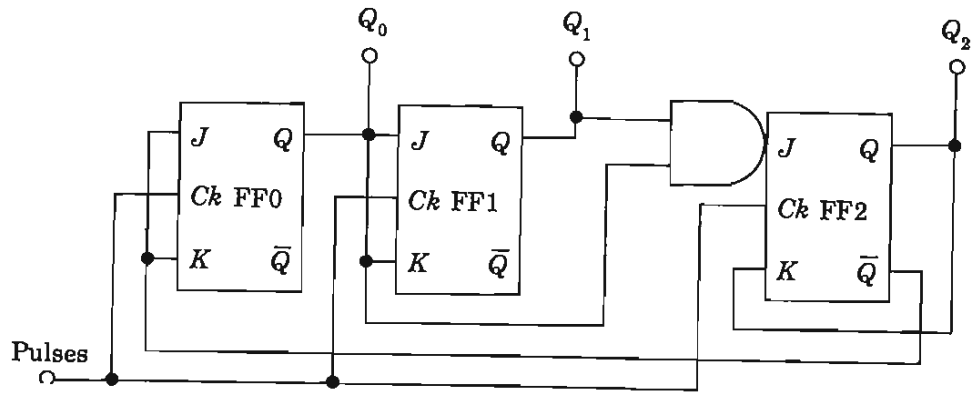
17-42 (*a*) The circuit shown is a *programmable* ripple counter. It is understood that $J = K = Cr = 1$ and that the latch in Fig. 17-38*b* exists between P_1 and P_2. If $Pr_0 = Pr_1 = 1$ and $Pr_2 = Pr_3 = 0$, what is the count N? Explain the operation of the system carefully.
(*b*) Why is the latch required?
(*c*) Generalize the result of part (*a*) as follows. The counter has n stages and is to divide by N, where $2^n > N > 2^{n-1}$. How must the preset inputs be programmed?



Prob. 17-42

17-43 Draw the logic diagram of a 5-bit UP-DOWN synchronous counter with series carry.

17-44 For the logic diagram of the synchronous counter shown, write the truth table of Q_0, Q_1, and Q_2 after each pulse and verify that this is a 5:1 counter.



Prob. 17-44

17-45 Consider a two-stage synchronous counter (both stages receive the pulses at the *Ck* input). In each counter $K = 1$. If $J_0 = \bar{Q}_1$ and $J_1 = Q_0$, draw the circuit. From a truth table of Q_0 and Q_1 after each pulse, demonstrate that this is a 3:1 counter.

17-46 Draw the waveform chart for a 6:1 divider from Fig. 17-36 and deduce the connections for a synchronous counter. Draw the logic block diagram.

17-47 Solve Prob. 17-46 for a 5:1 divider.

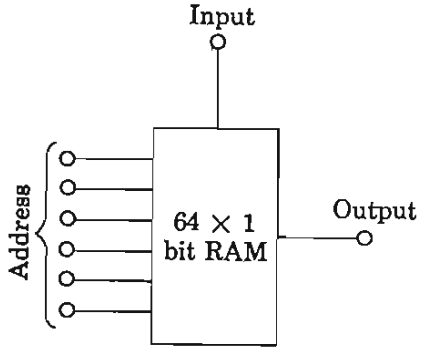
17-48 (*a*) Verify that the circuit of Fig. 17-44 performs the function of a NAND gate. Let the voltage levels of V_1 and V_2 be 0 V or $-V_{DD}$.
(*b*) Verify that this circuit dissipates less power than the corresponding circuit of Fig. 10-17.
(*c*) Draw the circuit of a dynamic NOR gate corresponding to Fig. 10-8. Repeat parts *a* and *b* for this circuit.

17-49 Show that in the four-phase shift-register stage of Fig. 17-48 there is no dc current path to ground even when clocks ϕ_1 and ϕ_2 overlap or when clocks ϕ_3 and ϕ_4 overlap. Assume that the input terminal is maintained at zero volts.

17-50 Draw the logic diagrams of a recirculating or refresh memory to store 512 words each 4 bits long, using the TI 3309JC (shown in Fig. 17-49) as the basic building block. Input data are available in parallel form, and data output must be presented also in parallel form.

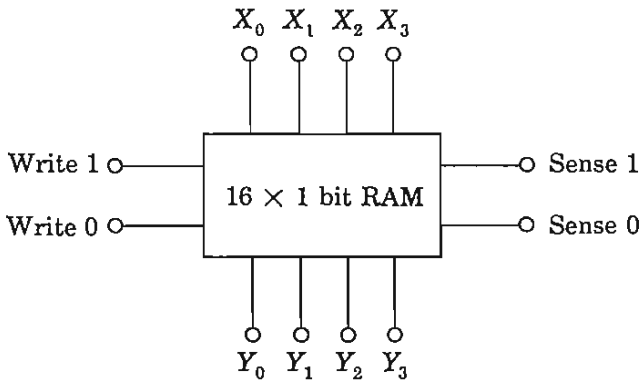
17-51 Draw a 16-word 4-bit RAM matrix using the basic 1-bit RAM of Fig. 17-52 and using linear selection.

17-52 The figure shows a 64-word 1-bit RAM with on-chip decoding. The memory accepts a 6-bit address word. Using the above memory unit as a building block, construct a 64-word by 4-bit memory.



Prob. 17-52

17-53 The figure shows a 16-bit coincident memory matrix. A specific bit is selected by applying a logic 1 to the coincident X and Y address lines.
(*a*) Draw the diagram of a 16-word by N-bit memory (each word N bits long) using the above RAM as the basic building block.
(*b*) What determines the maximum value of N in this configuration?



Prob. 17-53

17-54 (*a*) For the D/A converter of Fig. 17-60 show that when the second most significant bit is 1 and all other bits are zero, the output is $V_o = V_R/4$.
(*b*) Find V_o if only the third MSB is 1.
(*c*) Find V_o if only the LSB is 1.

17-55 The figure shows a binary weighted resistor D/A converter.
(*a*) Show that the output resistance is independent of the digital word and that

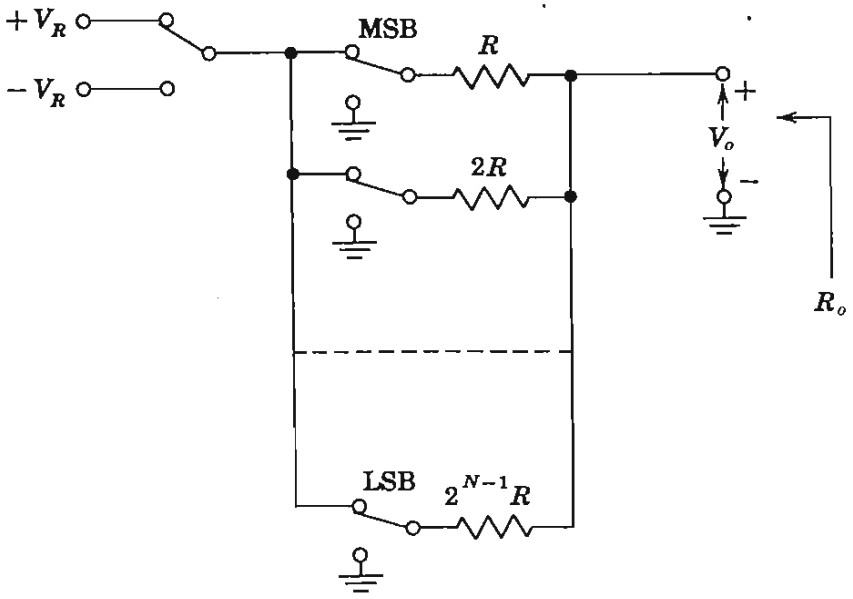
$$R_o = \frac{2^{N-1}}{2^N - 1} R$$

(*b*) Show that the analog output voltage for the most significant bit is

$$V_o = \frac{2^{N-1}}{2^N - 1} V_R$$

(*c*) Show that the analog output voltage for the least significant bit is

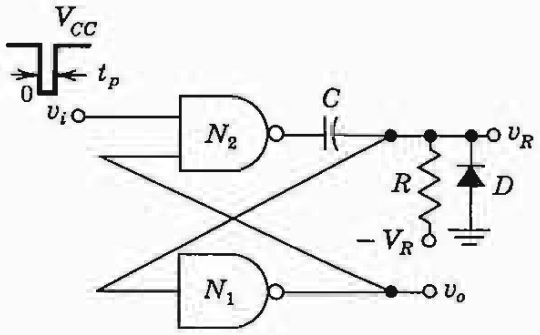
$$V_o = \frac{1}{2^N - 1} V_R$$



Prob. 17-55

17-56 Modify the block diagram of Fig. 17-64 to display M lines of N characters each on the face of a CRT.

17-57 The circuit shown consists of two cross-coupled NAND gates. The coupling from the output of N_1 to the input of N_2 is direct (dc), whereas resistance-capacitance (ac) coupling is used from the output of N_2 to the input of N_1. Positive TTL logic is used and the levels are 0 and V_{CC}. Assume that a NAND gate changes



Prob. 17-57

state when its input voltage falls below V (≈ 1.6 V for a TTL gate). Neglect the drop across the clamping diode D. The input v_i is at V_{CC} and at $t = 0$ drops to 0 V for a short time t_p; that is, a negative narrow pulse is applied.
(*a*) Verify that the circuit behaves as a monostable multivibrator by drawing the waveforms v_R and v_o.
(*b*) Find the duration T of the output pulse, assuming $T > t_p$.

CHAPTER 18

18-1 (*a*) Nonlinear distortion results in the generation of frequencies in the output that are not present in the input. If the dynamic curve can be represented by Eq. (18-6), and if the input signal is given by

$$i_b = I_1 \cos \omega_1 t + I_2 \cos \omega_2 t$$

show that the output will contain a dc term and sinusoidal terms of frequency ω_1, ω_2, $2\omega_1$, $2\omega_2$, $\omega_1 + \omega_2$, and $\omega_1 - \omega_2$.
(*b*) Generalize the results of part *a* by showing that if the dynamic curve must be represented by higher-order terms in i_b, the output will contain intermodulation frequencies, given by the sum and difference of integral multiples of ω_1 and ω_2, for example, $2\omega_1 \pm 2\omega_2$, $2\omega_1 \pm \omega_2$, $3\omega_1 \pm \omega_2$, etc.

18-2 A transistor supplies 0.85 W to a 4-K load. The zero-signal dc collector current is 31 mA, and the dc collector current with signal is 34 mA. Determine the percent second-harmonic distortion.

18-3 The input excitation of an amplifier is $i_b = I_{bm} \sin \omega t$. Prove that the output current can be represented by a Fourier series which contains only odd sine components and even cosine components.

18-4 Supply the missing steps in the derivation of Eqs. (18-18).

18-5 Obtain a five-point schedule for determining B_0, B_1, B_2, B_3, and B_4 in terms of I_{max}, $I_{0.707}$, I_C, $I_{-0.707}$, and I_{min}.

18-6 The p-n-p transistor whose input and output characteristics are given in Fig. 18-5 is used in the circuit of Fig. 18-4, with $R_s = 0$ and $R'_L = (N_1/N_2)^2 R_L = 10\ \Omega$. The quiescent point is $I_C = -1.1$ A and $V_{CE} = -7.5$ V. The peak-to-peak 2,000-Hz sinusoidal base-to-emitter voltage is 140 mV.
(a) What is the fundamental current output?
(b) What is the percent second-, third-, and fourth-harmonic distortion?
(c) What is the output power?
(d) What is the rectification component B_o of the collector current?
Neglect any changes in the operating point.

18-7 Verify the data plotted in Fig. 18-6 for $R'_L = 20\ \Omega$.

18-8 For the operating conditions indicated in Fig. 18-5, calculate the fundamental power P_1 for (a) $R'_L = 5\ \Omega$, (b) $R'_L = 30\ \Omega$.

18-9 Repeat Prob. 18-6, but now assume a current drive (large R_s) so that the base current is sinusoidal, with a peak-to-peak value of 30 mA.

18-10 A power transistor operating class A in the circuit of Fig. 18-4 is to deliver a maximum of 5 W to a 4-Ω load ($R_L = 4\ \Omega$). The quiescent point is adjusted for symmetrical clipping, and the collector supply voltage is $V_{CC} = 20$ V. Assume ideal characteristics, as in Fig. 18-7, with $V_{min} = 0$.
(a) What is the transformer turns ratio $n = N_2/N_1$?
(b) What is the peak collector current I_m?
(c) What is the quiescent operating point I_C, V_{CE}?
(d) What is the collector-circuit efficiency?

18-11 Draw three transistor collector characteristics to correspond to base currents $I_B + I_{bm}$, I_B, $I_B - I_{bm}$. Draw the load line through the point $i_C = 0$, $v_{CE} = V_{CC}$, and the quiescent point $i_B = I_B$, $i_C = I_C$, and $v_{CE} = V_C$. This corresponds to a series-fed resistance load.
(a) Assuming that the input signal is zero, indicate on the i_C-v_{CE} plane the areas that represent the total input power to the collector circuit, the collector dissipation, and the power loss in the load resistance.
(b) Repeat part a if the input signal is sinusoidal, with a peak value equal to I_{bm}. Also, indicate the area that represents the output power.
(c) The ratio of what two areas gives the collector-circuit efficiency?
(d) Repeat parts a to c for a shunt-fed load. Assume that the static resistance is small but not zero.

18-12 In a push-pull system the input (base current) to transistor $Q1$ is $x_1 = X_m \cos \omega t$, and the input to transistor $Q2$ is $x_2 = -X_m \cos \omega t$. The collector current in each transistor may be expressed in terms of the input excitation by a series of the form

$$i_C = I_C + a_1 x + a_2 x^2 + a_3 x^3 + \cdots$$

(a) With the aid of this series, show that the output current contains only odd cosine terms.
(b) Show that the collector supply current contains only even harmonics, in addition to a dc term.

18-13 Prove, without recourse to a Fourier series, that mirror symmetry [Eq. (18-37)] exists in a push-pull amplifier. Start with $i = k(i_1 - i_2)$ and make use of Eq. (18-34).

18-14 A single transistor is operating as an ideal class B amplifier with a 1-K load. A dc meter in the collector circuit reads 10 mA. How much signal power is delivered to the load?

18-15 Given an ideal class B transistor amplifier whose characteristics are as in Fig. 18-9. The collector supply voltage V_{cc} and the effective load resistance $R'_L = (N_1/N_2)^2 R_L$ are fixed as the base-current excitation is varied. Show that the collector dissipation P_C is zero at no signal ($V_m = 0$), rises as V_m increases, and passes through a maximum given by Eq. (18-42)] at $V_m = 2V_{CC}/\pi$.

18-16 The idealized push-pull class B power amplifier shown in Fig. 18-8 has $R_2 = 0$, $V_{CC} = 20$ V, $N_2 = 2\,N_1$, and $R_L = 20\ \Omega$, and the transistors have $h_{FE} = 20$. The input is a sinusoid. For the maximum output signal at $V_m = V_{CC}$, determine (*a*) the output signal power, (*b*) the collector dissipation in each transistor.

18-17 The power transistor whose characteristics are shown in Fig. 18-5 is used in the class B push-pull circuit of Fig. 18-8, with $R_2 = 0$ and $-V_{CC} = -20$ V. If the base current is sinusoidal, with a peak value of 20 mA and $R'_L = (N_1/N_2)^2 R_L = 15\,\Omega$, calculate (*a*) the third-harmonic distortion, (*b*) the power output, (*c*) the collector-circuit efficiency.

18-18 Repeat Prob. 18-17, using $-V_{CC} = -15$ V, $R'_L = 7.5\,\Omega$, and a peak base current of 30 mA.

18-19 The power transistor whose characteristics are shown in Fig. 18-5 is used in the class B push-pull circuit of Fig. 18-8, with $R_2 = 0$ and $-V_{CC} = -20$ V and $R'_L = 15\,\Omega$. If the base voltage is sinusoidal, with a peak value of 0.4 V, plot the output collector current. Note the crossover distortion.

18-20 Sketch the circuit of a push-pull class B transistor amplifier in the common-collector configuration (*a*) with an output transformer, (*b*) without an output transformer.

18-21 Discuss the push-pull complementary circuit of Fig. 18-11. In particular, show that no even harmonics are present.

18-22 The circuit shown represents a transformerless class B single-ended complementary-symmetry push-pull power amplifier. Transistors $Q2$ and $Q3$ are matched silicon devices, with $h_{FE} \approx h_{fe} = 100$ and $h_{ie} = 50\,\Omega$. $Q1$ is a silicon transistor whose small-signal h parameters are given in Table 8-2, and $h_{FE} = 50$.

(*a*) Explain the operation of this circuit. Note especially the role of the capacitor C_2. Neglect the reverse saturation currents.

(*b*) Calculate the quiescent currents in all the resistors, and determine the value of R_3 so that

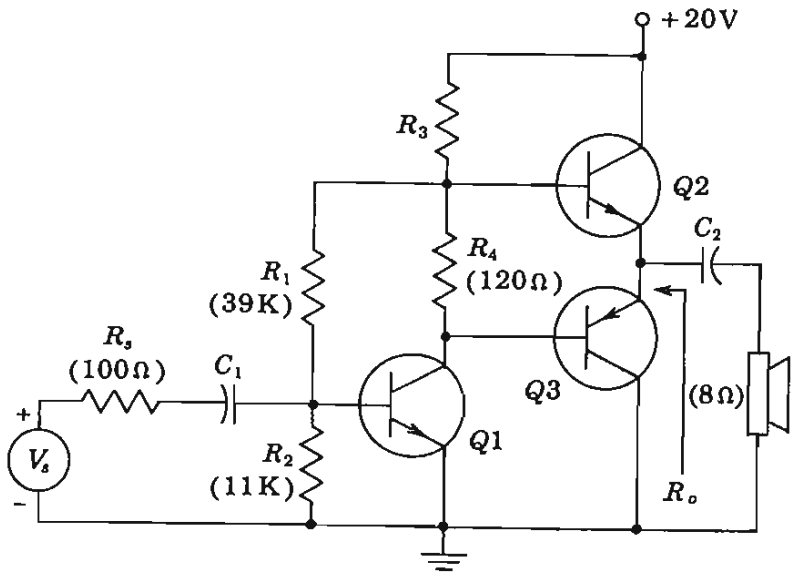
$$|V_{CE3}| = |V_{CE2}|$$

(*c*) Find the output resistance R_o, assuming ideal class B operation.

(*d*) Calculate the maximum power that can be delivered to the 8-Ω speaker. Take the output resistance R_o into account, and assume $V_{CE,sat} \approx 0$.

HINT: In parts *c* and *d*, assume that for class B operation $R_4 = 0$.

Prob. 18-22



18-23 Verify Eqs. (18-57) and (18-58).

18-24 Find the output resistance of the series-regulated power supply as given by Eq. (18-59). HINT: Short-circuit the input, $V_i = 0$, and derive the expression for the output current, using an auxiliary voltage source.

18-25 Design a regulated power supply as shown in Fig. 18-17 with the following specifications:

Nominal unregulated input voltage $V_i = 30$ V and $r_o = 8\ \Omega$
Nominal regulated outout voltage $V_o = 12$ V
Maximum load current $I_{L,\max} = 200$ mA
Control transistor $Q1$ (silicon): $h_{FE} = h_{fe} = 100$, $h_{ie} = 200\ \Omega$
Amplifier transistor $Q2$ (silicon): $h_{FE} = h_{fe} = 200$, $h_{ie} = 1$ K
Reference avalanche diode D: $V_R = 6$ V, $R_z = 10\ \Omega$ at $I_z = 20$ mA

(*a*) Sketch the complete circuit and obtain reasonable values for R_1, R_2 and R_3.
(*b*) Calculate the voltage stabilization factor S_V.
(*c*) Calculate the output resistance R_o.

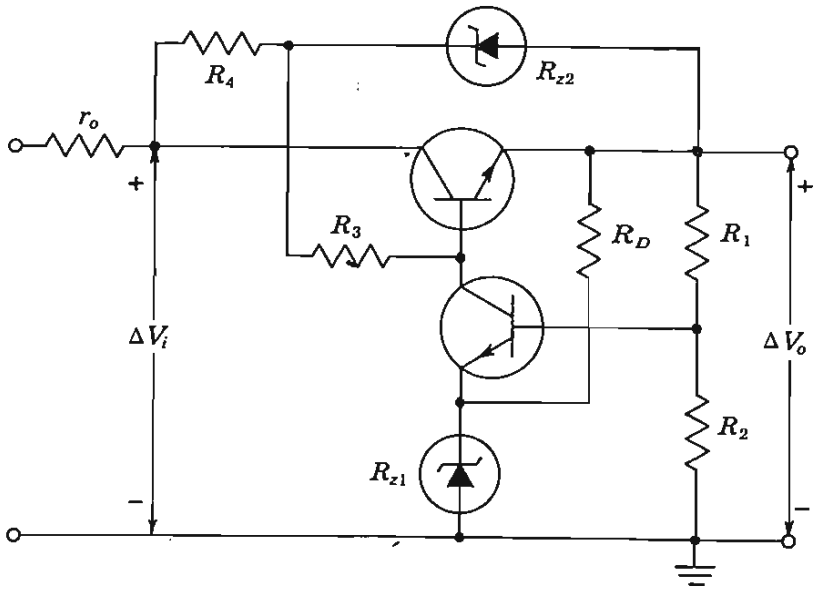
18-26 In the circuit of Fig. 18-18, the control transistor $Q1$ is replaced by a Darlington pair $Q1$-$Q3$. The junction of R_3 and the collector of $Q2$ is connected to the base of $Q3$.
(*a*) Discuss the possible improvement in S_V over the value for the circuit of Fig. 18-18.
(*b*) Show that the output resistance is

$$R_o \approx \frac{r_o + \dfrac{R_3 + h_{fe3}h_{ie1}}{h_{fe1}h_{fc3}}}{1 + G_m(R_3 + r_o)}$$

where G_m is as given by Eq. (18-57).

18-27 Repeat Prob. 18-25 using the circuit of Prob. 18-26. Assume that $Q2$ and $Q3$ are identical.

18-28 The circuit shown employs a Zener diode preregulator.
(*a*) Explain carefully the operation of the circuit.
(*b*) Obtain an approximate expression for the input regulation factor S_V.
HINT: Assume $\Delta V_o \approx 0$ when $\Delta V_i \gg \Delta V_o$.

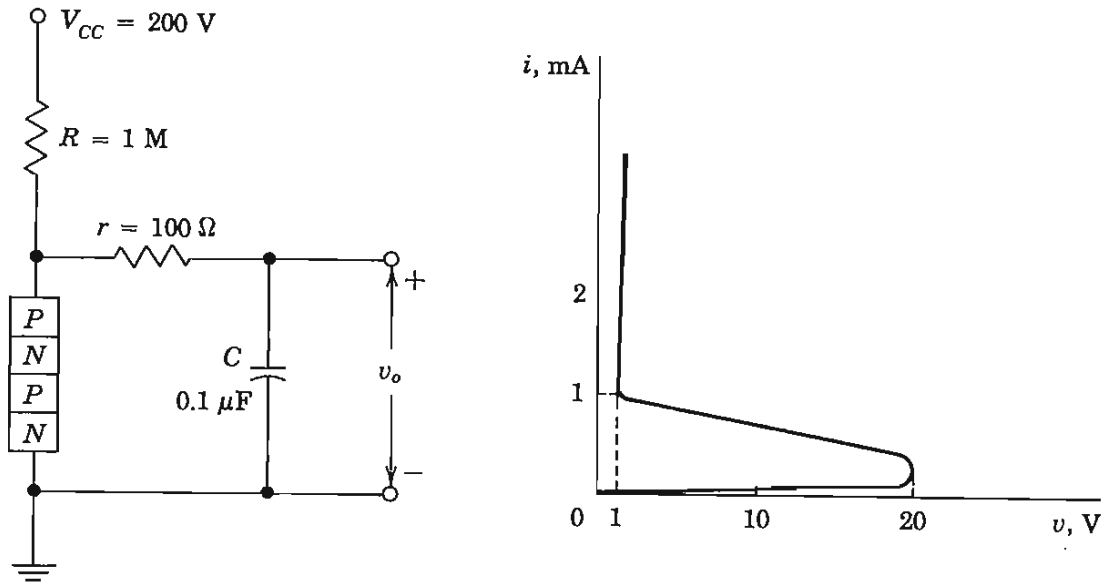


Prob. 18-28

18-29 Sketch the circuit of a regulated semiconductor power supply whose output is positive with respect to ground, using (*a*) *p-n-p* transistors, (*b*) complementary transistors.

18-30 Sketch the circuit of a regulated semiconductor power supply whose output is negative with respect to ground, using (*a*) *p-n-p* transistors, (*b*) *n-p-n* transistors, (*c*) complementary transistors.

18-31 If the *V-I* characteristic of the *p-n-p-n* diode is as shown, calculate and plot the output voltage v_o. Show all critical voltage and time values.



Prob. 18-31

18-32 The circuit of Fig. 18-31 is adjusted so that conduction commences 90° after the start of each positive half cycle of applied voltage. The SCR voltage drop is negligible. The applied voltage is 300 V sinusoidal rms, and the load is a 50-Ω resistor. Calculate

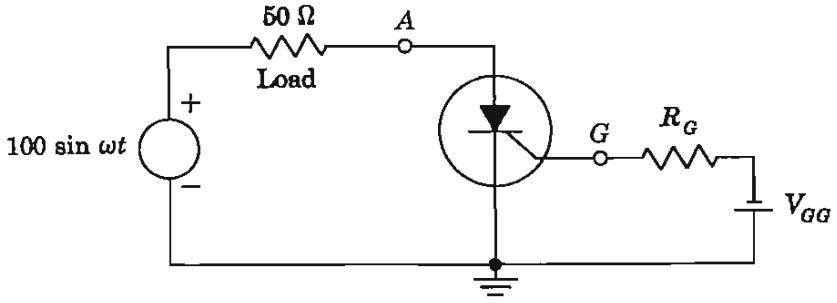
(*a*) The dc load current.
(*b*) The power dissipated by the load.
(*c*) The rms load current.

18-33 The circuit of Fig. 18-34 is adjusted so that the conduction angle is 60°. The rectifier and SCR voltage drops when conducting are negligible. The applied voltage is 300 V rms, and the load is a 10-Ω resistor. Calculate

(*a*) The reading of a true rms reading ammeter in series with the load.
(*b*) The reading of a dc ammeter in series with the load.
(*c*) The reading of a true rms reading voltmeter across the load.
(*d*) The reading of a dc voltmeter across the load.
(*e*) The dc load power.
(*f*) The total power dissipated by the load resistor.

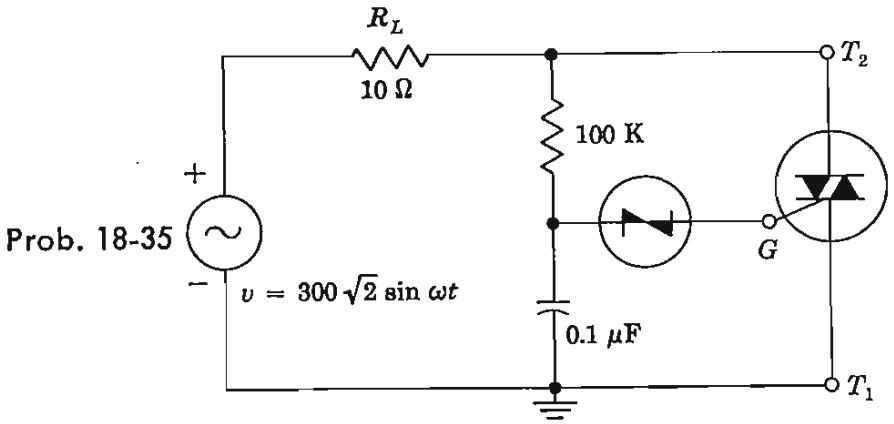
18-34 The SCR is used to control the power delivered to the 50-Ω load by the sinusoidal source. If the gate supply V_{GG} is adjustable:

(*a*) Over what range may the conduction angle of the SCR be continuously varied?
(*b*) Over what range may the load dc current be continuously varied if the frequency is 60 Hz?



Prob. 18-34

18-35 The circuit shown is used to control the power dissipated in the 10-Ω load resistor. Assume that the bilateral switching diode has a breakdown voltage of ±2.8 V and that the holding voltages of the diode and the triac are negligible.



Prob. 18-35

The applied sinusoidal voltage is 300 V rms, at 60 Hz.
(*a*) Compute the conduction angle.
(*b*) Draw the waveform of the voltage applied to the load.
(*c*) Compute the total power dissipated by the load resistor.

CHAPTER 19

19-1 The specific gravity of tungsten is 18.8, and its atomic weight 184.0. Assume that there are two free electrons per atom. Calculate the numerical value of n and E_F.

19-2 How many electrons per cubic meter in metallic tungsten have energies between 8.5 and 8.6 eV (*a*) at 0°K, (*b*) at 2500°K?

19-3 (*a*) Calculate the maximum energy of the free electrons in metallic aluminum at absolute zero. Assume that there are three free electrons per atom. The specific gravity of aluminum is 2.7.
(*b*) Repeat part *a* for the electrons in metallic silver. The specific gravity of silver is 10.5. Assume that there is one free electron per atom.

19-4 (*a*) Show that the average energy E_{av} of the electrons in a metal is given by

$$E_{av} = \frac{\int E\, dn_E}{\int dn_E}$$

(*b*) Prove that the average energy at absolute zero is $3E_F/5$.

19-5 If the emission from a certain cathode is 10,000 times as great at 2000 as at 1500°K, what is the work function of this surface?

19-6 (*a*) If the temperature of a tungsten filament is raised from 2300 to 2320°K, by what percentage will the emission change?
(*b*) To what temperature must the filament be raised in order to double its emission at 2300°K?

19-7 Prove that the fractional change in thermionic current is given by

$$\frac{dI_{th}}{I_{th}} = \left(2 + \frac{E_W}{kT}\right)\frac{dT}{T}$$

19-8 If 10 percent of the thermionic-emission current is collected, what must be the retarding voltage at the surface of the metal? The filament temperature is 2000°K.

19-9 What fraction of the thermionic current will be obtained with zero applied voltage between the cathode and anode of a diode? The work function of the cathode is 4.50 V, and the work function of the anode is 4.75 V. The cathode temperature is 2000°K.

19-10 A plane cathode having a work function of 3.00 V is connected directly to a parallel-plane anode whose work function is 5.00 V. The distance between anode and cathode is 2.00 cm. If an electron leaves the cathode with a normal-to-surface velocity of 5.93×10^5 m/s, how close to the anode will it come?

19-11 A diode has an oxide-coated cathode operating at a temperature of 1000°K. With zero plate voltage the anode current is essentially zero, indicating that the contact potential is high enough to keep most of the electrons from reaching the plate. The applied voltage is increased so that a small current is drawn. Show that there is a tenfold increase in current for every 0.2-V increase in voltage.

19-12 A diode with plane-parallel electrodes is operated at a temperature of 1500°K. The filament is made of tungsten, the area being such that a thermionic current 10 μA is obtained. The contact difference of potential between cathode and anode is 0.5 V, with the cathode at the higher potential.
(*a*) What current is obtained with zero applied voltage?
(*b*) What applied voltage will yield a current of 1 μA?
(*c*) What fraction of the electrons emitted from this filament can move against an *applied retarding* field of 1 V?

19-13 Indicate by letter which of the following statements are true:
(*a*) The work function of a metal is always less than the potential barrier at the surface of a metal.
(*b*) The potential barrier at the surface of a metal is a solid hill made up of the material of the metal.
(*c*) The ionic structure of a metal shows that the inside of the metal is not an equipotential volume.
(*d*) At absolute zero the electrons in a metal all have zero energy.
(*e*) The ionic structure of a metal shows that the surface of a metal is not at a specific location.
(*f*) For an electron to escape from a metal, the potential barrier at the surface of the metal must first be broken down.
(*g*) The distribution function for the electrons in a metal shows how many electrons are close to a nucleus and how many are far away.

19-14 Indicate by letter which of the following statements are true:
(*a*) The potential energy as a function of distance along a row of ions *inside* a metal varies very rapidly in the immediate neighborhood of an ion but is almost constant everywhere else inside the metal.
(*b*) The potential-energy barrier at the surface of a metal *cannot* be explained on the basis of the modern crystal-structure picture of a metal, but it can be explained on the basis of classical electrostatics (image forces).
(*c*) To remove any one of the free electrons from a metal, it is necessary only to give this electron an amount of energy equal to the work function of the metal.
(*d*) The symbol E_F used in the energy distribution function represents the maximum number of free electrons per cubic meter of metal at absolute zero.
(*e*) The area under the energy distribution curve represents the total number of free electrons per cubic meter of metal at any temperature.
(*f*) The Dushman equation of thermionic emission gives the current that is obtained from a heated cathode as a function of applied plate voltage.

19-15 Evaluate n given by Eq. (19-29). HINT: Refer to a table of definite integrals.

19-16 Verify the expression for p in Eq. (19-35). HINT: Refer to a table of definite integrals.

19-17 If the effective mass of an electron is equal to twice the effective mass of a hole, find the distance (in electron volts) of the Fermi level in an intrinsic semiconductor from the center of the forbidden band at room temperature.

19-18 (*a*) Verify the numerical values in Eqs. (19-41) and (19-42).
(*b*) From Eq. (19-42) and the numerical values given in Table 2-1 evaluate $m_n m_p/m^2$.

19-19 (*a*) Prove that the fractional change in the conductivity of an intrinsic semiconductor is given by

$$\frac{d\sigma}{\sigma} = \frac{dn_i}{n_i} = \left(\frac{3}{2} + \frac{E_{Go}}{2kT}\right)\frac{dT}{T}$$

(*b*) Using the result of part (*a*), show that the conductivity of Ge (Si) at room temperature increases approximately 6 (8) percent per degree increase in temperature.

19-20 (*a*) In *n*-type germanium the donor concentration corresponds to 1 atom per 10^8 germanium atoms. Assume that the effective mass of the electron equals one-half the true mass. At room temperature, how far from the edge of the conduction band is the Fermi level? Is E_F above or below E_C?
(*b*) Repeat part (*a*) if impurities are added in the ratio of 1 donor atom per 10^3 germanium atoms.
(*c*) Under what circumstances will E_F coincide with E_C?

19-21 (*a*) In *p*-type silicon the acceptor concentration corresponds to 1 atom per 10^8 silicon atoms. Assume that $m_p = 0.6$ m. At room temperature, how far from the edge of the valence band is the Fermi level? Is E_F above or below E_V?
(*b*) Repeat part (*a*) if impurities are added in the ratio of 1 acceptor atom per 5×10^3 silicon atoms.
(*c*) Under what condition will E_F coincide with E_V?

19-22 In *n*-type silicon the donor concentration is 1 atom per 2×10^8 silicon atoms. Assume that the effective mass of the electron equals the true mass. At what temperature will the Fermi level coincide with the edge of the conduction band?

19-23 In *p*-type germanium at room temperature (300°K), for what doping concentration will the Fermi level coincide with the edge of the valence band? Assume $m_p = 0.4$ m.

19-24 (*a*) A germanium tunnel diode has impurity concentration at the *p* side of 3 parts in 10^3 atoms, and at the *n* side of 2 parts in 10^3 atoms. If $m_n = m_p = 0.4$ m, calculate E_G, E_o, and $E_F - E_{Cn}$ of this diode.
(*b*) Draw the energy bands for this diode using the results of part (*a*).

19-25 (*a*) A region of a semiconductor has a one-dimensional current flow in the x direction, with current density J A/m^2, due entirely to the hole-concentration gradient. J is constant with x and time; at $x = 0$, the hole concentration is $p(0)$. Find the hole concentration as a function of x. Recombination, field due to the stored charge, and conductivity modulation are all neglected. (This situation corresponds to the base region in a step-graded *p-n-p* transistor.)
(*b*) Now suppose that there is also an electric field of magnitude $\mathcal{E}$ V/m in the negative x direction. The same constant current J flows, but the hole concentration is now $p'(0)$ at $x = 0$. Noting that J is the diffusion current less

the conduction current, show that (if $\mathcal{E}$ is independent of x) the hole concentration is

$$p(x) = \epsilon^{-x/x_o}\left[p'(0) + \frac{J}{q\mu_p\mathcal{E}}\right] - \frac{J}{q\mu_p\mathcal{E}}$$

and find x_o.

(*c*) Show that for small x the formula in part *b* reduces to

$$p(0) = p'(0) - x\left[\frac{J}{qD_p} + p'(0)\frac{\mu_p\mathcal{E}}{D_p}\right]$$

where D_p is the diffusion constant for holes.

(*d*) Sketch the results of parts (*a*) and (*b*) on the same axes for $p'(0) > p(0)$. How do the slopes compare?

19-26 (*a*) Let Q be the excess minority charge stored within a volume of cross section A and length L. If there is no electric field within this volume, and if the current i flowing perpendicular to the section A is due exclusively to minority-carrier diffusion, show that the stored charge Q satisfies the equation

$$\frac{dQ}{dt} + \frac{Q}{\tau} = i$$

where τ is the mean lifetime of the minority carriers.

(*b*) Show that the steady-state current is

$$I_{ss} = \frac{Q}{\tau}$$

19-27 A semiconductor diode carries a dc current I_F in the forward direction. At $t = 0^+$ the current is changed abruptly to $-I_R$. Show that the time t_s required for the removal of the excess minority-carrier charge Q_o is

$$t_s = \tau \ln\left(1 + \frac{I_F}{I_R}\right)$$

where τ is the mean lifetime of holes and electrons. HINT: Use the results of Prob. 19-26 and note that at $t = 0$, $Q = Q_o = \tau I_F$.

19-28 (*a*) Verify Eq. (19-91).

(*b*) Calculate $[d(\ln I_o)]/dT$ for Ge and Si (for rated current).

19-29 (*a*) Consider a diode biased in the forward direction at a fixed voltage V. Prove that the fractional change in current with respect to temperature is

$$\frac{1}{I}\frac{dI}{dT} = \frac{V_{GO} - V}{\eta T V_T} + \frac{m}{T}$$

(*b*) Find the percentage change in current per degree centigrade for Ge at $V = 0.2$ V and for Si at $V = 0.6$ V.

19-30 Carry out in detail the derivation of the dynamic diffusion capacitance outlined in Sec. 19-12.

19-31 Verify Eq. (19-117).

19-32 (*a*) If it is not assumed that $W/L_B \ll 1$, prove that Eqs. (19-114) and (19-116) remain valid provided that

$$a_{11} = Aq\left(D_p \frac{p_{no}}{L_B} \coth \frac{W}{L_B} + \frac{D_n n_{EO}}{L_E}\right)$$

$$a_{12} = a_{21} = -AqD_p \frac{p_{no}}{L_B} \operatorname{csch} \frac{W}{L_B}$$

$$a_{22} = Aq\left(D_p \frac{p_{no}}{L_B} \coth \frac{W}{L_B} + \frac{D_n n_{CO}}{L_C}\right)$$

(*b*) Show that if $W/L_B \ll 1$, these expressions reduce to those given by Eqs. (19-115) and (19-117).

19-33 Using the results of Prob. 19-32*a*, verify that $\alpha = \beta^*\gamma$, where γ is given by Eq. (19-123) and β^* by Eq. (19-124).

19-34 If $W/L_B \ll 1$, verify that Eqs. (19-125) and (19-126) follow from Eqs. (19-123) and (19-124), respectively.

19-35 Starting with Eqs. (19-131) and (19-132) and assuming $I_B \gg I_{CO}$, prove that

$$V_{CE} \approx \pm V_T \ln \frac{1 + \dfrac{I_C}{I_B}(1 - \alpha_I)}{\alpha_I\left(1 - \dfrac{I_C}{I_B}\dfrac{1 - \alpha_N}{\alpha_N}\right)} = \pm V_T \ln \frac{1 + h_{FEI} + \dfrac{I_C}{I_B}}{h_{FEI}\left(1 - \dfrac{I_C}{h_{FE} I_B}\right)}$$

where $h_{FE} = \alpha_N/(1 - \alpha_N)$ and $h_{FEI} = \alpha_I/(1 - \alpha_I)$. Compare with Eq. (5-31).

19-36 (*a*) The incremental resistance between collector and emitter for a grounded-emitter switch at constant base current may be computed as

$$r_{CE} = \left|\frac{dV_{CE}}{dI_C}\right|_{I_B} = \left|\frac{d(V_E - V_C)}{dI_C}\right|_{I_B}$$

where V_E and V_C are, respectively, the voltage drops across the emitter and collector junctions. Using Eqs. (19-131) and (19-132), show that

$$r_{CE} = V_T\left[\frac{1 - \alpha_N}{\alpha_N I_B - I_C(1 - \alpha_N) + I_{CO}} + \frac{1 - \alpha_I}{I_B + I_C(1 - \alpha_I) + I_{EO}}\right]$$

(*b*) If $I_B \gg I_{CO}$ and if $\dfrac{1 - \alpha_N}{\alpha_N}\dfrac{I_C}{I_B} \ll 1$, show that

$$r_{CE} \approx \frac{V_T}{I_B}\frac{1 - \alpha_N\alpha_I}{\alpha_N}$$

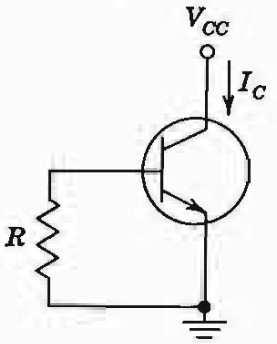
19-37 (*a*) Show that I_C is given approximately by

$$I_C = I_{CER} = \frac{\left[1 + \dfrac{I_{EO}(R + r_{bb'})}{V_T}\right] I_{CO}}{1 - \alpha_N\alpha_I + (1 - \alpha_N)\dfrac{I_{EO}(R + r_{bb'})}{V_T}}$$

where $r_{bb'}$ is the base-spreading resistance. HINT: Assume that the collector junction is reverse-biased and that the emitter junction is *slightly* forward-biased. Take advantage of the approximations which are allowed because the forward bias is small.

(*b*) A germanium transistor operating at room temperature has $\alpha_N = 0.98$, $I_{CO} = 2\ \mu A$, $I_{EO} = 1.6\ \mu A$, and $r_{bb'} = 200\ \Omega$. Calculate I_C for $R = 0$ and $R = \infty$.

(*c*) What value of R will give a collector current midway between the currents corresponding to a shorted and open base?



Prob. 19-37

19-38 Use the Ebers-Moll equations to show that the transconductance of a transistor in the active region is given by

$$g_m = \frac{dI_C}{dV_E}\bigg|_{V_C=\text{const}} \approx \frac{1}{V_T}\left[I_C - \frac{(1-\alpha_I)I_{CO}}{1-\alpha_N\alpha_I}\right] \approx \frac{I_C}{V_T}$$

HINT: Assume $\epsilon^{V_C/V_T} \ll 1$.

19-39 A type 2N404 germanium transistor is operated at room temperature in the CE configuration. The supply voltage is 6 V, the collector-circuit resistance is 200 Ω, and the base current is 20 percent higher than the minimum value required to drive the transistor into saturation. Assume the following transistor parameters: $I_{CO} = -5\ \mu A$, $I_{EO} = -2\ \mu A$, $h_{FE} = 100$, and $r_{bb'} = 250\ \Omega$. Find $V_{BE,\text{sat}}$ and $V_{CE,\text{sat}}$.

19-40 The type 2N1708 double-diffused silicon transistor has parameters $h_{FE} = 30$, $h_{FEI} = 0.2$, $r_{bb'} = 30\ \Omega$, and $I_{CO} = 13$ nA and has a collector body resistance of 6 Ω. It operates with $I_B = 1$ mA and $I_C = 10$ mA. Find V_{BE} and V_{CE} at room temperature.