INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR (IIITN)

Department of ECE and CSE

Analog Electronics (Code: ECL101)

Semester End Exam || Semester-1

Slot: E
Date: Nov 24, 2017
Time: 02:00–05:00 P.M.
Maximum Marks: 60

Time: 3 hours

Roll No. _____

Important instructions:

- All questions are compulsory.
- All questions map to Course Outcomes (CO) 1 and 2.
- Maximum marks that can be obtained for a particular question are indicated on the right of the corresponding question.
- Non-programmable calculators are permitted for use during the examination.
- The cut-in/ knee voltages for Si, Ge, and GaAs are 0.7 V, 0.3 V and 1.2 V respectively.

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1. Fill in the blanks (No justification, No marks!)
   (a) A Field Effect Transistor is a _____ (unipolar/bipolar) device. [2]
   (b) A Bipolar Junction Transistor is a _____ (symmetric/asymmetric) device, whereas a Field Effect Transistor is a _____ (symmetric/asymmetric) device. [2]
   (c) An ideal value of gate current in FET is _____ mA. [2]
   (d) A Bipolar Junction Transistor can act as a controlled _____ (current/voltage) source. [2]
   (e) A Field Effect Transistor can act as a controlled _____ (current/voltage) source. [2]

2. For the single-stage transistor circuit shown in Figure 2, assume $\beta = 50$, $h_i = 1.1k\Omega$, $h_r = 250\mu$, $h_f = 50$, $h_o = 25\mu$
   (a) Using dc analysis, determine the Quiescent point (V_{CE}, I_C). [2]
   (b) Determine the region of operation of the transistor (Active/ Saturation/ Cutoff). Justify your answer. [2]
   (c) Neatly draw and label the h-parameter model. (No labelling, no marks!) [4]
   (d) Calculate the following: (A_I, Z_i, A_V, Z_o). [8]
   (e) Explain the operation of the transistor as an amplifier. [4]

3. (a) Draw the input and output characteristics of n-channel MOSFET. [4]
   (b) For the circuit shown in the Figure 3, determine the drain-to-source voltage V_{DS}. Assume $\frac{\mu_n C_{ox} \frac{W}{L}}{2} = 600\mu A/V^2$ (i.e. k). Assume $V_{th} = 2V$. [4]
   (c) For the circuit shown in the Figure 3, determine the maximum value of R_D in order to retain the MOSFET in saturation. [2]

4. (a) Define positive and negative feedback. [2]

Question 4 continues on the next page...

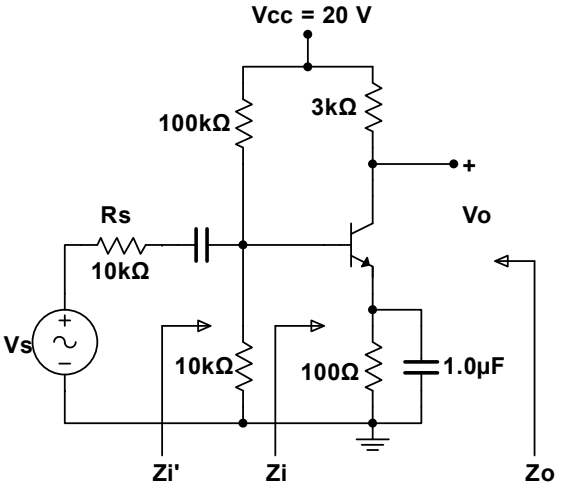

Figure 2: Figure for Q.2

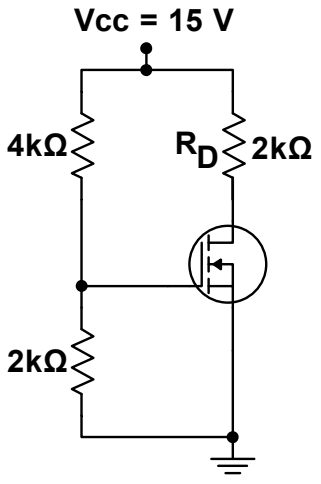

Figure 3: Figure for Q.3b

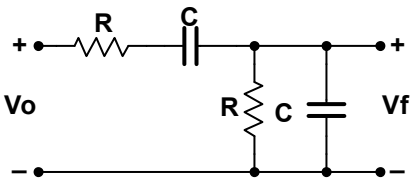

Figure 4: Figure for Q 4c

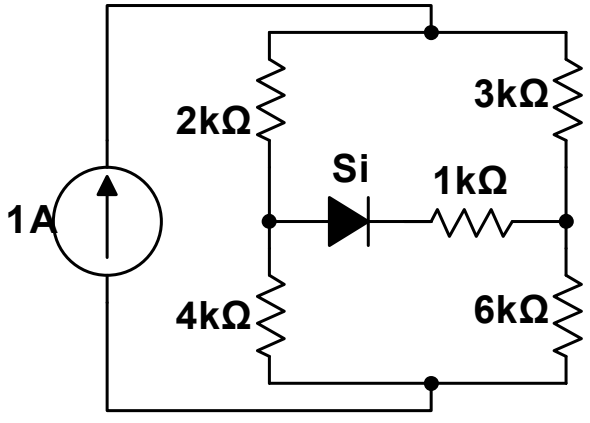

Figure 5: Figure for Q.5a

(b) What is Barkhausen's criterion? [2]

(c) For the C-R circuit shown in the Figure 4, find the expression of oscillation frequency. [4]

(d) For the C-R circuit shown in the Figure 4, find the range of A (gain of amplifier stage) and β (gain of feedback circuit) required for oscillations. [2]

5. (a) For the circuit shown in Figure 5, determine the voltage across the diode. Assume Silicon diode. [4]

(b) Find the current through $3k\Omega$ resistor. [3]

(c) Calculate the voltage across the $4k\Omega$ resistor. [3]

End of exam

Q1

a] UNIPOLAR Because the current is contributed by either electrons or holes not both!

b] BJT → Asymmetric ∴ collector & Emitter cannot be interchanged

FET → Symmetric ∴ Source & Drain are not interchangeable.

c] 0 mA : As gate is insulated from channel, the gate current is ideally ZERO

d] BJT is a controlled current source as the collector (output) current is controlled with respect to the voltage V_{BE} (input)

e] FET is a controlled current source as the drain current (output) is controlled using gate voltage

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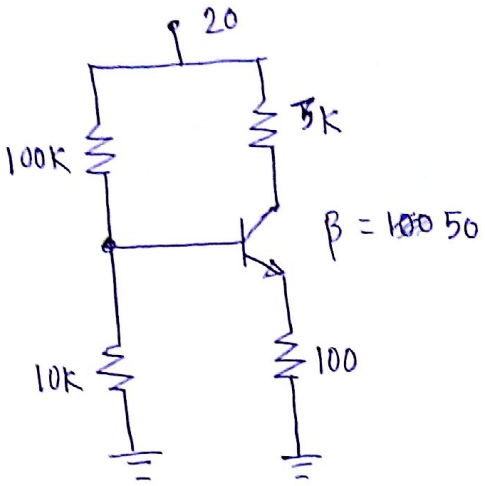
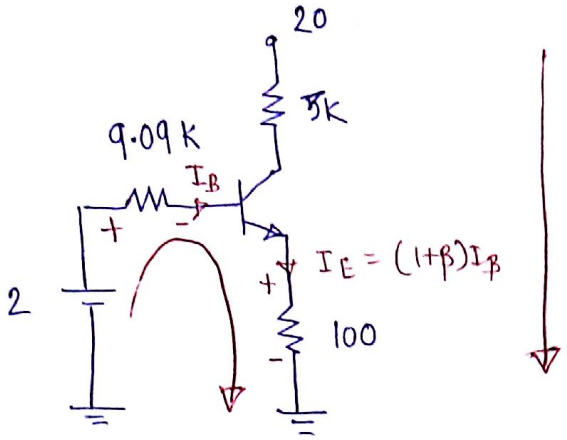
Q.2 a]





KVL in input loop :

$$V_{th} - 9.09K\, I_B - 0.7 - 100\left(\frac{51}{\cancel{50}}\right) I_B = 0$$

$$V_{th} = \frac{20 \times 10K}{100K} = 2V \; ; \quad R_{th} = 100K \,||\, 10K = 9.09\,K$$

$$\Rightarrow \quad I_B = \frac{2 - 0.7}{9.09K + 5100} = 91.61\ \mu A$$

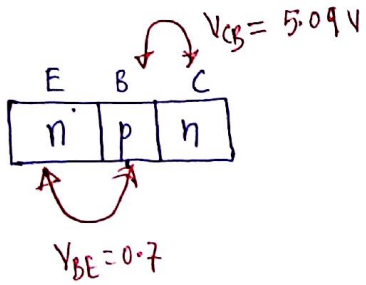
$$\Rightarrow \quad \boxed{I_{CQ} = 4.58\ mA} \qquad I_E = 4.67\ mA$$

KVL in output loop : $20 - 3K(I_C) - V_{CE} - 100 \times I_E = 0$

$$\therefore \quad \boxed{V_{CEQ} = 5.79\ V}$$

$\therefore$ The Q-point is $(V_{CEQ}, I_{CQ}) = (5.79, 4.58\,m)$

b]



$V_C = 20 - I_C \times 3K = 6.26\,V$

$V_B = 1.167\,V$

$\boxed{V_{CB} = 5.09\ V}$ POSITIVE

$\boxed{V_{BE} = 0.7}$ I_B is positive

~~As V_{BE} is~~ As Base-Emitter junction is Forward-bias and Collector-Base junction is Reverse-bias, the transistor is operating in ~~AET~~ $\boxed{\text{FORWARD ACTIVE}}$ region of operation.

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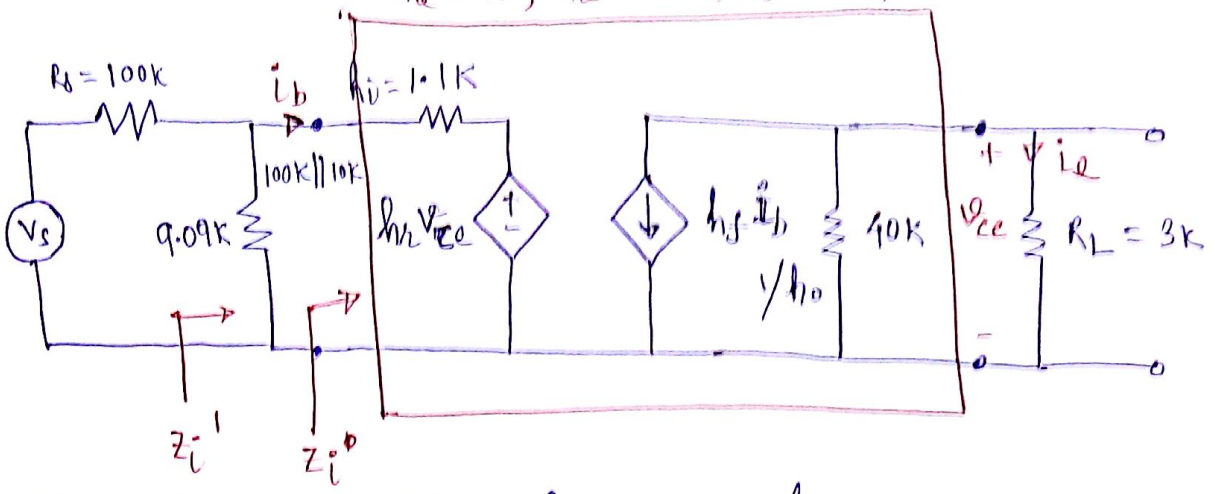
c]

$h_{ie} = 1.1K$; $h_{re} = 250\mu$; $h_{fe} = 50$; $1/h_o = 40K$; $h_o = 25\mu$



d]

(1) Current gain : $A_I = A_I'' = \dfrac{i_c}{i_b} = \dfrac{-h_f}{1 + h_o R_L} = \dfrac{-50}{1 + 25\mu \times 3K}$

$$A_I = \frac{i_c}{i_b} = -46.51$$

(2) Input Impedance (Z_i'') :

$$Z_i'' = h_i + h_r A_I'' R_L = 1.065K$$

$$Z_i' = 9.09K \,||\, 1.065K = 953.40\,\Omega$$

(3) Voltage gain (A_V') :

$$A_V'' = \frac{A_I'' R_L}{Z_i''} = -131.01$$

(4) Output Impedance (Z_o) :

$$Z_o = h_o - \frac{h_f h_r}{h_i + R_s}$$

R_s effective $= 100K \,||\, 9.09K = 47.61\,K$

$$Z_o = 24.74\,\mu$$

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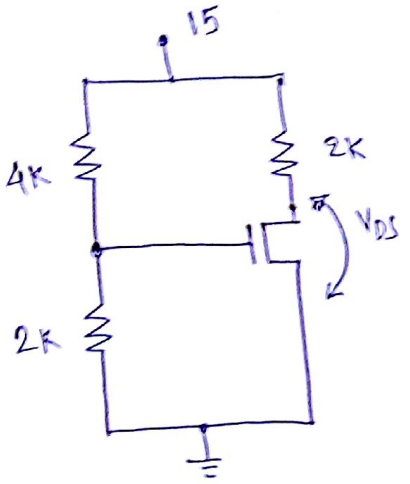
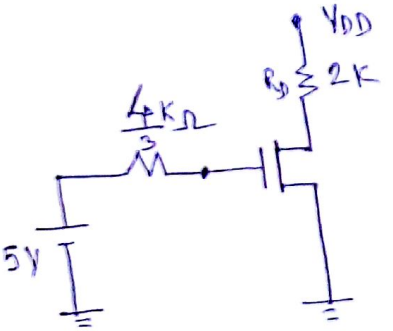
Q.3

b]





$V_{GS} = 5\ V \qquad V_{th} = 2\ V$

$$K = \frac{\mu_n C_{ox}}{2}\frac{W}{L} = 600\ \mu$$

Assuming saturation region of operation,

$$I_D = 600\mu (V_{GS} - V_{th})^2 = 5.4\ mA$$

$$\therefore \boxed{V_{DS} = V_{DD} - I_D R_D = 10.8\ V}$$

$V_{DS} > V_{GS} - V_{th}$ This verifies the assumption

c] For $R_{D,max}$: In order for nMOS to remain in saturation

$$V_{DS} \geq V_{GS} - V_{th}$$

$$\therefore 15 - I_D R_D \geq 3$$

$$\Rightarrow R_D \leq 12/5.4m \Rightarrow 2.22\ K\Omega$$

$$\Rightarrow \boxed{R_{D,max} = 2.22\ K\Omega}$$

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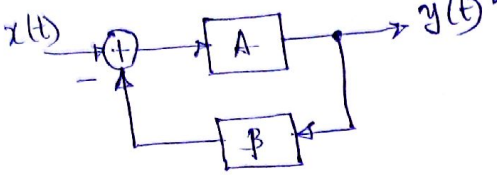
Q.4

a] Feedback gain $A_f = \frac{A}{1+A\beta}$



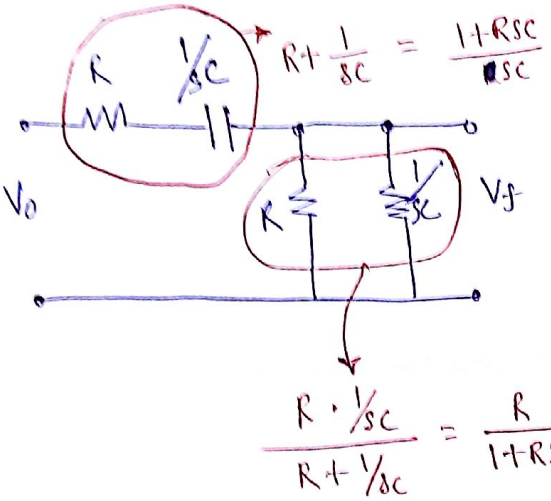
If $|A_f| > |A| \Rightarrow$ POSITIVE / REGENERATIVE FEEDBACK

$|A_f| < |A| \Rightarrow$ NEGATIVE / DEGENERATIV FEEDBACK

b] $\boxed{-A\beta = 1}$ Barkhausen's Criterion.

i.e. $|A\beta| = 1$ & $\angle A\beta = 0^\circ$ or $K\,180^\circ$ (integer)

c]



$$\frac{V_f}{V_o} = \frac{\frac{R}{1+RSC}}{\frac{R}{1+RSC} + \frac{1+RSC}{SC}}$$

$$\frac{R \cdot \frac{1}{SC}}{R + \frac{1}{SC}} = \frac{R}{1+RSC}$$

$$= \frac{\frac{R}{1+RSC}}{\frac{RSC + 1 + 2RSC + (RSC)^2}{SC(1+RSC)}}$$

$$\therefore \frac{V_f}{V_o} = \frac{RSC}{1 + 3RSC + (RSC)^2} = \frac{1}{3 + \frac{1}{RSC} + RSC}$$

$$= \frac{1}{3 + j\left(\omega RC - \frac{1}{\omega RC}\right)}$$

For 180° phase shift, imaginary part must be zero.

$$\therefore \omega RC = \frac{1}{\omega RC} \Rightarrow \omega RC = 1$$

$$\Rightarrow \boxed{f = \frac{1}{2\pi RC}}$$

d] For Barkhausen Criterion $|A\beta| = 1 \Rightarrow \frac{V_f}{V_o} = \boxed{\frac{1}{3} = \beta}$ { As $\omega RC = 1$

and $\angle AB = 0$

$\therefore \boxed{A \geq 3}$

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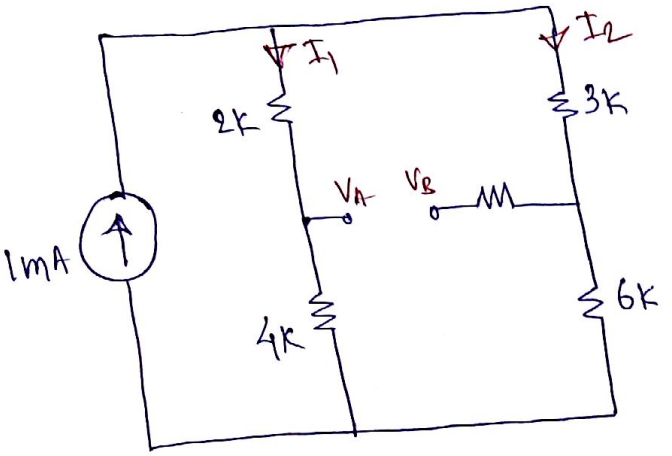
Q.5

a] Step 1 : Determine the states of the diode by open-circuiting it



Using Current division,

$$I_1 = \frac{9k}{9k+6k} \, 1m = \frac{9}{15} \, m$$

$$I_2 = \frac{6k}{6k+9k} \, 1m = \frac{6}{15} \, m$$

$$\therefore V_A = I_1 \times 4k = \frac{36}{15} \, V$$

$$V_B = I_2 \times 6k = \frac{36}{15} \, V$$

$$\Rightarrow \boxed{V_A - V_B = 0 \, V} \; !$$

$\therefore$ The voltage across diode is 0V, hence the diode will remain OFF (Bridge)

b] Current through 3k = $I_1 = \frac{9}{15} \, m = 0.6 \, m$

c] Voltage across 4k = $V_A = \frac{36}{15} = 2.4 \, V$

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