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Digital Logic PYQ XXII

Special class

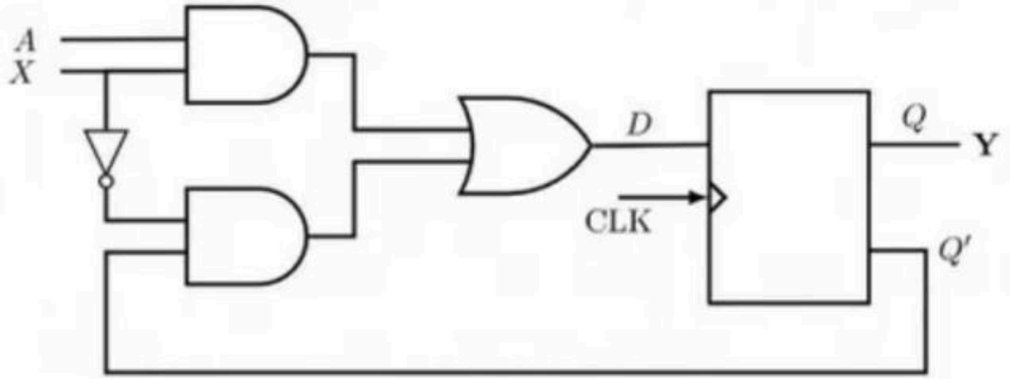
Amit Khurana • May 24, 2023

AMIT KHURANA

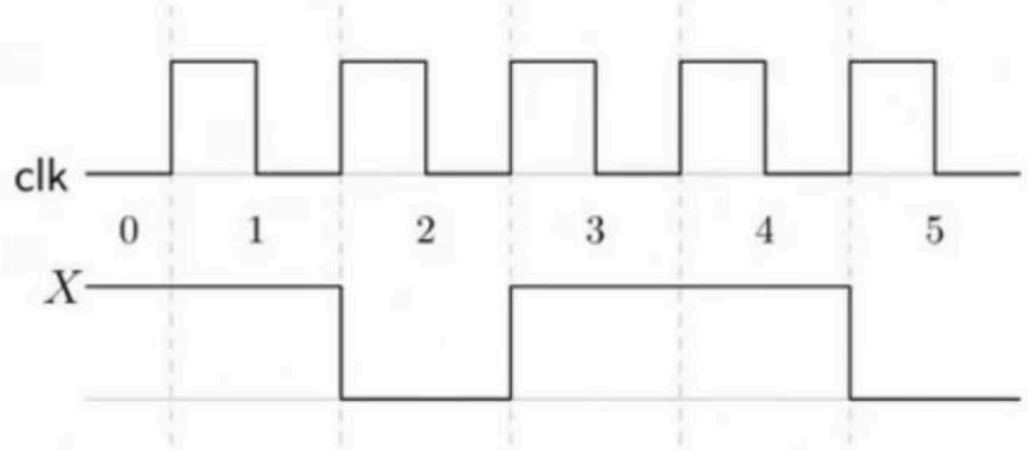
- AIR 94 GATE 2020
- Selected in IIT BOMBAY for M.Tech.
- Qualified UGC NET in 2012 & 2013
- 12+ Teaching Experience
- Mentored 50,000+ Students

Gate 2005

Consider the following circuit involving a positive edge triggered D FF.



Consider the following timing diagram. Let A_i represents the logic level on the line A in the i-th clock period.

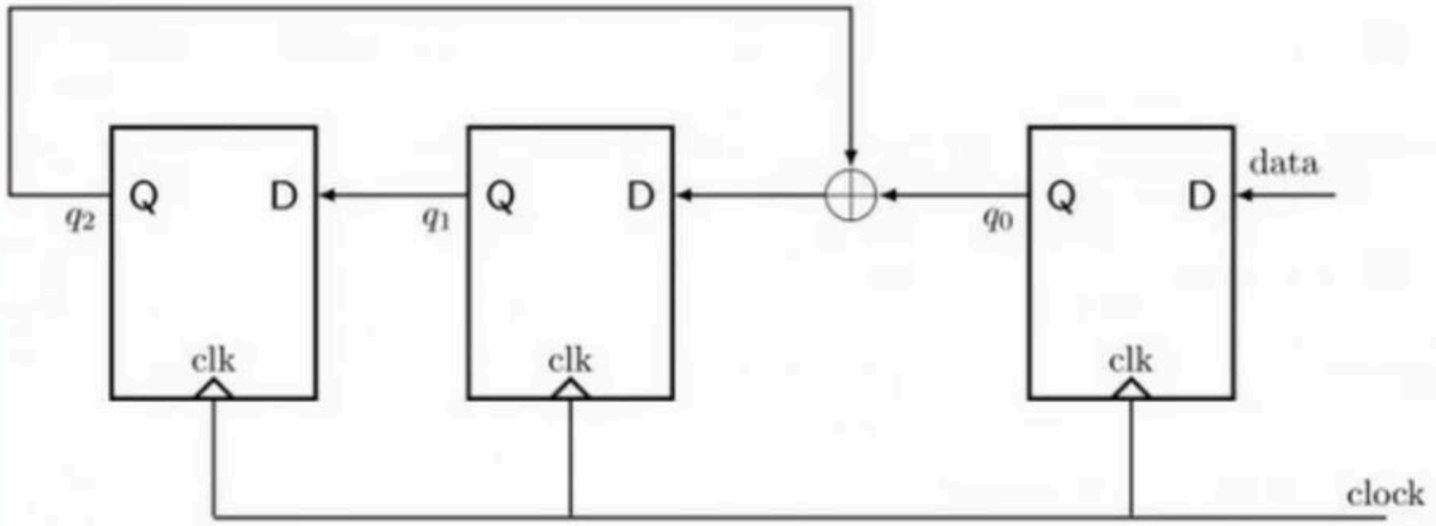


Let A' represent the complement of A. The correct output sequence on Y over the clock periods 1 through 5 is:

A. $A_0A_1A_1'A_3A_4$
B. $A_0A_1A_2'A_3A_4$
C. $A_1A_2A_2'A_3A_4$
D. $A_1A_2'A_3A_4A_5'$

Gate 2006

Consider the circuit in the diagram. The $\oplus$ operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared).

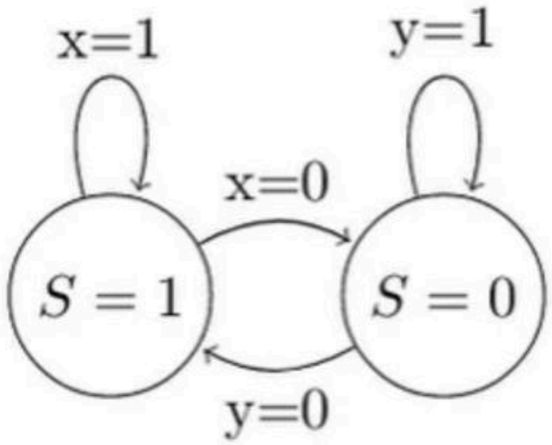


The following data: 100110000 is supplied to the "data" terminal in nine clock cycles. After that the values of $q_2q_1q_0$ are:

A. 000
B. 001
C. 010
D. 101

Gate 2006

For a state machine with the following state diagram the expression for the next state S^+ in terms of the current state S and the input variables x and y is



A. $S^+ = S'.y' + S.x$
B. $S^+ = S.x.y' + S'.y.x'$
C. $S^+ = x.y'$
D. $S^+ = S'.y + S.x'$

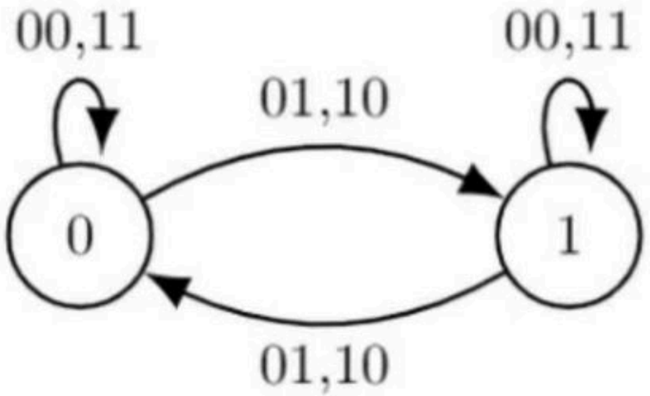
GATE 2007

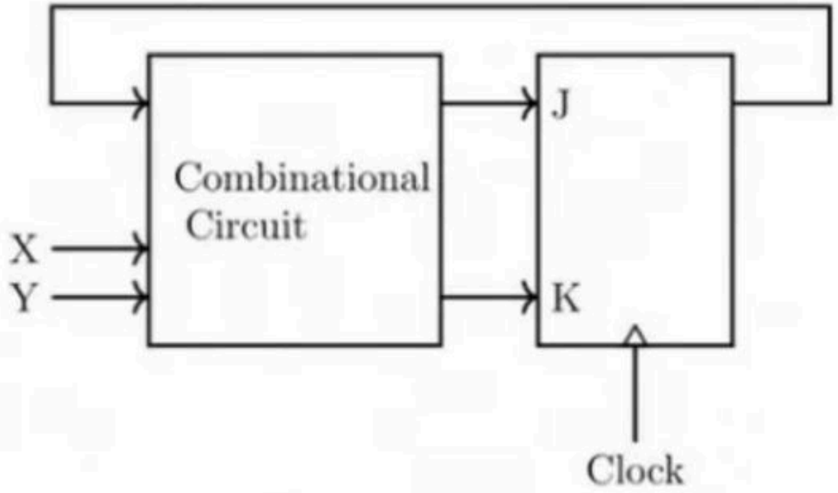
Which of the following input sequences for a cross-coupled $R - S$ flip-flop realized with two $NAND$ gates may lead to an oscillation?

A. $11, 00$
B. $01, 10$
C. $10, 01$
D. $00, 11$

GATE 2008

Consider the following state diagram and its realization by a JK flip flop



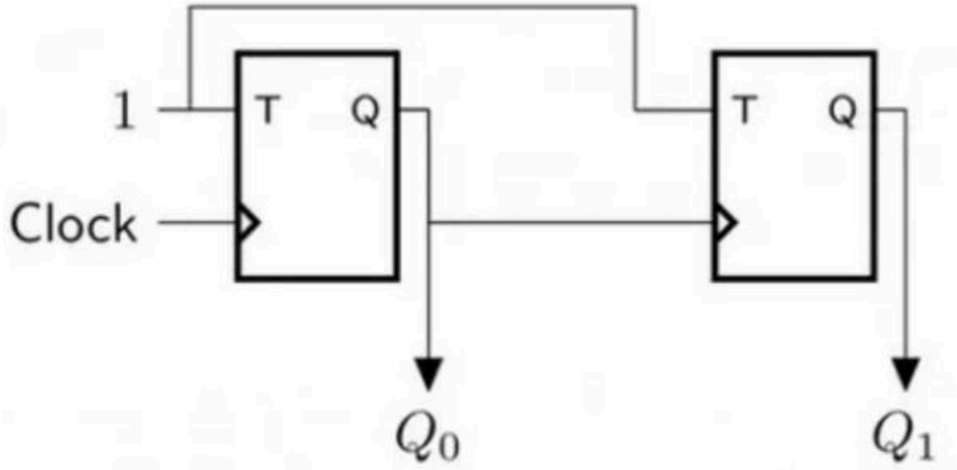


The combinational circuit generates J and K in terms of x, y and Q.
The Boolean expressions for J and K are :

A. $\overline{x \oplus y}$ and $\overline{x \oplus y}$
B. $\overline{x \oplus y}$ and $x \oplus y$
C. $x \oplus y$ and $\overline{x \oplus y}$
D. $x \oplus y$ and $x \oplus y$

GATE 2010

In the sequential circuit shown below, if the initial value of the output Q_1Q_0 is 00. What are the next four values of Q_1Q_0?



A. $11, 10, 01, 00$
B. $10, 11, 01, 00$
C. $10, 00, 01, 11$
D. $11, 10, 00, 01$

GATE 2011

The minimum number of D flip-flops needed to design a mod-258 counter is

A. 9
B. 8
C. 512
D. 258

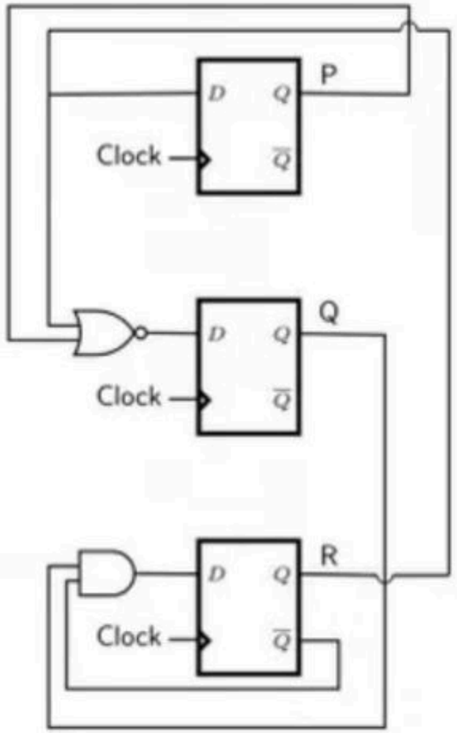
GATE 2011

The minimum number of D flip-flops needed to design a mod-258 counter is

A. 9
B. 8
C. 512
D. 258

GATE 2011

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.

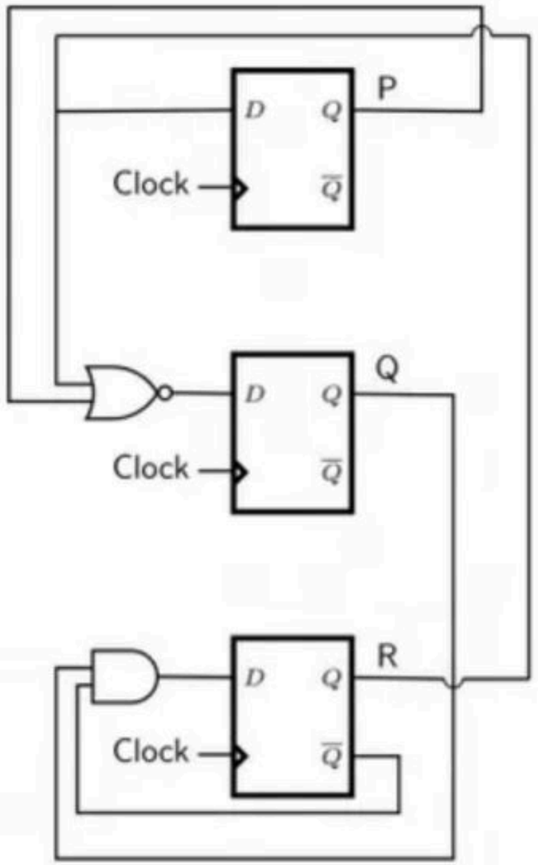


If at some instance prior to the occurrence of the clock edge, P, Q and R have a value $0, 1$ and 0 respectively, what shall be the value of PQR after the clock edge?

A. 000
B. 001
C. 010
D. 011

GATE 2011

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.



If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter?

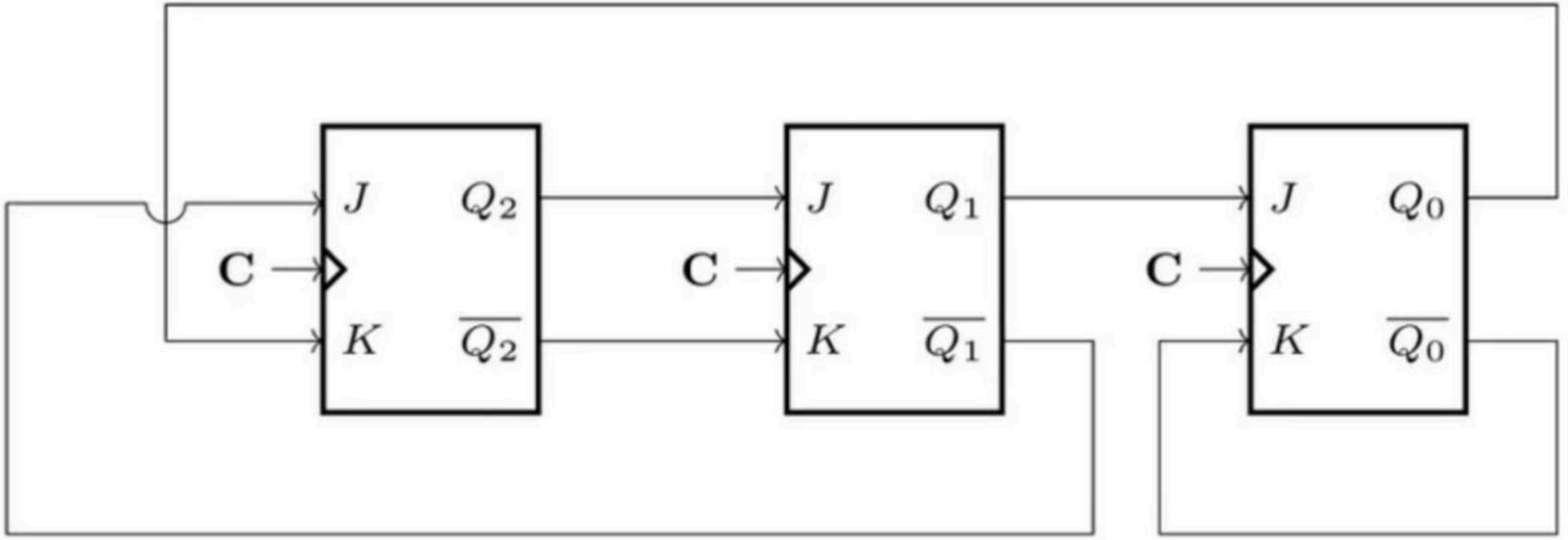
A. 3
B. 4
C. 5
D. 6

GATE 2014

Let $k = 2^n$. A circuit is built by giving the output of an n-bit binary counter as input to an n-to-2^n bit decoder. This circuit is equivalent to a

A. k-bit binary up counter.
B. k-bit binary down counter.
C. k--bit ring counter.
D. k-bit Johnson counter.

GATE 2014



The above synchronous sequential circuit built using JK flip-flops is initialized with $Q_2Q_1Q_0 = 000$. The state sequence for this circuit for the next 3 clock cycles is

A. $001, 010, 011$
B. $111, 110, 101$
C. $100, 110, 111$
D. $100, 011, 001$

GATE 2015

Consider a 4-bit Johnson counter with an initial value of 0000. The counting sequence of this counter is

A. $0, 1, 3, 7, 15, 14, 12, 8, 0$
B. $0, 1, 3, 5, 7, 9, 11, 13, 15, 0$
C. $0, 2, 4, 6, 8, 10, 12, 14, 0$
D. $0, 8, 12, 14, 15, 7, 3, 1, 0$

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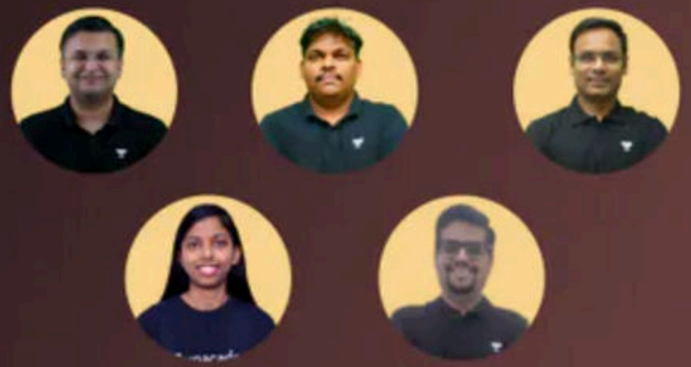

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