A Novel Gateless NPN Device for the ESD Protection

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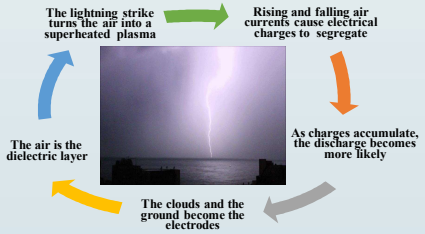
Abstract

In today's era, semiconductor chips are very essential in all aspects of daily life. The continuous scaling of semiconductors has led to unprecedented growth in the semiconductor industry or integrated circuits (ICs) market. However, this leads to a surge in several reliability concerns. Among them, electrostatic discharge (ESD) is one of the major reliability problems in ICs and is responsible for ~ 72% of total failures in the semiconductor industry. It has been reported that the ESD window intrudes at lower technology nodes into the semiconductor operating region, which could lead to a false ESD triggering.

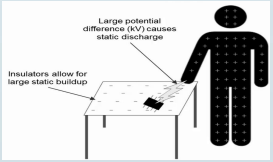
Here, we came up with a new and very simple gateless pnp device for ESD protection using the device physics of the diode. Whose hold and trigger voltages are lying in the ESD window. Its hold voltage is 1.204V and 1.738V, trigger voltage is 1.56V and 1.738V, R_{on} is 2204.08Ω and 990Ω, and breakdown voltage is 2.21V and 2.483V respectively for TLP and VFTLP models. Which are definitely in the ESD design window region.

Introduction

In nature, we see how lightning occurs. It is based on the triboelectric effect.



The same way Electrostatic discharge Occurs. Which is a major problem for the IC industries.



AIR:
- ~ 36 kV/cm
- Typical 0.5 cm spark ~ 20 kV

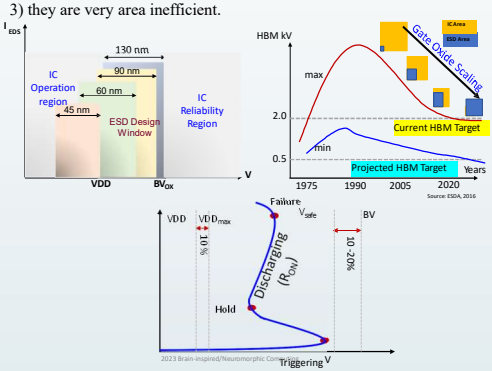
SiO_2:
- ~ 10 MV/cm
- Typical 10nm breakdown 10V

The 10V is detrimental to our Ics, as The maximum bearable voltage of ICs is about 1.2V. We need an additional circuit for ESD protection so that the protection can absorb the extra voltage and ICs could be saved.

Problem Statement

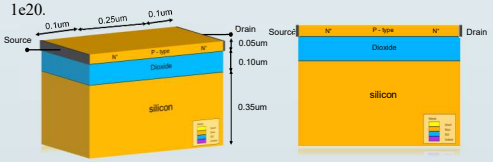
For lower technology nodes where the maximum voltage handling capacity of the thin gate oxide semiconductor devices used in the range of 0.7 V to 1 V, will require an ESD protection device with trigger voltage < 3 V. There are mainly three major issues in every existing ESD protection technic -

1) they need an additional device or trigger circuit for reducing the trigger voltage,
2) relatively show a higher trigger voltage > 3 V, and
3) they are very area inefficient.



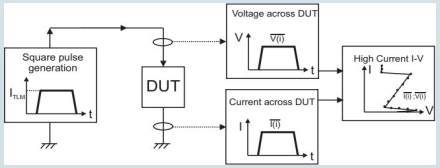
Methodology

As shown in the picture, we designed this device with Silicon, dioxide, and p-n doping. We took n^+ type doping as 1e18 and p-type doping as 1e20.

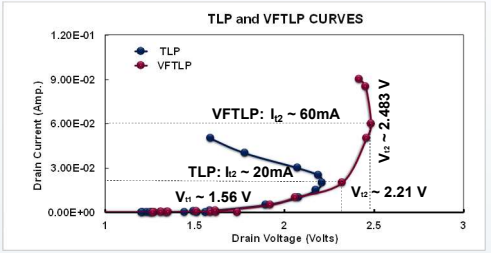


- There are two methods for ESD Characterization:
  —Transmission Line Pulsing (TLP): Rise Time 10 ns, Pulse Width 100 ns
  —Very Fast Transmission Line Pulsing (VF-TLP): Rise Time 200 ps, Pulse Width 10 ns

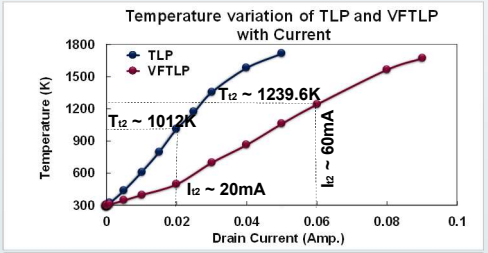
We did standard TLP, VFTLP, and HBM simulations in the Silvaco Software. And for calculating Voltage, we took an average of voltage present during the 30 to 90% of the total pulse width. As shown in the picture, we designed this device with Silicon, dioxide, and p-n doping.

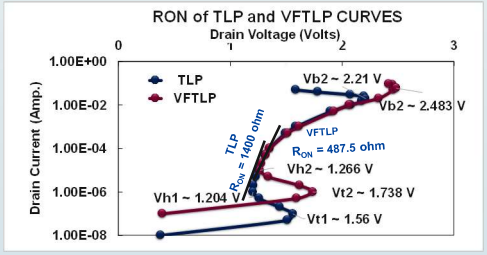


Results

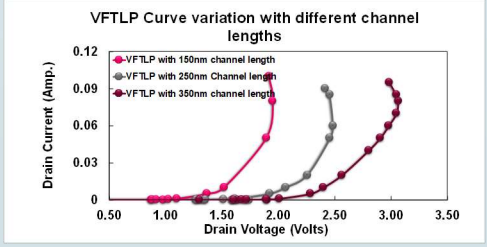


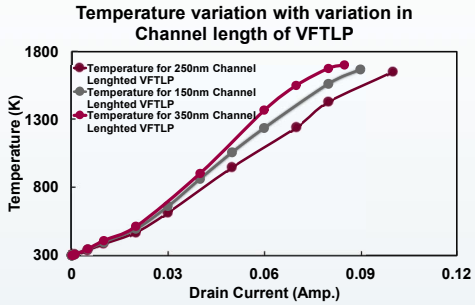
Here, TLP which is a slower transient, has an early thermal breakdown because of self-heating. This is happening due to the allowance of carriers to impact ionization more. The rate of breakdown will be much higher than the VFTLP which is a faster transient.





The On Resistance of TLP is comparatively more due to self-heating.





Conclusion

1. Here, we got hold and trigger voltages in the ESD Design window, and the trigger voltage is less than the breakdown voltage.
2. We didn't use any trigger circuit for reducing trigger voltage. we came up with a new and very simple gateless pnp device for ESD protection using the device physics of the diode. Thus our pnp device is also an area-efficient device.
3. Here, we can conclude that on increasing the channel length of p-type doping our curve is sliding to the right side.
4. Our Ron is very high compared to other devices

References

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Publication

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