Department of E&C Engineering

VLSI LAB

VLSI LAB PROJECT REPORT

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8 BIT ALU: SOUL OF MICROPROCESSORS

SUMITTTED TO

KALPANA BHAT
ASSISTANT PROCESSOR
EC DEPT, NITK

SUBMITTED BY
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ABSTRACT:

In computing, an arithmetic logic unit (ALU) is a digital circuit that performs arithmetic and logical operations. The ALU is a fundamental building block of the central processing unit (CPU) of a computer, and even the simplest microprocessors contain one for purposes such as maintaining timers. The processors found inside modern CPUs and graphics processing units (GPUs) accommodate very powerful and very complex ALUs; a single component may contain a number of ALUs.

OBJECTIVE:

The purpose of this project is to design, implement and layout an 8-bit ALU using the magic spice layout tool software and CMOS design principles studied in the course.

DESIGN PROCEDURE:

The ALU design allows for 8 operations and accepts 2, 8-bit inputs(A and B), 3 control inputs(S0,S1,S2) and produces an 8 bit output (Z) and a carry output for the operations involving the use of the adder.

THE FUNCTION TO BE IMPLEMENTED AS

- ADDITION(ADD)
- ADDITION WITH CARRY(ADDC)
- SUBTRACTION(SUB)
- SUBTRACTION WITH CARRY(SUBC)
- NAND
- NOR
- OR
- AND

Relevance of the functions(Why have we selected these functions only):

- Addition and subtraction are most important function of any microprocessor or CPU.
- Addition with carry and subtraction with carry are used when two or more cascaded ALU chip implement 16 bit(or as required) arithmetic operation then carry of last stage is

given to next stage and added(subtracted) with the functions ADDC, SUBC.

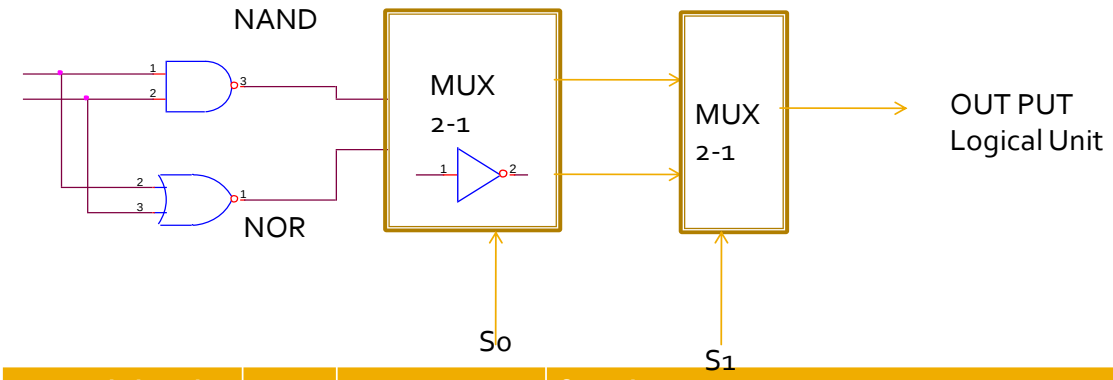
- AND, OR, NAND, NOR are the basic functions of LU. Many operations involves these bitwise operation over A, B.

What does it consist of

- Logical Unit
  - NAND gate
  - NOR gate
  - MUX
  - NOT gate
- Arithmetic unit
  - Full Adder
    - 2-Xor gates for sum bit
    - 3,2-input nand gates, one 3-input nand gate for carry out
  - Subtraction unit
    - Use of FA with
    - NOT gate(B') and one mux(selection of B or B')

Schematic for

Logical unit



Control signals			function
s2	s1	s0	
0	0	0	nand
0	0	1	nor
0	1	0	and
0	1	1	or

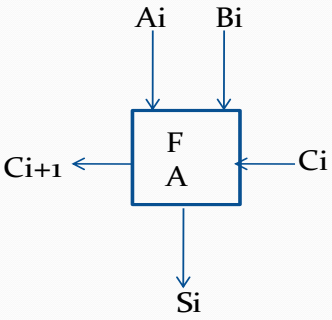
Logic optimization:

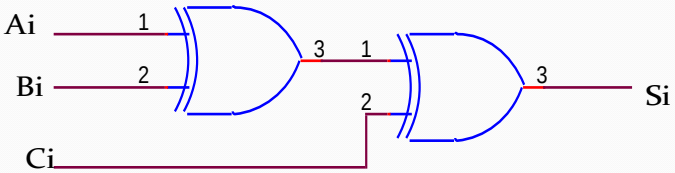
1. Selection of nand, nor through mux
2. Implementation of AND, OR fn from the output of above mux only as inbuilt NOT gate in the mux.
3. Selection of outputs of mux with other mux

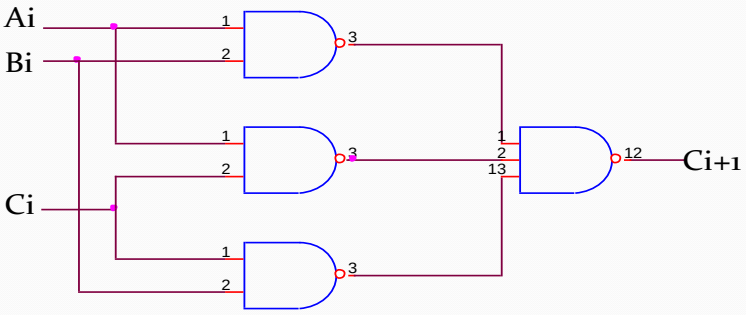
- Resources Utilization:
  - one NAND gate,
  - one NOR gate,
  - Two 2-to-1 muxs

Schematic for

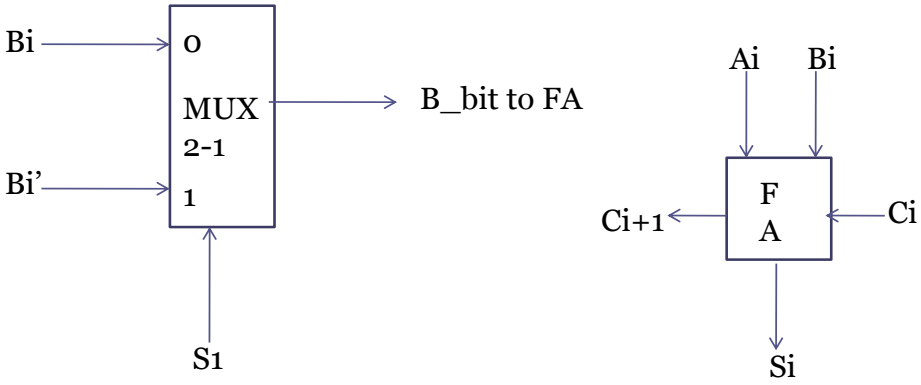
Fulladder for addition and subtraction



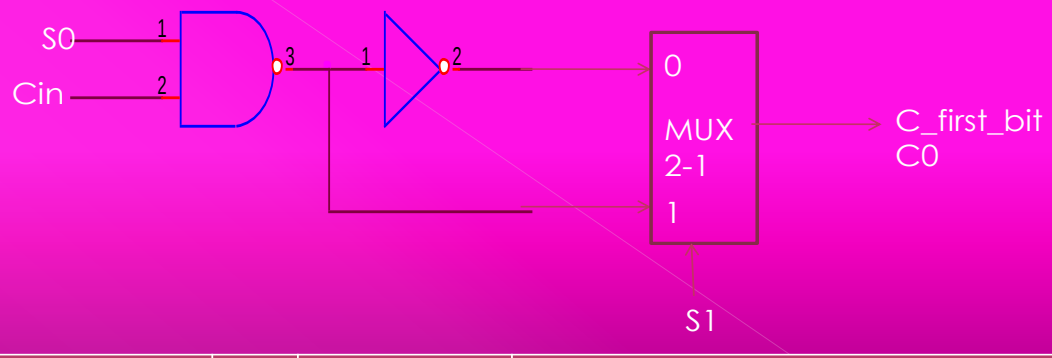




Cont…



Carry Generate for first bit FA



Control signals			function
1	0	0	Add A+B
1	0	1	Add with carry A+B+Cin
1	1	0	Sub. A-B
1	1	1	Sub. With carry A-B-Cin

Logic optimization:

4. Implementation of all Arithmatic fn(ADD,ADDC,SUB,SUBC) from the same FA.
5. No Selection needed as output of FA itself is selected for the fn.

- Resources Utilization:
  - 2-Xor gates for sum bit,
  - 3,2-input nand gates, one 3-input nand gate for carry out
  - NOT gate(B') and one 2-to-1 mux(selection of B or B')

LOGIC for implemention of all Arithmatic fn (ADD, ADDC, SUB, SUBC) from the same FA.

When So=0,S1=0

C_first_bit Co=0 → A+B → (ADD)

When So=1,S1=0

C_first_bit Co=Cin → A+B+Cin → (ADDC)

When So=0, S1=1

C_first_bit Co=1 → A-B(A+B'+1) → (SUB)

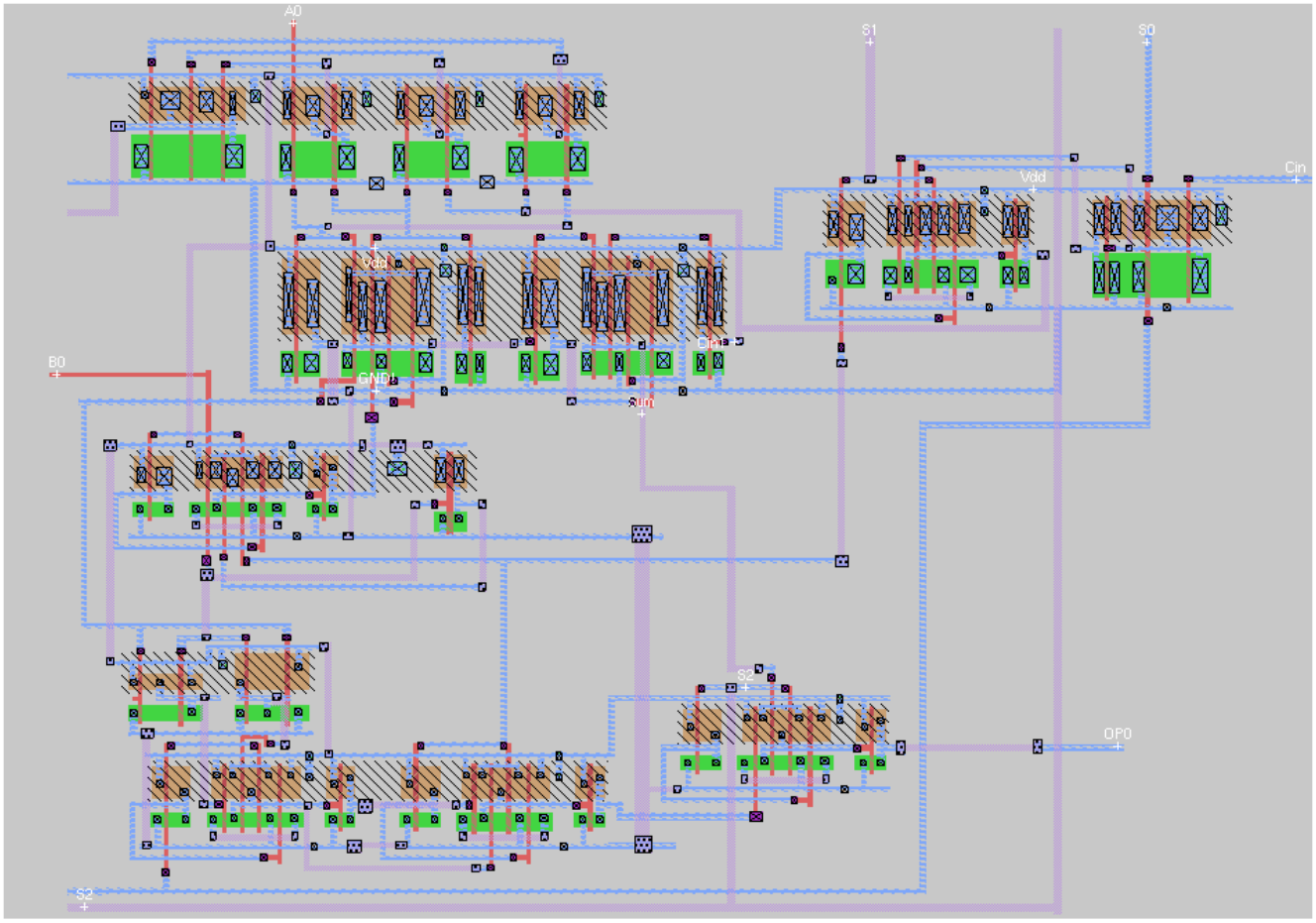
When So=1, S1=1

C_first_bit Co=Cin' → A-B-Cin(A+B'+Cin'= A+B'+(1-Cin)) → (SUBC)

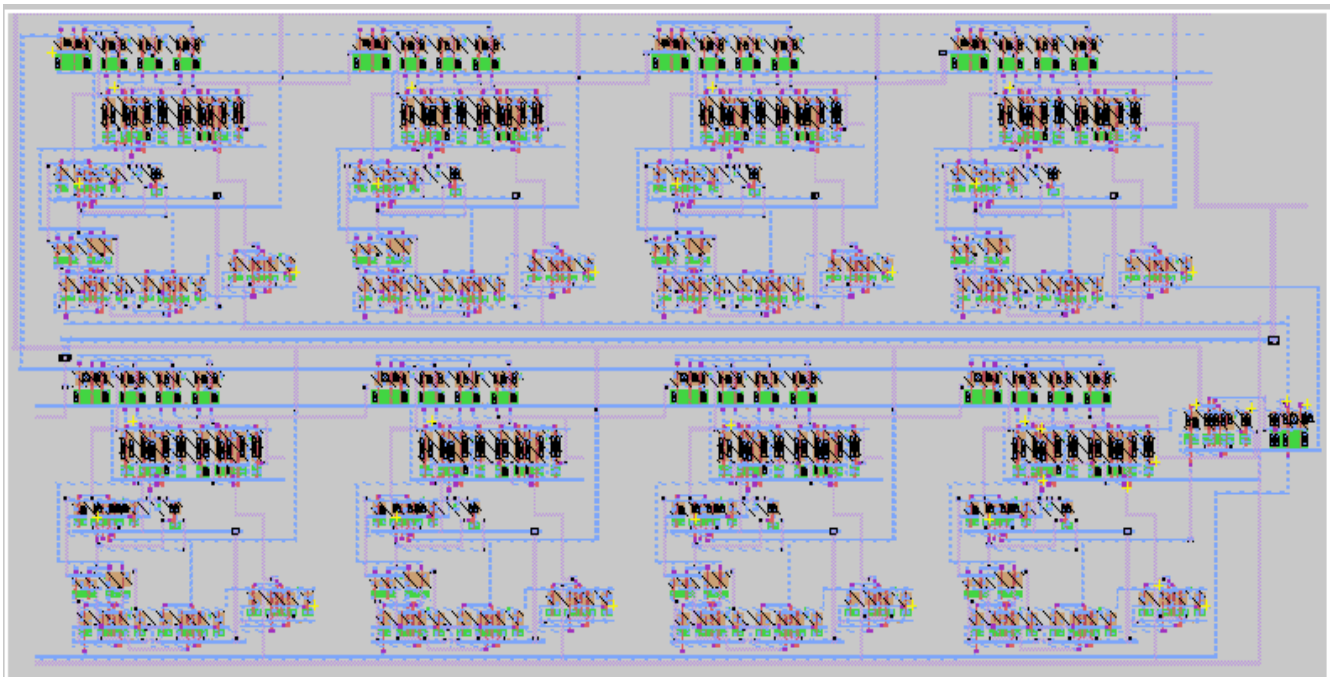
- ALU can be used for both signed and unsigned addition and subtraction.

Layout:

One Bit ALU



8 bit ALU Layout:

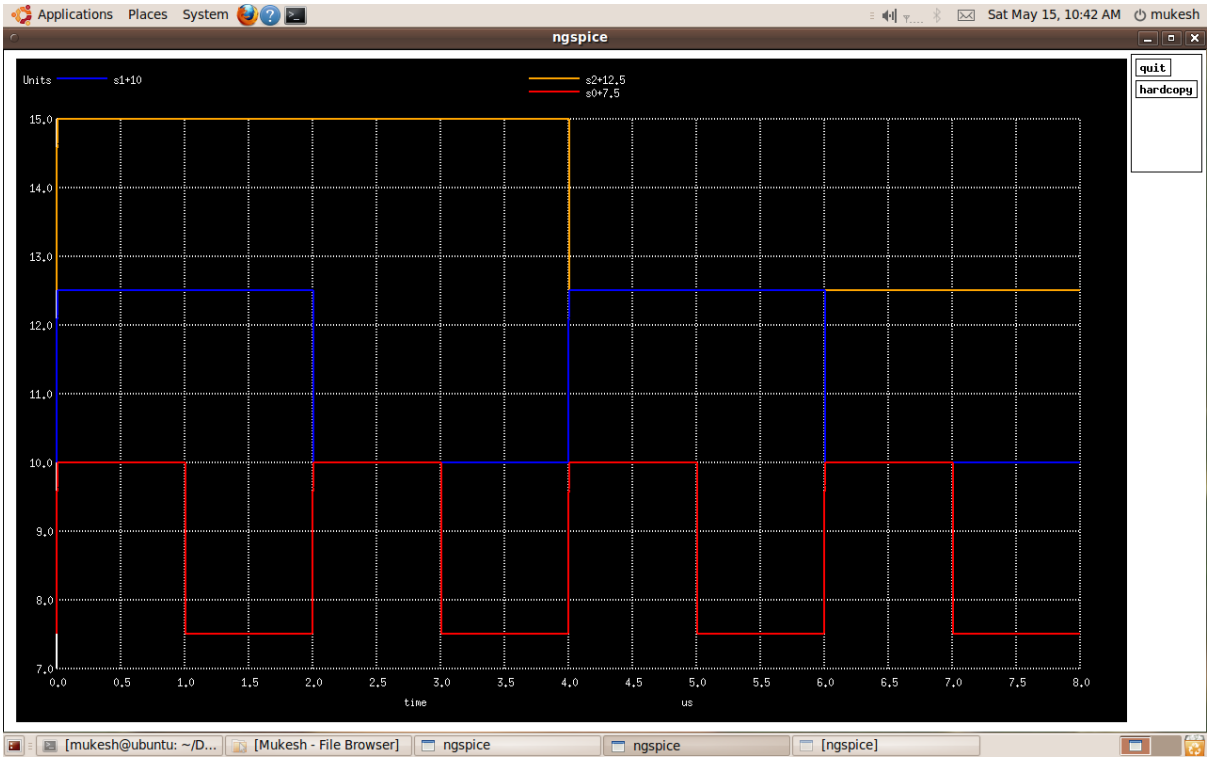


Simulation Results:

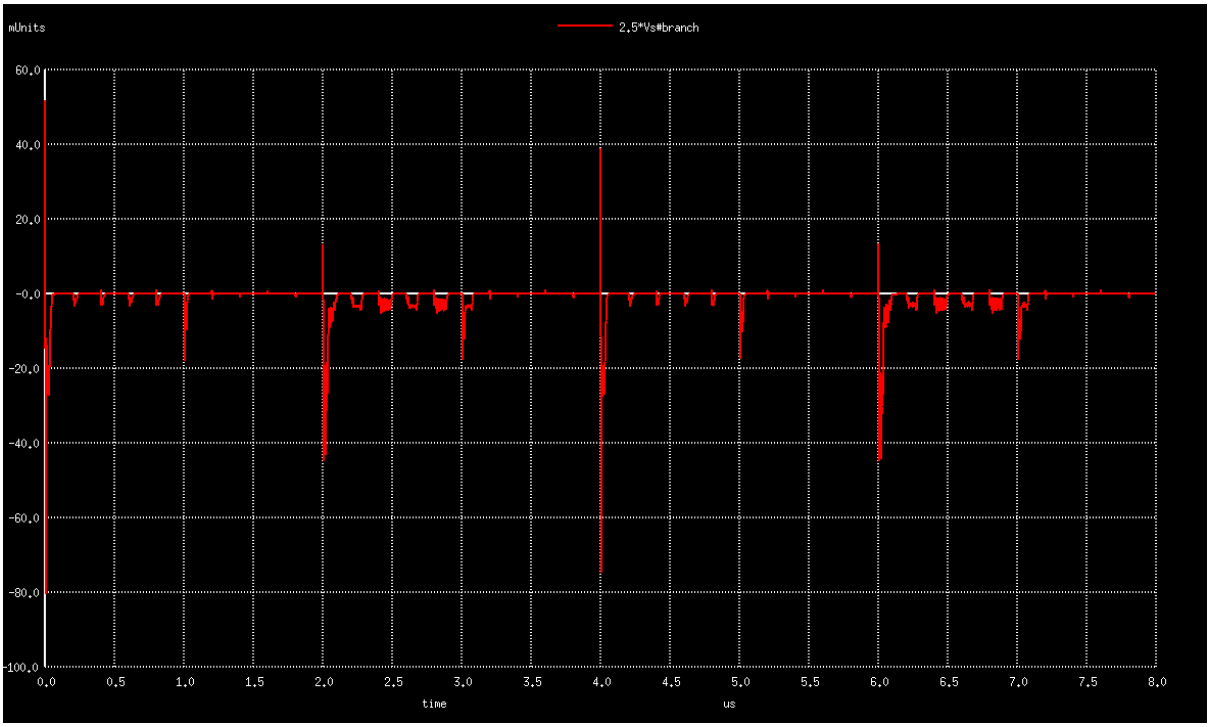
simulation

- A=10110100
- B=11011011
- And =10010000
- Or=11111111
- Nand=01101111
- Nor=00000000
- Addition=(1)10001111
- Addition with carry=(1)10010000
- Subtraction=(0)11011001
- Sub with carry whenCin=0
  =(0)11011001
  whenCin=1
  =(0)11011000

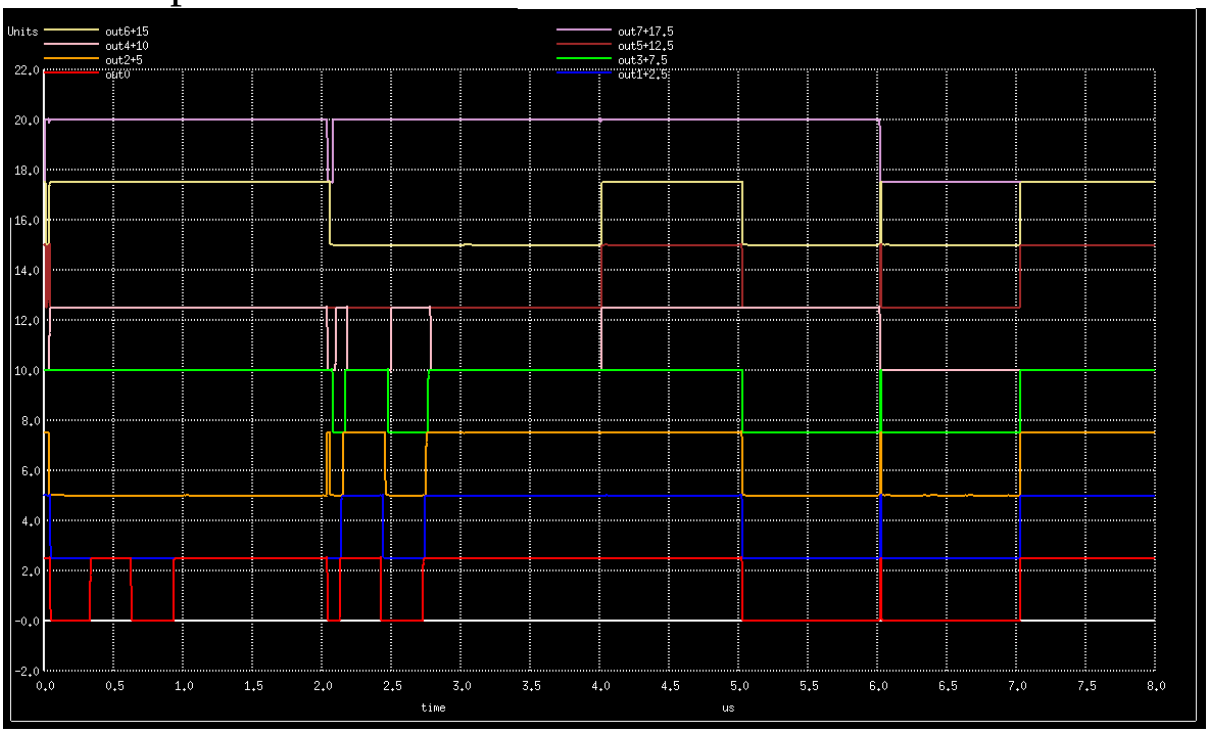
Select Lines(control lines)



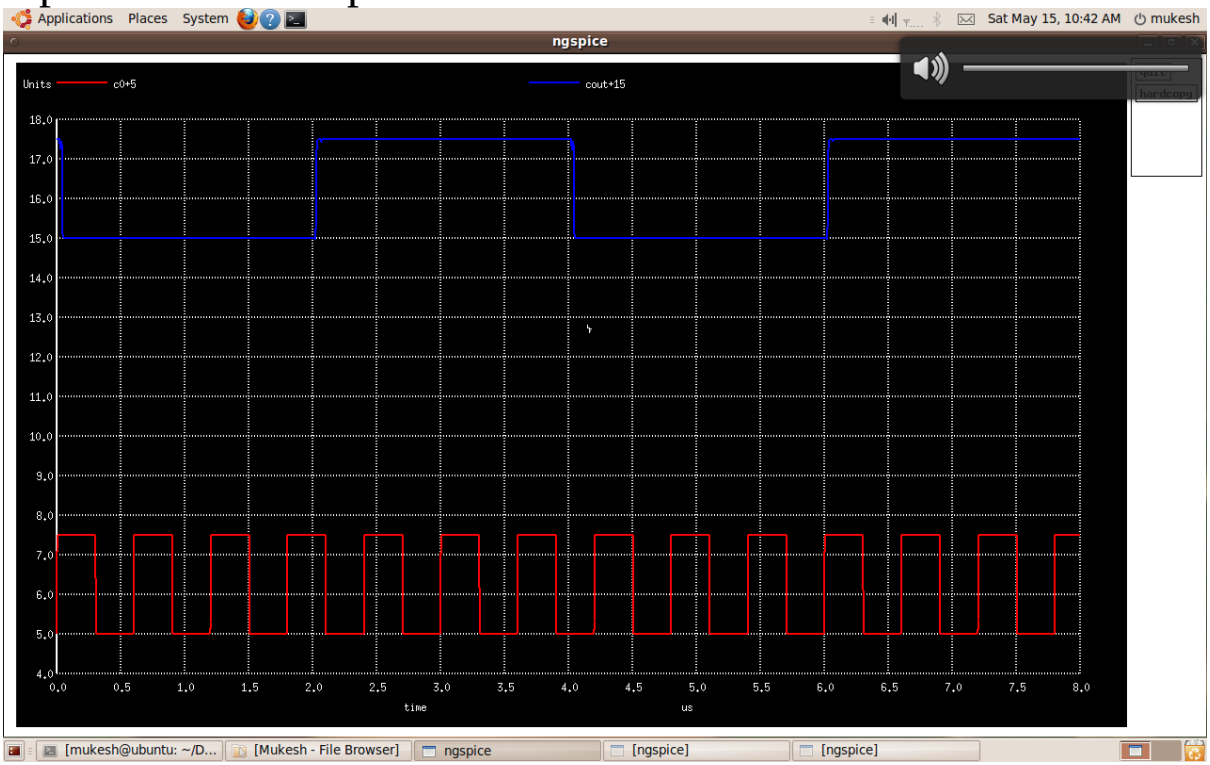
Power consumption:



8 bit Output:



Input Cin and Output Cout:



INDIVIDUAL MEMBER CONTRIBUTION:

- RAKESH RANGDAL
  Design and analysis of AU implementing ADD and SUB
  Report for the Unit Designed
- PINTULAL MEENA
  Design and analysis of Logical Unit implementing NAND, NOR, AND, OR functions.
  Report for the Unit Designed
  Making document on MS word and typing.
- MUKESH KUMAR
  Design of Carry Generate for first bit FA implementing ADD, ADDC, SUB and SUBC with the help of AU implementing ADD and SUB. Idea and searching of material on internet.

Assembly all the units for one bit and then making it for 8 bit and interconnecting was done by all of us.

Performance measuement

- Maximum power consumption: 80mw (at transitions)
- Area of the layout : 2500x1200
- Worst case delay = : 100ns

Conclusion

- 8 bit ALU was designed , simulated and verified
- Only CMOS logic was used improving power performance.
- The layout was optimized for logic and was found efficient in power ,speed and area

REFERENCE:

- **Dcoa By Raffiquzman**
- **Digital Logic Design By Morris Mano**
- **Class notes and Lab expt manuals for spice and magic layout tool.**
- VLSI - Digital Integrated Circuits (Rabaey)