

VLSI DESIGN LAB

Report Submitted in partial fullfilment of course
on VLSI Design Lab (EC364)

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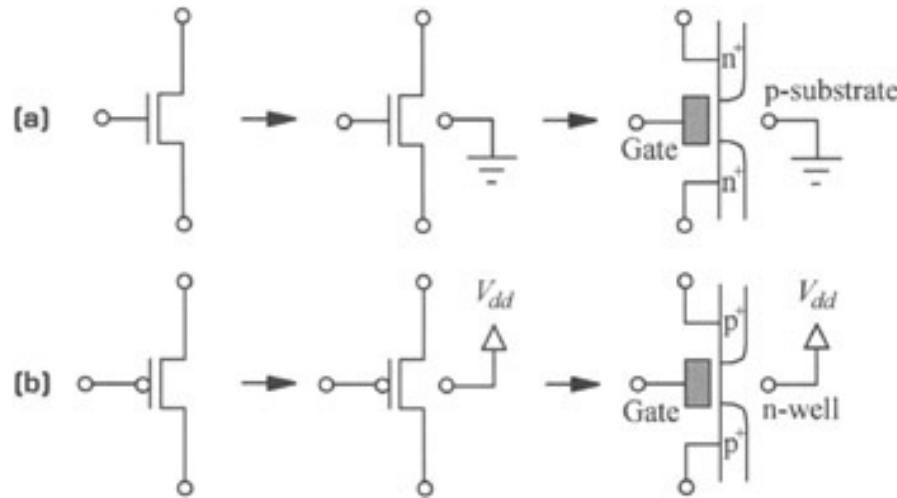
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MODULE-1 REPORT : CIRCUIT SIMULATION WITH NGSPICE

Lab 1: NMOS input, output characteristics with parametric sweeps

Objective: Study the input and output characteristic of NMOS transistor. Effect of length, width, VTO, VSB, lambda, and temperature on the behavior of transistor.



Parameters:

Voh : Maximum output voltage when the output level is logic "1"

Vol : Minimum output voltage when the output level is logic "0"

Vil : Maximum input voltage which can be interpreted as logic "0"

Vih : Minimum input voltage which can be interpreted as logic "1"

Rise Time: Time taken for output voltage to change from low to high upon change in input.

Fall Time: Time taken for output voltage to change from high to low upon change in input.

Noise Margin: NMI = Vil - Vol NMH = Voh - Vih

Propagation Delay: Time it takes for the output signal voltage to switch after the input signal voltage has been applied.

Vm: Point on the transfer characteristics curve where Vin= Vout.

Input Output Characteristics

```
m1 d g 0 0 my_nmos l = .5u w = 0.5u
```

```
*sources
v_dd d 0 dc 5
v_gg g 0 dc 3
```

```
.dc v_dd 0 5 0.1 v_gg 0 3 1
plot -v_dd#branch
```

```
end  
.endc  
.end
```

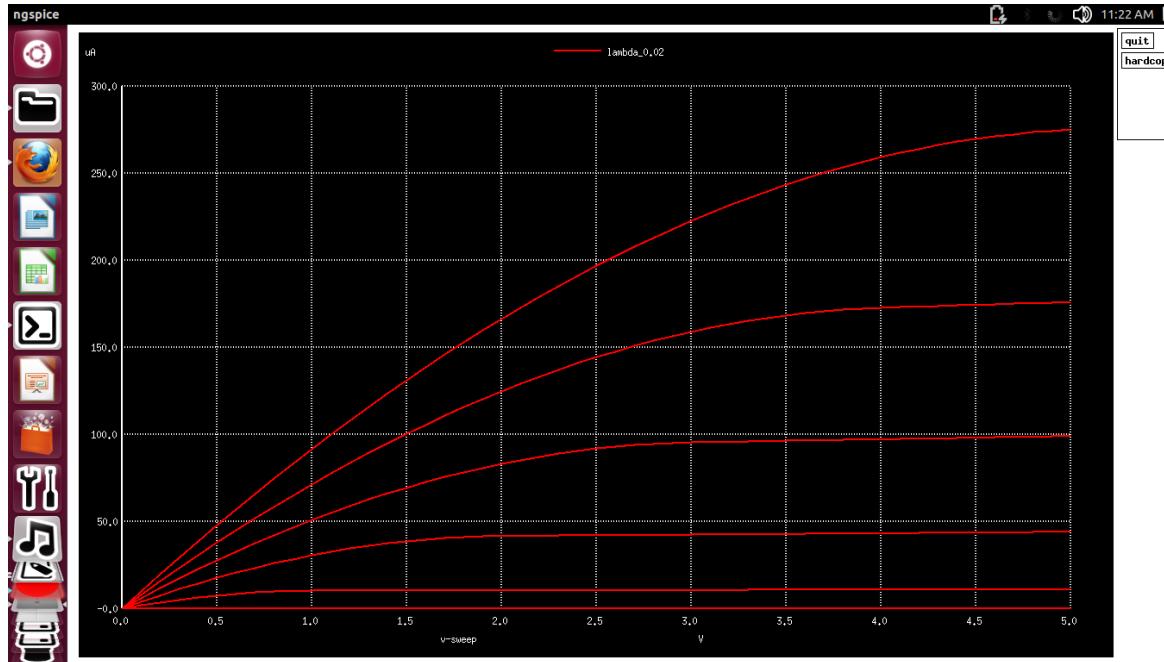


Figure 1: Id vs Vdd Characteristics

Input Characteristics of nmos

```
m1 d g 0 0 my_nmos l = .5u w = 0.5u

*sources
v_dd d 0 dc 5
v_gg g 0 dc 3

.dc v_gg 0 5 0.1
plot -v_dd#branch
end
.endc
.end
```

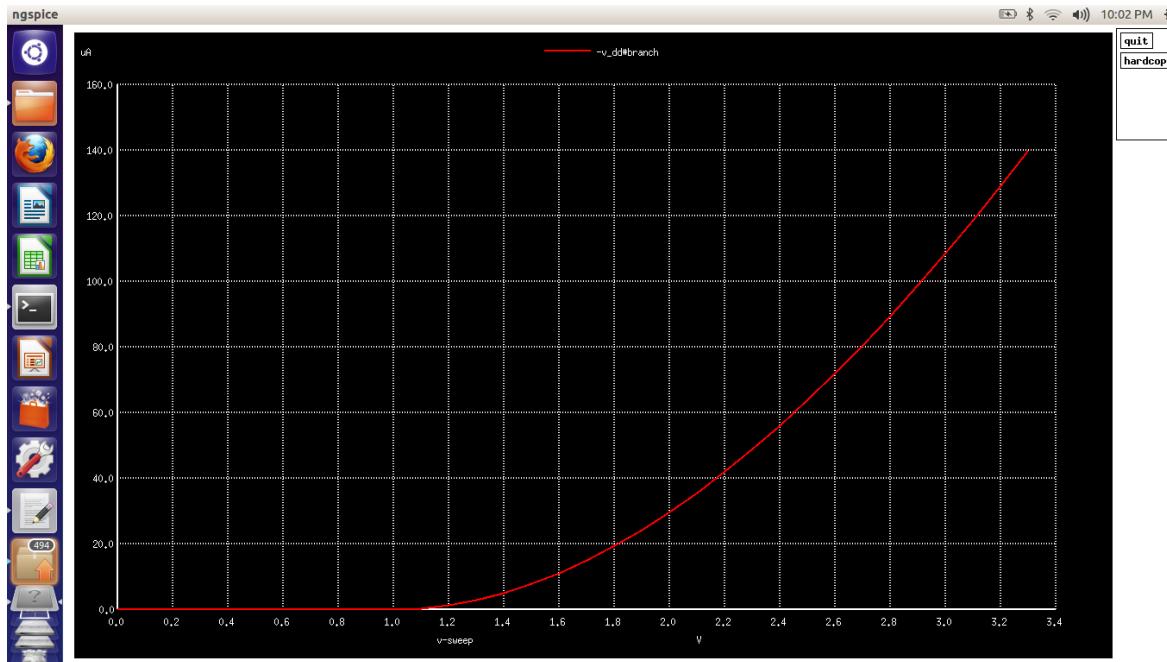


Figure 2: Input Characteristics

Varying Lambda Id vs Vdd

```
m1 d g 0 0 my_nmos l = .5u w = 0.5u

*sources
v_dd d 0 dc 5
v_gg g 0 dc 3

.dc v_dd 0 5 0.1 v_gg 0 3 1

*response for various lambda

.control
foreach lmda .01 .05 .09
altermod m1 LAMBDA=$lmda
run
end
.endc
```

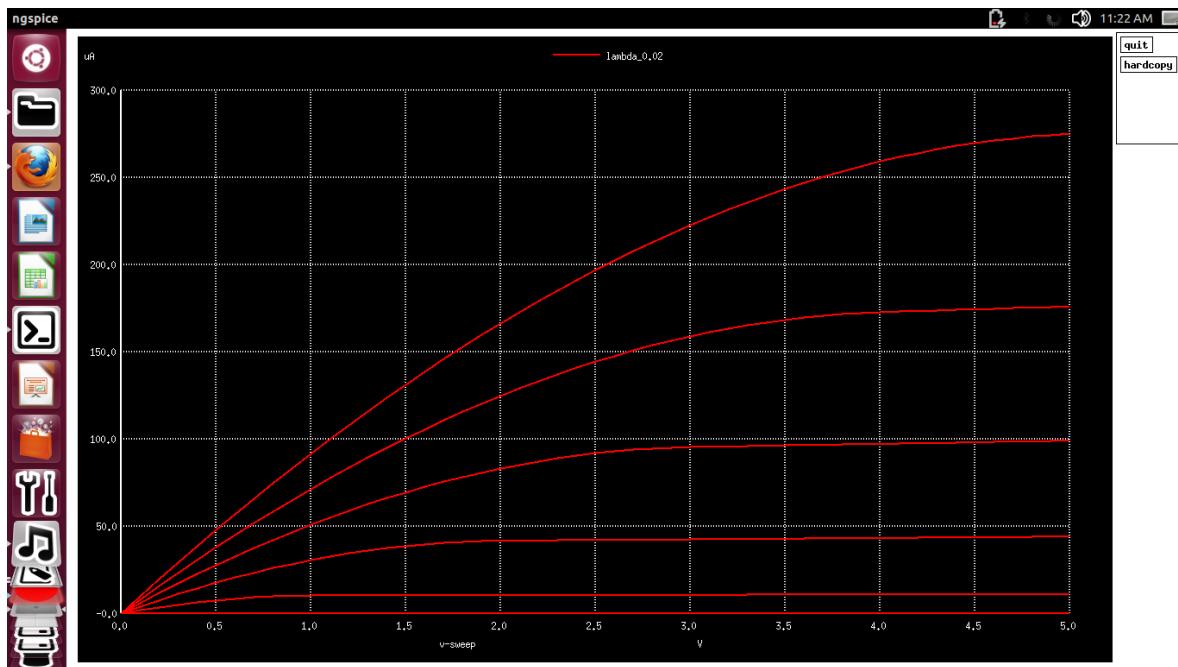


Figure 3: Id vs Vdd for lambda 0.01

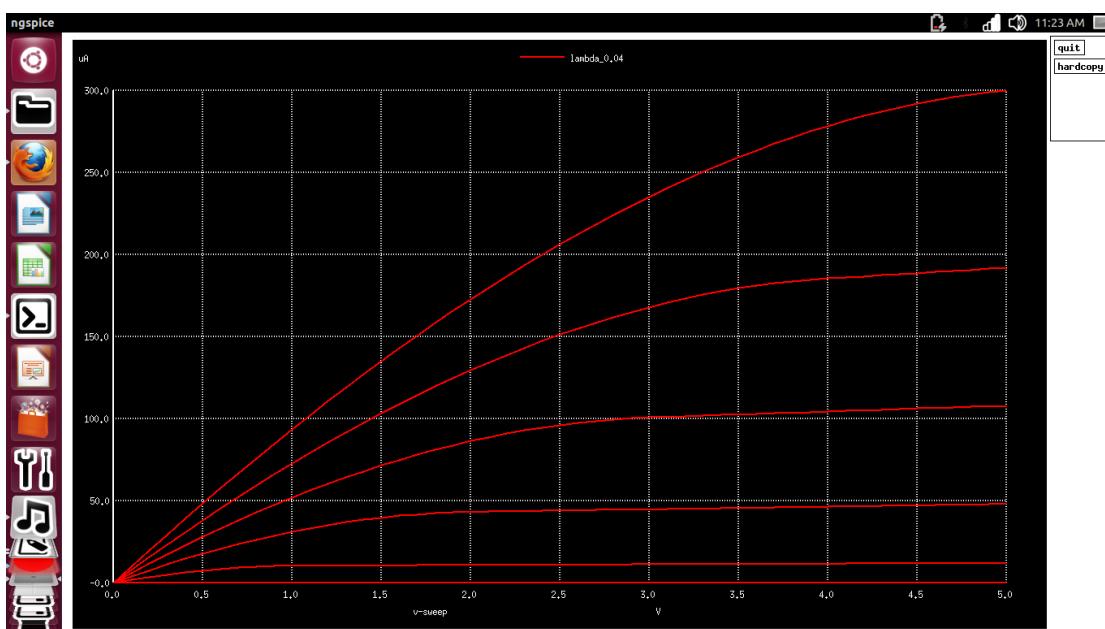


Figure 4: Id vs Vdd for lambda 0.05

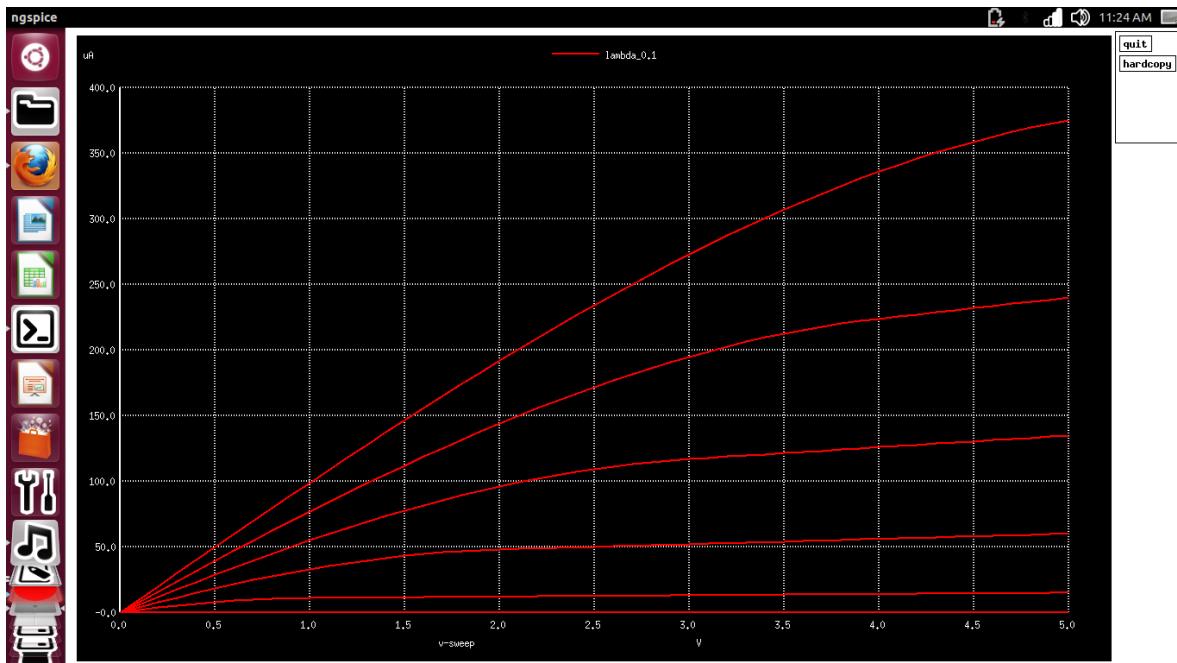


Figure 5: Id vs Vdd for lambda 0.09

```
.control
foreach iter 1 2 3
setplot dc$iter
plot -v_dd#branch
end
.endc
.end
```

Reason : The Id vs Vdd curve is at first linear then becomes varies slowly in saturation region due to channel length modulation which should be otherwise constant.

Varying Temperature

```
.include /home/Ankit/Desktop/11ec86-93/t14y_tsmc_025_level1.txt
m0 out in Vss 0 RITSUBN1 TEMP=27

*sources
Vgng Vss 0 dc 0
vdd out 0 dc 5
Vin in 0 dc 5

.dc Vin 0 5 .1
.control
foreach t1 27 50 100
alter m0 TEMP =$t1
run
end
.endc
```

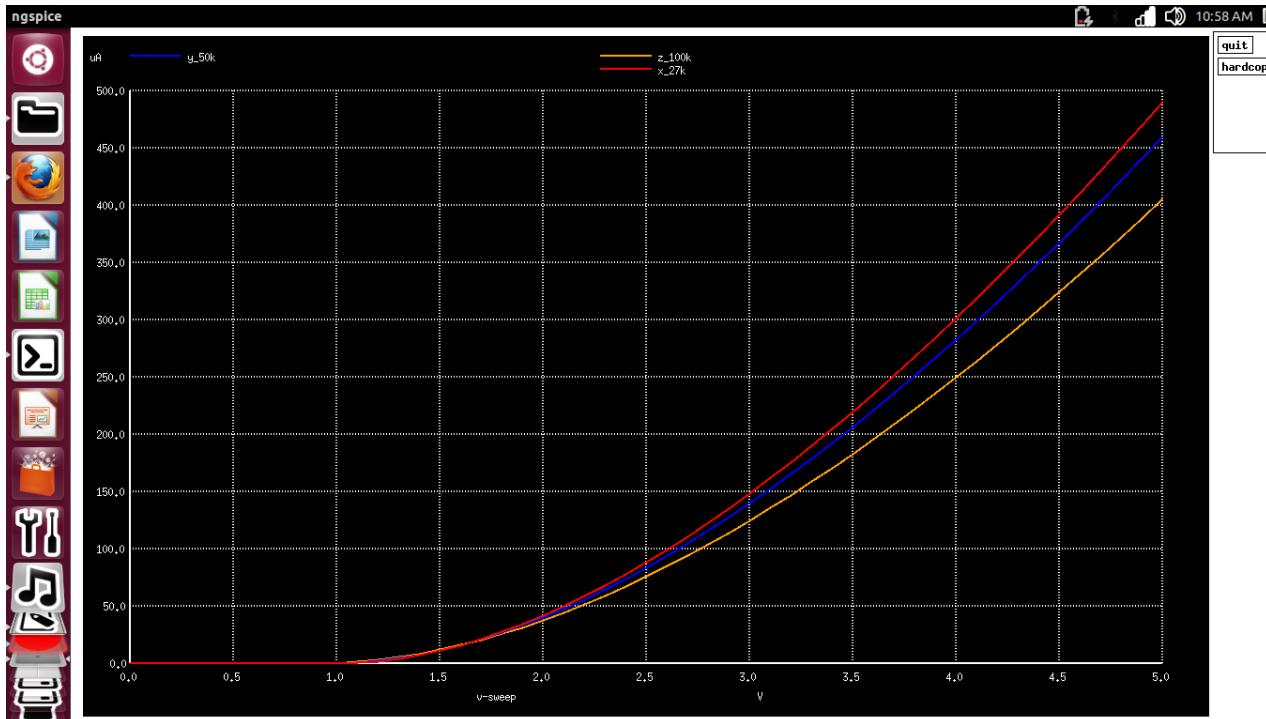


Figure 6: Temperature Variation

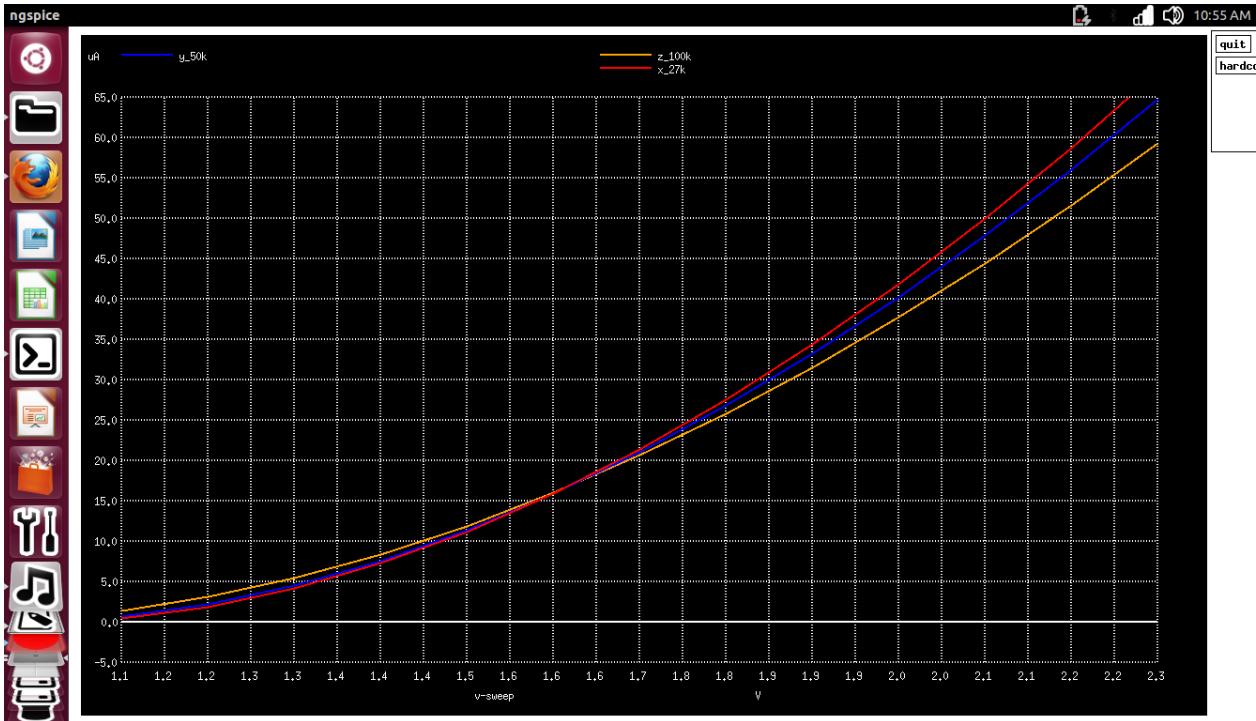


Figure 7: Temperature Variation Flipover of curv (zoom)

Conclusion: In the above figure for VI characteristics, as the value of temperature increases, the current decreases. Hence, the current is inversely proportional to the temperature.

Varying Length

```
*nmos characteristics varing length

*include model files

.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level1.txt

*netlist
m1 drain gate 0 0 RITSUBN1 l=3u w=0.5u

*define the sources
vdd drain 0 dc 5
vgg gate 0 dc 5
.dc vdd 0 5 0.1 vgg 0 5 1

*Computing the response for various width('len' variable)
.control
foreach len 1.5e-6 6e-6 3e-5
alter m1 l = $len
run
end
.endc
```

```

*plotting the output for various length
.control
foreach iter 1 2 3
setplot dc$iter
plot -vdd#branch
end
.endc

```

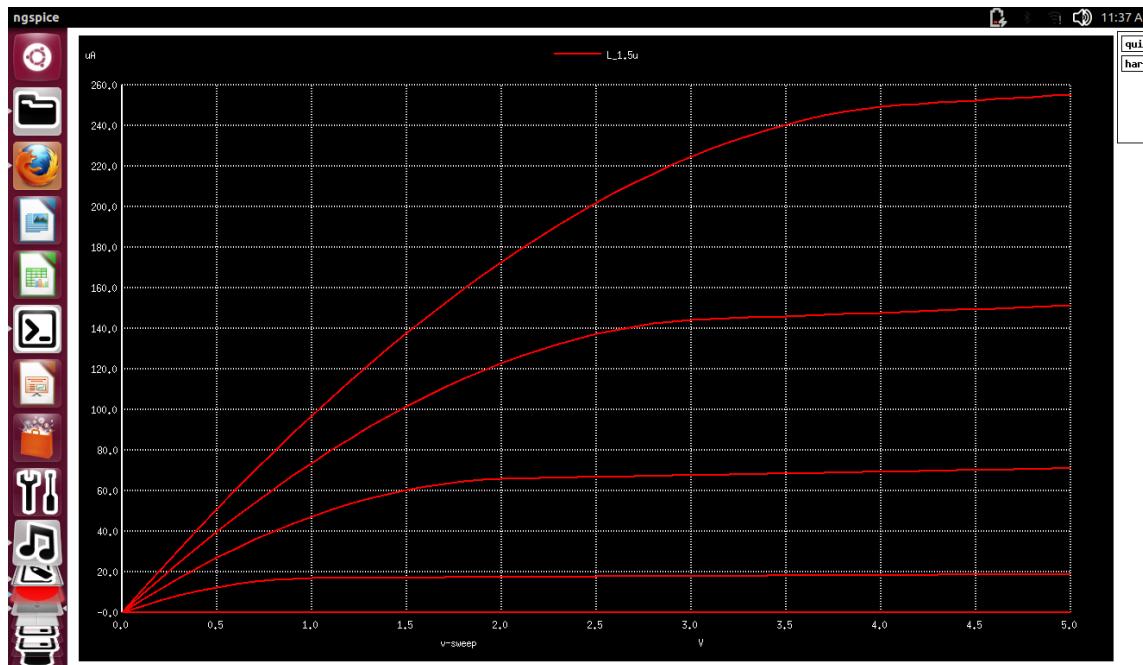


Figure 8: For Length 1.5u

Conclusion: In the above figure for the VI characteristics. With increase in the value of L, the drain current decreases as shown.

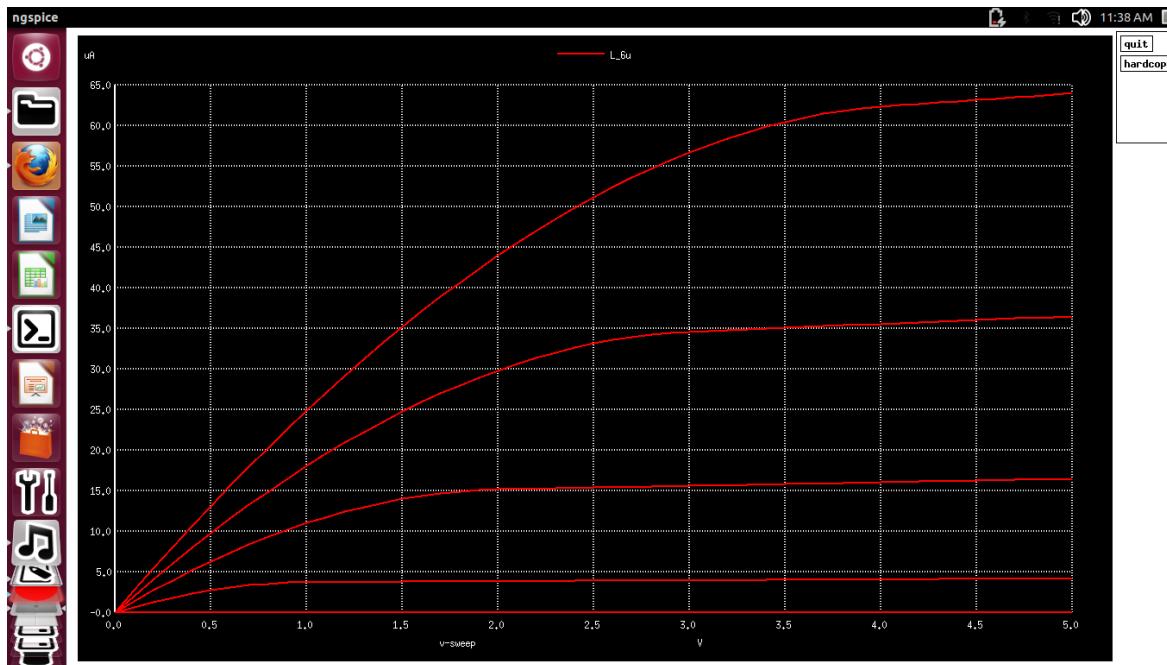


Figure 9: For Length 6u

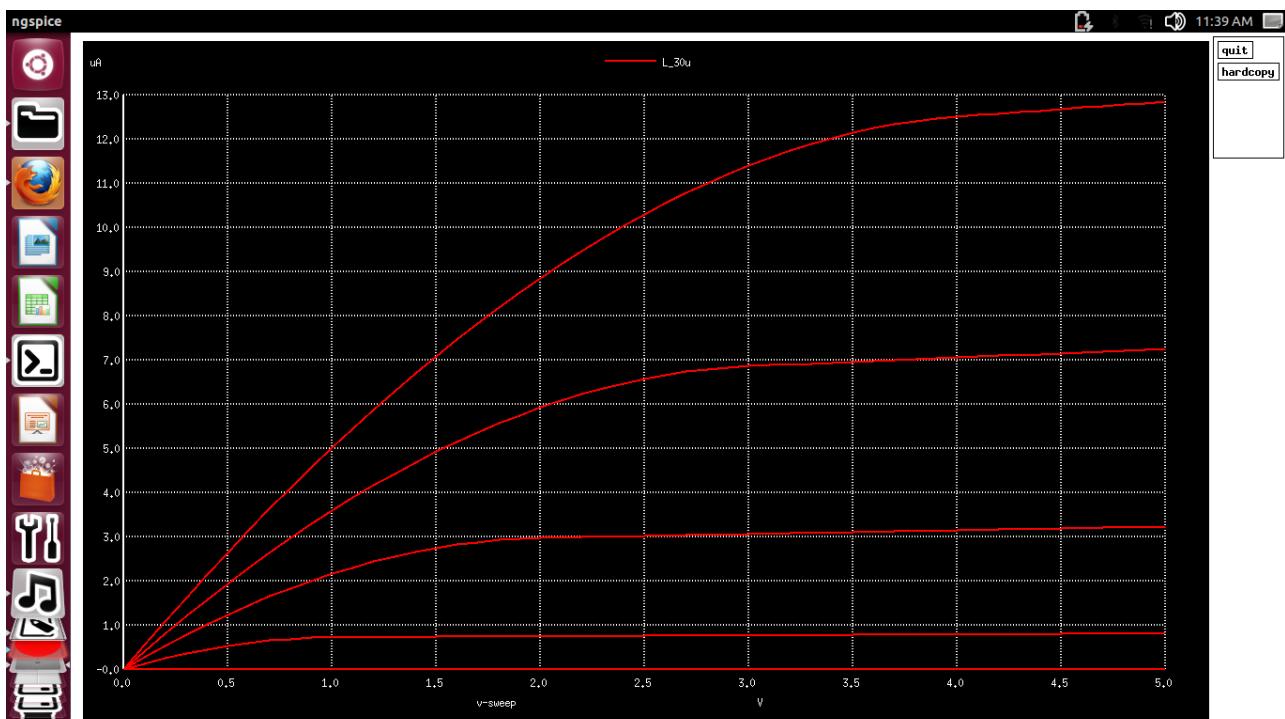


Figure 10: For Length 30u

Varying VTO

```
.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level1.txt
.model my_nmos nmos LEVEL=1 VT0=.03
m0 out in Vss 0 my_nmos

*sources
Vgnd Vss 0 dc 0
vdd out 0 dc 5

*input_source
Vin in 0 dc 5
.dc Vin 0 5 .1

.control
foreach res 0.5 1 2
altermod m0 VT0= $res
run
end
.endc

.control
foreach iter 1 2 3
setplot dc$iter
plot -vdd#branch
end
.endc
```

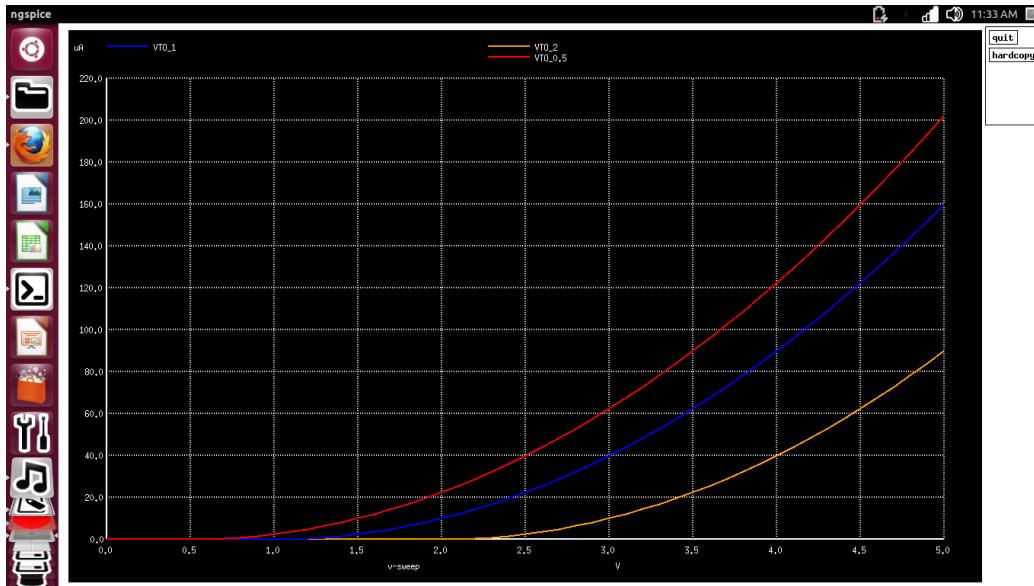


Figure 11: For Varying VTO

Conclusion : In the above figure for VI characteristics, As the value of VTo increases, the current decreases. Hence, the current is inversely proportional to VTo.

Varying VSB

```
.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level3.txt
m1 drn gate s 0 cmosn l=1u w=.5u

vdd drn 0 5
vin gate 0 5
vss s 0 0

.dc vin 0 6 .1 vss 0 3 1
.control
run
plot -vdd#branch
.end
```

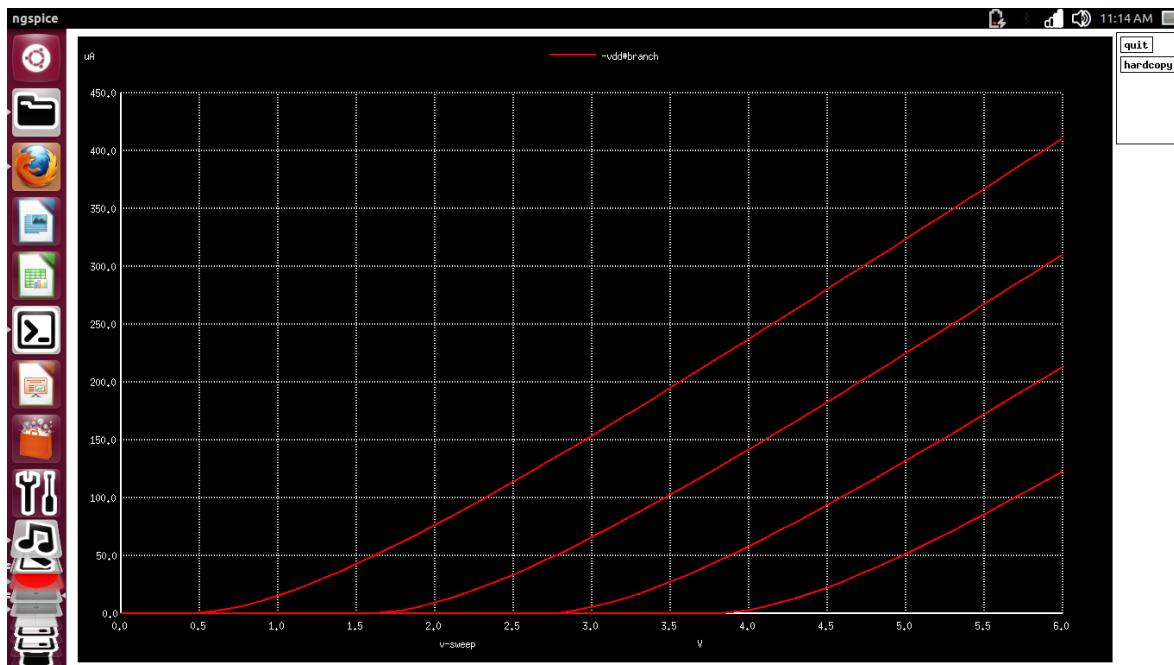


Figure 12: For varying VSB

Varying Width

```
*nmos characteristics
.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level1.txt

*netlist
m1 drain gate 0 0 RITSUBN1 l=3u w=0.5u

*define the sources
vdd drain 0 dc 5
vgg gate 0 dc 5
```

```

.dc vdd 0 5 0.1 vgg 0 5 1

*Computing the response for various width
.control
foreach wid 1e-6 3e-6 5e-6
alter m1 w = $wid
run
end
.endc

*plotting the output for various width
.control
foreach iter 1 2 3
setplot dc$iter
plot -vdd#branch
end
.endc

```

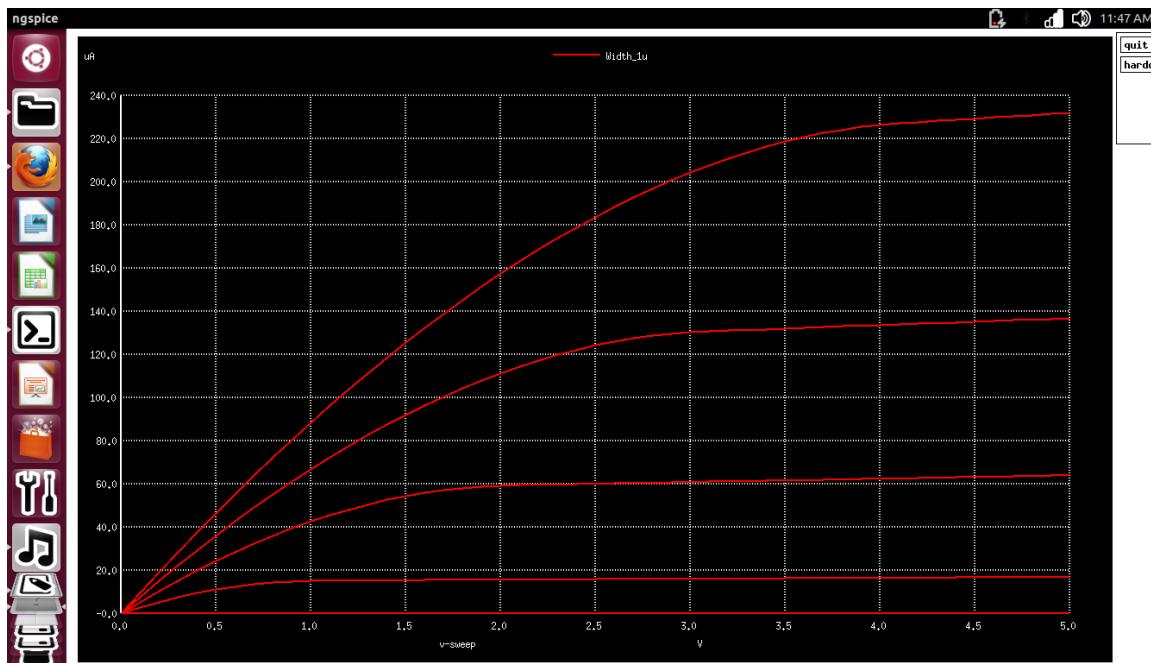


Figure 13: For varying Width

Conclusion: In the above figure for the VI characteristics. With increase in the value of W, the drain current increases as shown.

Figure 14: For varying Width

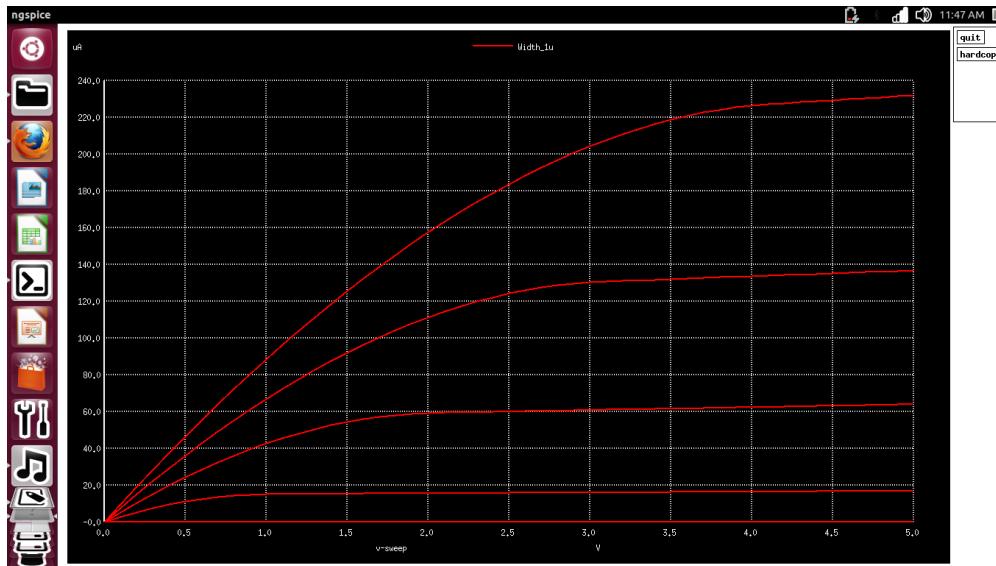


Figure 15: For Width = 1u

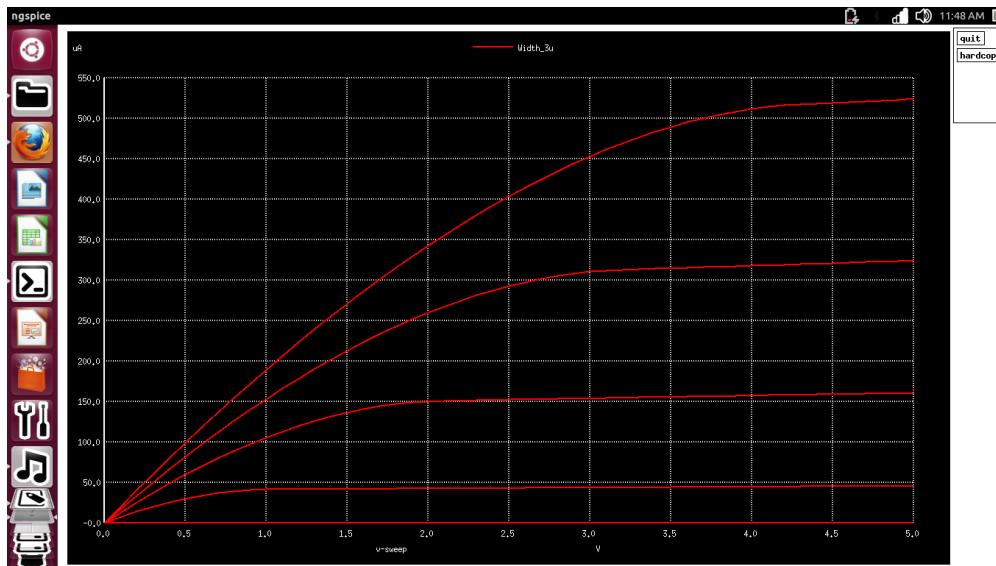


Figure 16: For Width= 3u

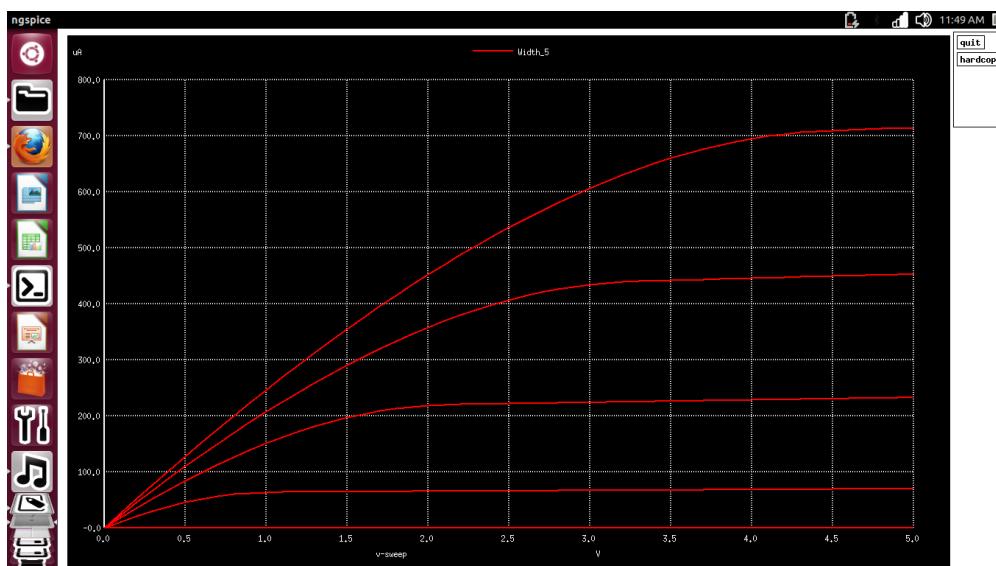


Figure 17: For Width = 5u

Conclusion: As L increases, I_d decreases. As W increases, I_d increases. As V_{To} increases, I_d decreases. As Lambda increases, I_d increases. As VSB increases, I_d decreases (As VT increases)
As temperature increases, I_d decreases

Parameters:

Voh : Maximum output voltage when the output level is logic "1"

Vol : Minimum output voltage when the output level is logic "0"

Vil : Maximum input voltage which can be interpreted as logic "0"

Vih : Minimum input voltage which can be interpreted as logic "1"

Rise Time: Time taken for output voltage to change from low to high upon change in input.

Fall Time: Time taken for output voltage to change from high to low upon change in input.

Noise Margin: NMI = Vil - Vol NMH = Voh - Vih

Propagation Delay: Time it takes for the output signal voltage to switch after the input signal voltage has been applied.

Vm: Point on the transfer characteristics curve where $V_{in} = V_{out}$.

Lab 2: Study of MOS inverter with passive resistive load

Objective: Study the transfer function, Noise margin, effect on risetime, falltime, propagation delay, power and energy consumed of a MOS Inverter for various L, W, Load Capacitance and rise/fall time of input.

Circuit Diagram

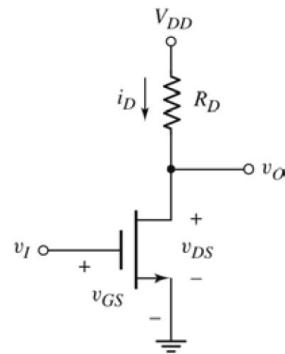


Figure 18: NMOS inverter with resistive load

Varying Resistive Load and Varying Width

*nmos characteristics

```
*include model files
.include /home/vlsilab/UG_students_2014/11ec8611ec93/t14y_tsmc_025_level3.txt
*netlist
m1 out in 0 0 CMOSN l=1u w=0.5u
```

```
* Input voltage source
Vdd vdd 0 5
r0 vdd out 100
V_in in 0 dc 2.5 pulse(0 5 0 1n 1n 2n 4n)
*DC voltage source
.dc 0 5 0.000004
.tran 1n 4n
```

```
*Computing the response for various resistiv_load
```

```
.control
foreach res 100 1k 100k
alter r0 = $res
run
end
.endc
```

```

*plotting the output for various width
.control
foreach iter 1 2 3
setplot dc$iter
plot in out
plot -Vdd#branch
setplot tran$iter
plot in out
plot -Vdd#branch
end
.endc

```

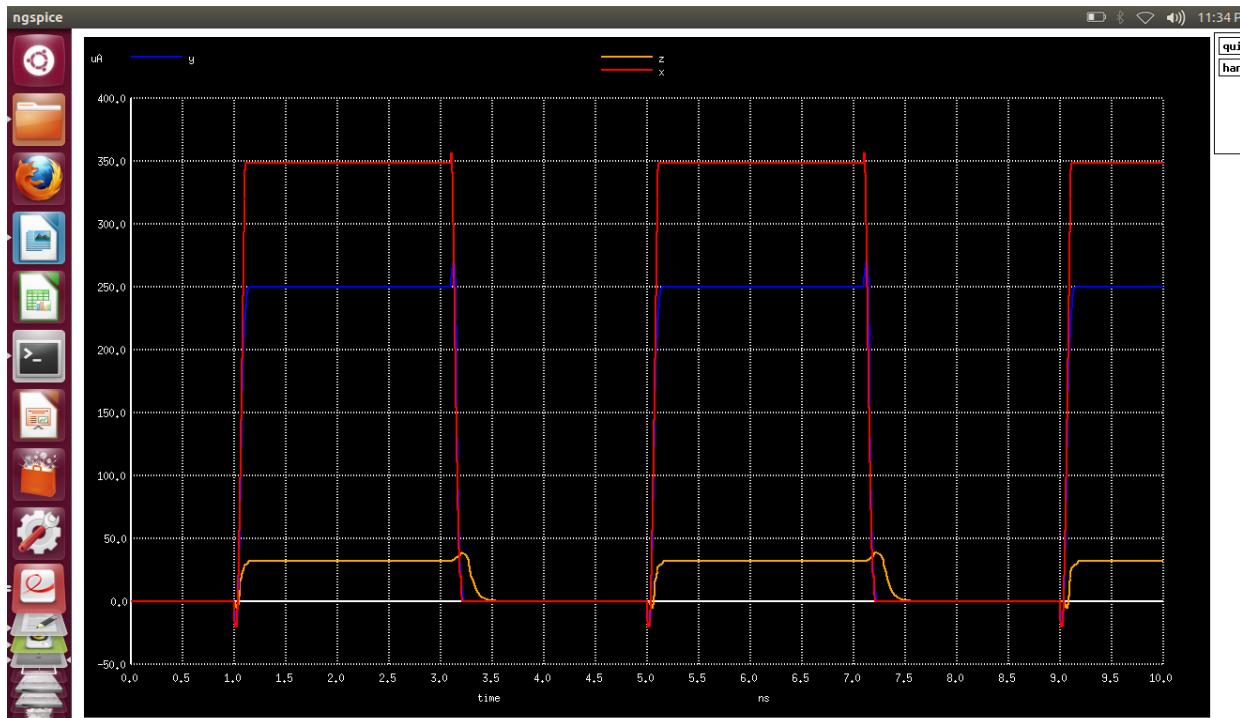


Figure 19: For Current due to varying Resistance

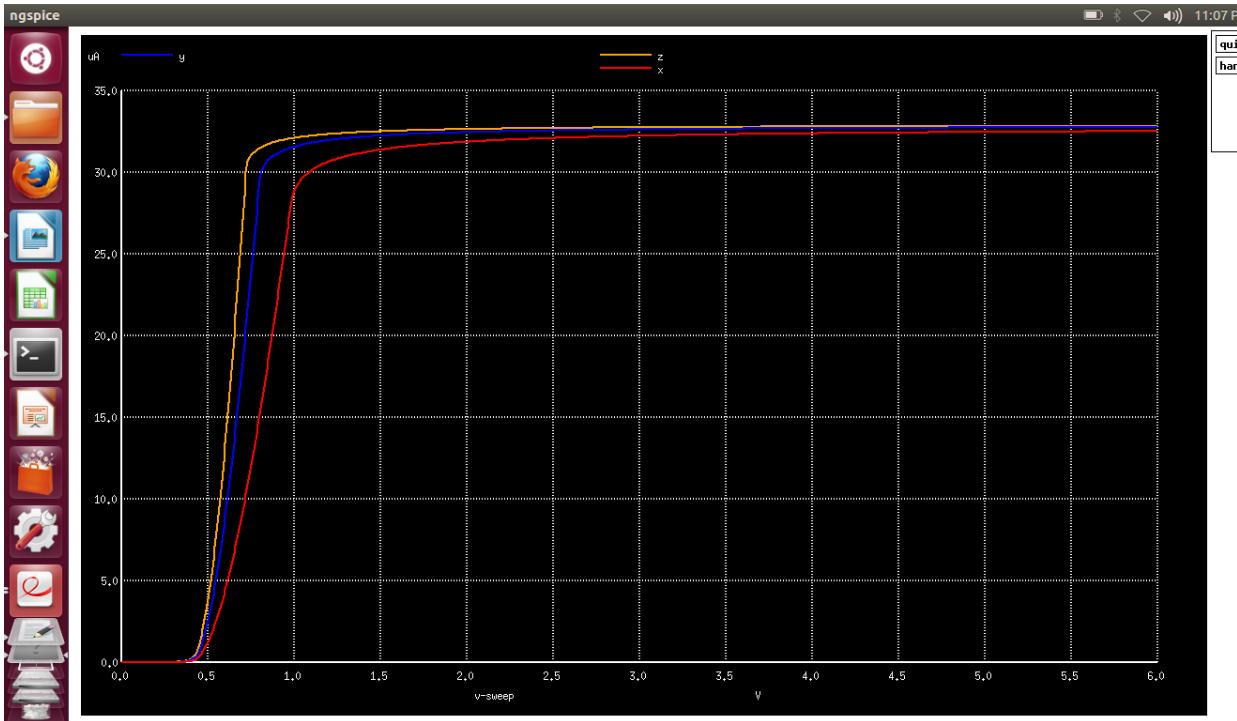


Figure 20: For Current due to W/L ratio variation

Inverter DC Transfer Characteristics

* nmos inverter resistiv_load DC transfer function only

```
.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level3.txt
r1 vd out 0.1k
m1 out in 0 0 CMOSN l=1u w=1u

*sources
vdd vd 0 dc 3.3
vin in 0 dc 3.3

.dc vin 0 6 .01

* for transfer fun pic
.control
run
plot out
.endc
end
```

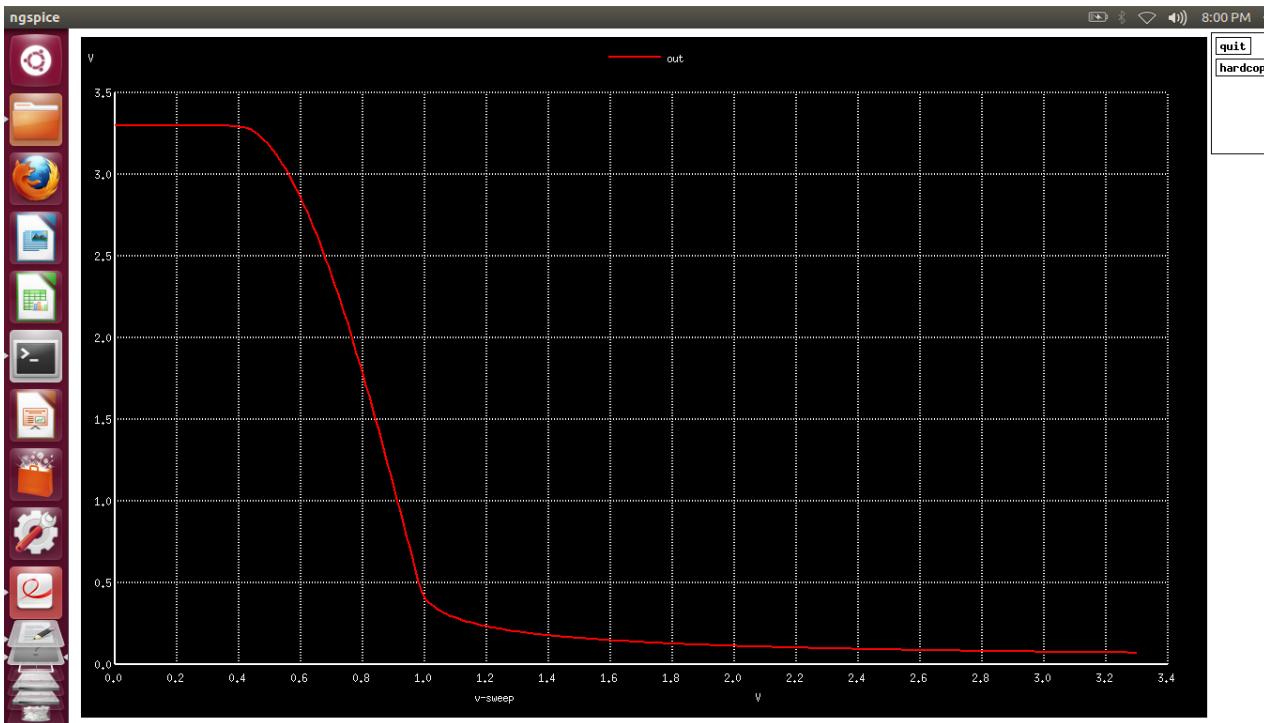


Figure 21: Transfer Characteristics

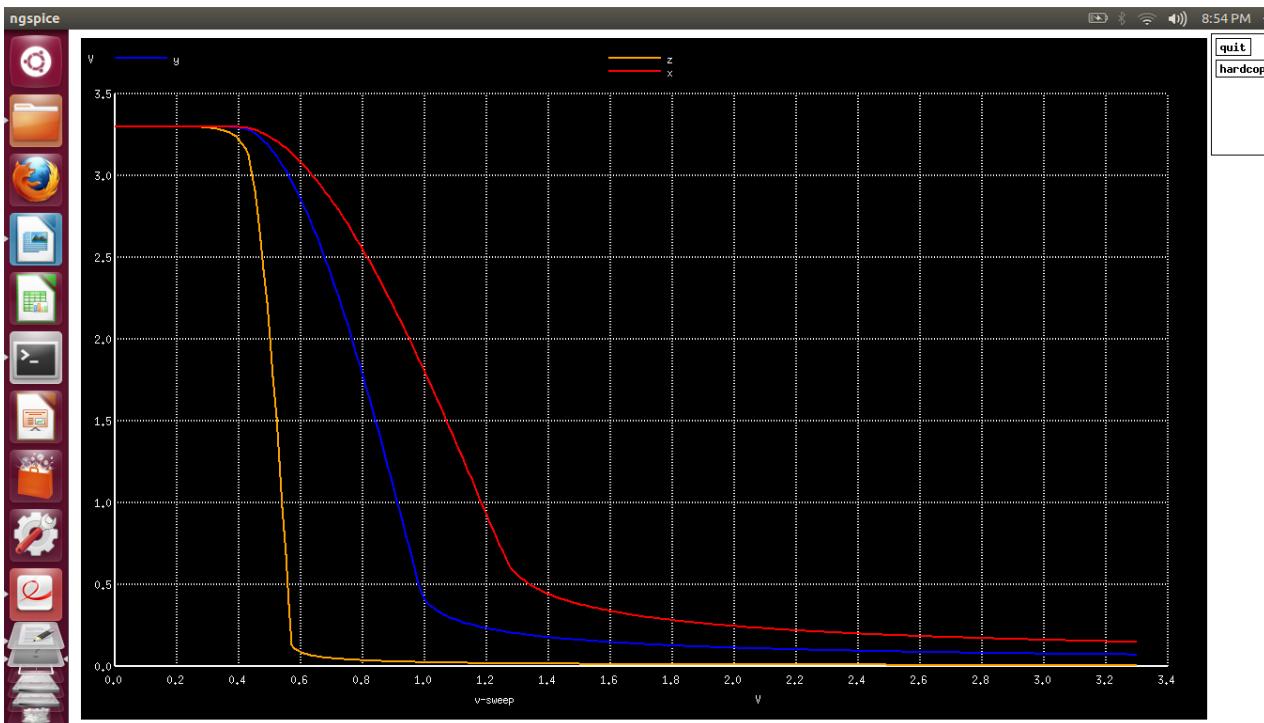


Figure 22: For varying Width

Conclusion: In the above figure for the VI characteristics. With increase in the value of W , the drain current increases as shown.

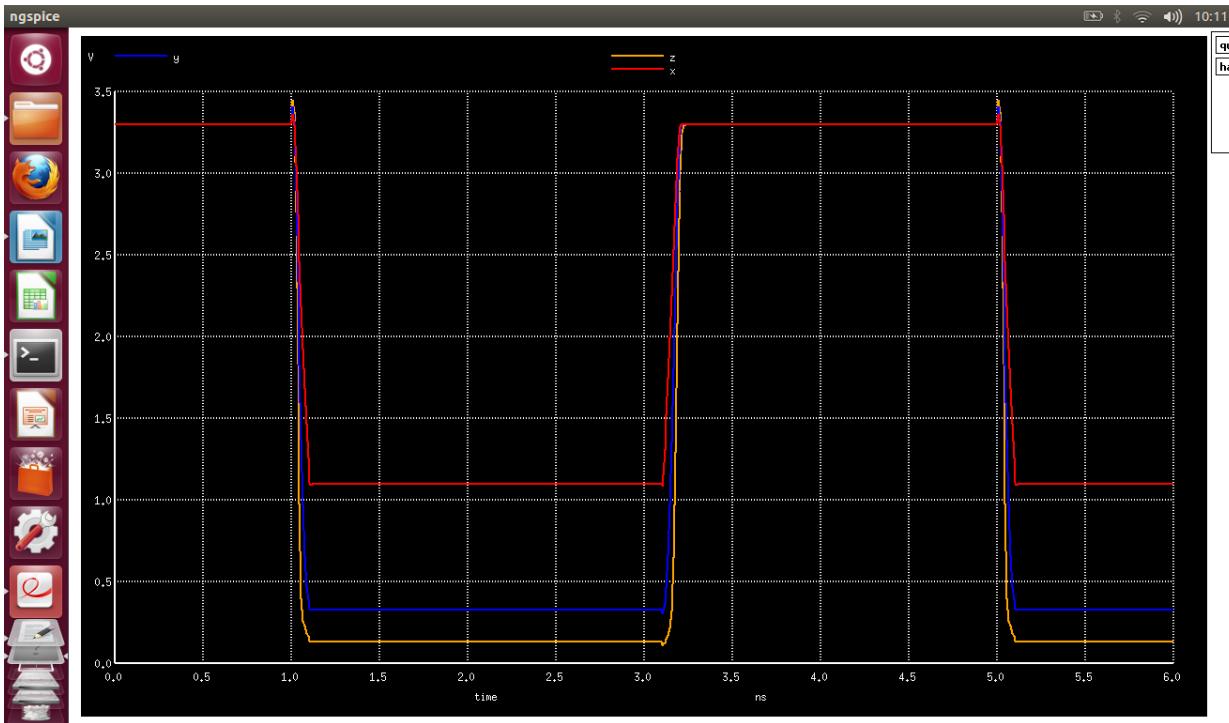


Figure 23: Effect on Tran on varying W/L Ratio

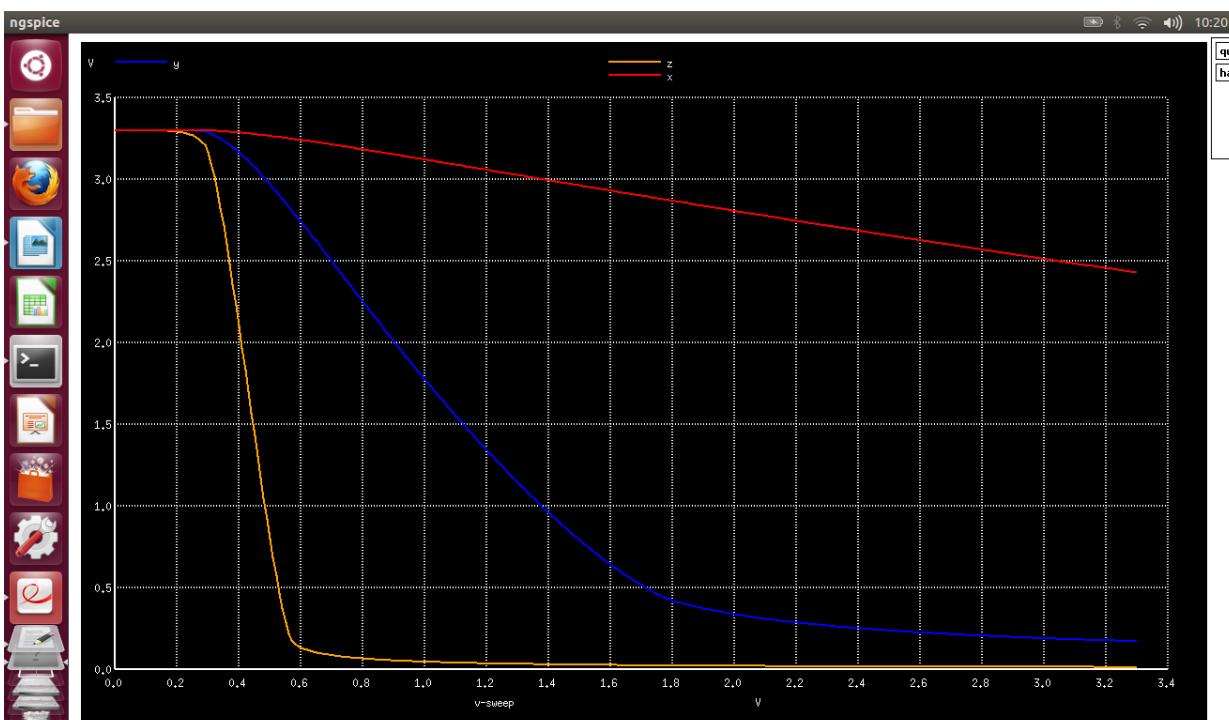


Figure 24: Effect on Transfer Characteristics due to varying Resistance

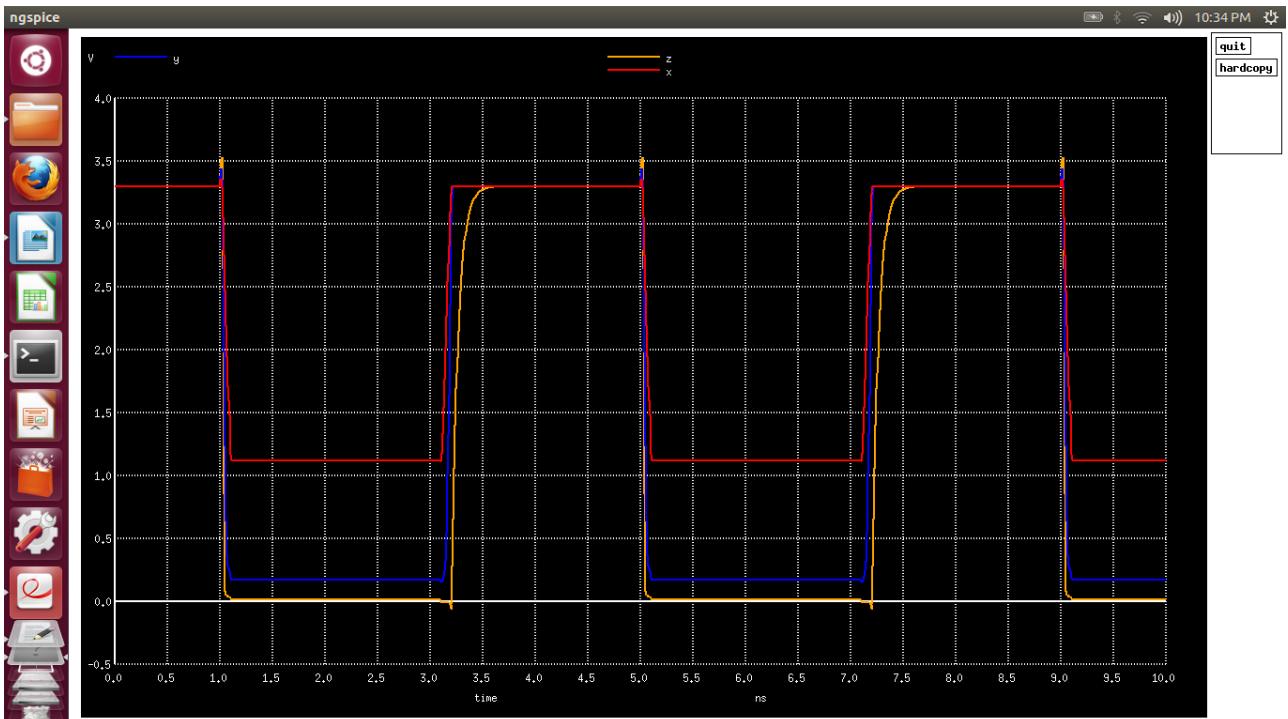


Figure 25: Effect on Transfer Characteristics due to varying Resistance

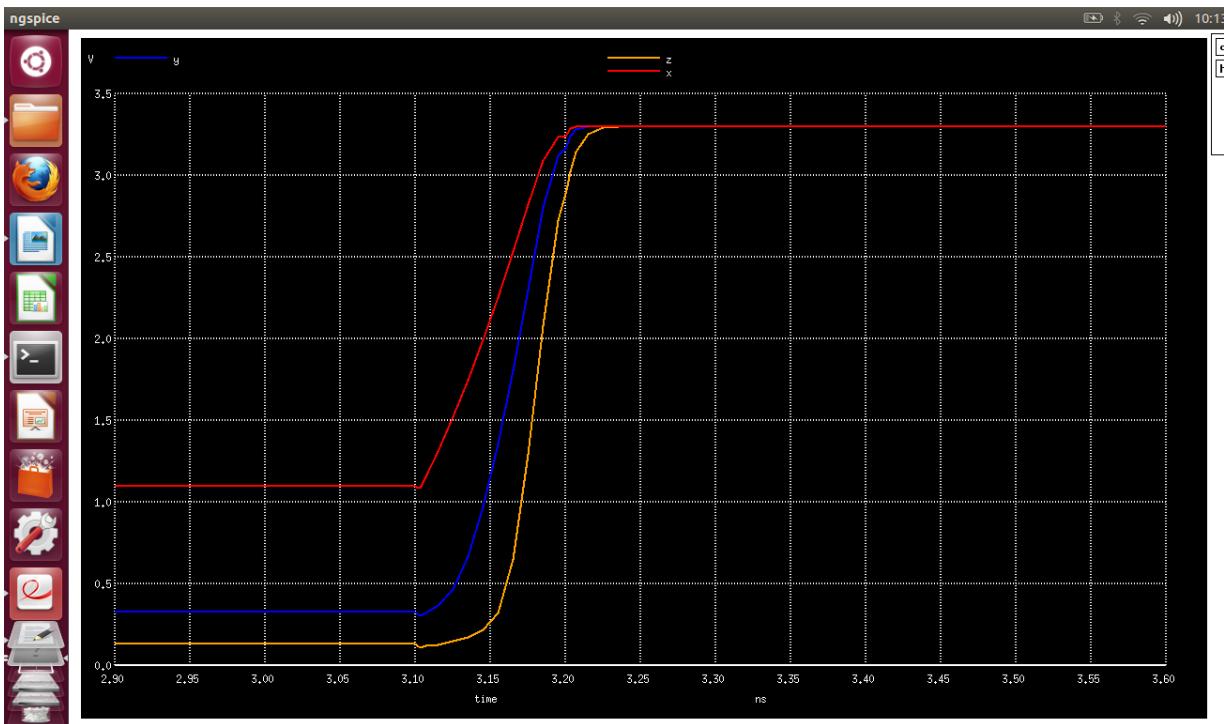


Figure 26: Effect on Rise Time due to W/L Ratio

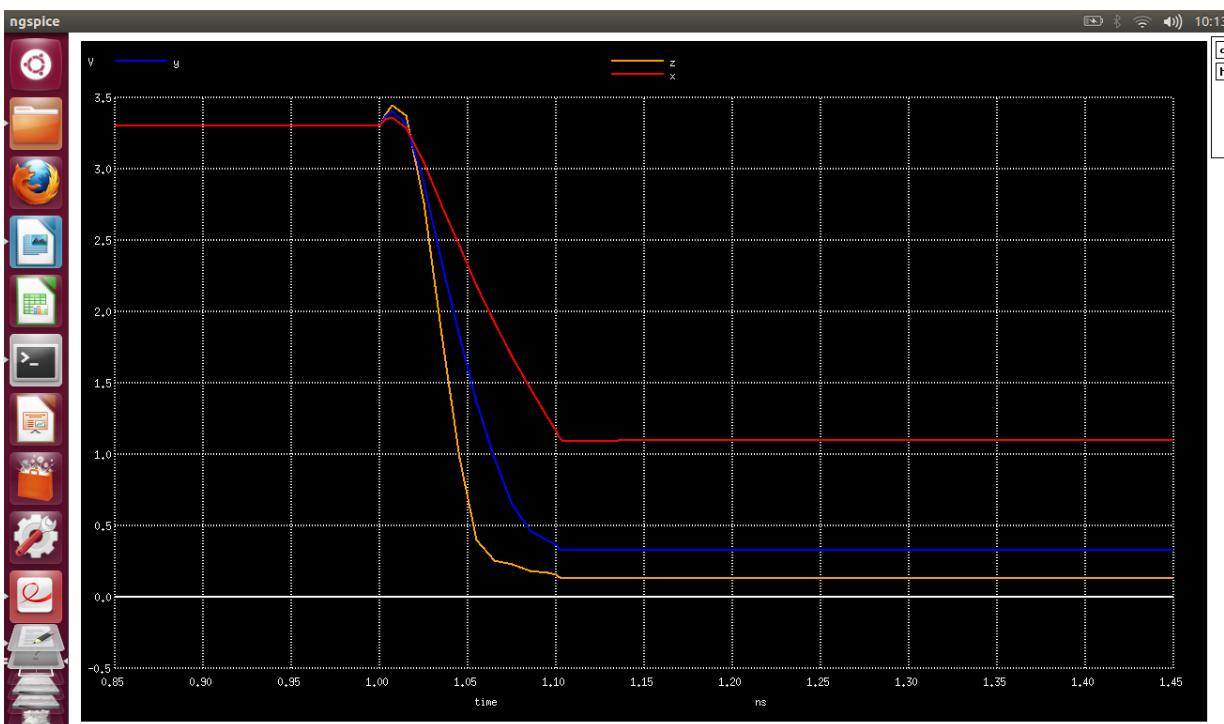


Figure 27: effect on Fall Time due to W/L Ratio

Power Variation

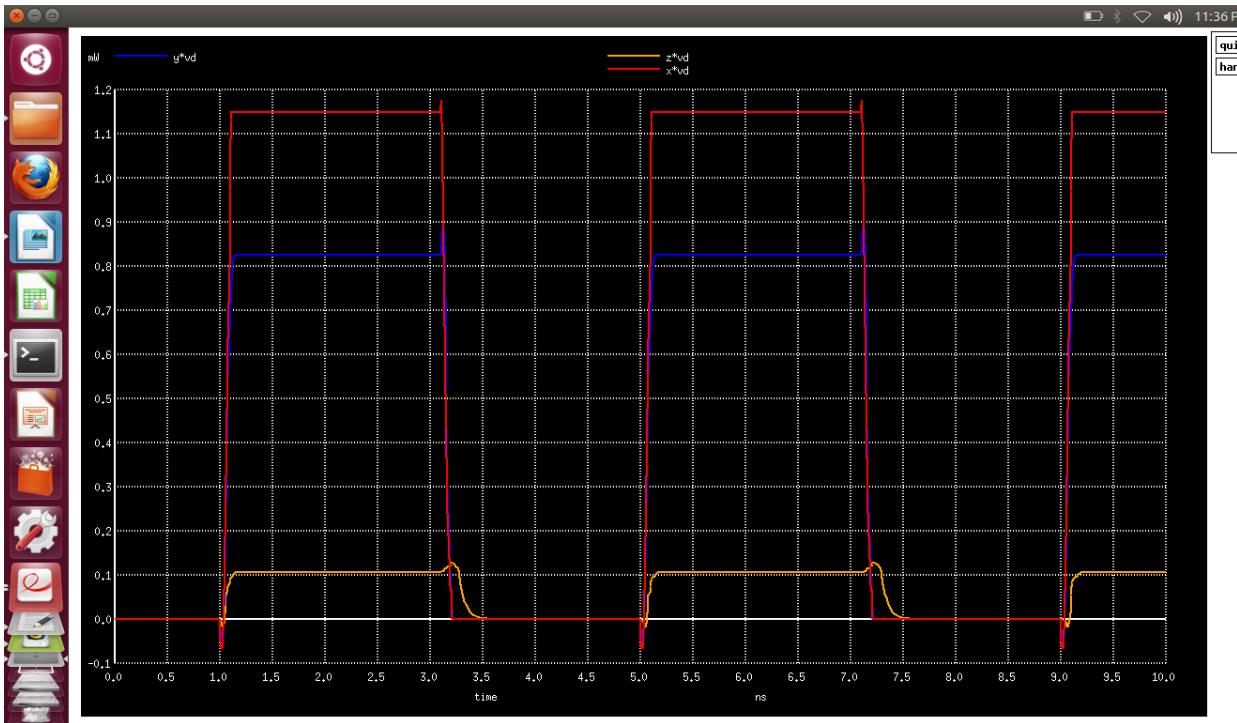


Figure 28: Effect on Power due to varying Resistance

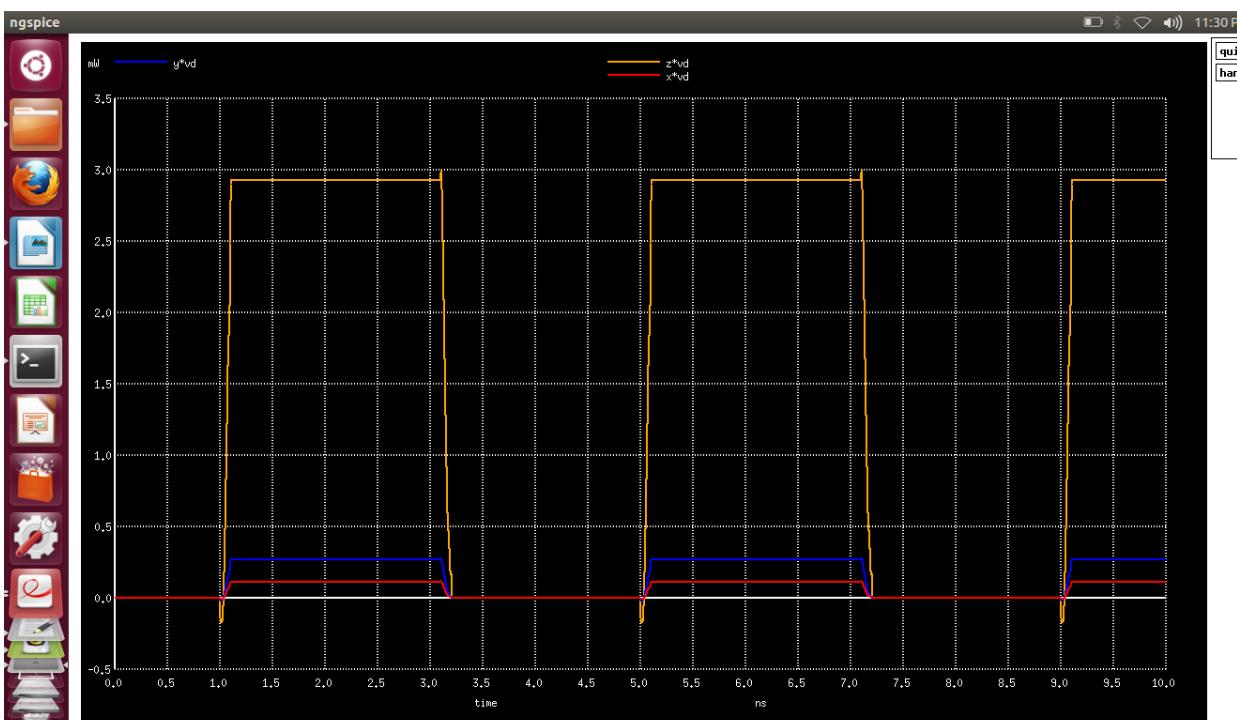


Figure 29: Effect on Power due to W/L Ratio

Rise Time Fall Time due to Capacitance

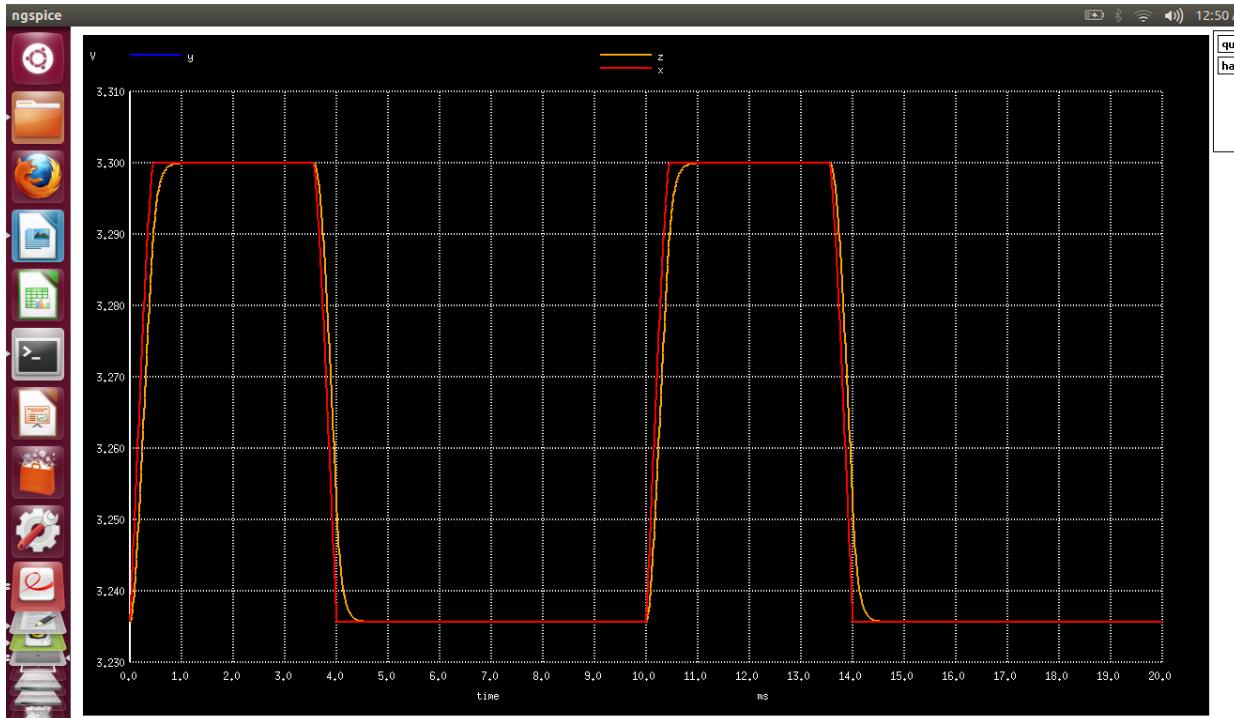


Figure 30: Effect on Rise Time and Fall Time due to Varying Capacitance

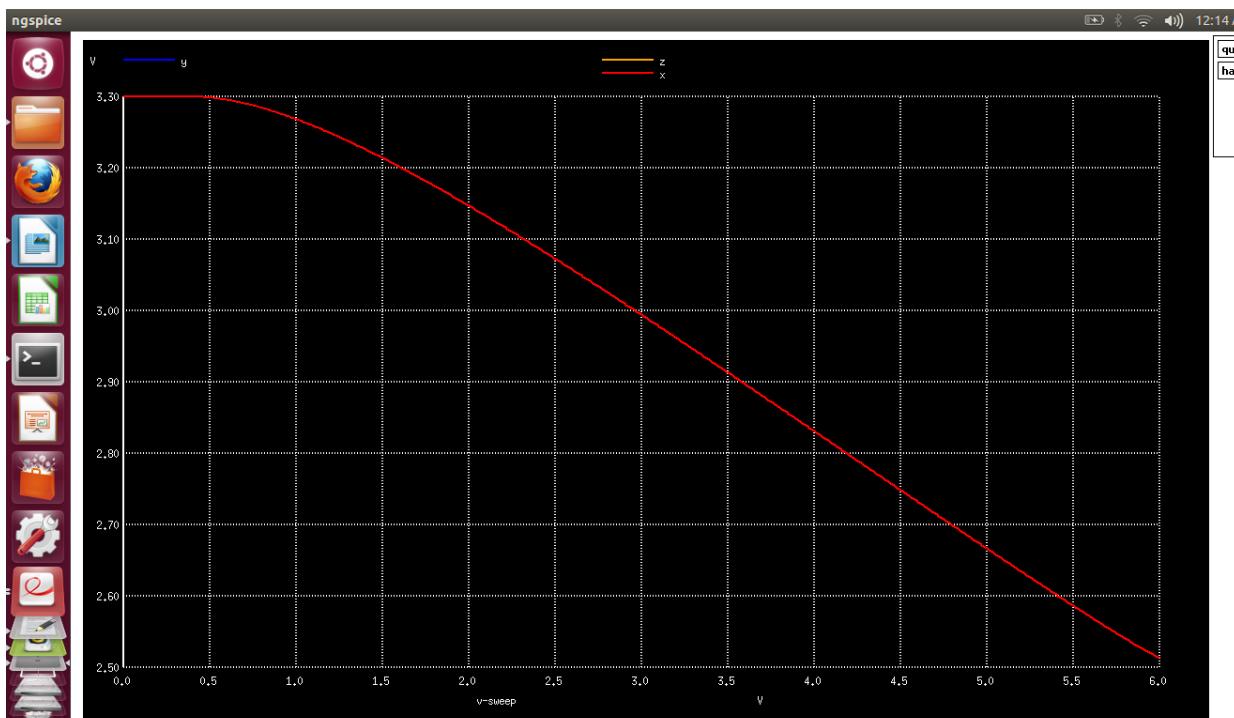


Figure 31: DC Transfer Characteristics due to varying Capacitance

Conclusion:
As Load Resistance increases

- VTC shifts towards left
- The gain of the transition region in the VTC increases
- VOL decreases as R becomes larger than Resistance offered by nmos.
- Rise time and fall time of transient response decreases.
- Power consumption decreases.

As W/L ratio increases:

- VTC shifts towards left
- NML decreases and NMH increases
- TPLH increases and TPHL decreases
- the gain of the transition region in the VTC increases
- VOL decreases as Resistance offered by nmos decreases.
- Rise time and fall time of transient response decreases.
- Static and Dynamic Power consumption increases as resistance decreases.

Lab 3: Study of MOS inverter with active load NMOS and PMOS (pseudo NMOS load)

Objective: For a MOS inverter with active load NMOS and PMOS (pseudo NMOS load), Study the transfer function, noise margin, effect on rise time, fall time, propagation delay, power and energy consumed by a NMOS inverter with NMOS, PMOS load for various L,W of the pull-up and pulldown transistors and to determine the power and energy consumed with non-ideal step input.

Circuit Diagram

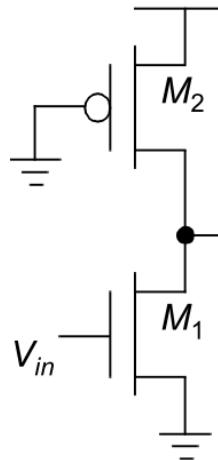


Figure 32: Pseudo Nmos

Pseudo Nmos load inverter DC transfer characteristics

```
.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level3.txt

m0 vd out 0 5 CMOSP l=2u w=1u
m1 out in 0 0 CMOSN l=2u w=1u

*sources
vdd vd 0 dc 5
vin in 0 dc 5

.dc vin 0 5 .001

*for transfer char pic
.control
run
plot out
end
.endc
```

Conclusion: VOH can never be equal to VDD as NMOS can pull up to only VDD-VT.

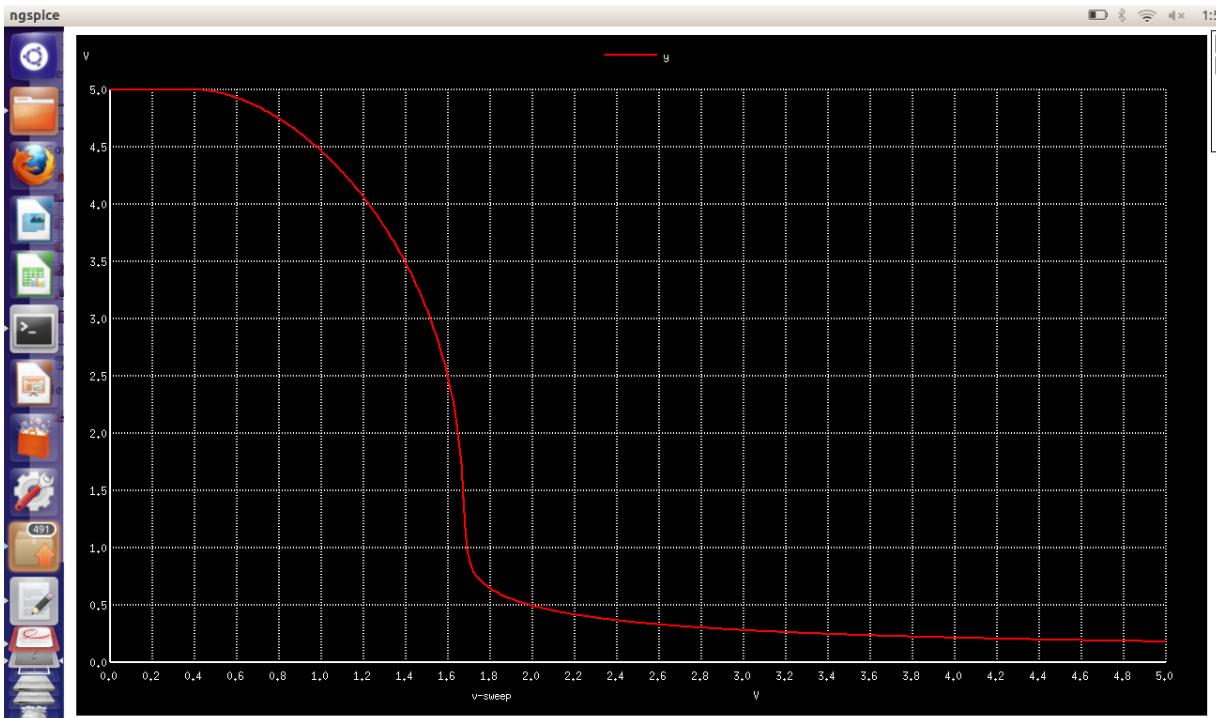


Figure 33: Transfer Characteristics

As W/L of NMOS LOAD decreases

Transient Response

```
.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level3.txt

m0 out 0 vd 5 CMOSP l=1u w=1u
m1 out in 0 0 CMOSN l=1u w=1u

*sources
vdd vd 0 dc 5
vin in 0 dc 5 pulse(5 0 1u 10u 10u 2m 4m)

*for transfer fun pic
.control
tran .01m 10m
run
plot out,in
end
.endc
```

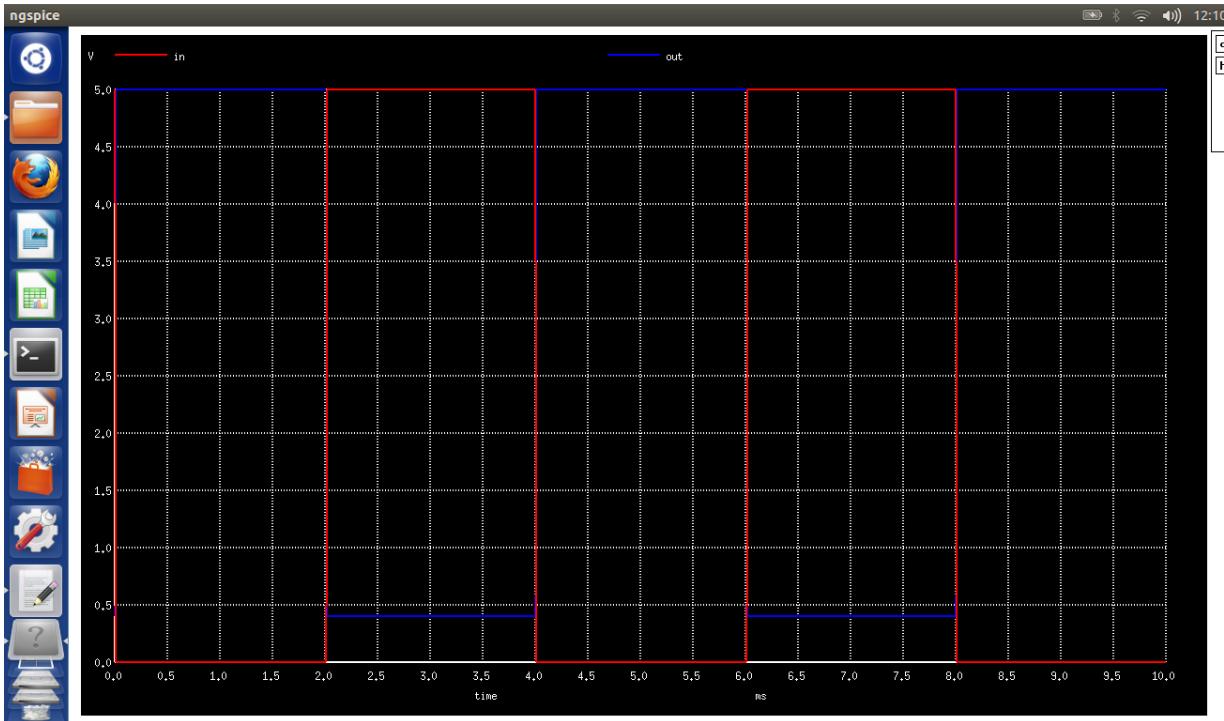


Figure 34: Transient Response

Transfer characteristics due to varying width of driver

```
.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level3.txt

m0 vd 0 out 5 CMOSP l=1u w=1u *LOAD
m1 out in 0 0 CMOSN l=1u w=1u *Driver

*sources
vdd vd 0 dc 5
vin in 0 dc 5

.dc vin 0 5 .01

*varing W/L ratio
.control
foreach wid 1u 2u 4u
alter m1 w = $wid
run
end
.endc

*plotting the output for various w of load
.control
foreach iter 1 2 3
setplot dc$iter
```

```

end
.endc

.control
let x= dc1.out
let y= dc2.out
let z= dc3.out
plot x,y,z
end
.endc

```

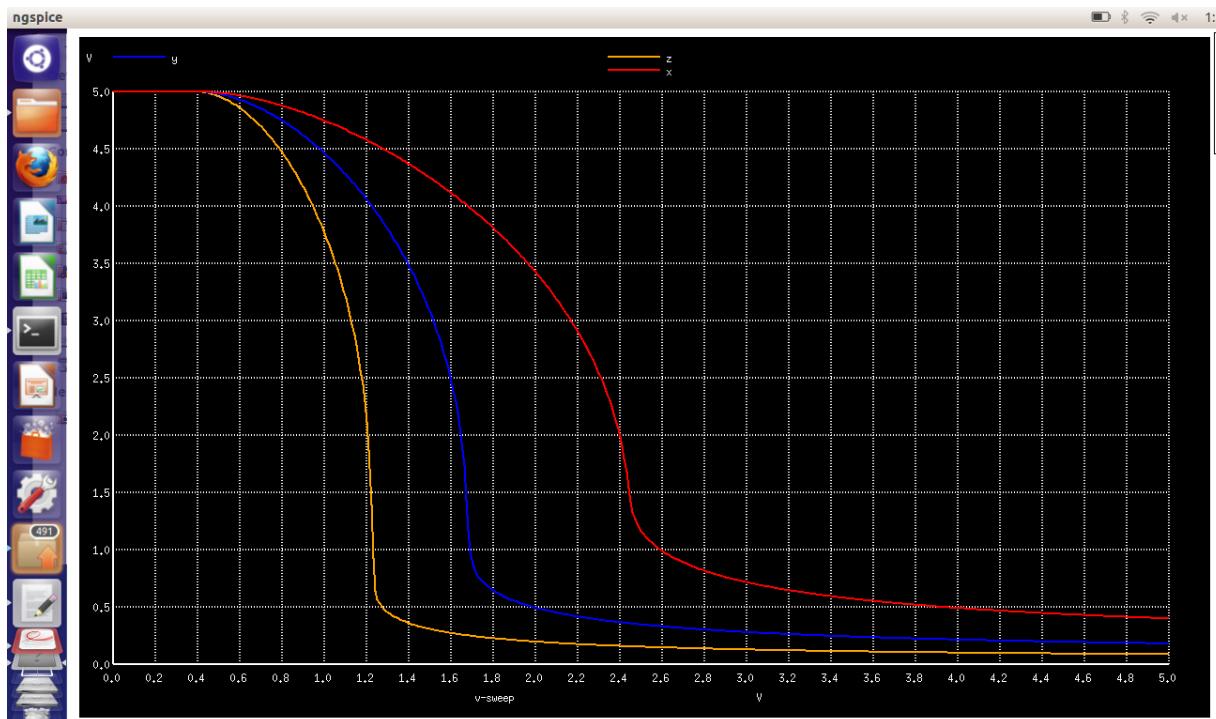


Figure 35: Transfer Characteristics due to varying of W of the Driver

Transient Response due to varying width of driver

```

.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level3.txt

m0 vd 0 out 5 CMOSP l=2u w=1u *LOAD
m1 out in 0 0 CMOSN l=2u w=1u *Driver

*sources
vdd vd 0 dc 5
vin in 0 dc 5 pulse(0 5 10n 10u 10u 1m 2m)

*.dc vin 0 5 .01

```

```

*vavring W/L ratio
.control
foreach wid .5u .8u 1.5u
alter m1 w = $wid
tran 0.01m 5m
end
.endc

*plotting the output for various w of load
.control
foreach iter 1 2 3
setplot tran$iter
end
.endc

.control
let x= tran1.out
let y= tran2.out
let z= tran3.out
plot x,y,z
end
.endc

```

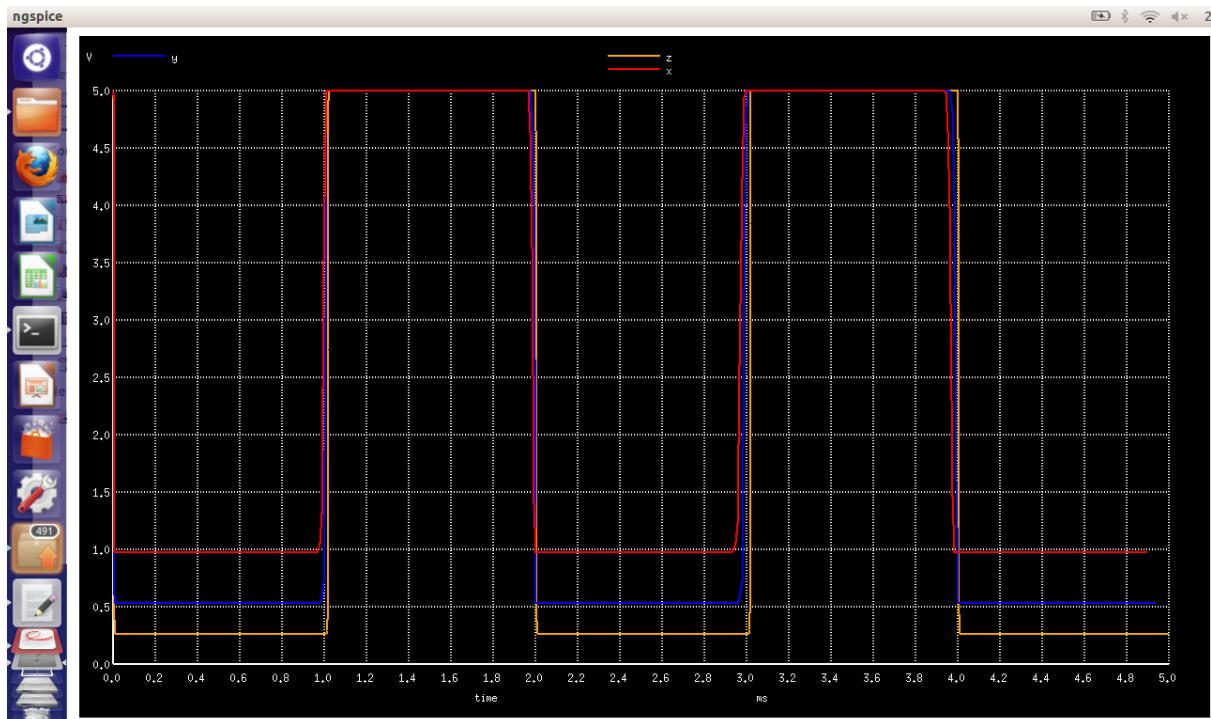


Figure 36: Transient Response after varying W of the Driver

Transfer Function and Transient Response due to varying length of driver

```
.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level3.txt

m0 vd 0 out 5 CMOSP l=2u w=1u
m1 out in 0 0 CMOSN l=2u w=1u

*sources
vdd vd 0 dc 5
vin in 0 dc 5 pulse(0 5 10n 10u 10u 1m 2m)

*varing L of driver
.control
foreach len .5u 2u 4u
alter m1 l = $len
run
tran 0.01m 5m
end
.endc

*plotting the output for various w of load
.control
foreach iter 1 2 3
setplot tran$iter
end
.endc

.control
let x= tran1.out
let y= tran2.out
let z= tran3.out
plot x,y,z
end
.endc
```

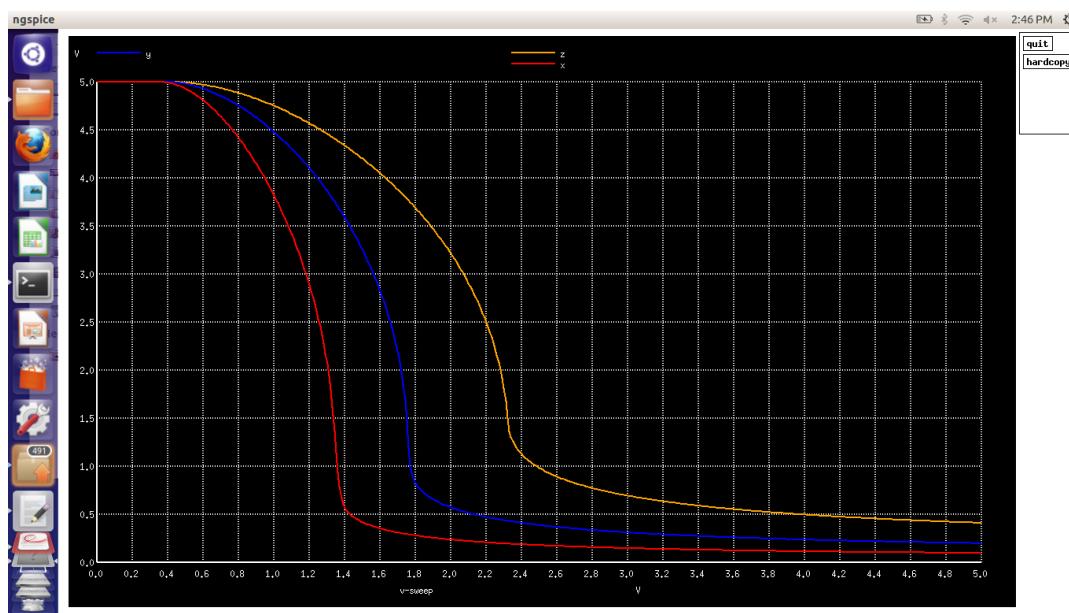


Figure 37: Transfer characteristics due to varying the length of the Driver

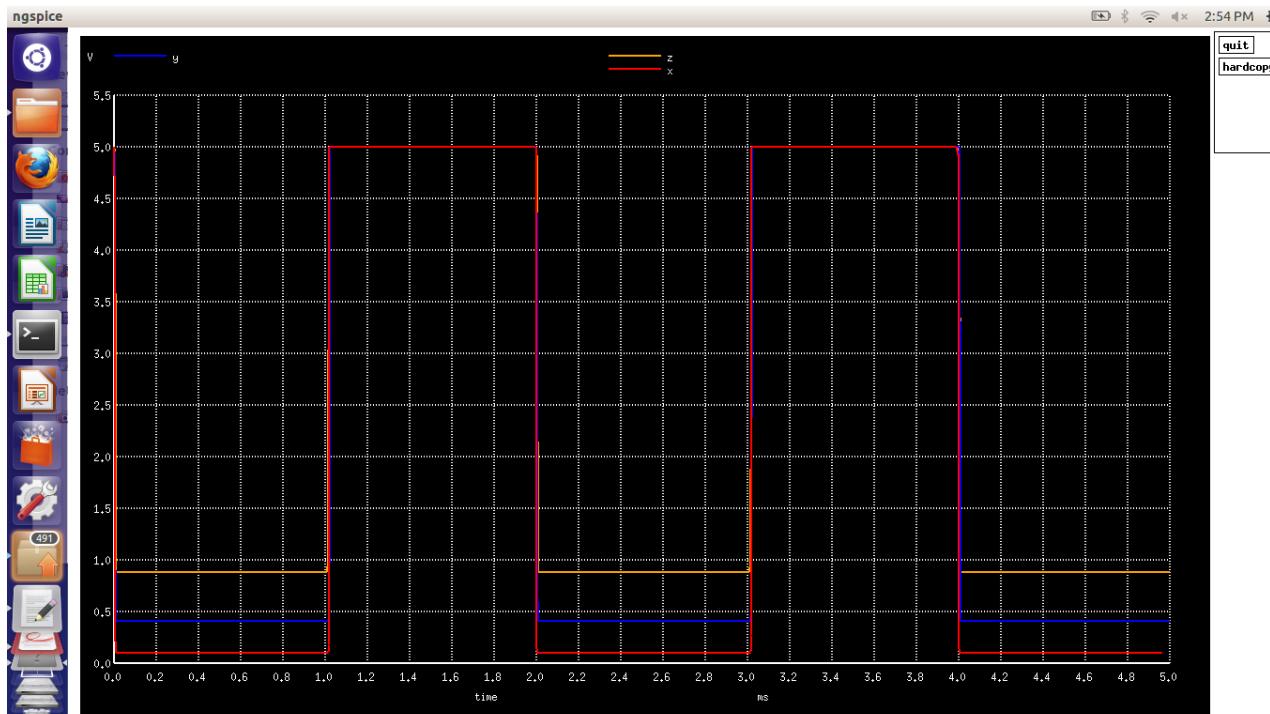


Figure 38: Transient Response due to varying the Length of the driver

Transfer Characteristics due to varying width of load

```
.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level3.txt

m0 vd 0 out 5 CMOSP l=1u w=1u *LOAD
m1 out in 0 0 CMOSN l=1u w=1u *Driver

*sources
vdd vd 0 dc 5
vin in 0 dc 5 pulse

.dc vin 0 5 .01

*varing W of load pmos ratio
.control
foreach wid .125u .25u 2.5u
alter m0 w = $wid
run
end
.endc

*plotting the output for various w of load
.control
foreach iter 1 2 3
setplot dc$iter
end
.endc

.control
let x= dc1.out
let y= dc2.out
let z= dc3.out
plot x,y,z
end
.endc
```

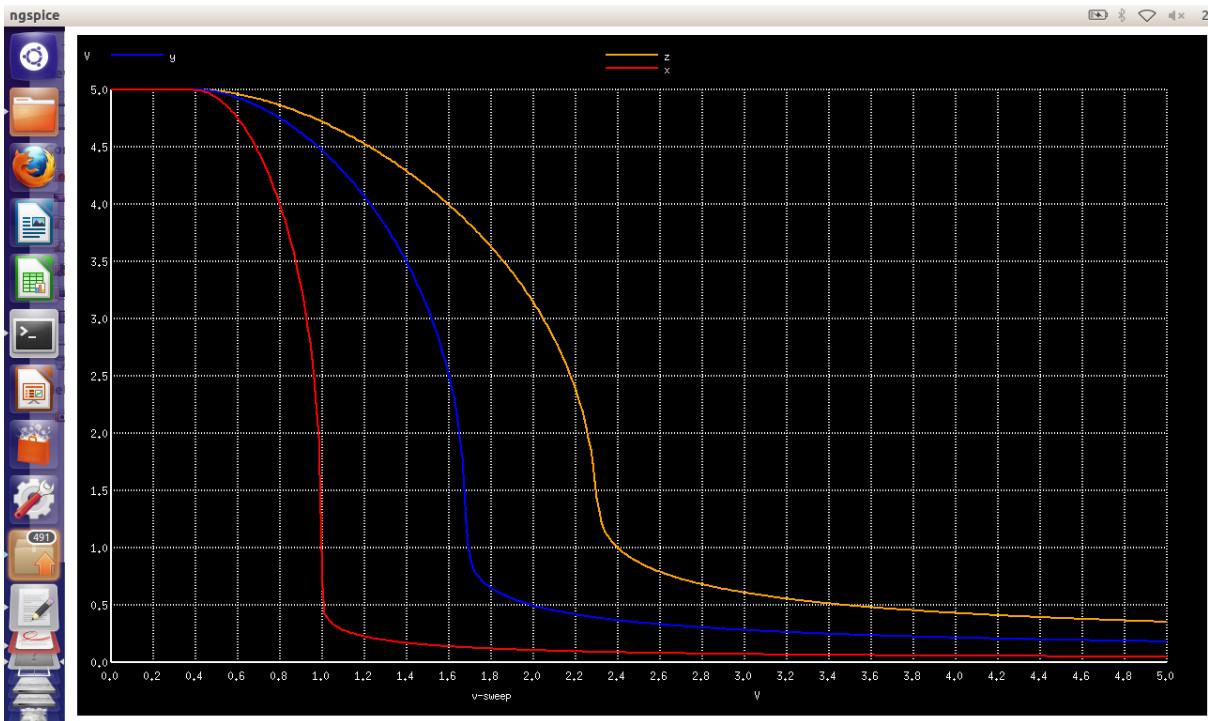


Figure 39: Transfer Function on varying the Width of the Load

Transient Response on varying length of load

```
.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level3.txt

m0 vd 0 out 5 CMOSP l=1u w=1u *LOAD
m1 out in 0 0 CMOSN l=1u w=1u *Driver

*sources
vdd vd 0 dc 5
vin in 0 dc 5 pulse(0 5 0 0 0 .5m 1m)

*varying W/L ratio
.control
foreach len 1u 2u 5u
alter m0 l = $len
run
tran 0.01m 2m
end
.endc

*plotting the output for various L of load
.control
foreach iter 1 2 3
setplot trans$iter
```

```
end
.endc

.control
let x= tran1.out
let y= tran2.out
let z= tran3.out
plot x,y,z
end
.endc
```

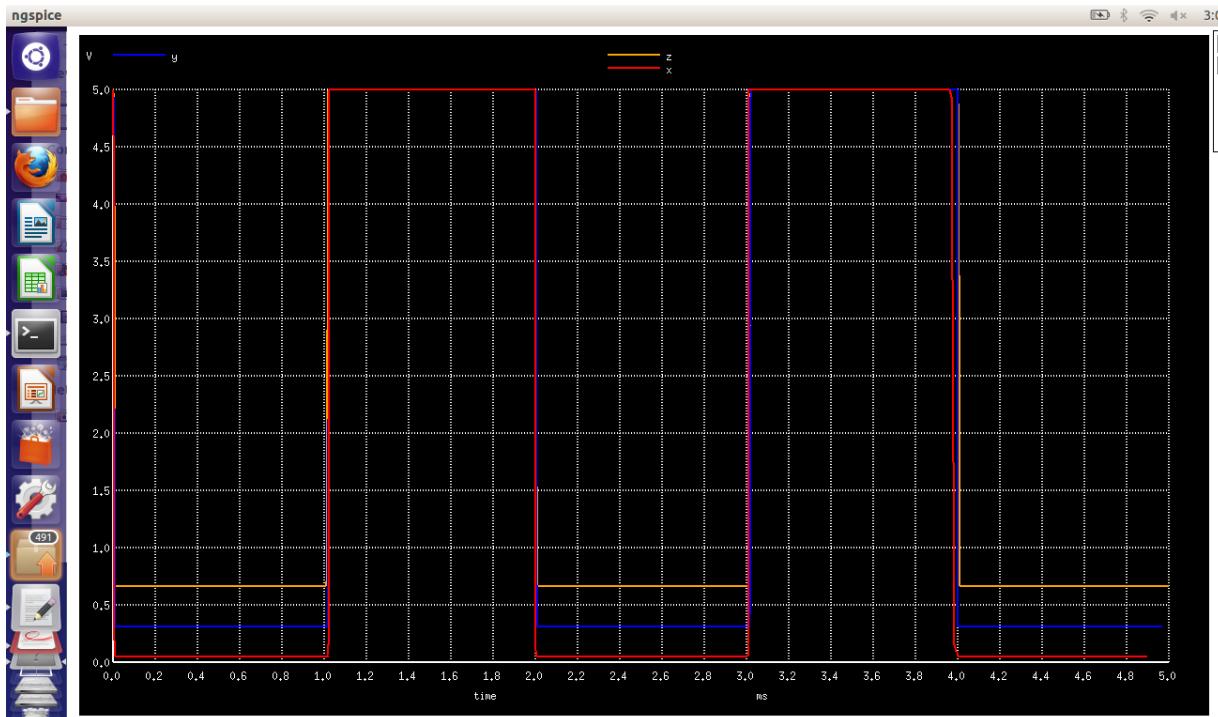


Figure 40: Transient Response due to varying the Length of the Load

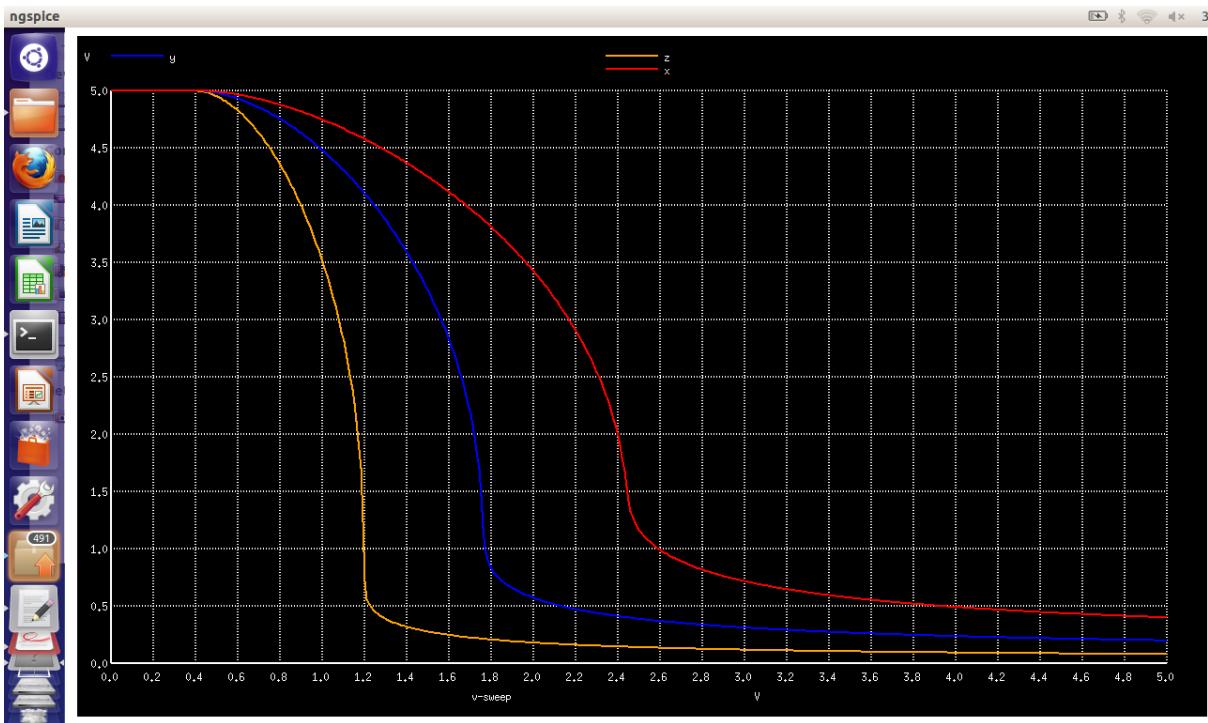


Figure 41: Transfer Characteristics due to varying the Length of the load

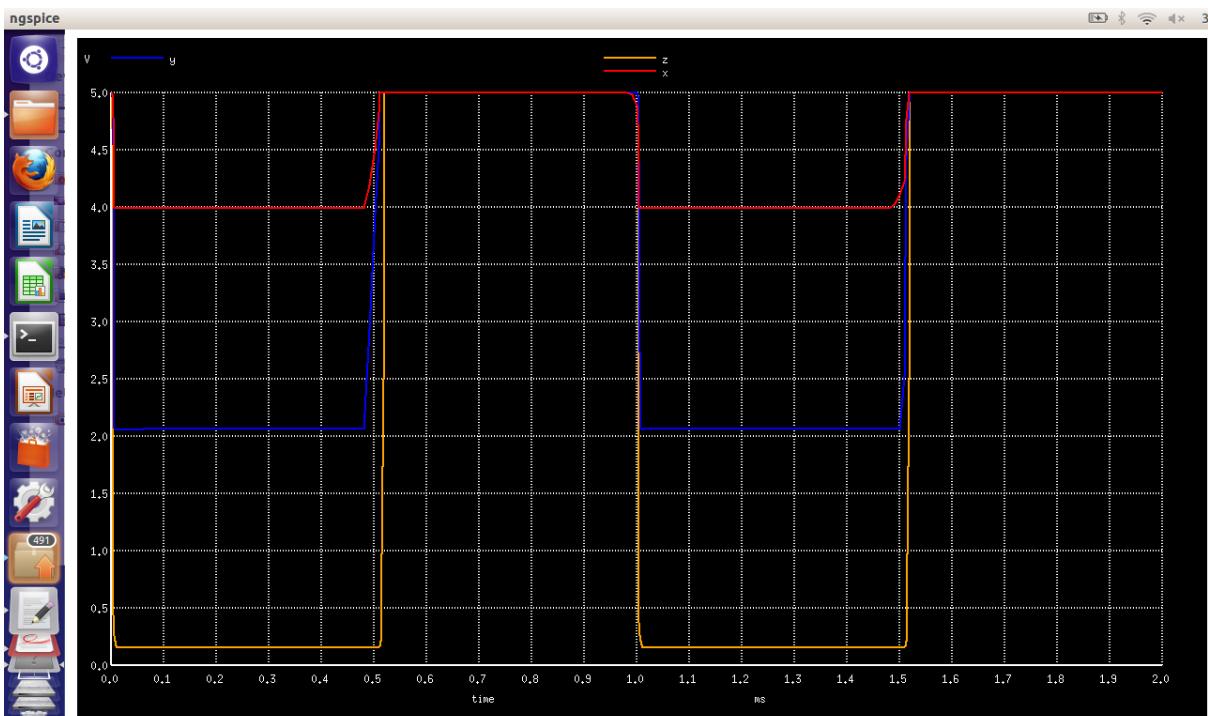


Figure 42: Transient Response due to varying the length of the load

Conclusion:

As W/L of NMOS increases

- VTC shifts towards left
- The gain of the transition region in the VTC increases.
- NML decreases and NMH increases
- TPLH increases and TPHL decreases
- VOL decreases as R becomes smaller than Resistance offered by pmos.
- Power Dissipation Increases as R is smaller and also energy consumed per transition increases.
- Rise/Fall time reduces.

As W/L of PMOS LOAD decreases

- VTC shifts towards left
- the gain of the transition region in the VTC increases
- NML decreases and NMH increases
- TPLH increases and TPHL decreases
- VOL decreases as Resistance offered by pmos increases.
- Static and Dynamic Power Dissipation decreases as R is larger and also energy consumed per transition decreases.
- Rise/Fall time reduces.

As Load Capacitance increases, Rise/Fall time of output increases and Energy consumed per transition increases.

Also Static power increases. As input rise time and fall time increases TPHL and TPLH increases

Study of inverter with NMOS load

Objective: For a inverter with NMOS load,study the transfer function, effect on rise time, fall time, propagation delay, power and energy consumed by inverter with variation in L,W of the pull-up and pulldown transistors and to determine the power and energy consumed with non-ideal step input.

Circuit Diagram

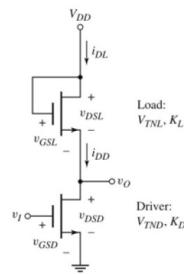


Figure 43: Nmos Inverter with enhancement load

Transient Response due to varying length of load

```
.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level3.txt

m0 vd vd out 0 CMOSN l=1u w=.3u
m1 out in 0 0 CMOSN l=1u w=5u
c1 out 0 1p

*sources
vdd vd 0 dc 5
vin in 0 dc 5 pulse(0 5 0 0 0 2u 4u)

*varing W of driver
.control
foreach len 1u 2u 5u
alter m0 l = $len
tran .01u 10u
run
end
.endc

*plotting the output for various length of load
.control
foreach iter 1 2 3
setplot tran$iter
end
.endc
```

```
*ploting graph for transient out
.control
let x= tran1.out
let y= tran2.out
let z= tran3.out
plot x,y,z
end
.endc
```

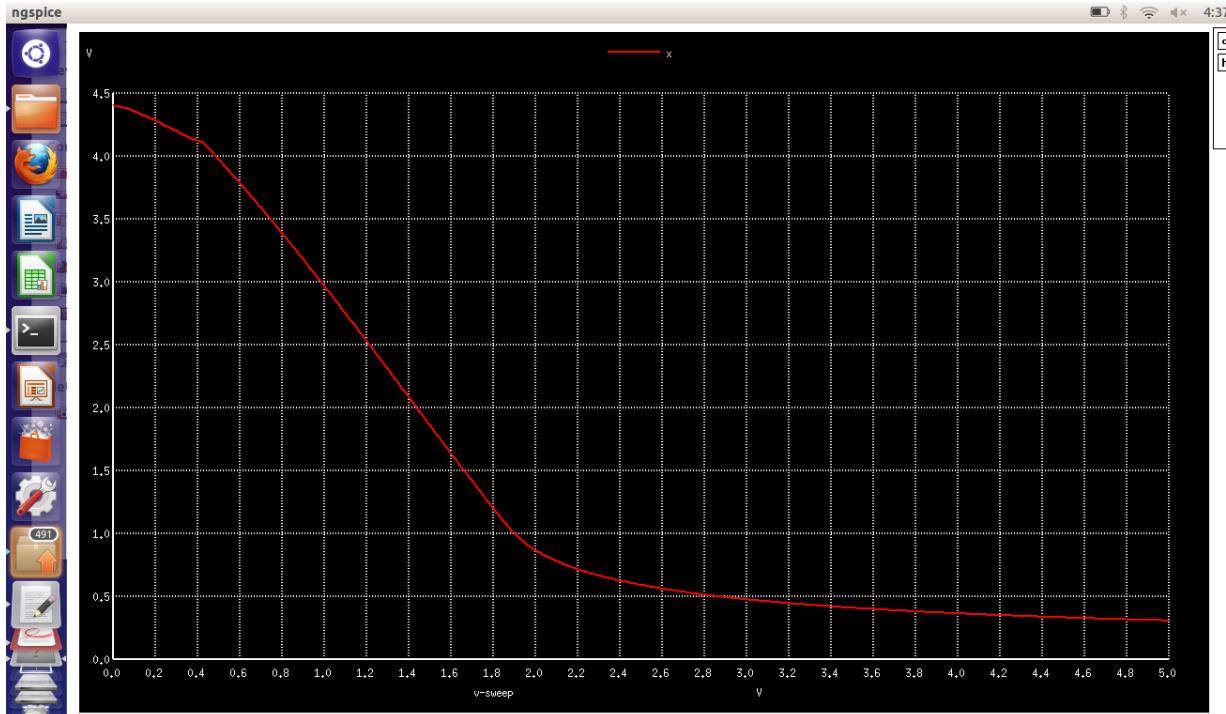


Figure 44: Transfer function of inverter with NMOS load

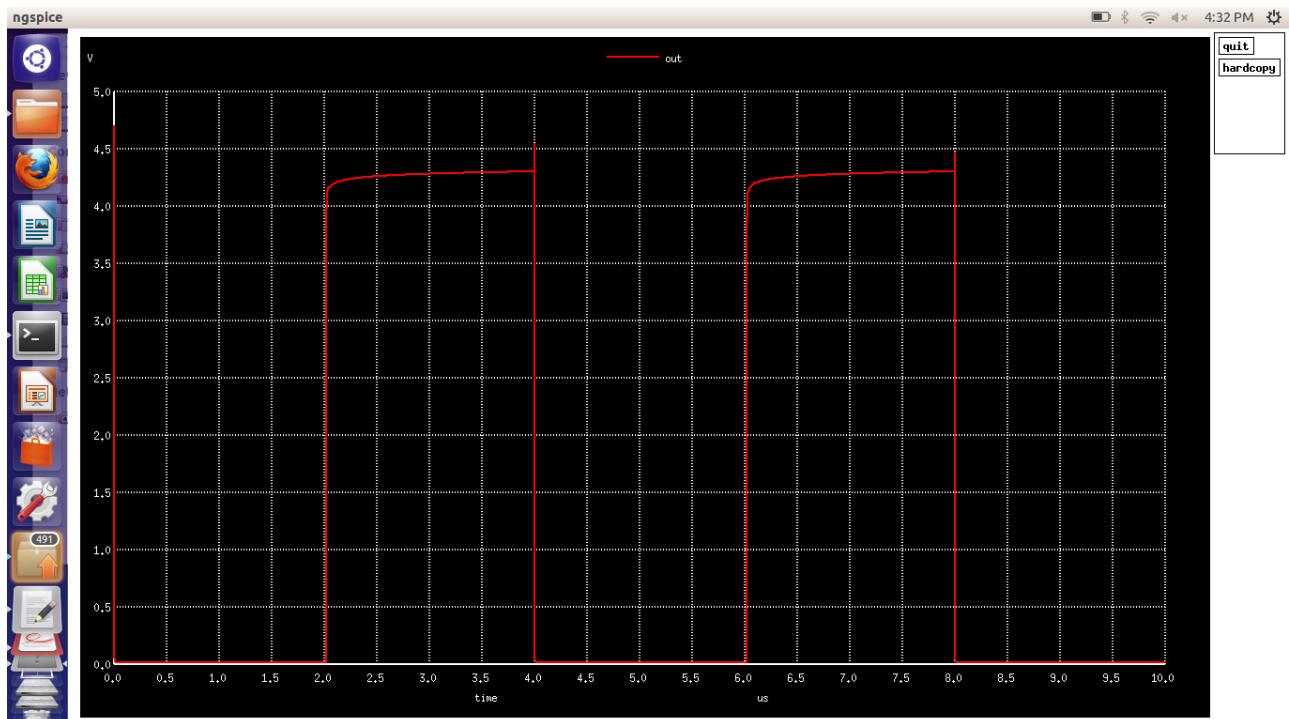


Figure 45: Transient output

Transient Response due to varying width of load

```
* inverter with NMOS load
*transient response only

.include /home/krunal/VLSI_LAB/t14y_tsmc_025_level3.txt

m2 vd vd out 0 cmosn l=1u w=.1u
m1 out in 0 0 cmosn l=1u w=5u

*sources
vdd vd 0 dc 5
vin in 0 dc 5 pulse(0 5 0 0 0 2u 4u)

.control
tran .01u 10u
run
plot out,in
.endc
```

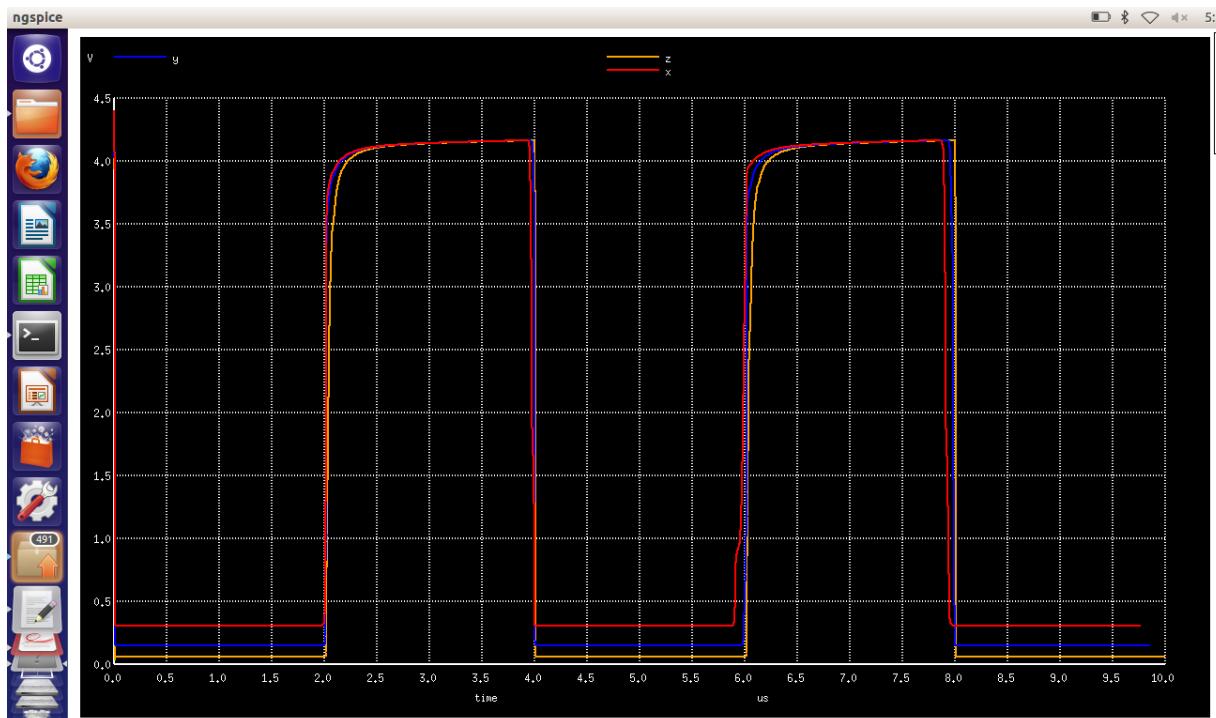


Figure 46: Transient Response due to varying the Width of the Driver

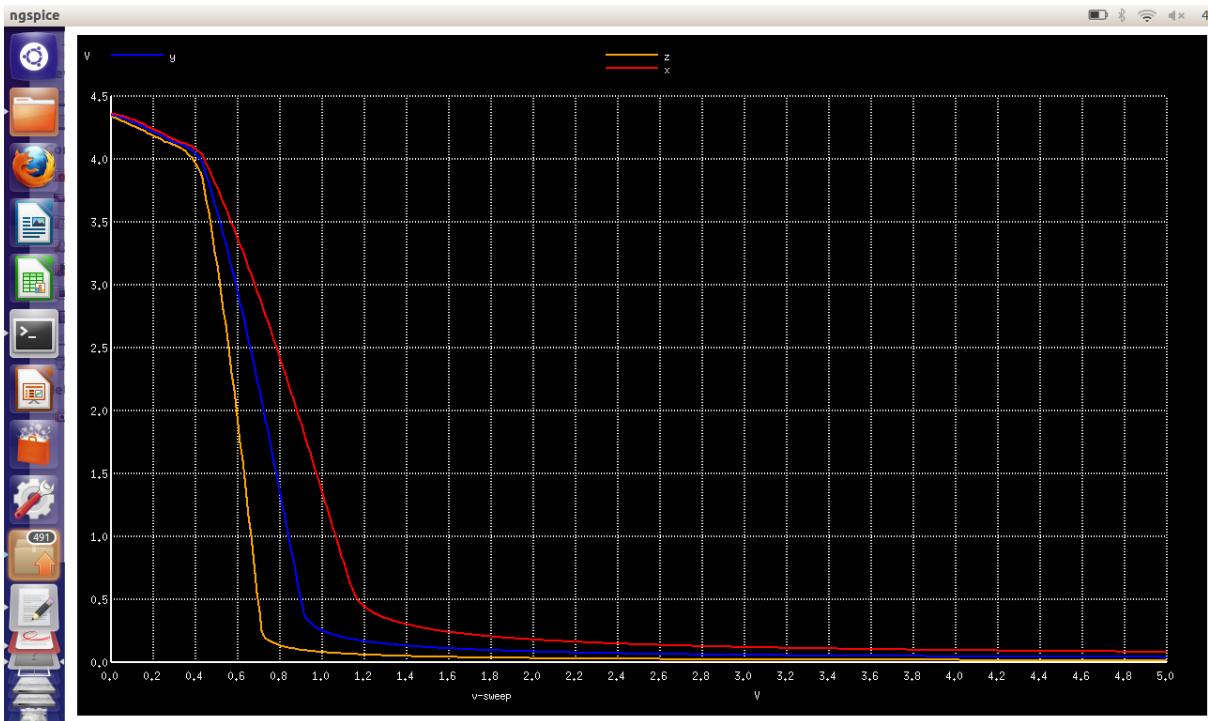


Figure 47: Transfer due to varying the width of driver

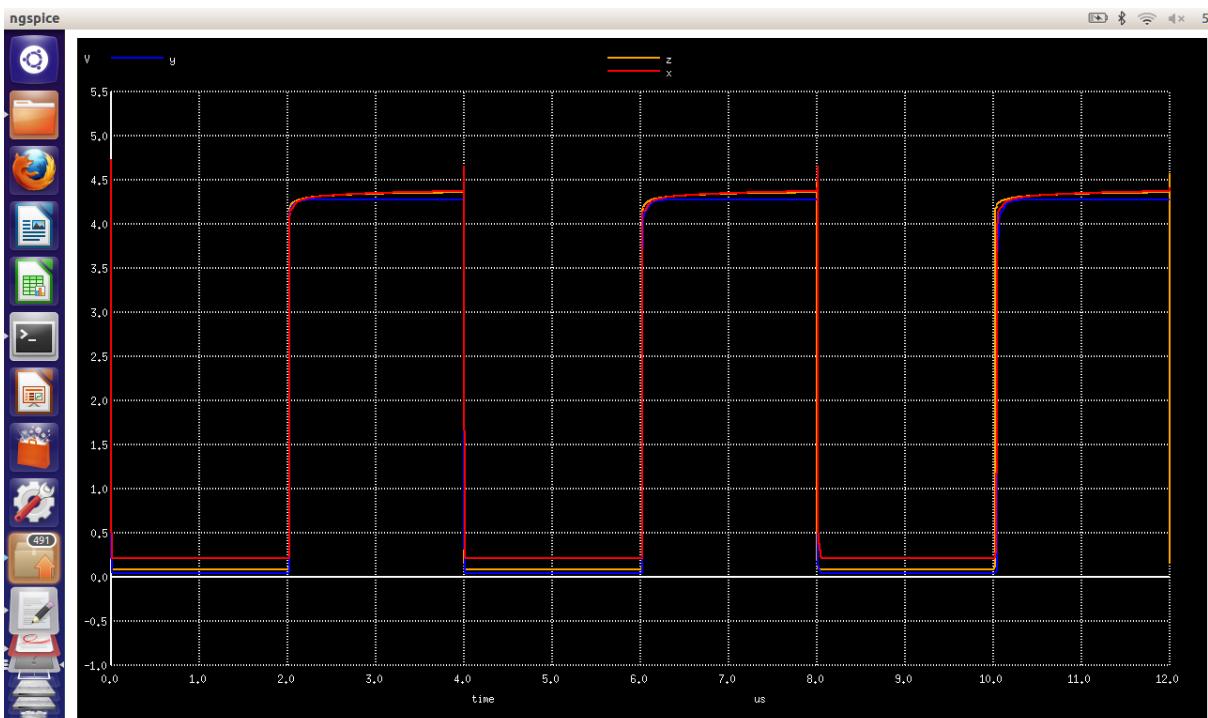


Figure 48: Transient Response due to varying the length of the Driver

Transient Response due to varying length of driver

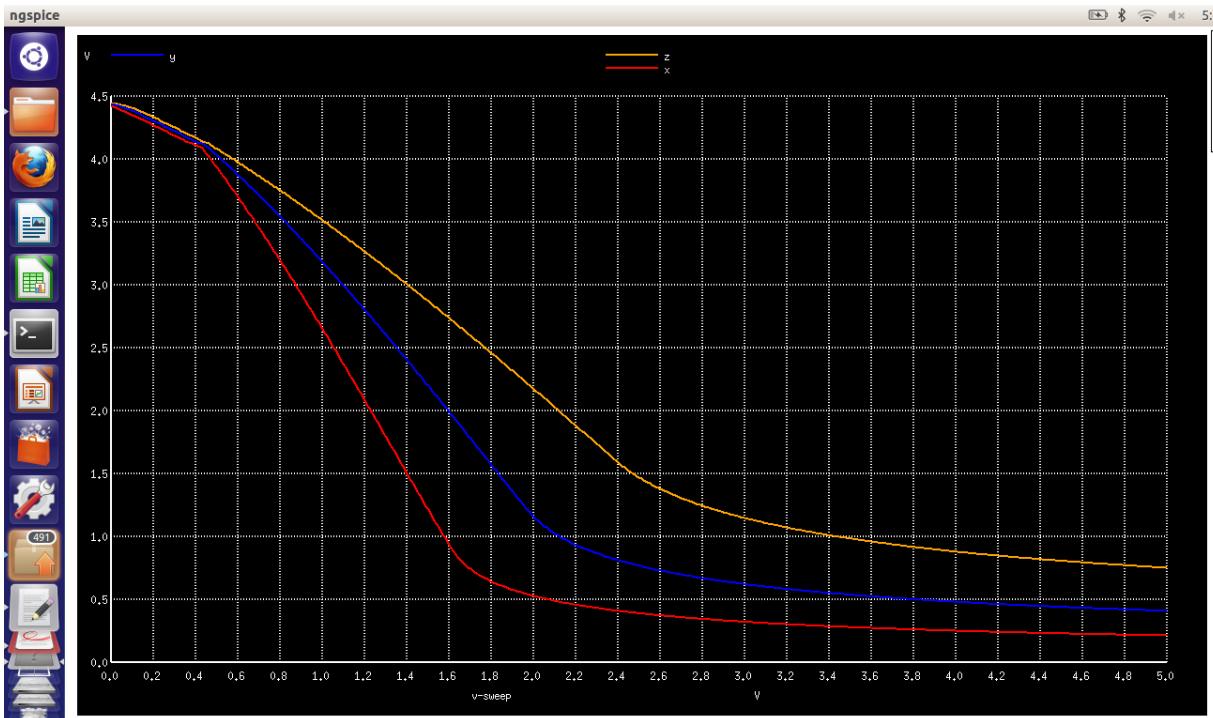


Figure 49: Transfer Characteristics due to varying the length of the driver

```

.include /home/krunal/VLSI_LAB/VINAY/t14y_tsmc_025_level3.txt

m0 vd vd out 0 CMOSN l=1u w=1u *LOAD
m1 out in 0 0 CMOSN l=1u w=5u *Driver

*sources
vdd vd 0 dc 5
vin in 0 dc 5 pulse(0 5 0 0 0 2u 4u)

*.dc vin 0 5 .01

*varying W/L ratio
.control
foreach len 1u .2u .4u
alter m1 l = $len
tran .01u 15u
run
end
.endc

*plotting the output for various length of driver
.control
foreach iter 1 2 3
setplot tran$iter
end

```

```
.endc
```

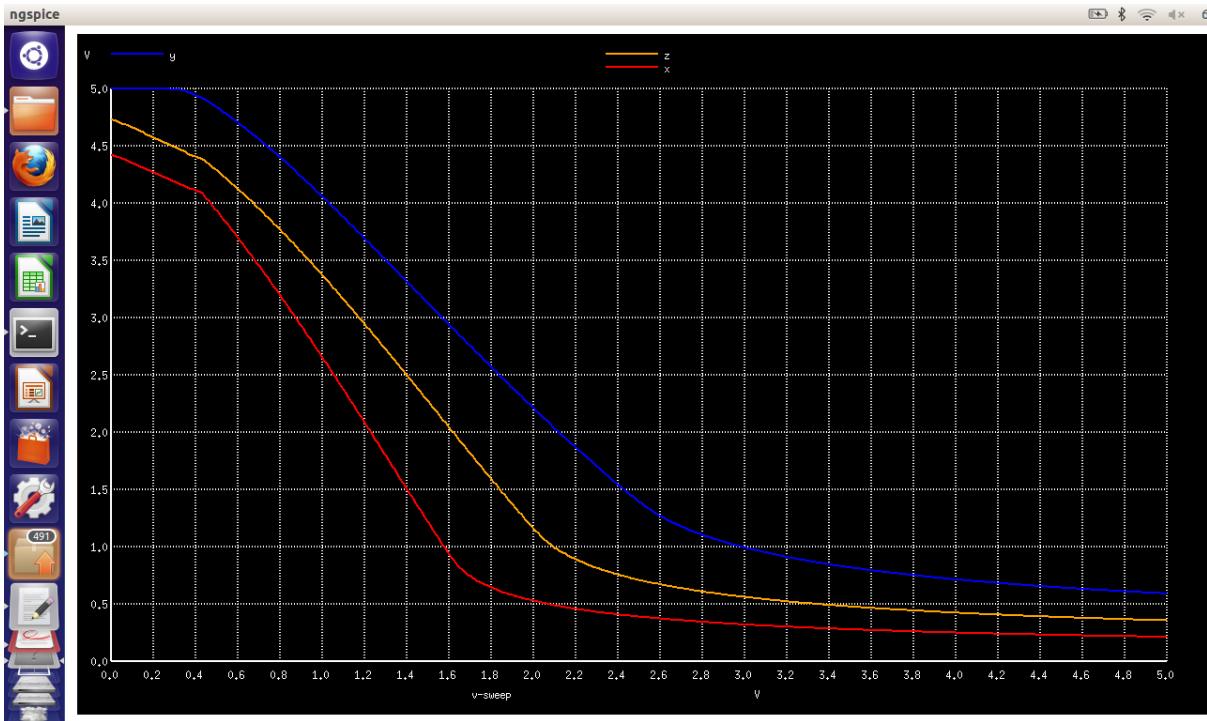


Figure 50: Transfer function due to varying the length of the load - nmos

Static Power due to variation in length

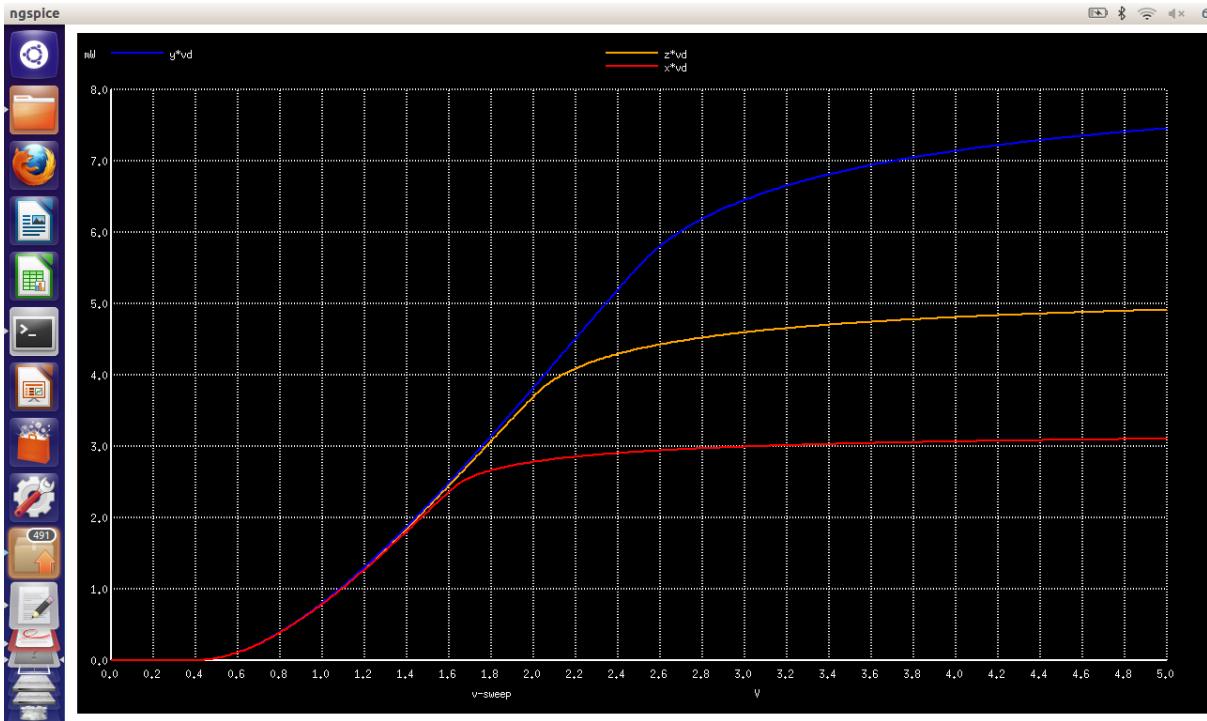


Figure 51: Static Power due to varying the Length of load nmos

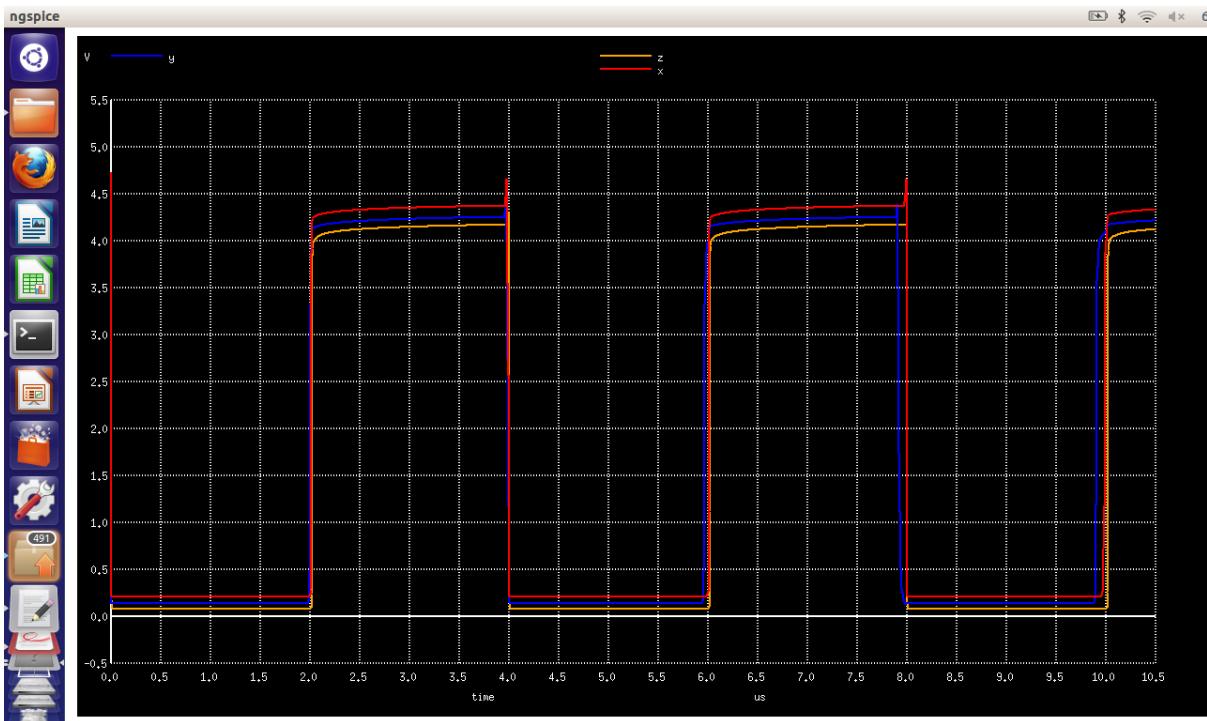


Figure 52: Transient Response due to varying the length of the load

Dynamic Power due to varying the length of load nmos

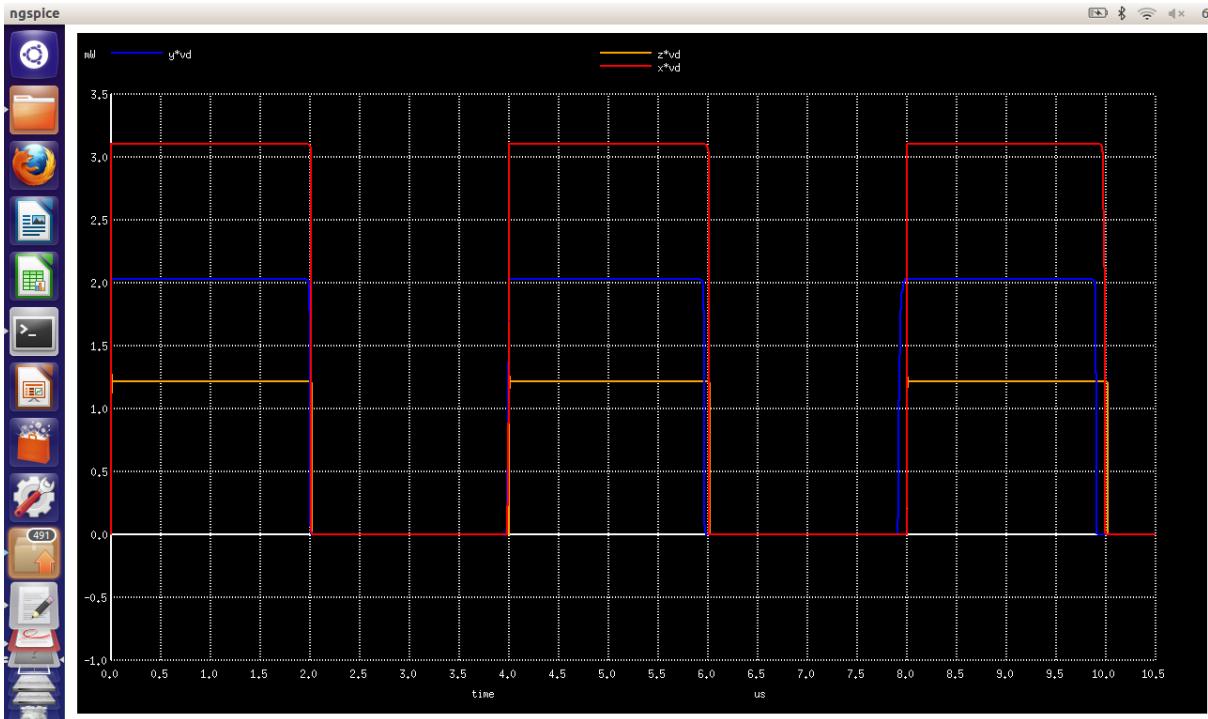


Figure 53: Dynamic Power due to varying the Length of load nmos

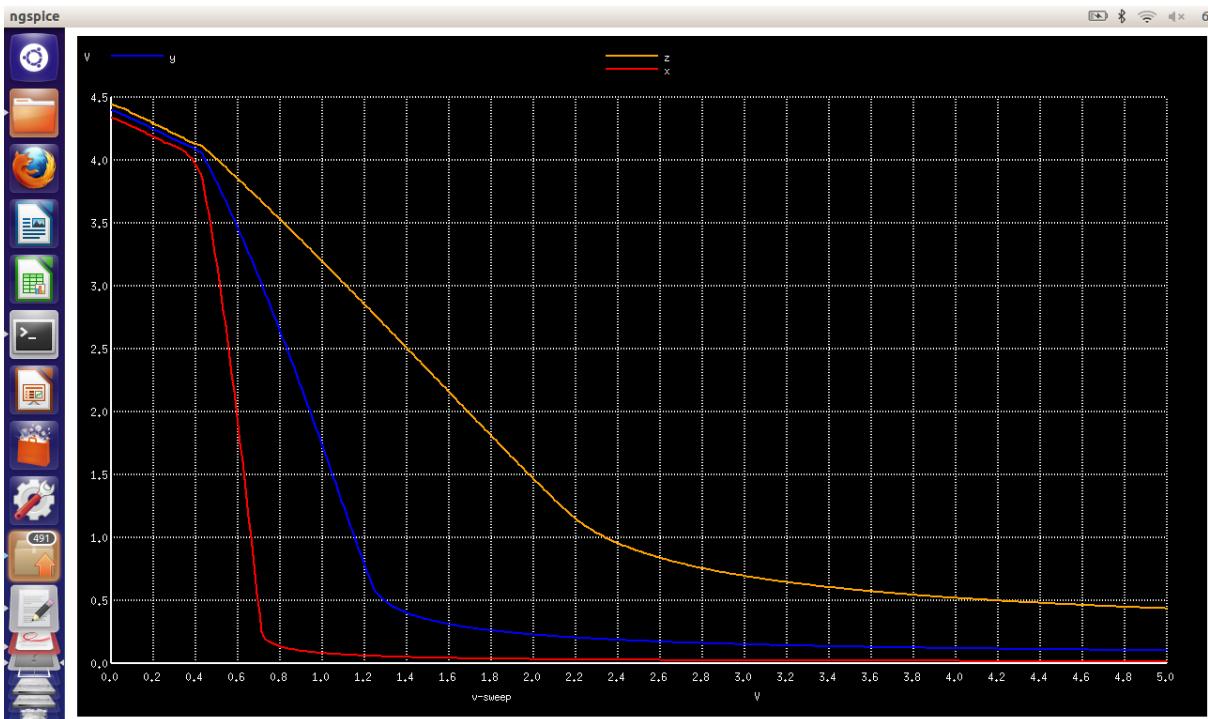


Figure 54: Transient Characteristics due to varying the Width of load- nmos

Static Power due to varying Width of load

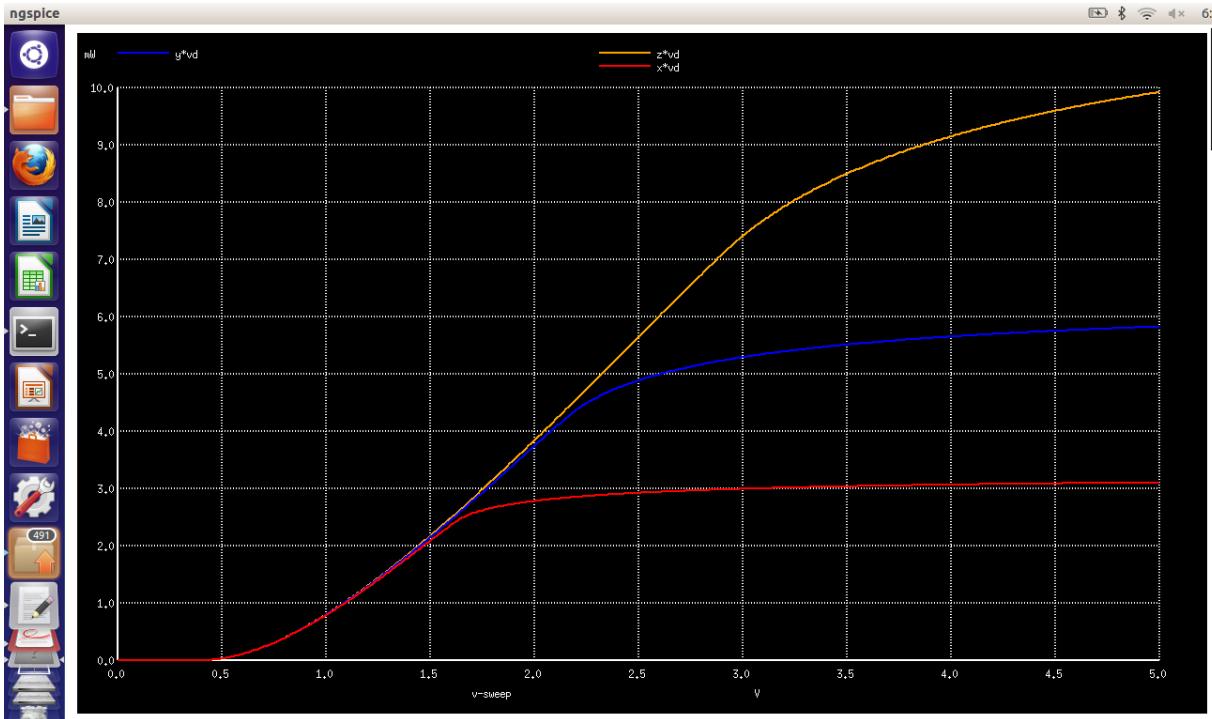


Figure 55: Static Power due to varying W of the load nmos

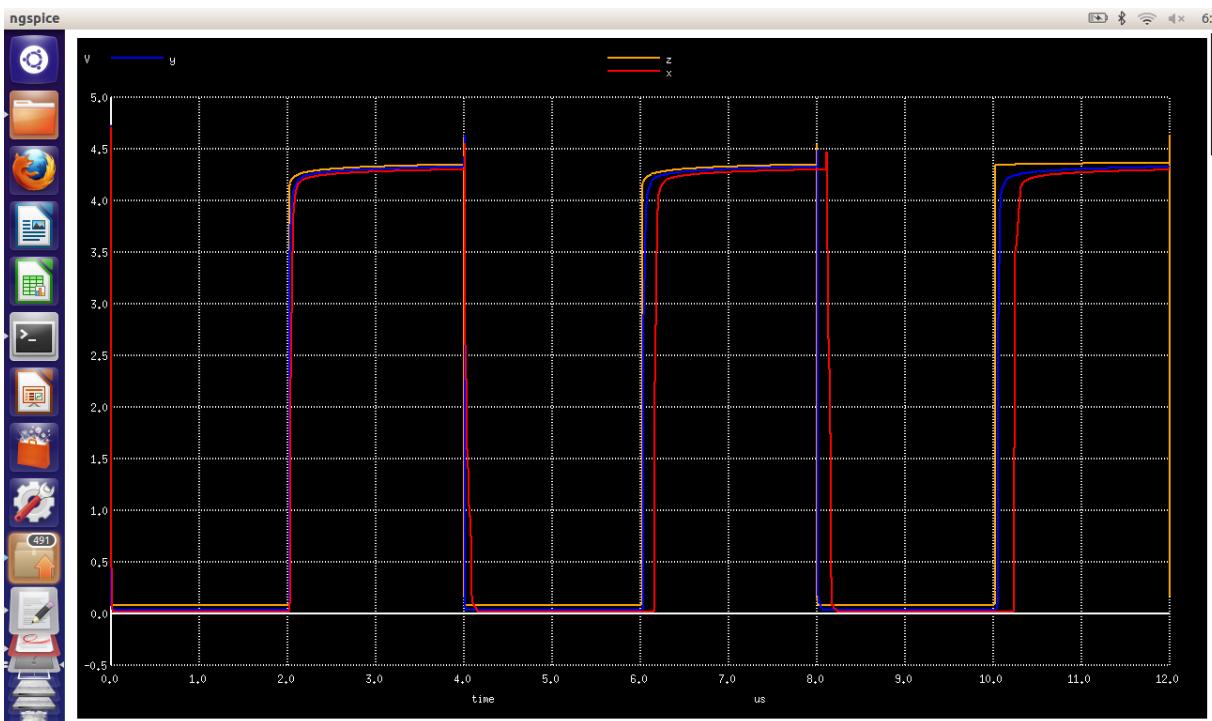


Figure 56: Transient Response due to varying the Width of the load nmos

Dynamic Power due to varying width of load nmos

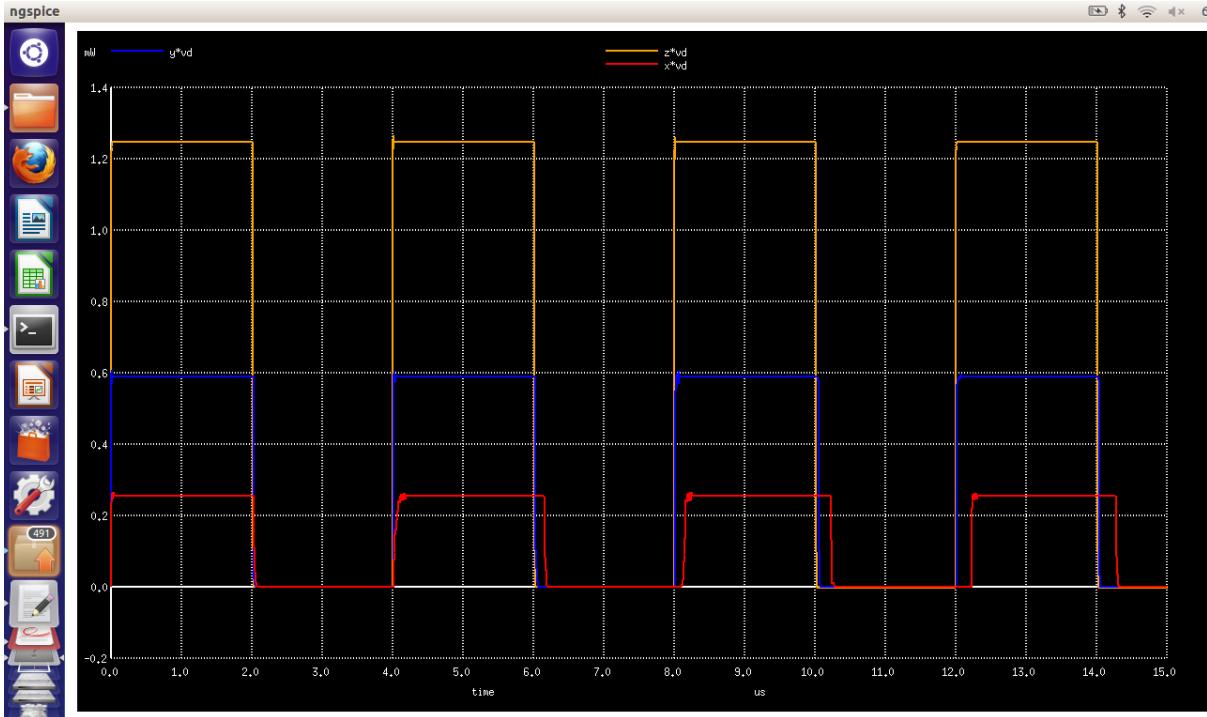


Figure 57: Dynamic Power due to varying the Width of the load nmos

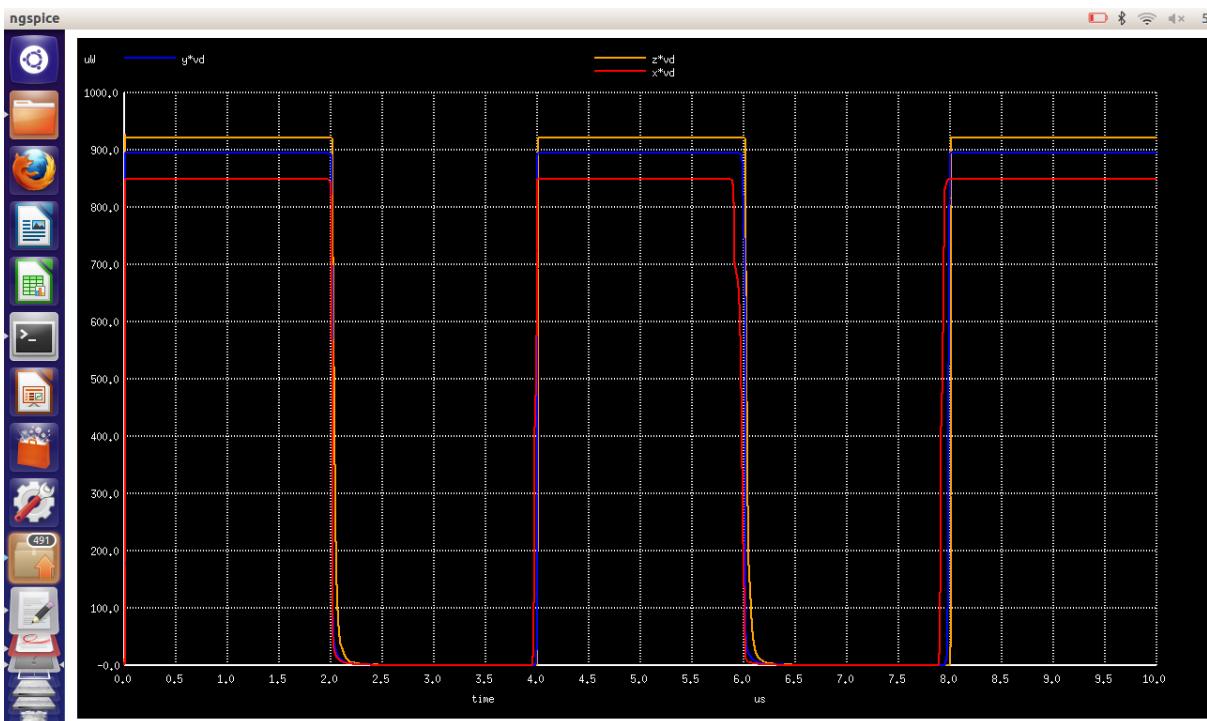


Figure 58: Dynamic Power due to varying the Width of the driver

Static Power due to varying Width of Driver

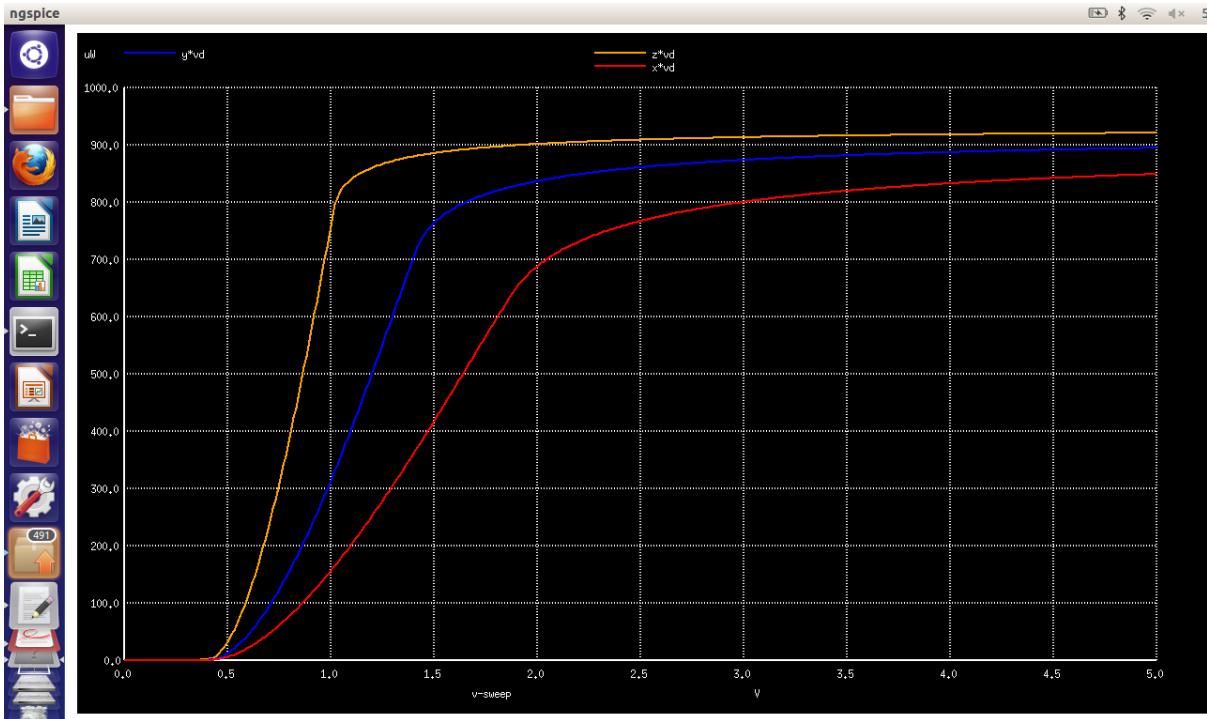


Figure 59: Static Power due to varying the Width of the Driver

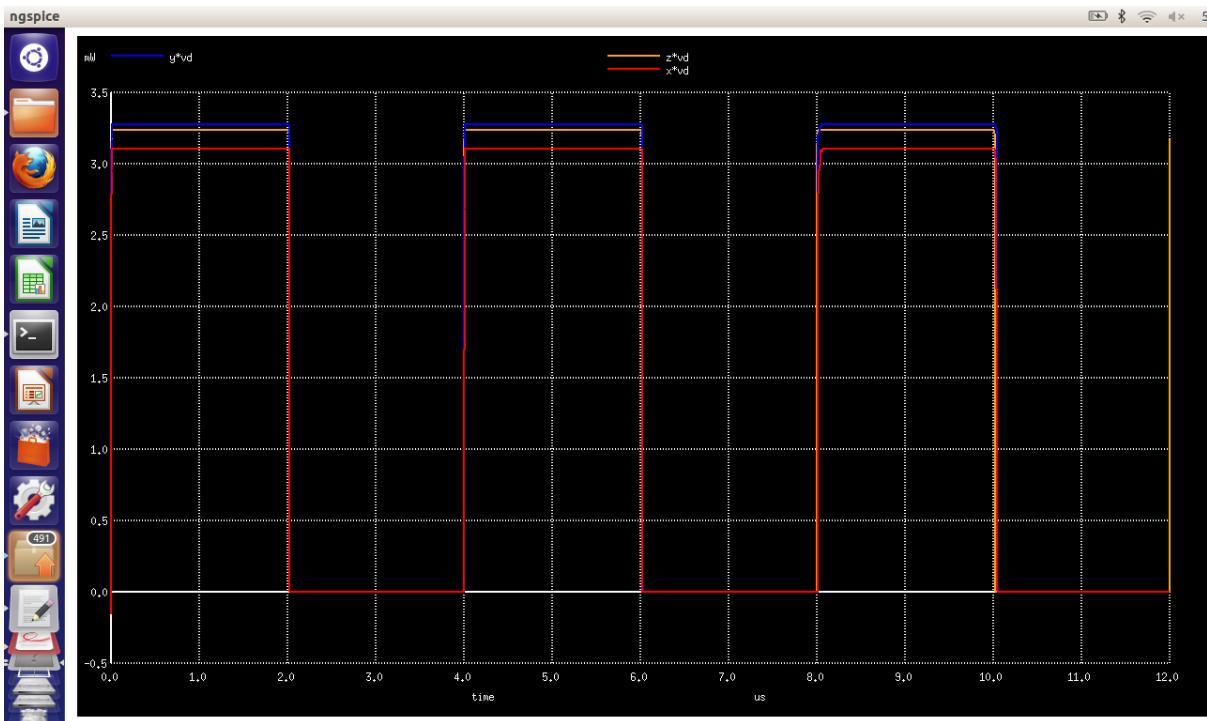


Figure 60: Dynamic Power due to varying the Length of the Driver

Conclusion: VOH can never be equal to VDD as NMOS can pull up to only VDD-VT.
As W/L of NMOS LOAD decreases

- VTC Shifts towards left
- The gain of the transition region in the VTC increases
- NML decreases and NMH increases
- TPLH increases and TPHL decreases
- VOL decreases as Resistance offered by nmos increases.
- Power Dissipation decreases as R is larger and also energy consumed per transition decreases.
- Rise/Fall time of output reduces.

As W/L of NMOS increases

- VTC Shifts towards left
- the gain of the transition region in the VTC increases.
- NML decreases and NMH increases
- TPLH increases and TPHL decreases
- VOL decreases as R becomes smaller than Resistance offered by pmos.
- Power Dissipation Increases as R is smaller and also energy consumed per transition increases.
- Rise/Fall time reduces

Depletion MOS and I vs V characteristics of PMOS

Objective: Study the behaviour of depletion MOS and PMOS transistors.

Depletion MOS Noise Margin

```
*include
.include /home/Ankit/Desktop/11ec86-93/t14y_tsmc_025_level3.txt

*nmos
m1 vdd out out 0 mnmos l=1u w=.2u
m2 out in 0 0 cmosn l=1u w=.2u
.model mnmos nmos level=1 vto=-0.7

*sources
v_dd vdd 0 dc 3.3
v_in in 0 dc 3.3

.control
dc v_in 0 3.3 0.01
run
end
plot out
plot deriv(out)
.endc
```

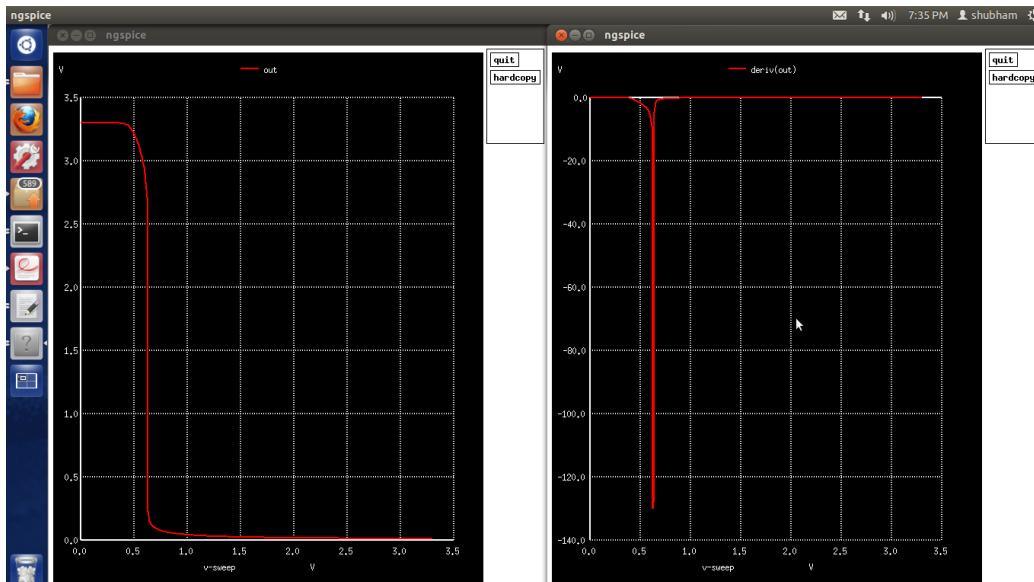


Figure 61: transient analysis and derivative for depletion MOS

I vs V characteristics

```
.include /home/Ankit/Desktop/11ec86-93/t14y_tsmc_025_level3.txt

m1 drain in vdd -3.3 cmosp l=1u w=0.5u
v_dd vdd 0 dc -3.3
v_in in 0 dc -3.3
v_drain drain 0 dc 0

.control
dc v_in 0 -3.3 -.01 v_dd 0 -3.3 -1
run
end
plot -v_dd#branch
.endc
```



Figure 62: I vs V characteristics for PMOS

Lab 4: Study of CMOS Inverter

Objective : Study the behaviour transfer function, noise margin, rise time ,fall time, propogation delay,paower of a CMOS inverter with variations in L and W of pullup and pulldown transistors.Also power and energy consumed with a non ideal step input

Circuit Diagram

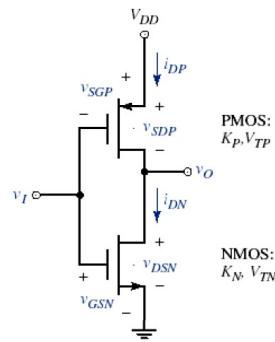


Figure 63: CMOS inverter

Transfer Function

```
* CMOS inverter *tranfer fun
.include /home/krunal/VLSI_LAB/VINAY/t14y_tsmc_025_level3.txt

m0 out in vd vd CMOSP l=1u w=2u *LOAD
m1 out in 0 0 CMOSN l=1u w=2u *Driver

*sources
vdd vd 0 dc 5
vin in 0 dc 5
* pulse(5 0 1n 1n 1n 2u 4u)

.dc vin 0 5 .01

*output graph
.control
*tran .01u 10u
run
plot out,in
.endc
```

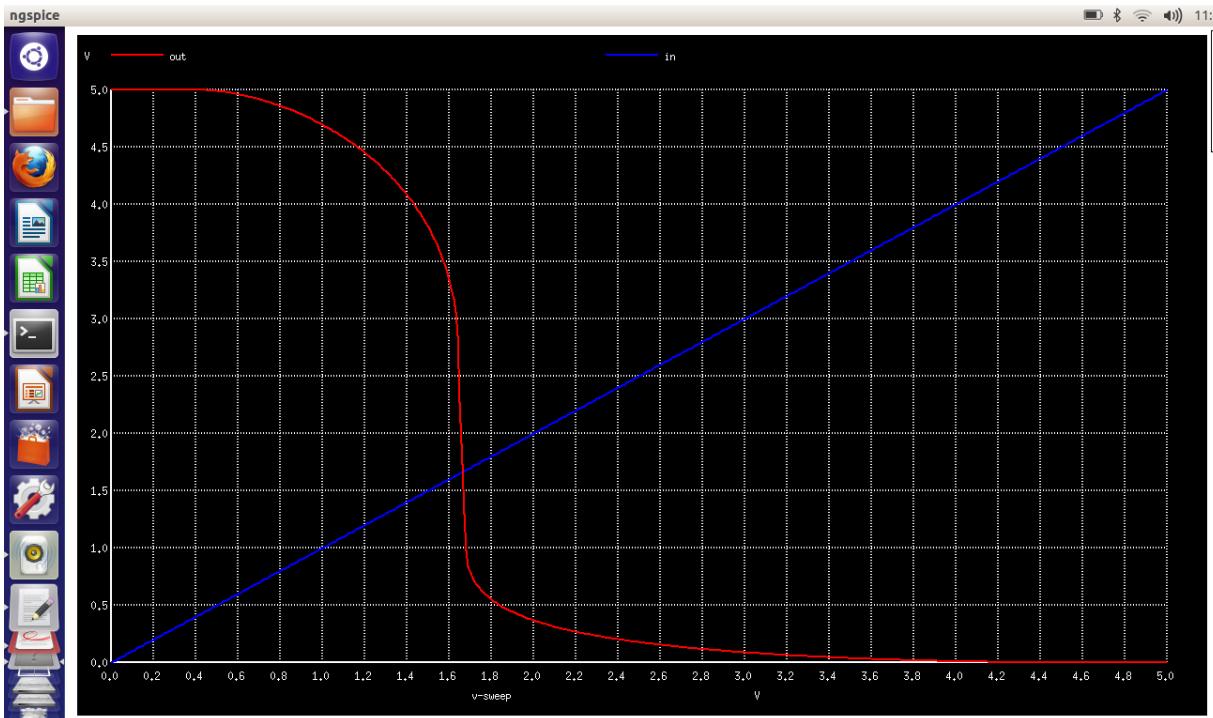


Figure 64: Transfer Function

Transfer Function due to varying Width of Nmos

```

* CMOS inverter
*tranfer_char/transient response/power for varing W of nmos

.include /home/krunal/VLSI_LAB/VINAY/t14y_tsmc_025_level3.txt

m0 out in vd 5 CMOSP l=1u w=.6u *LOAD
m1 out in 0 0 CMOSN l=1u w=.2u *Driver

*sources
vdd vd 0 dc 5
vin in 0 dc 5 pulse(5 0 .01m .2m .2m .5m 1m)

*.dc vin 0 5 .01

*varing W/L ratio

.control
foreach wid .6u 2u 10u
alter m1 w = $wid
tran .001m 1m
run
end
.endc

```

```
*plotting the output for various w of load
```

```
.control
foreach iter 1 2 3
setplot tran$iter
*setplot dc$iter
end
.endc
```

```
*plotting graph for transfer char
```

```
.control
let x_500_nano= tran1.out
let y_2u= tran2.out
let z_6u= tran3.out
plot x_500_nano,y_2u,z_6u
end
.endc
```

```
ploting graph for power
```

```
.control
let x= -tran1.vdd#branch
let y= -tran2.vdd#branch
let z= -tran3.vdd#branch
plot x*vd, y*vd, z*vd
end
.endc
```

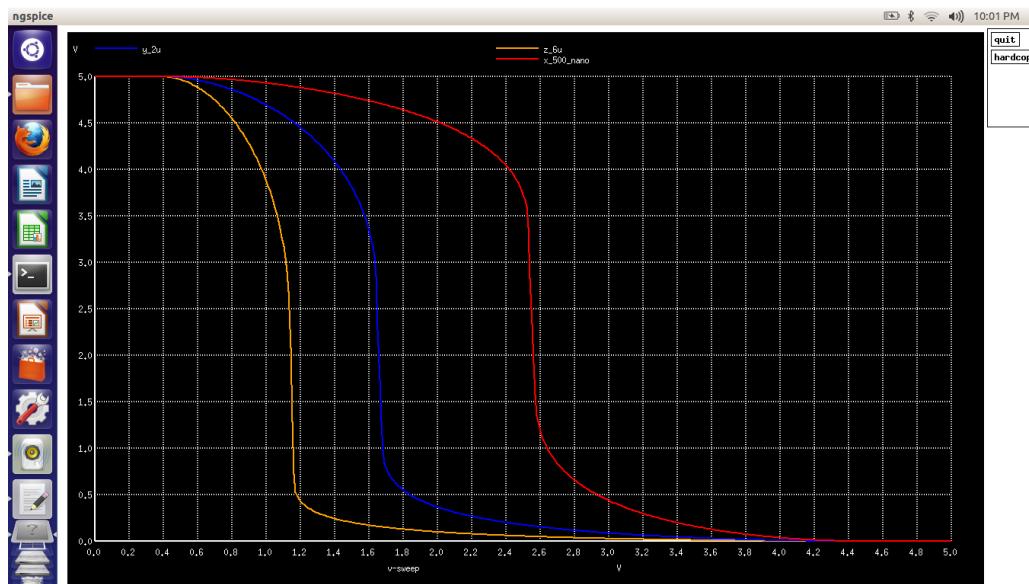


Figure 65: Transfer Function due to varying Width of Nmos

Effect on Rise Time due to W of Nmos

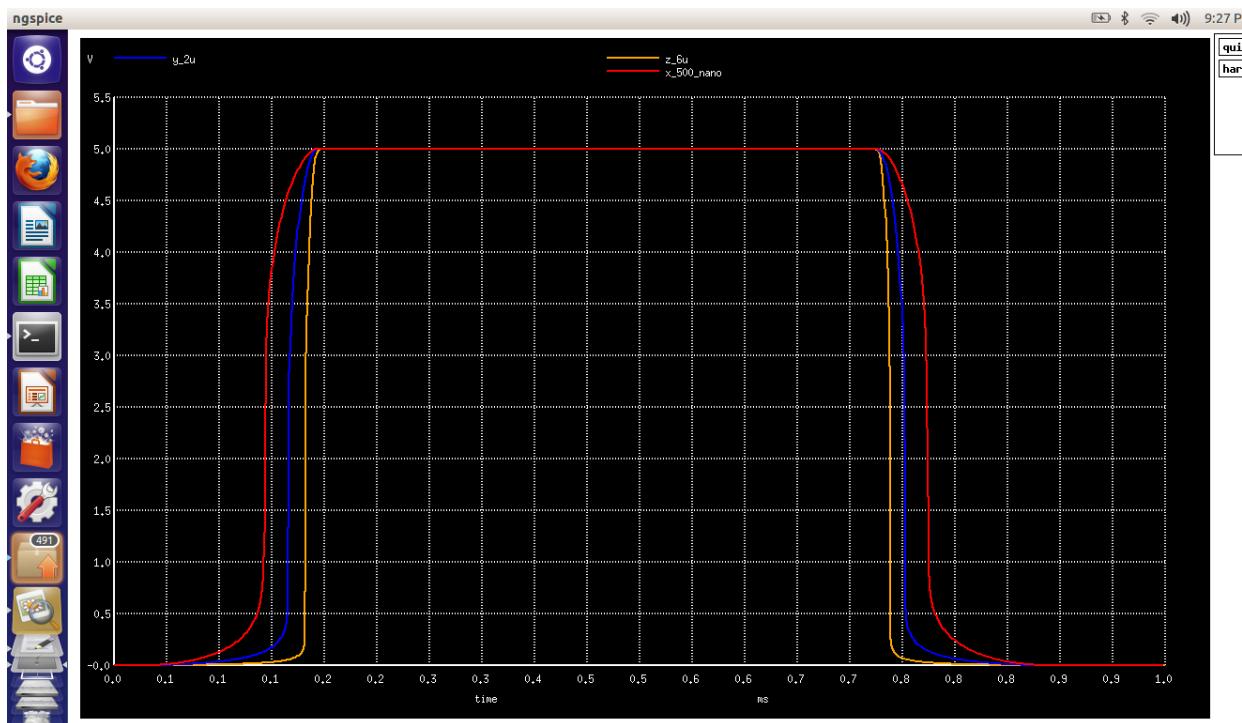


Figure 66: effect on rise time due to W of Nmos

Transfer Characteristic on varying L of Driver

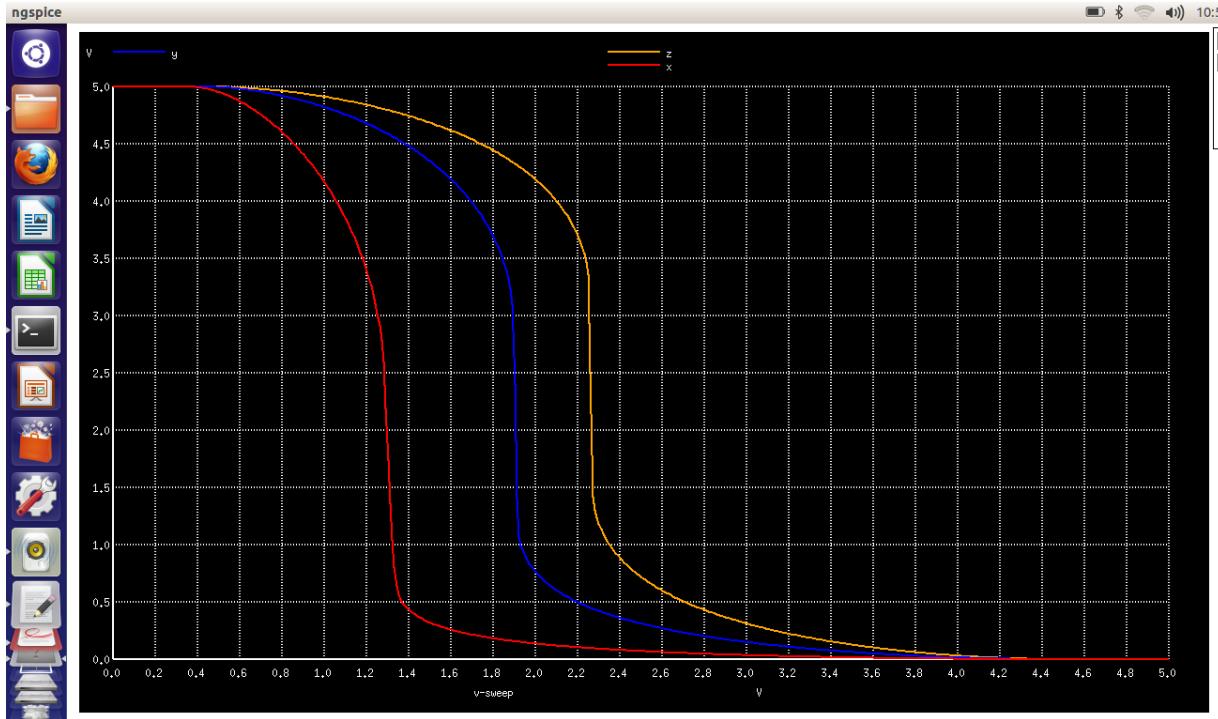


Figure 67: Transfer Characteristic on varying L of Driver

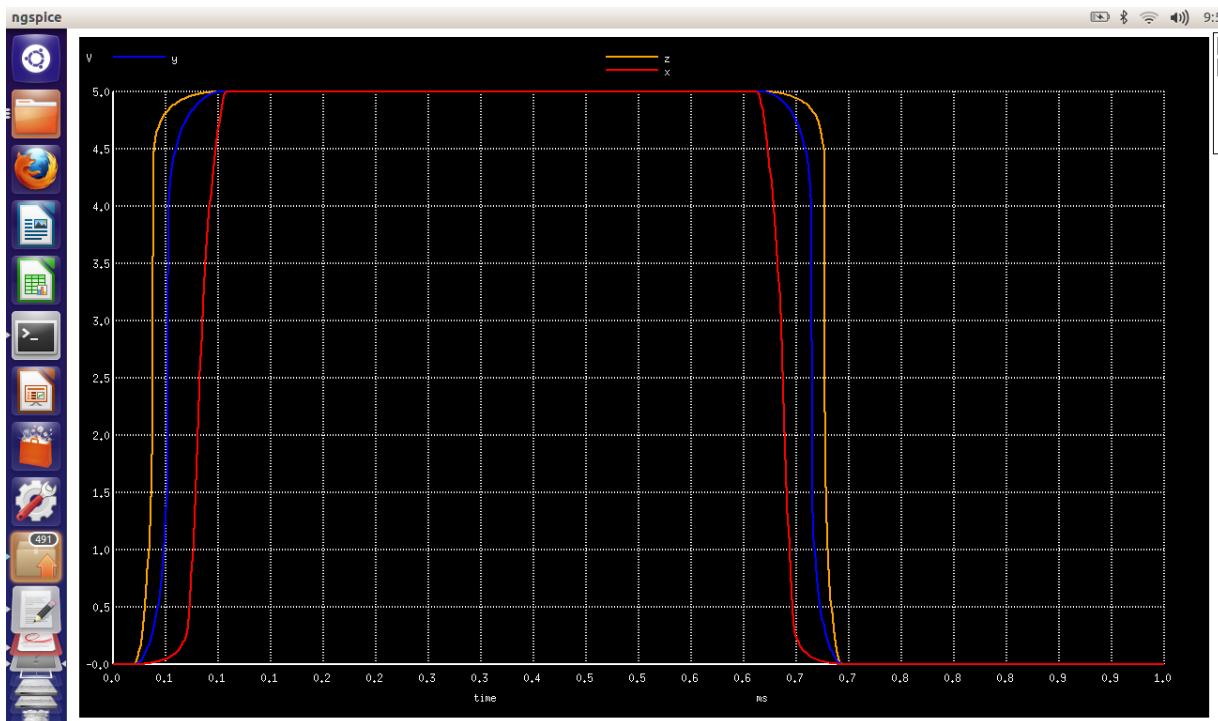


Figure 68: Effect on Rise and Fall time due to varing Length of nmos(driver)

Transient Response on varying L of load pmos

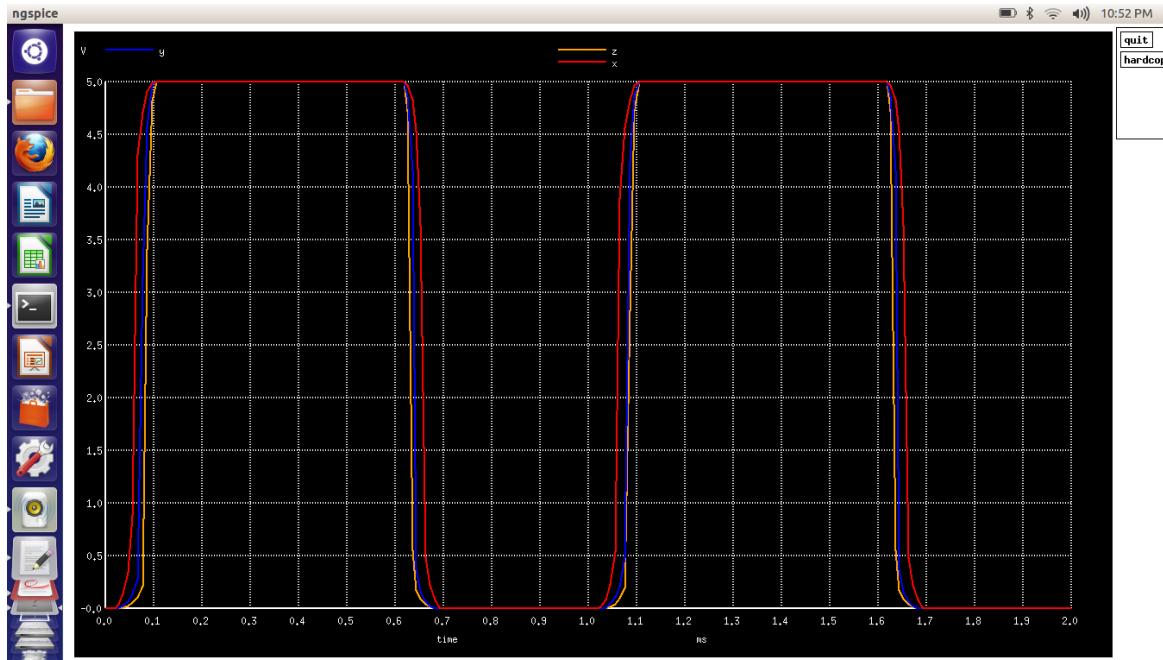


Figure 69: Transient Response on varying L of load pmos

Transfer Characteristics on varying L of load pmos

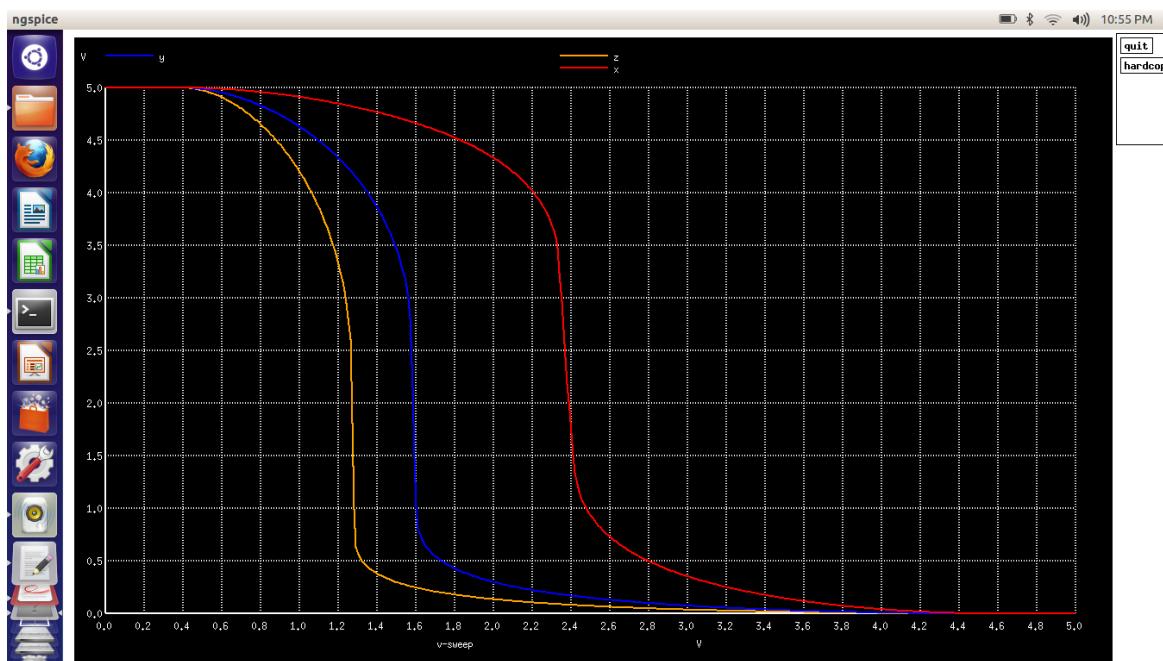


Figure 70: Transfer Characteristics on varying L of load pmos

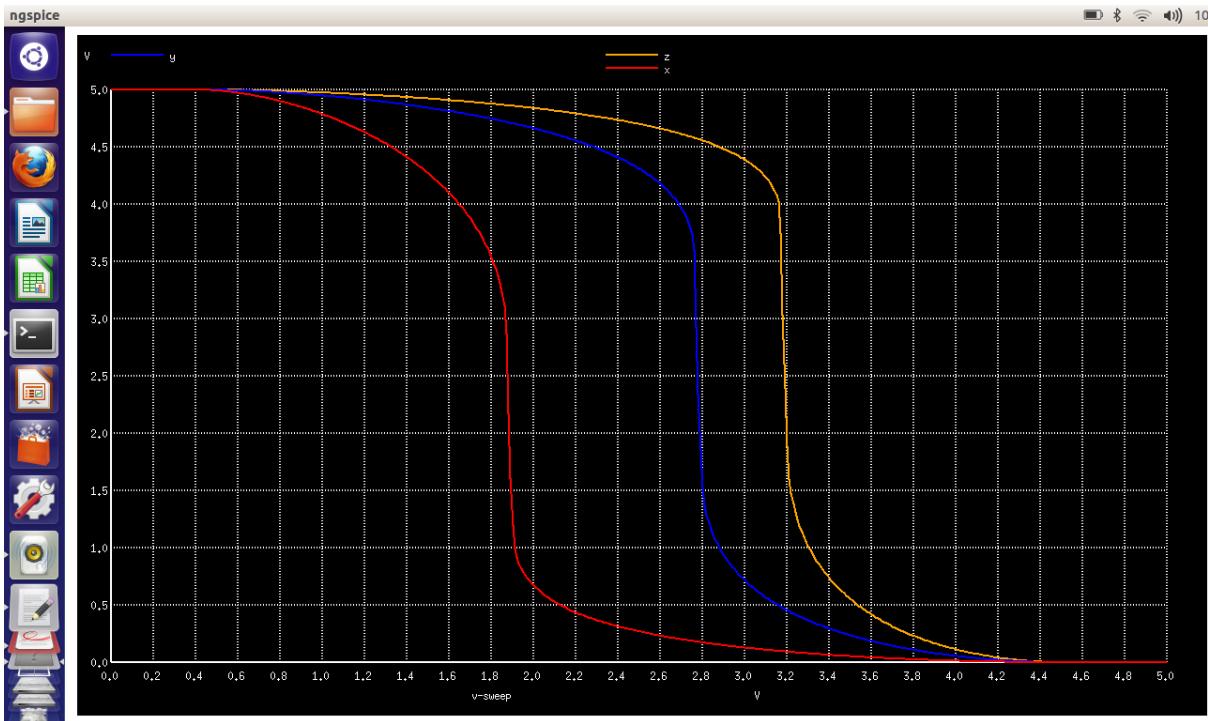


Figure 71: Dynamic Power due to varying the Length of the Driver

Effect on Rise Time due to varying W of pmos load

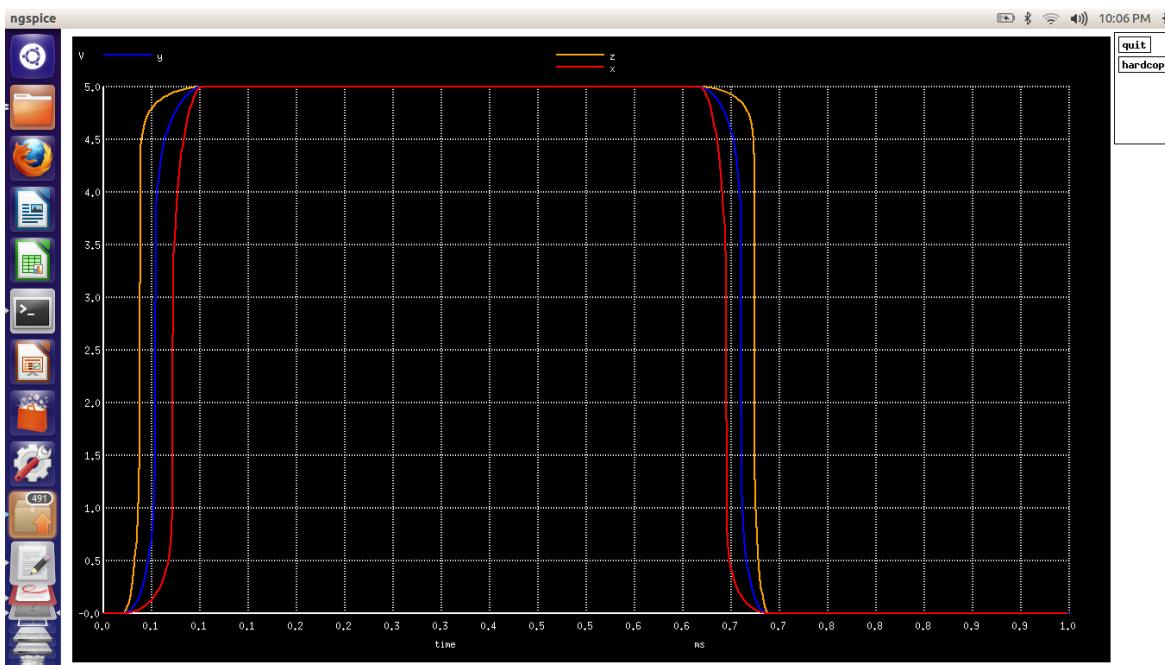


Figure 72: Effect on Rise Time due to varying W of pmos load

Effect on Rise Time due to varying W of pmos load

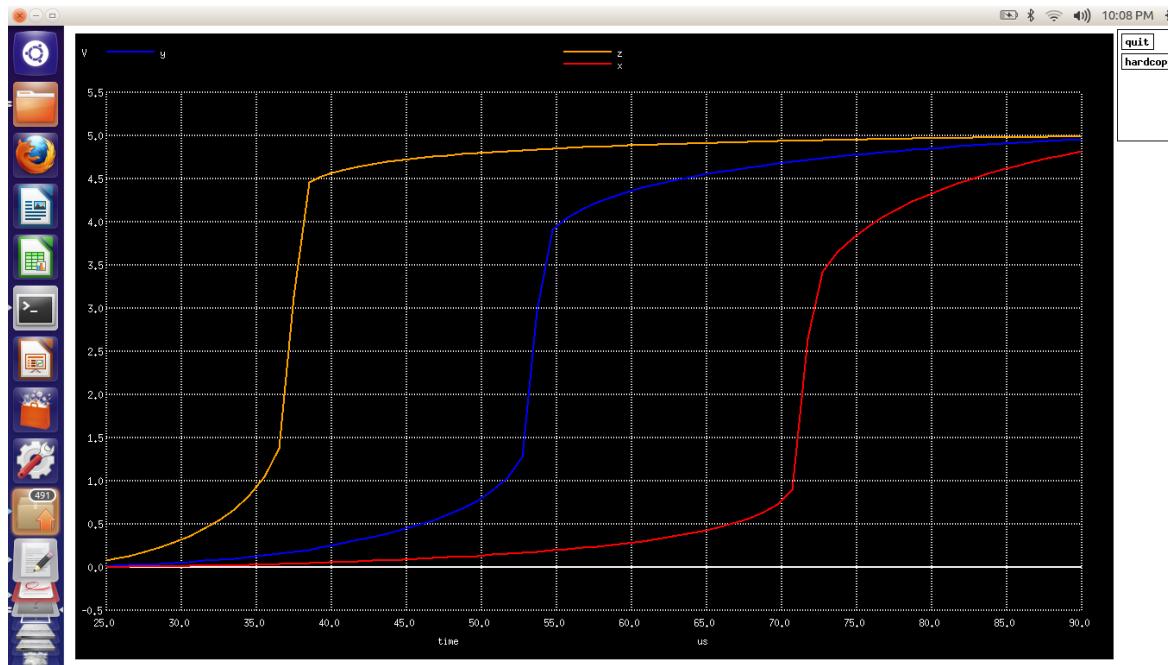


Figure 73: Effect on Rise Time due to varying W of pmos load

Effect on rise time due to varying L of pmos load

```
* CMOS inverter
*tranfer_char/transient response/power for varing L of nmos

.include /home/krunal/VLSI_LAB/VINAY/t14y_tsmc_025_level3.txt

m0 out in vd 5 CMOSP l=1u w=.8u *LOAD
m1 out in 0 0 CMOSN l=2u w=.2u *Driver

*sources
vdd vd 0 dc 5
vin in 0 dc 5 pulse(5 0 .01m .1m .1m .5m 1m)

*.dc vin 0 5 .01

*varing W/L ratio

.control
foreach len .12u 2u 10u
alter m1 l = $len
tran .001m 1m
run
end
.endc

*plotting the output for various w of load

.control
foreach iter 1 2 3
setplot tran$iter
*setplot dc$iter
end
.endc

*ploting graph for transfer char

.control
let x= tran1.out
let y= tran2.out
let z= tran3.out
plot x,y,z
end
.endc

*ploting graph for power

*.control
*let x= -tran1.vdd#branch
```

```
*let y= -tran2.vdd#branch  
*let z= -tran3.vdd#branch  
*plot x*vd, y*vd, z*vd  
*end  
.endc
```

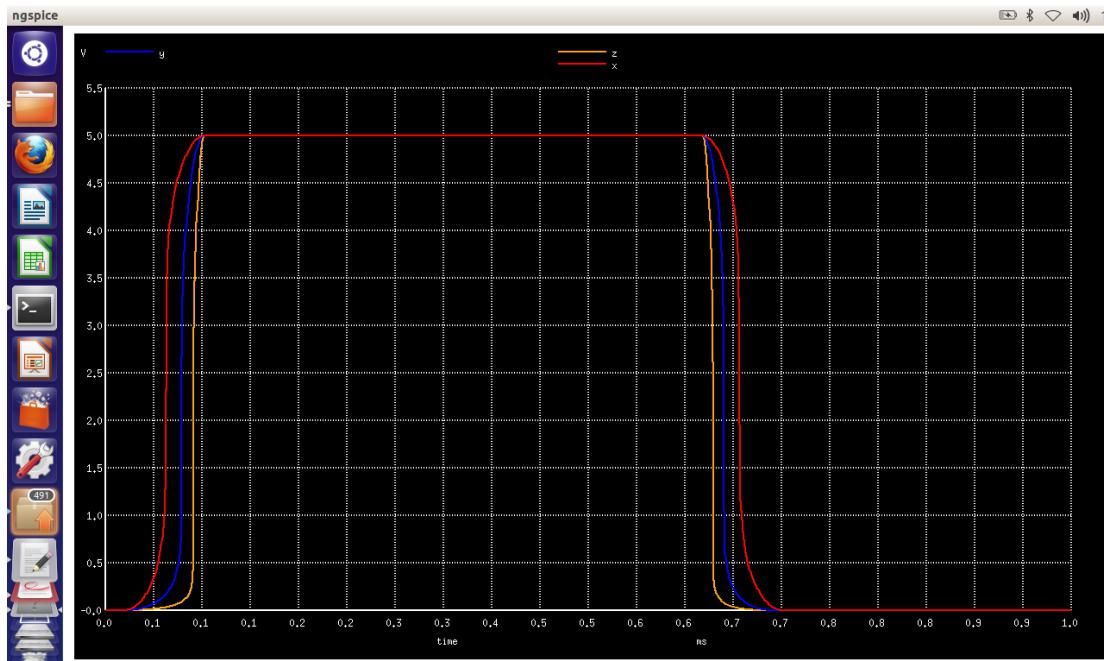


Figure 74: Effect on rise time due to varying L of pmos load

Dynamic Power due to varying length of the driver

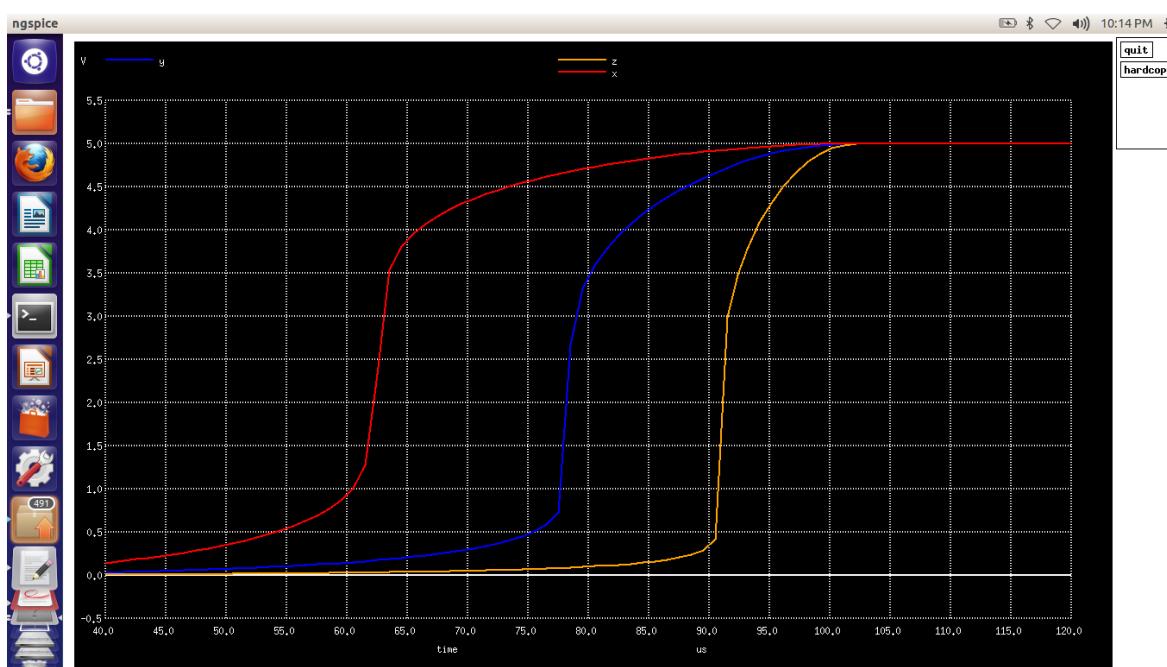


Figure 75: Dynamic Power due to varying the Length of the Driver

Effect on Transfer Characteristics due to varying load Capacitance

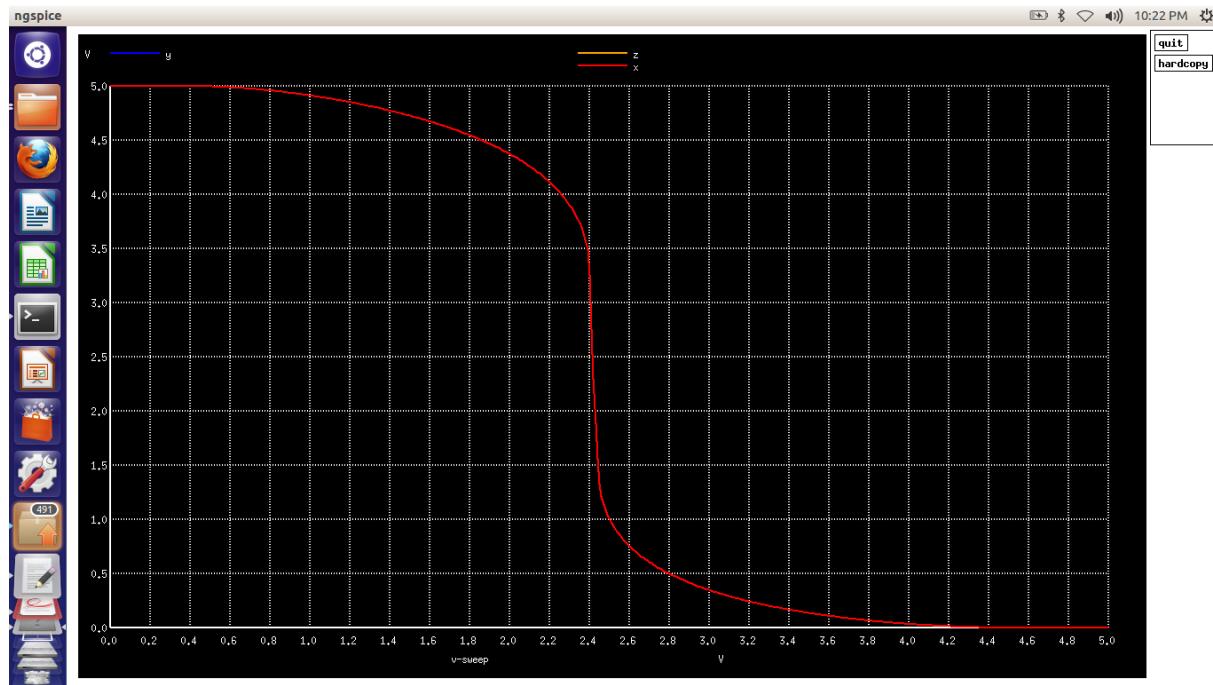


Figure 76: Effect on Transfer Characteristics due to varying load Capacitance

LAB 5: Study of CMOS gates

Objective : Study the behaviour transfer function,noise margin, rise time ,fall time, propogation delay,paower of a CMOS gates like NAND ,NOR functions (2 input AND gate ,2 input OR gate) with variations in L and W of pullup and pulldown transistors.

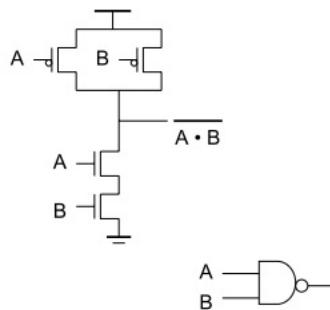


Figure 77: CMOS NAND gate

NAND GATE

*NAND Gate Implementation

```
.include /home/vlsilab/UG_students_2014/t14y_tsmc_025_level3.txt

M1 vdd1 A top1 0 cmosn L=1U W=10U
M2 top1 B 0 0 cmosn L=1U W=10U

M3 vdd1 A v_connect v_connect cmosp L=1U W=10U
M4 vdd1 B v_connect v_connect cmosp L=1U W=10U

v_dd v_connect 0 3.3
v_gs1 A 0 PULSE(0 3.3 0 0 0 8NS 16NS)
v_gs2 B 0 PULSE(0 3.3 0 0 0 16NS 32NS)

.control
tran 0.1NS 32NS
run
end
plot tran1.A tran1.B tran1.vdd1
.endc
.end
```

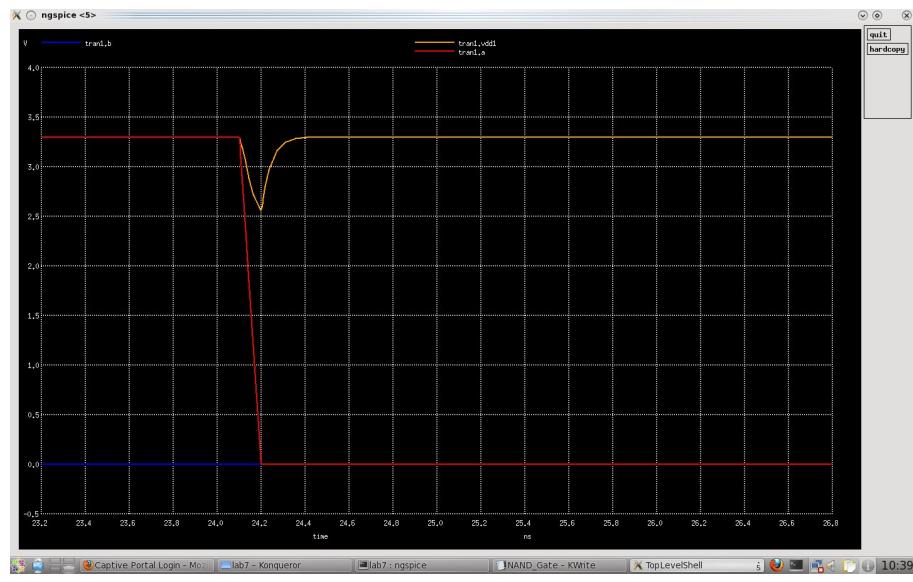


Figure 78: transient response for NAND gate for input a=0,b=0

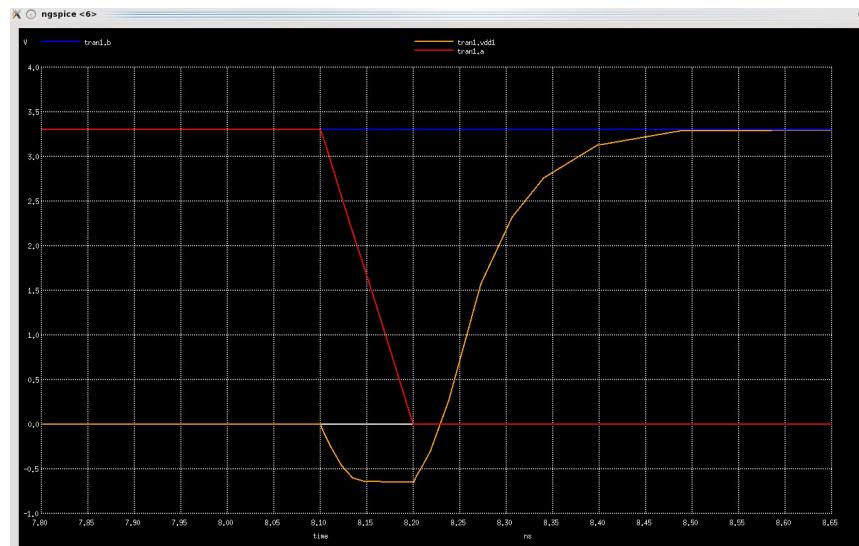


Figure 79: transient response for NAND gate for input a=0,b=1

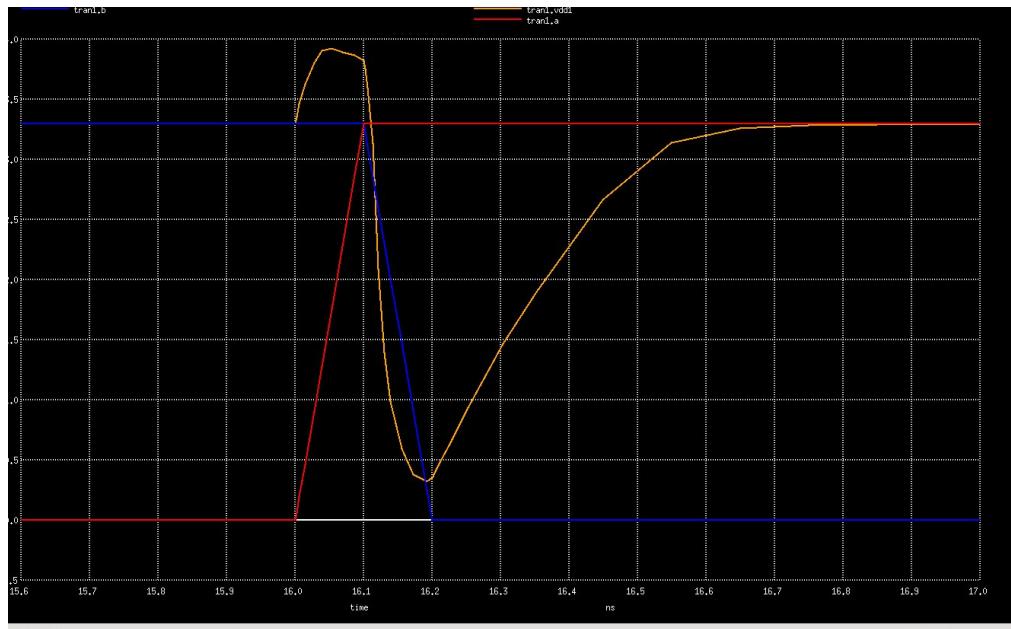


Figure 80: transient response for NAND gate for input a=1,b=0

AND GATE

```

top1 A v_connect v_connect cmosp L=1U W=10U *NAND Gate Implementation

.include /home/vlsilab/UG_students_2014/t14y_tsmc_025_level3.txt

M1 vdd1 A top1 0 cmosn L=1U W=10U
M2 top1 B 0 0 cmosn L=1U W=10U
M5 stage2 vdd1 0 cmosn L=1U W=10U

M3 vdd1 A v_connect v_connect cmosp L=1U W=10U
M4 vdd1 B v_connect v_connect cmosp L=1U W=10U
M6 stage2 vdd1 v_connect v_connect cmosp L=1U W=10U

v_dd v_connect 0 3.3
v_gs1 A 0 PULSE(0 3.3 0 0 0 8NS 16NS)
v_gs2 B 0 PULSE(0 3.3 0 0 0 16NS 32NS)

.control
tran 0.1NS 32NS
run
end
plot tran1.A tran1.B tran1.vdd1 tran1.stage2
.endc
.end

```

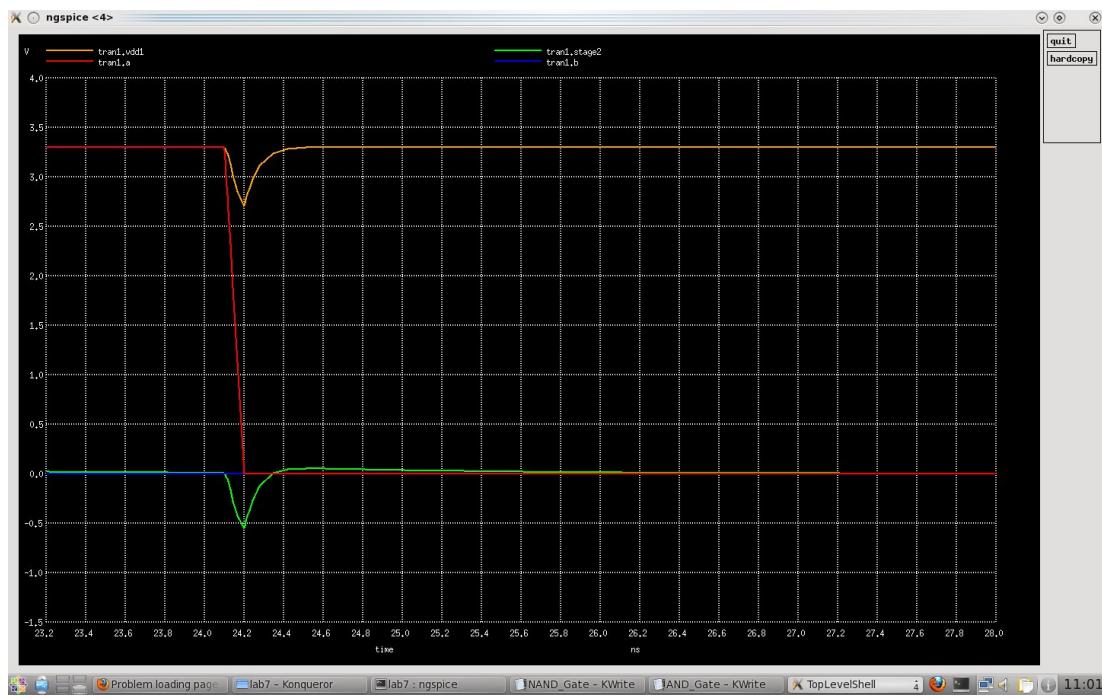


Figure 81: transient response for AND gate for input $a=0, b=0$

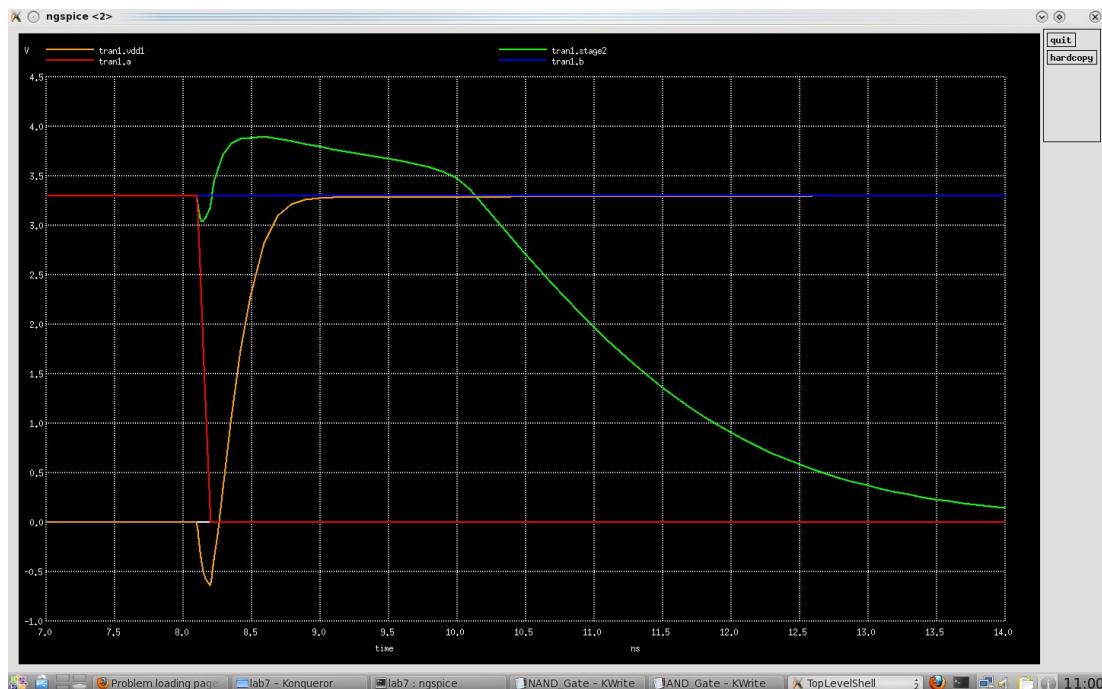


Figure 82: transient response for AND gate for input $a=0, b=1$

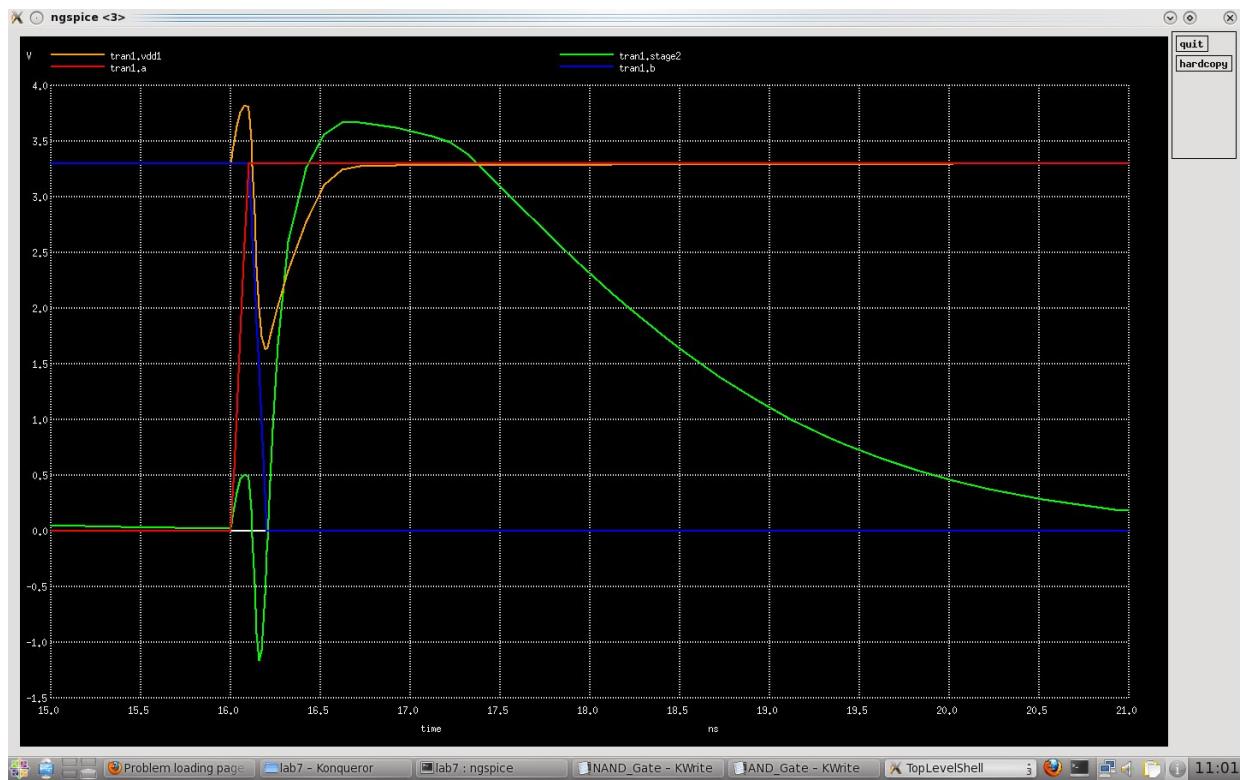


Figure 83: transient response for AND gate for input a=1,b=0

NOR GATE

*NOR Gate Implementation

```
.include /home/vlsilab/UG_students_2014/t14y_tsmc_025_level3.txt

M1 vdd1 A 0 0 cmosn L=1U W=10U
M2 vdd1 B 0 0 cmosn L=1U W=10U

M3 top1 A v_connect v_connect cmosp L=1U W=10U
M4 vdd1 B top1 top1 cmosp L=1U W=10U

v_dd v_connect 0 3.3
v_gs1 A 0 PULSE(0 3.3 0 0 0 8NS 16NS)
v_gs2 B 0 PULSE(0 3.3 0 0 0 16NS 32NS)

.control
tran 0.1NS 32NS
run
end
plot tran1.A tran1.B tran1.vdd1
.endc

.end
```

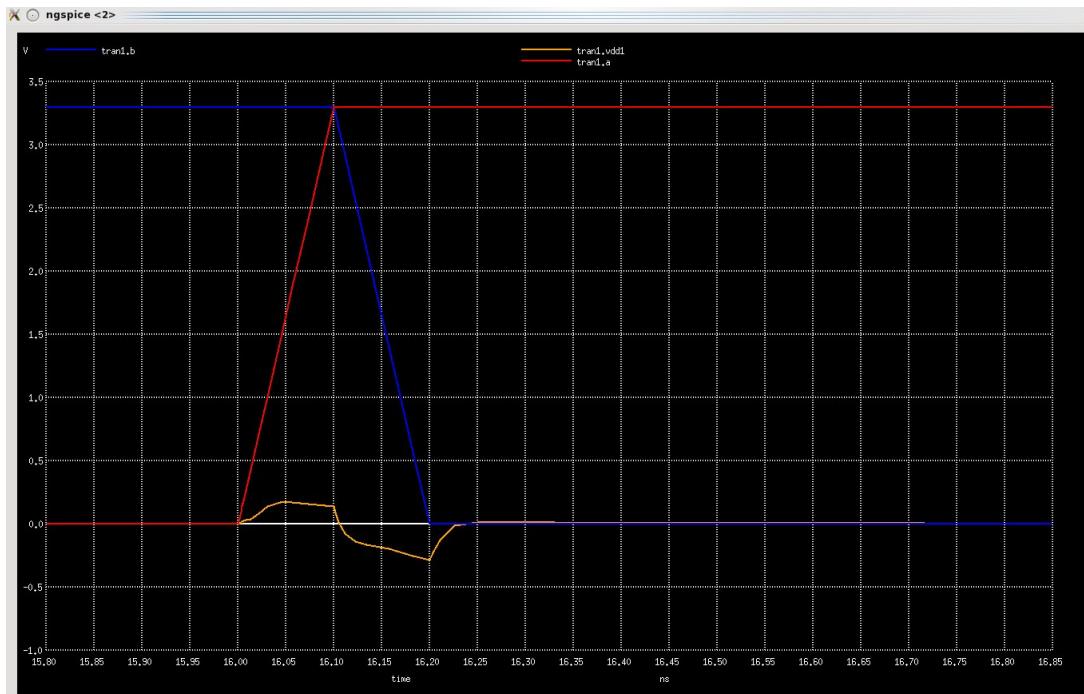


Figure 84: transient response for NOR gate for input $a=1, b=0$

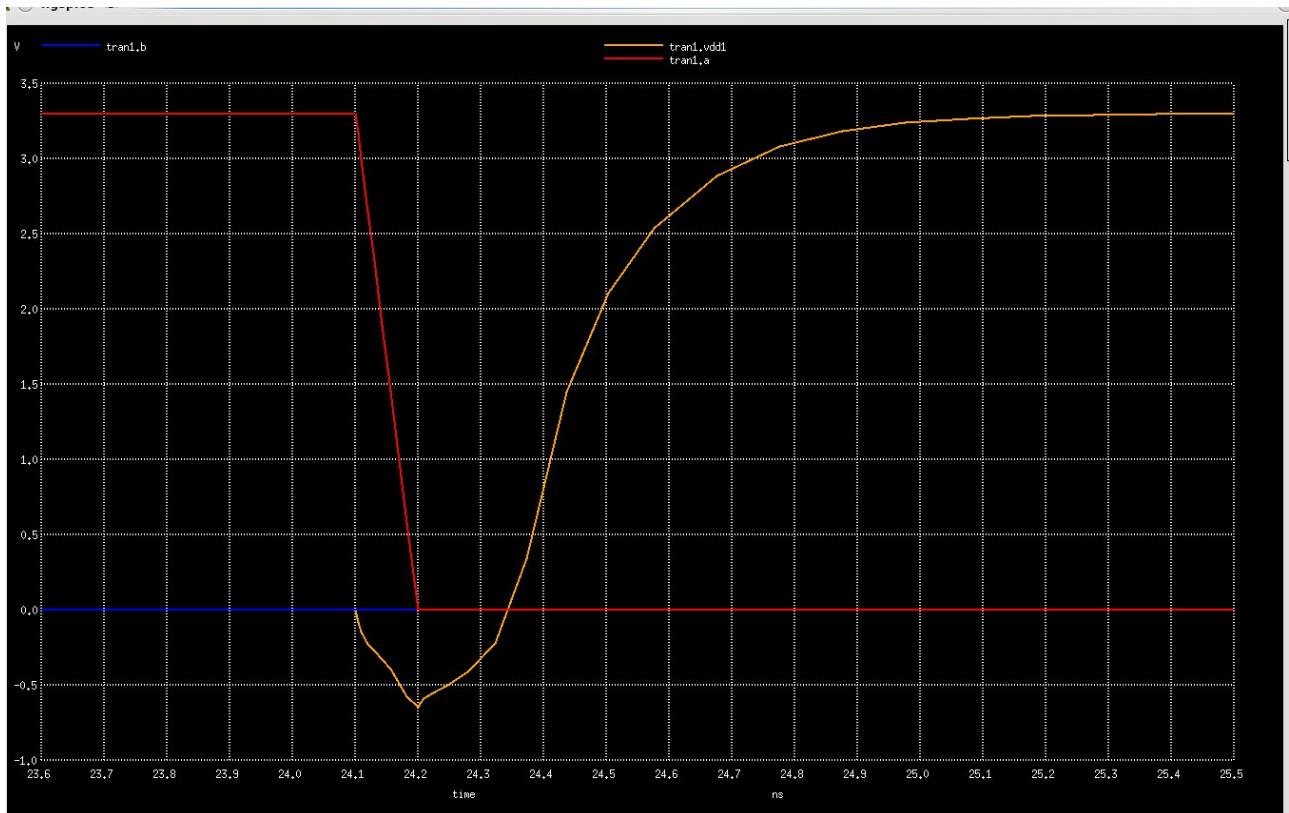


Figure 85: transient response for NOR gate for input a=1,b=1

OR GATE

OR Gate Implementation

```
.include /home/vlsilab/UG_students_2014/t14y_tsmc_025_level3.txt

M1 vdd1 A 0 0 cmosn L=2U W=4U
M2 vdd1 B 0 0 cmosn L=2U W=4U
M5 stage1 vdd1 0 0 cmosn L=2U W=4U

M3 top1 A v_c v_c cmosp L=2U W=12U
M4 vdd1 B top1 v_c cmosp L=2U W=12U
M6 stage1 vdd1 v_c v_c cmosp L=2U W=12U

v_dd v_c 0 3.3
v_gs1 A 0 PULSE(0 3.3 0.1p 0.1p 0.1p 4NS 8NS)
v_gs2 B 0 PULSE(0 3.3 0.1p 0.1p 0.1p 8NS 16NS)

.control
foreach wid 12u 24u 36u 28u
alter M3 W=$wid
```

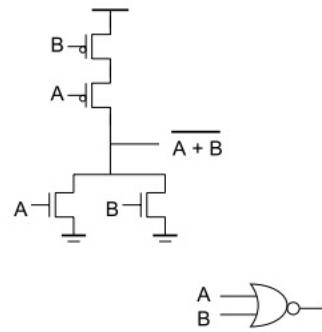


Figure 86: CMOS OR gate

```

alter M4 W=$wid
tran 0.1NS 20NS
run
plot A B vdd1
end
.endc
.end

```

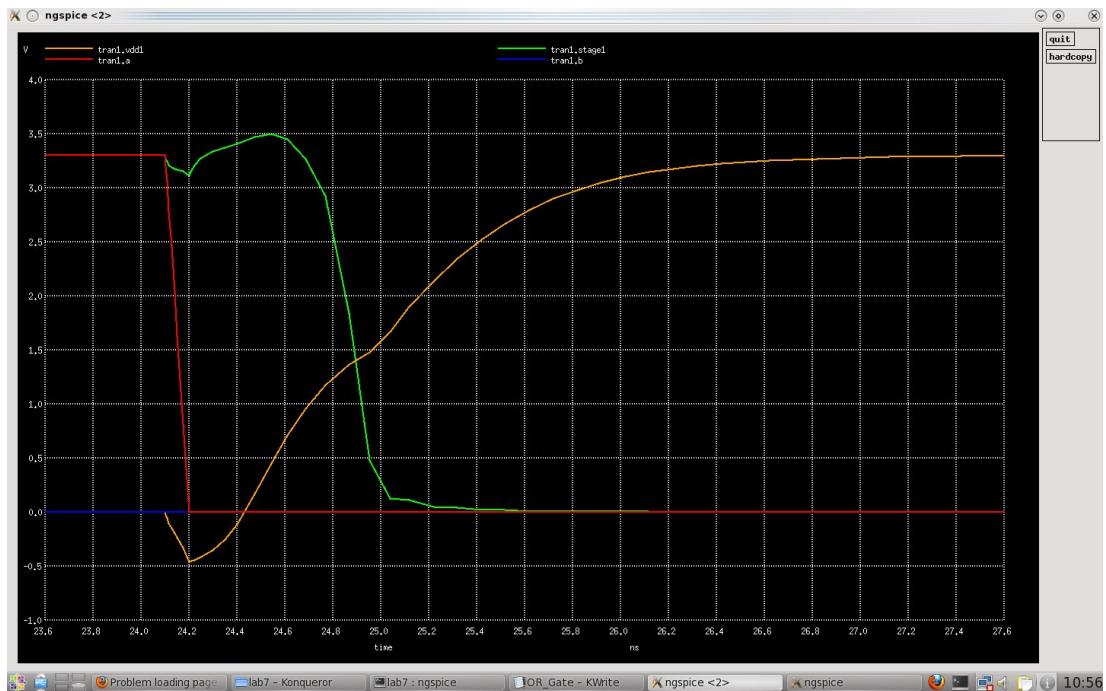


Figure 87: transient response for OR gate for input a=0,b=0

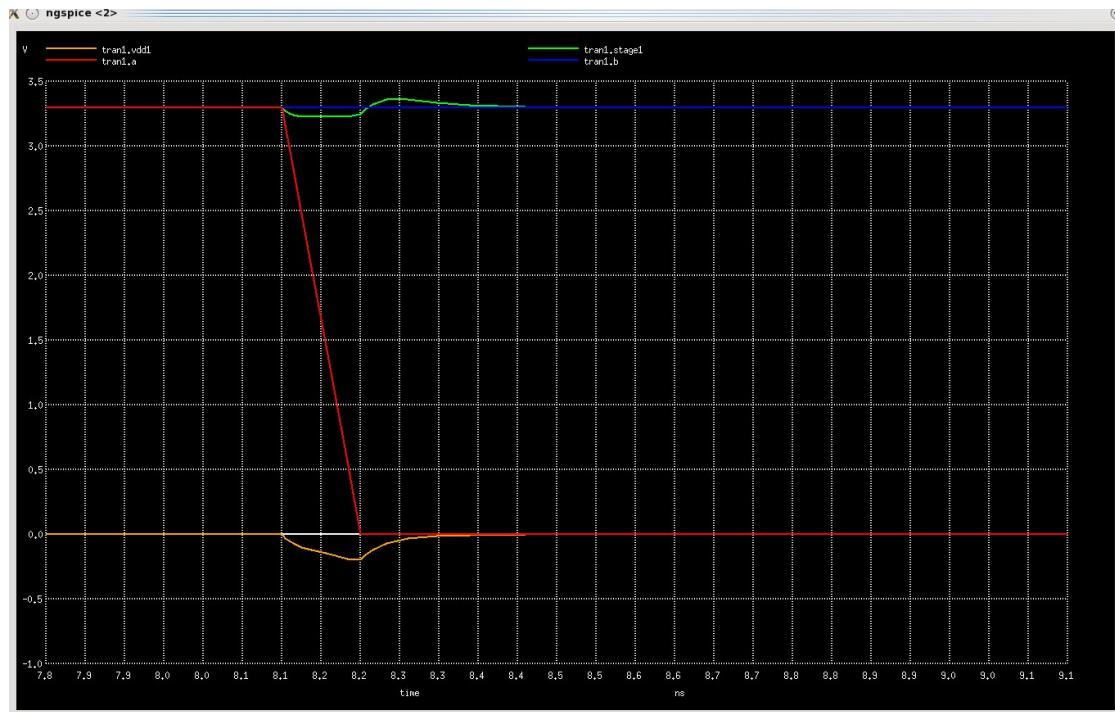


Figure 88: transient response for OR gate for input $a=0, b=1$

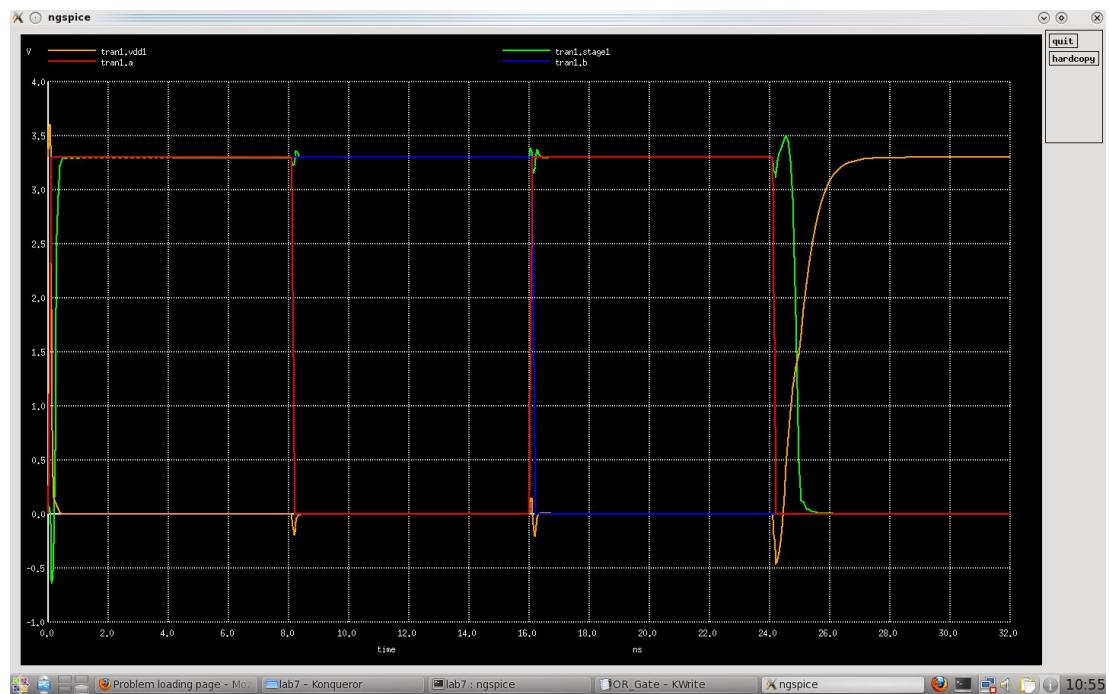


Figure 89: transient response for OR gate for all input combinations

XOR GATE

```
XOR gate
*Model include
.include t14y_tsmc_025_level3.txt
*models
M1000 v_b_bar v_b vdd vdd CMOSP w=9u l=3u
M1001 v_b_bar v_b vss Gnd CMOSN w=3u l=3u
M1002 xor_out v_a v_b vdd CMOSP w=6u l=3u
M1003 v_a v_b xor_out vdd CMOSP w=6u l=3u
M1004 xor_out v_a v_b_bar Gnd CMOSN w=3u l=3u
M1005 v_a v_b_bar xor_out Gnd CMOSN w=3u l=3u
*Sources
v_dd vdd 0 5
va v_a 0 pulse(0 5 0 1ps 1ps 40ns 80ns)
vb v_b 0 pulse(0 5 0 1ps 1ps 80ns 160ns)
v_ss vss 0 0
* Analyses
.control
tran 0.5ns 160ns
.endc
```

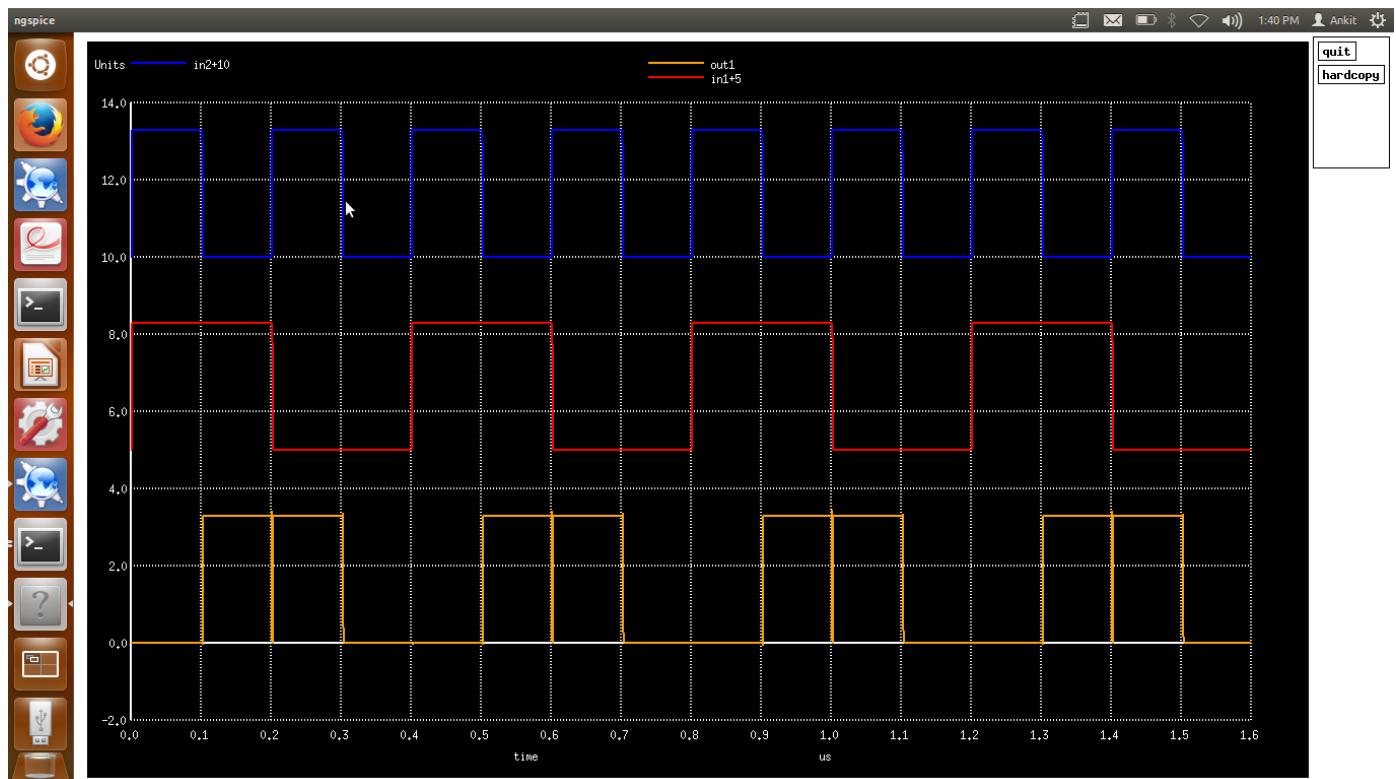


Figure 90: Simulation results for XOR gate

MODULE-2 REPORT :: LAYOUT DESIGNING WITH MAGIC

Layout design for CMOS inverter

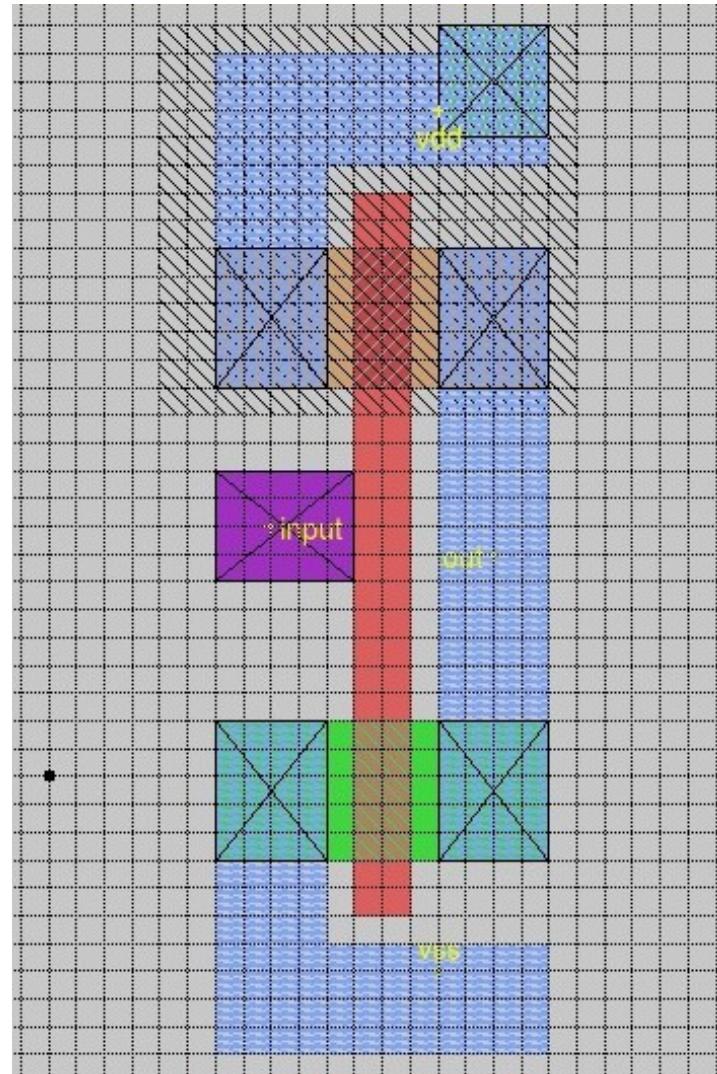


Figure 91: Layout design for CMOS inveter

Layout design for CMOS 2 input AND gate

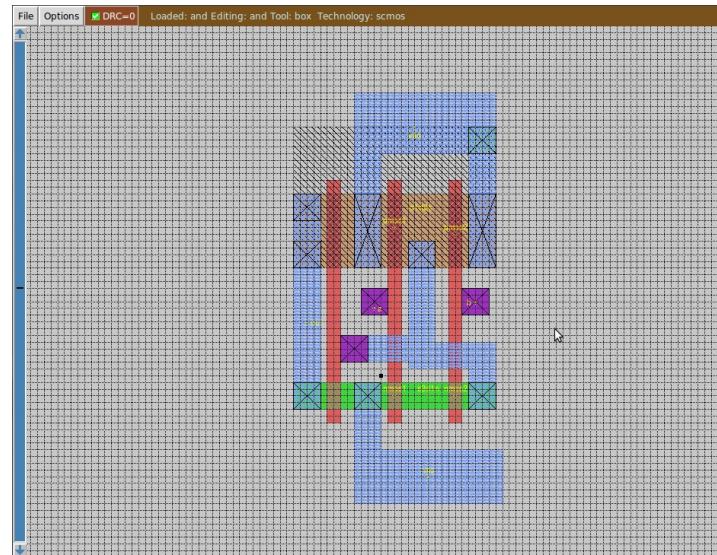


Figure 92: Layout design for CMOS 2 input AND gate

Rise Time for CMOS 2 input AND gate

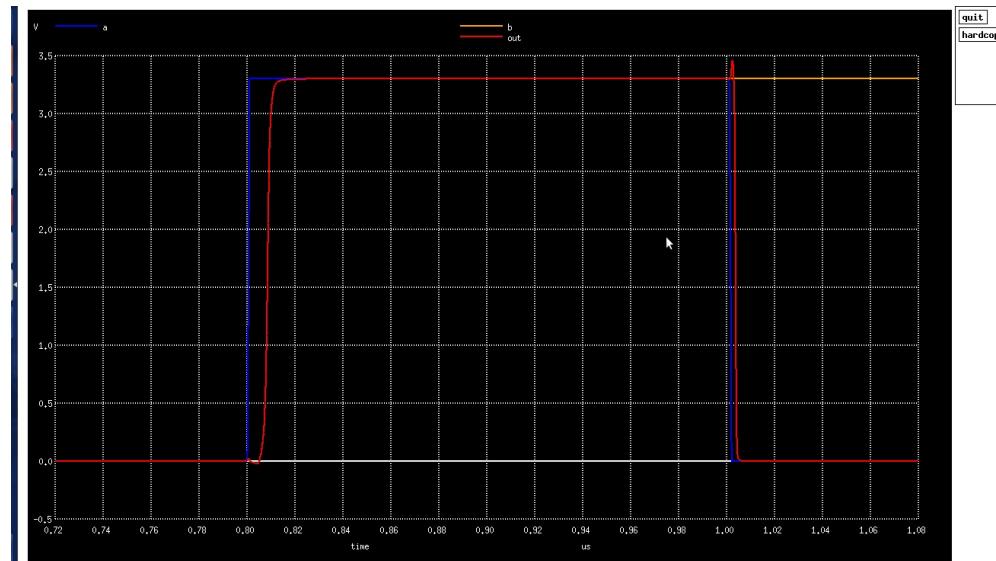


Figure 93: Rise Time for CMOS 2 input AND gate

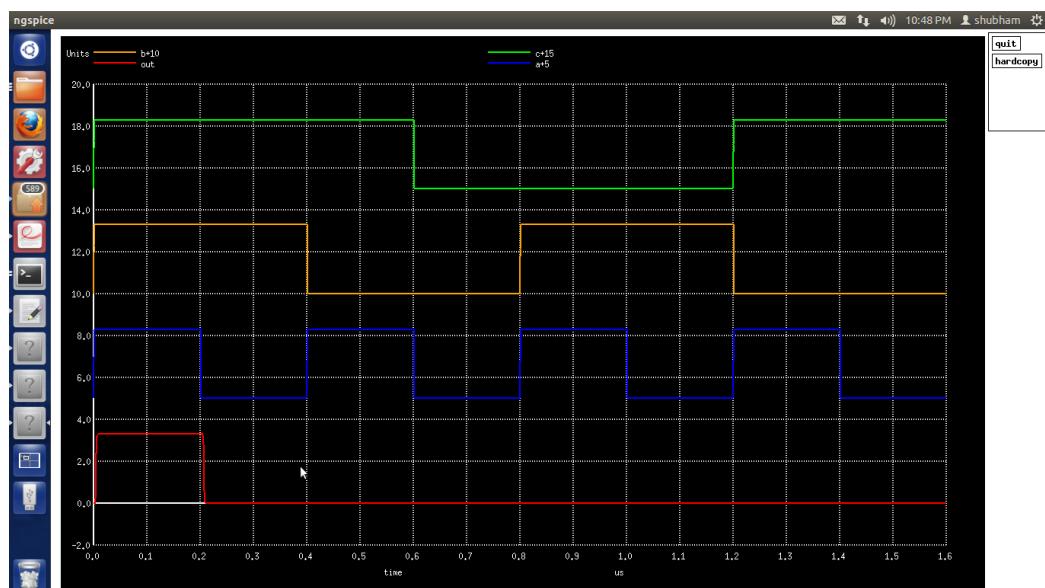


Figure 94: simulation results for CMOS 3 input NAND gate

Layout design for CMOS 3 input NAND gate

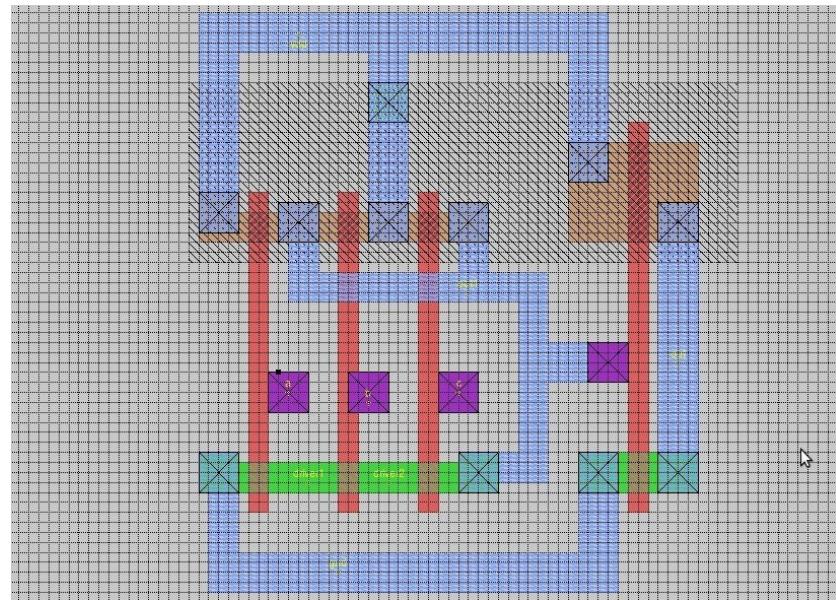


Figure 95: Layout design for CMOS 3 input NAND gate

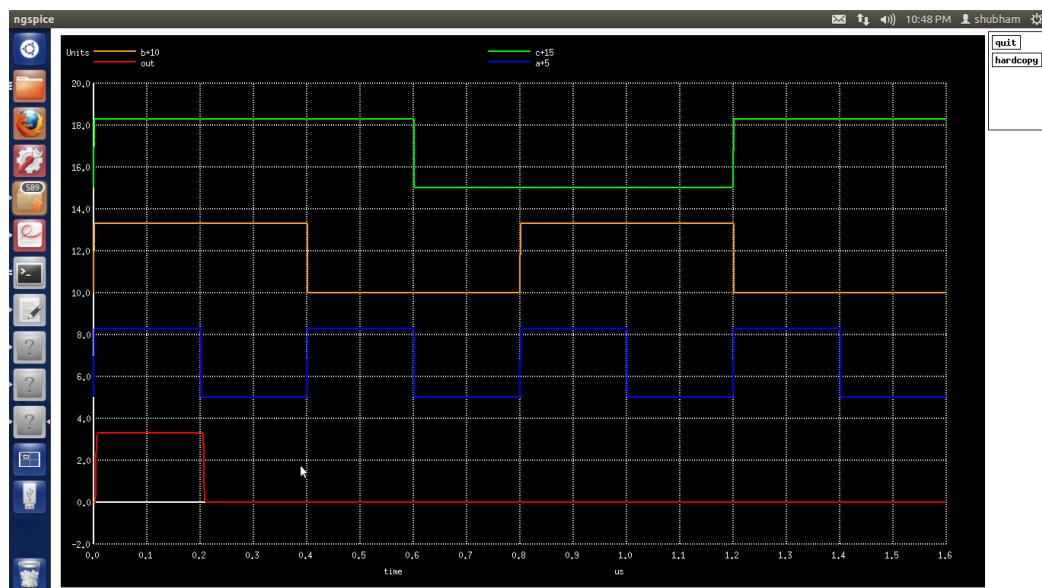


Figure 96: simulation results for CMOS 3 input NAND gate

Layout design for CMOS 2 input NOR gate

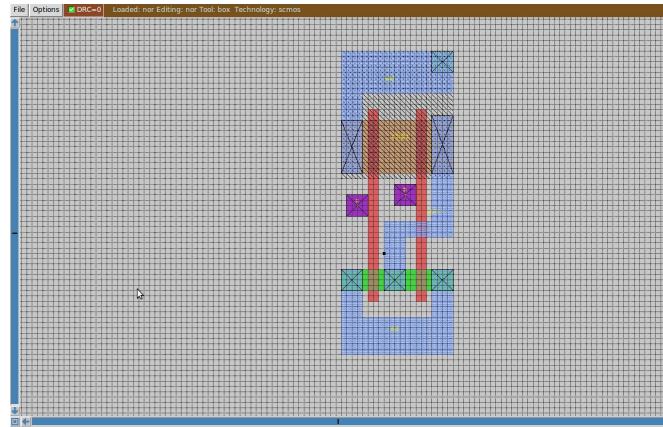


Figure 97: Layout design for CMOS 2 input NOR gate

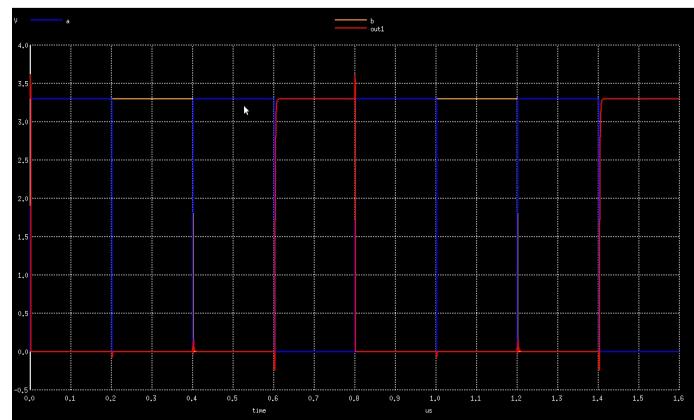


Figure 98: simulation results for CMOS 2 input NOR gate

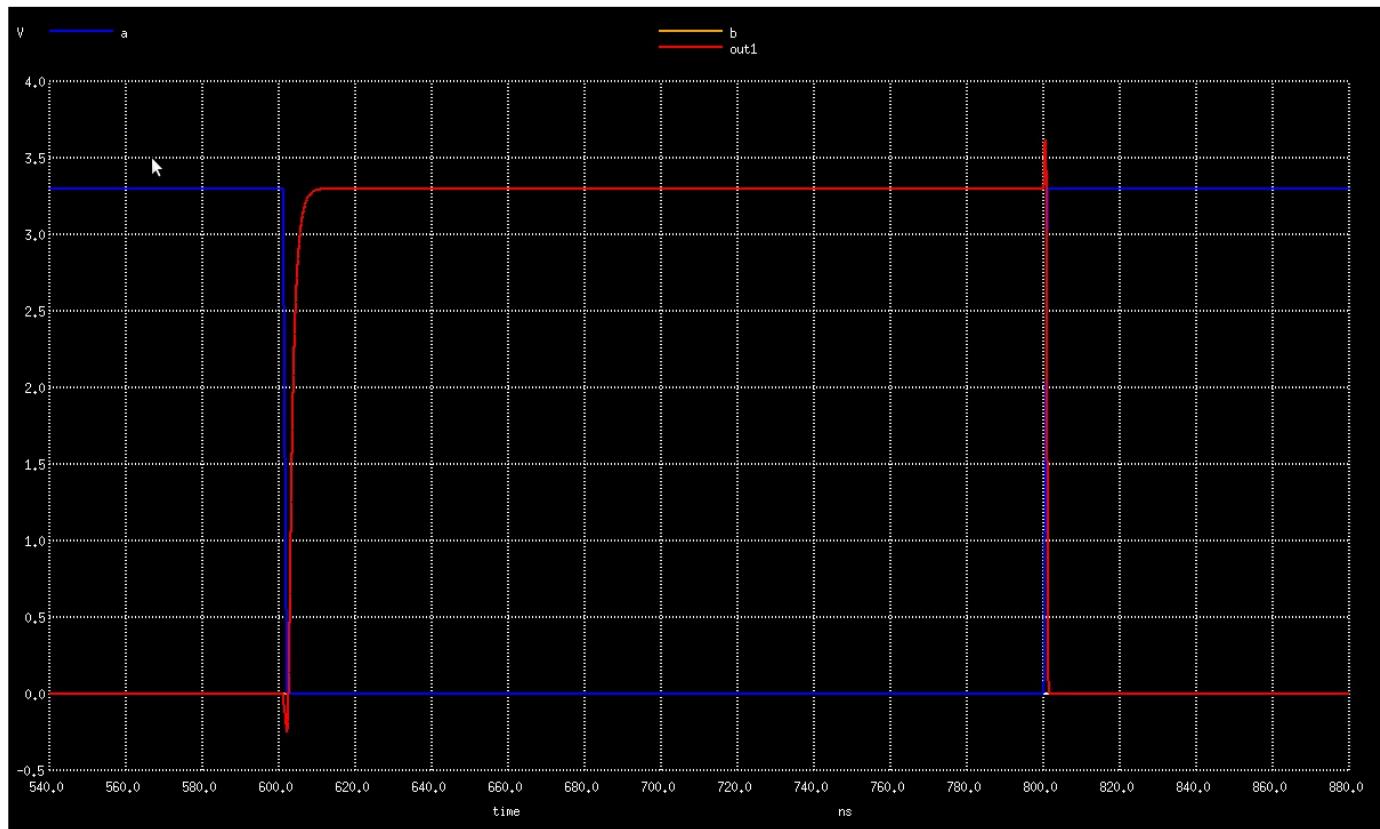


Figure 99: Rise Time for CMOS 2 input NOR gate

Layout design for CMOS 3 input NOR gate

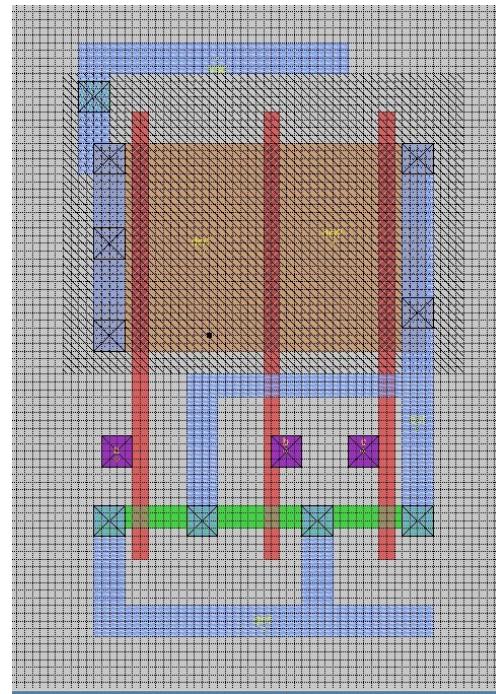


Figure 100: Layout design for CMOS 3 input NOR gate

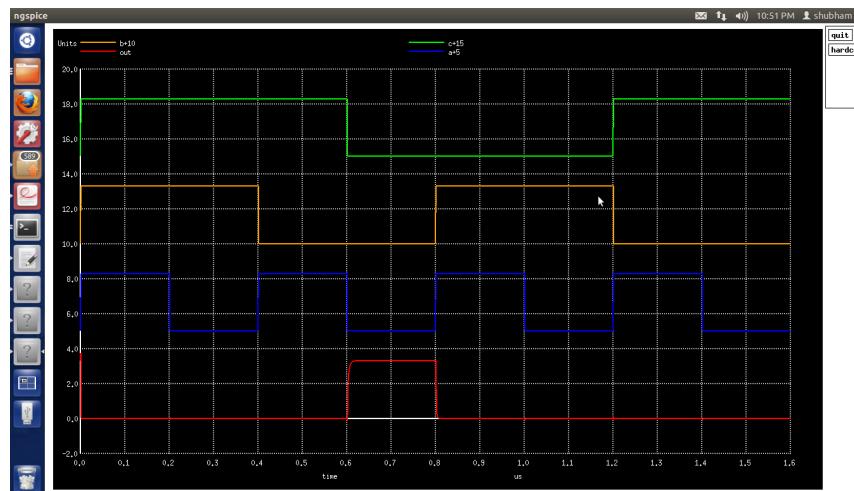


Figure 101: simulation results for CMOS 3 input NOR gate

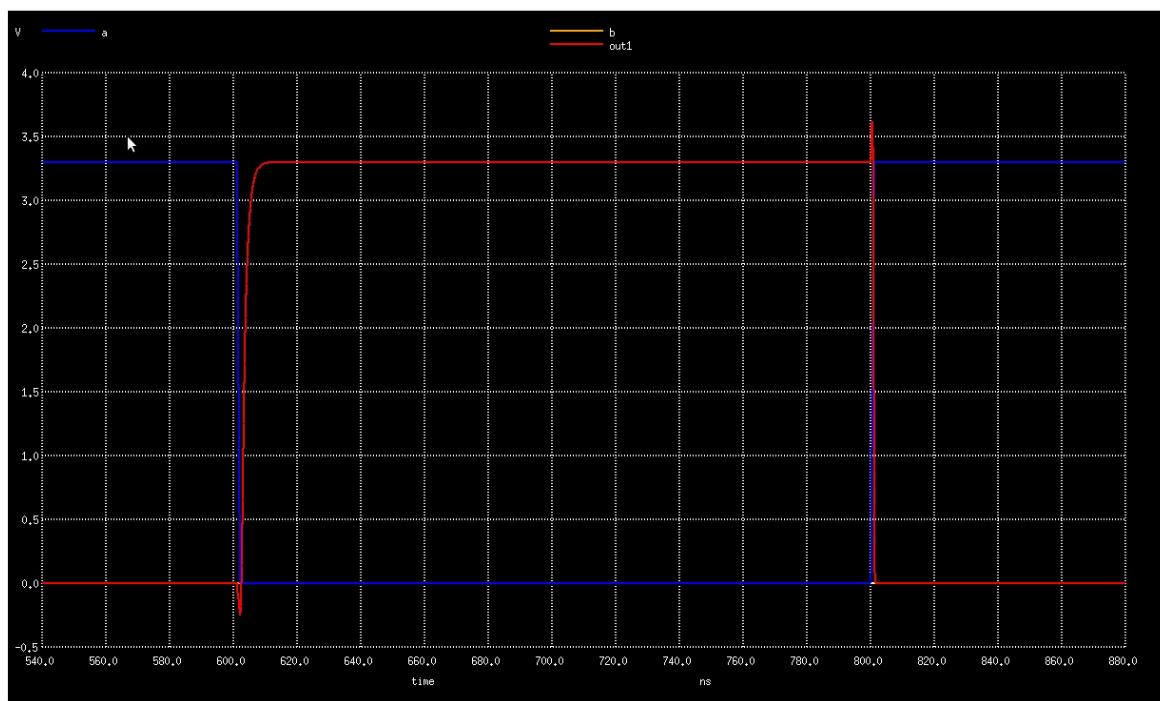


Figure 102: Rise Time for CMOS 3 input NOR gate

Layout design for CMOS 3 input XOR gate

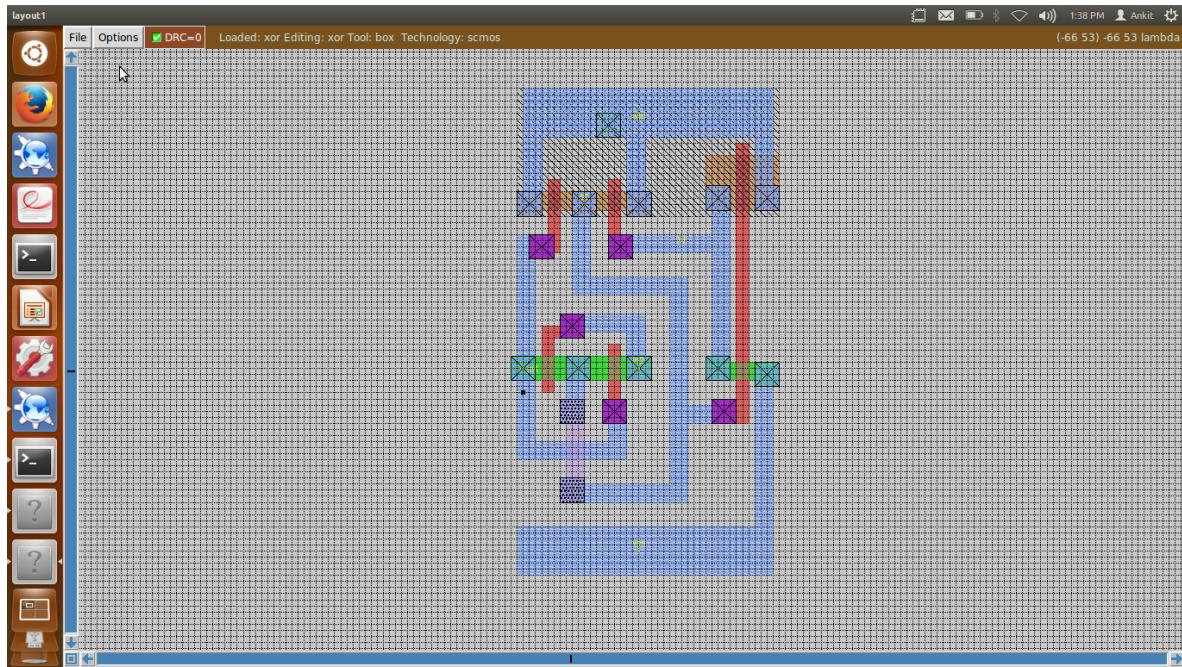


Figure 103: Layout design for CMOS 3 input XOR gate

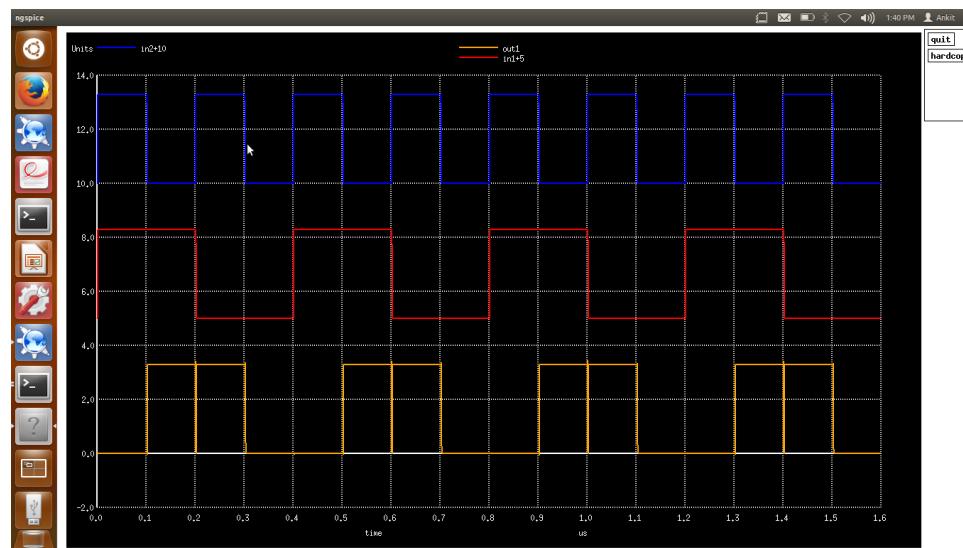


Figure 104: simulation results for CMOS 3 input XOR gate

Layout design for Transmission gate

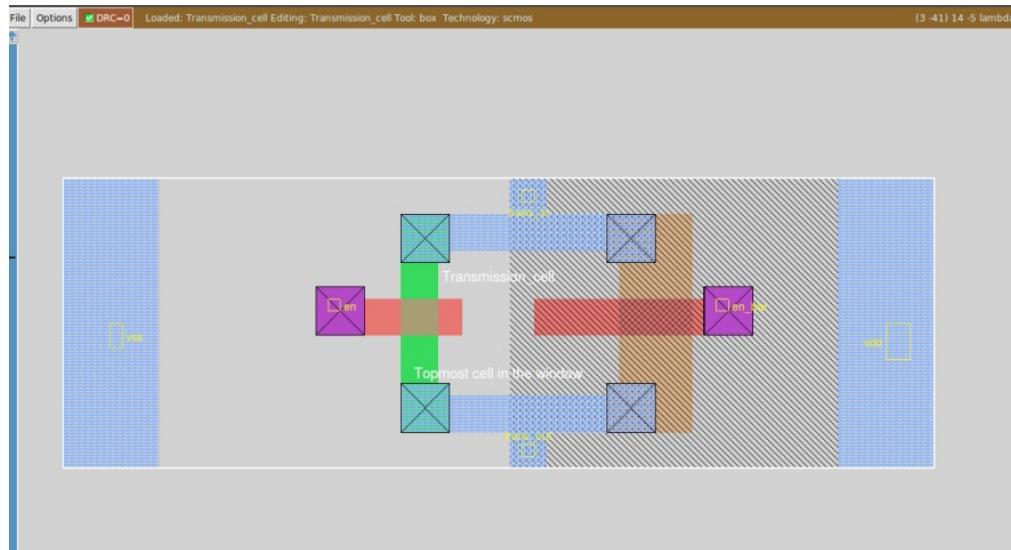


Figure 105: Layout design for Transmission gate

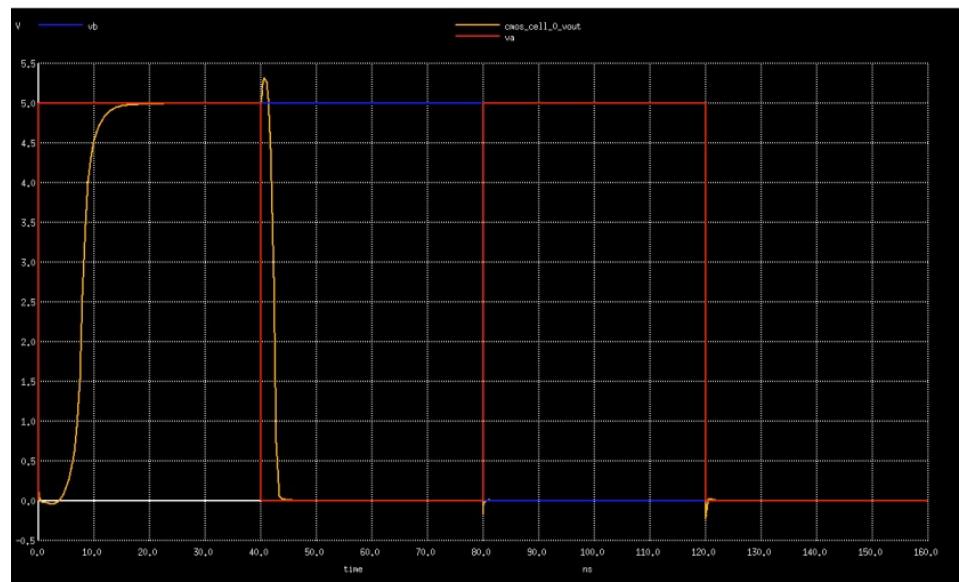


Figure 106: Simulation Results for Transmission gate

Layout designs for function $ab+c$ using CMOS and Pseudo NMOS

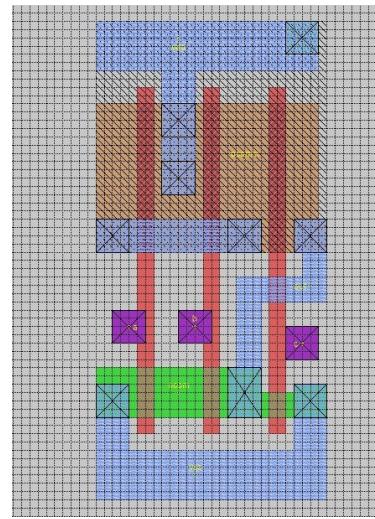


Figure 107: Layout design for $ab+c$ CMOS design

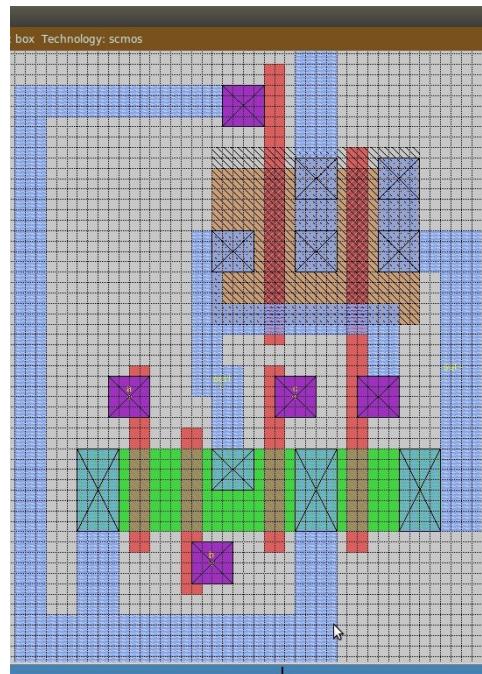


Figure 108: Layout design for $ab+c$ pseudo NMOS

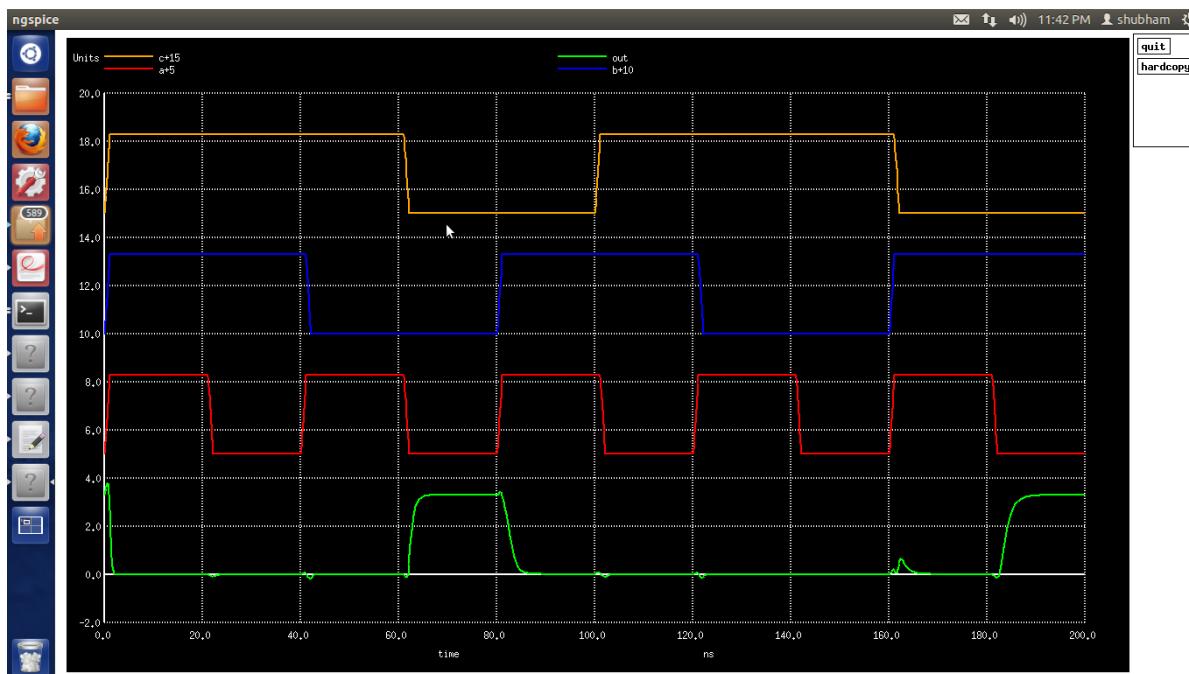


Figure 109: Simulation for ab+c pseudo NMOS

Layout design for D - Latch

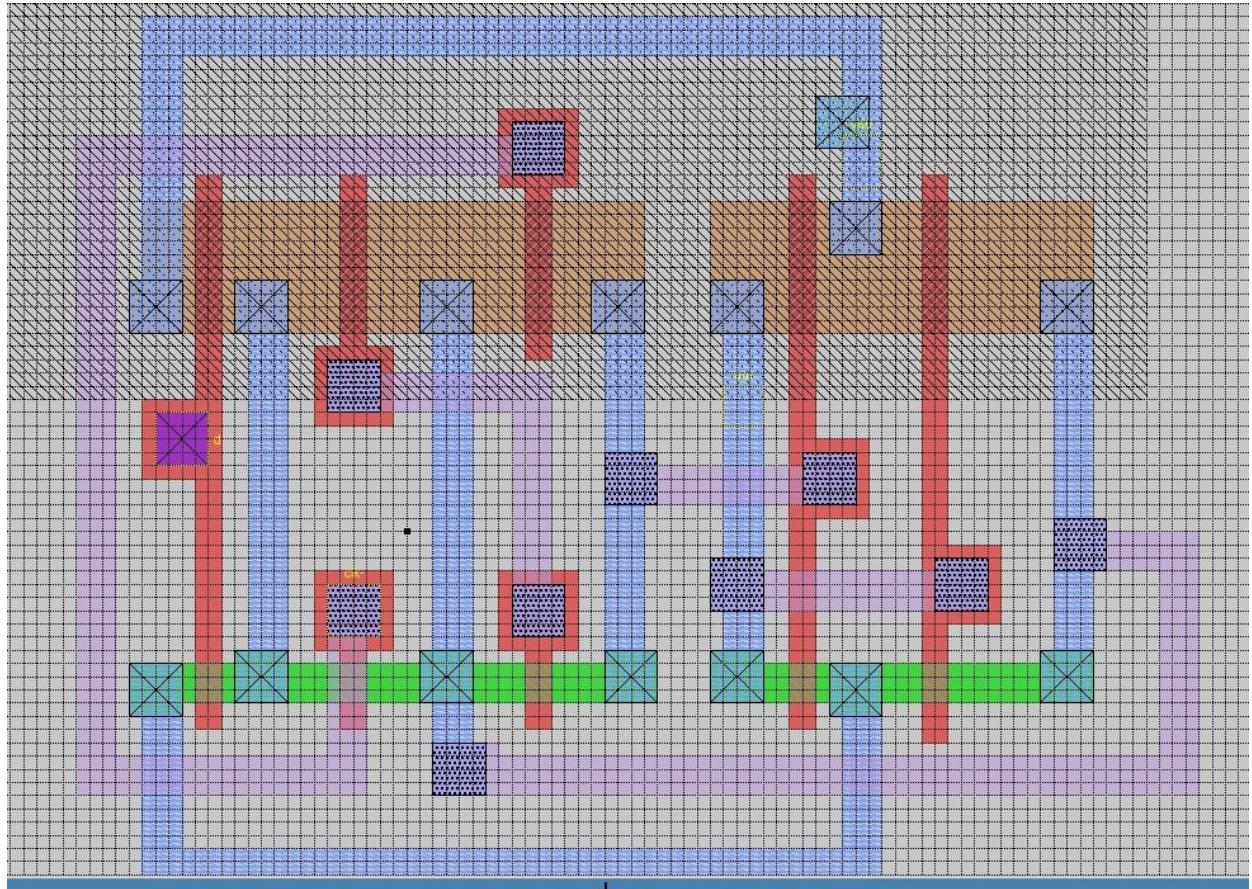


Figure 110: Layout design for D - Latch

Layout Design for 2:1 Mux

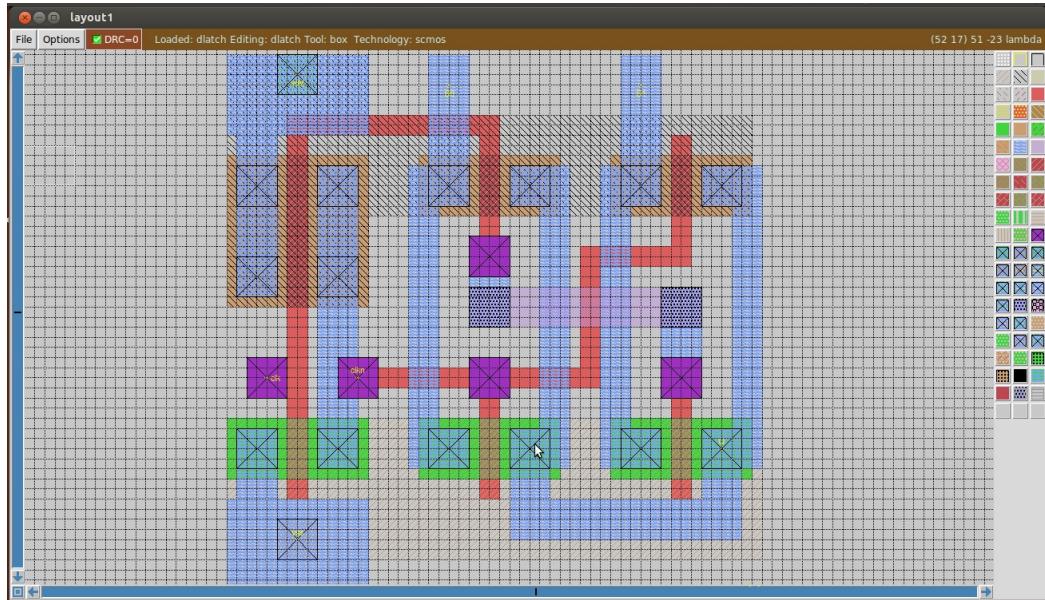


Figure 111: Layout design for 2:1 Multiplexer

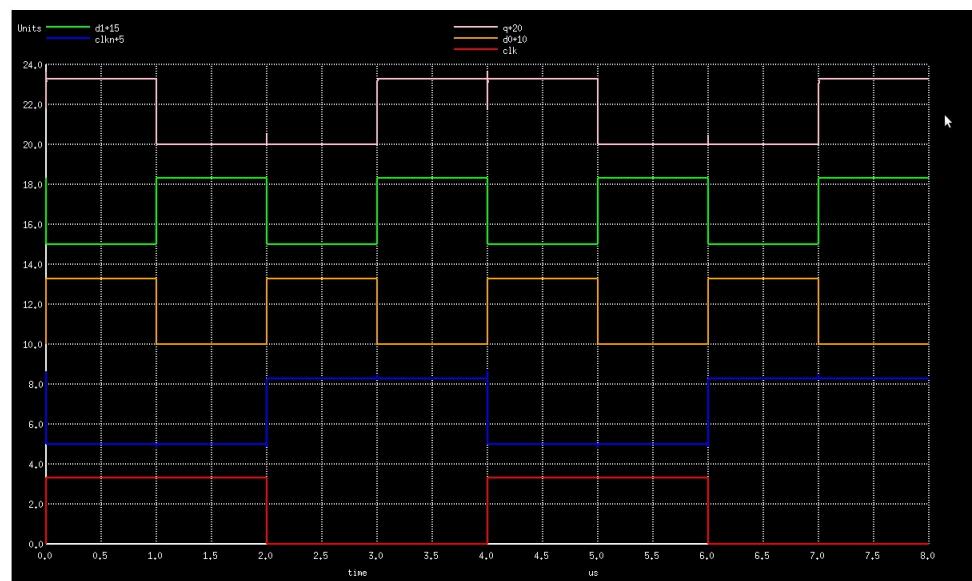


Figure 112: Simulation for 2:1 Multiplexer

Layout Design for 4:1 Mux

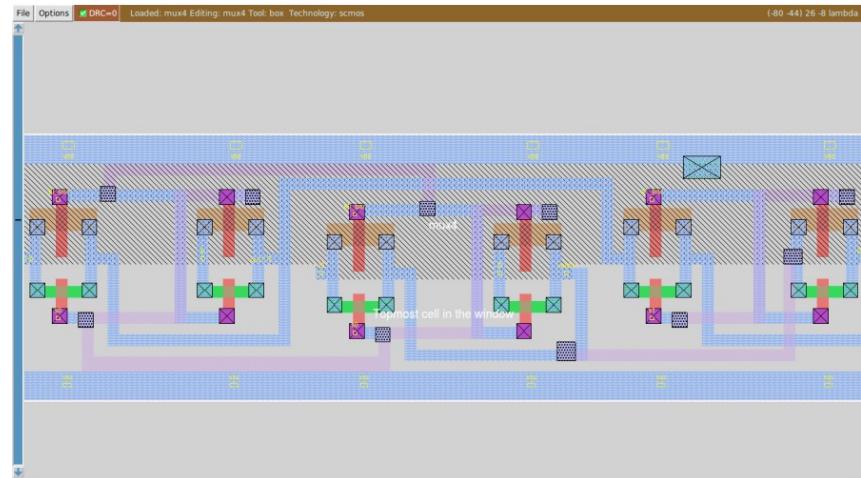


Figure 113: Layout design for 4:1 Multiplexer

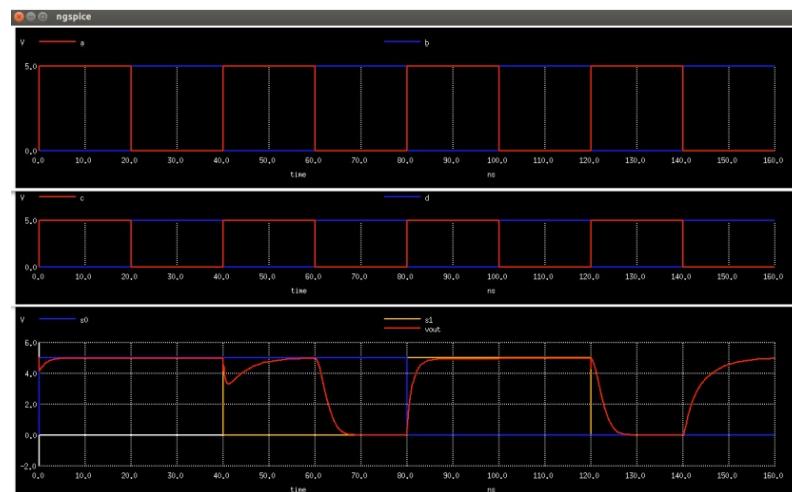


Figure 114: Simulation for 4:1 Multiplexer