VLSI DESIGN LAB

MODULE 1 REPORT : CIRCUIT SIMULATION WITH NGSPICE

Submitted by :

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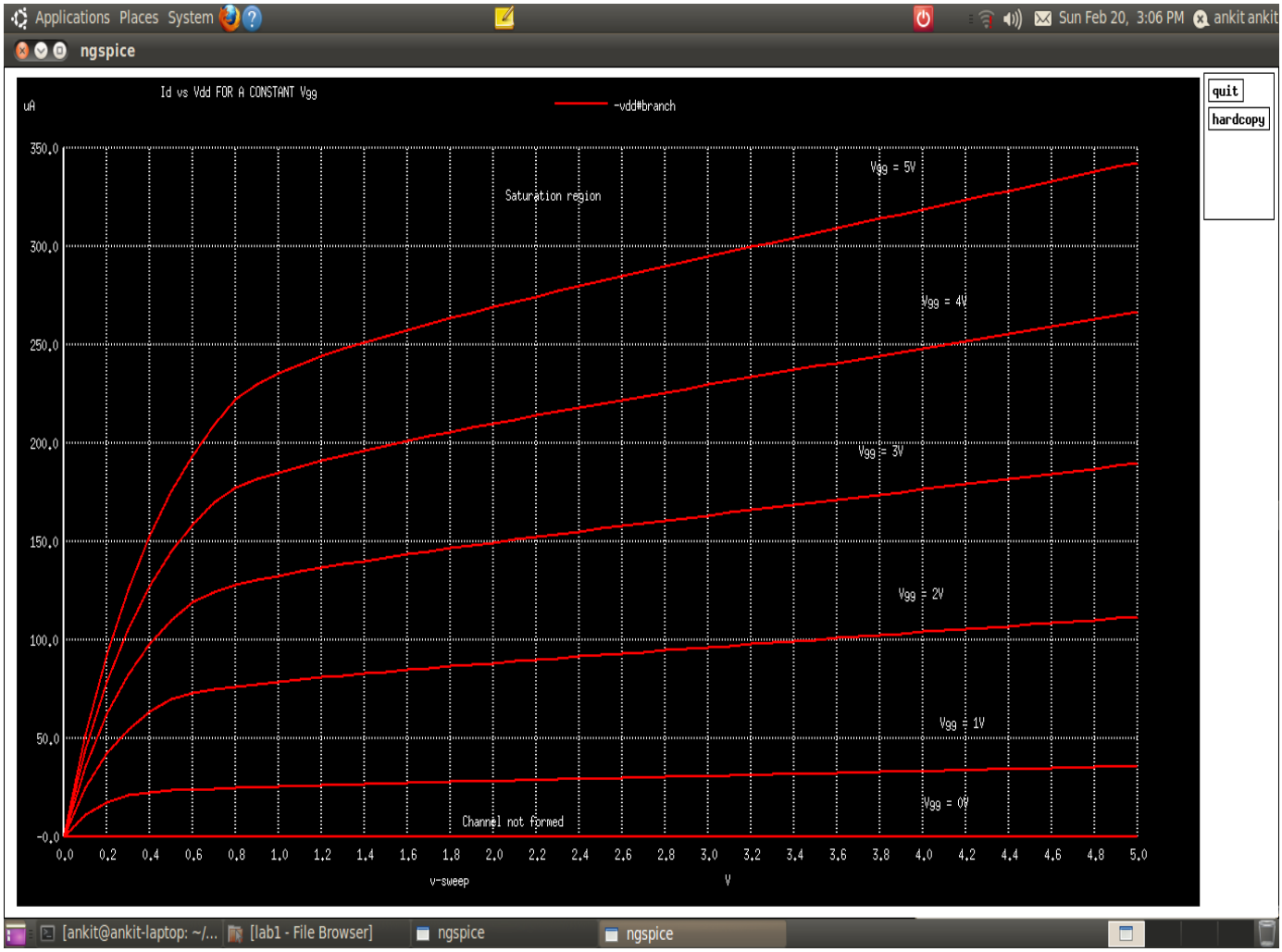
Lab 1:

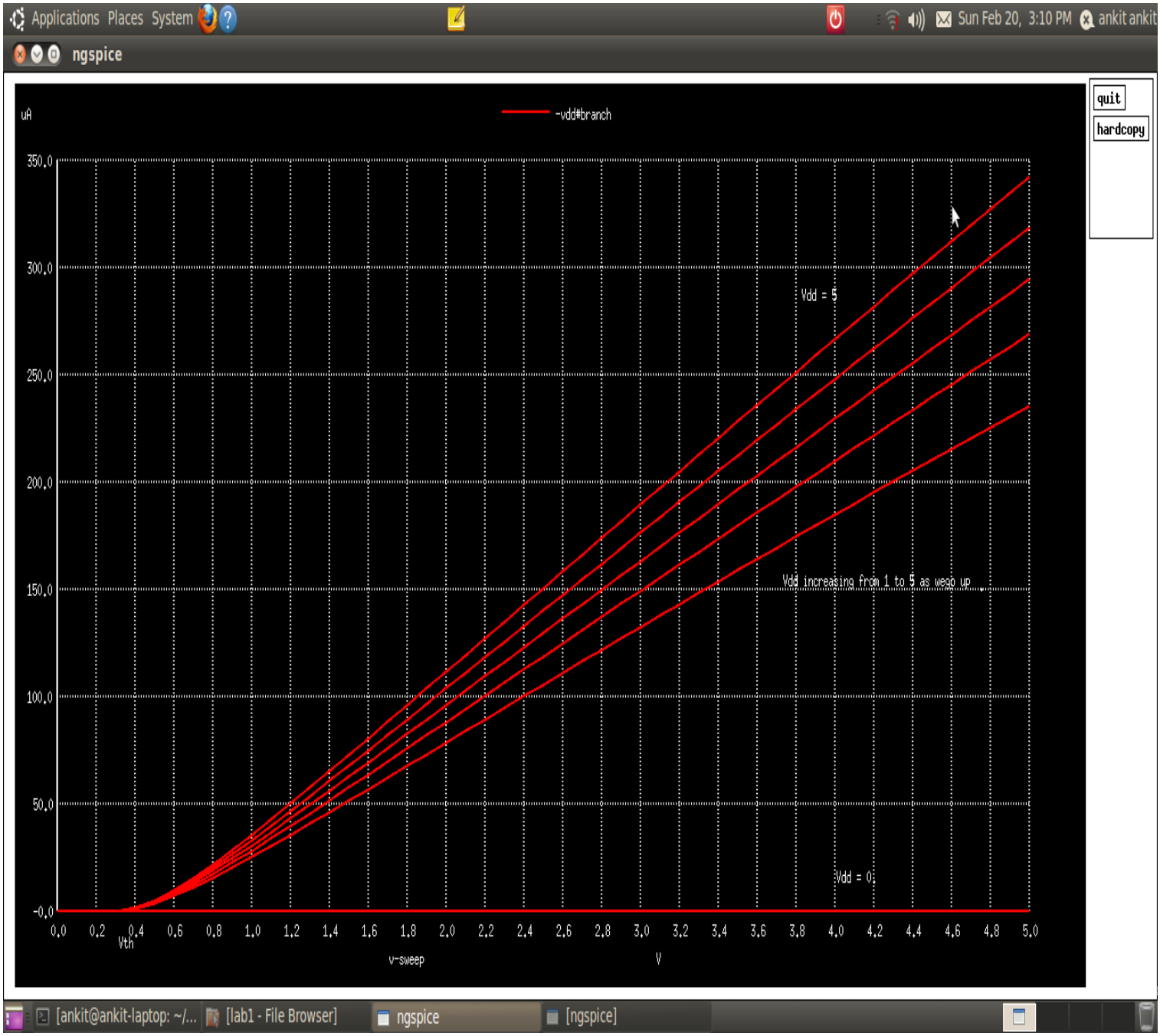
Study the input and output characteristic of NMOS transistor. effect of length ,width ,Vto ,Vsb ,lambda , and temperature on the behavior of transistor.

*Id vs Vdd:



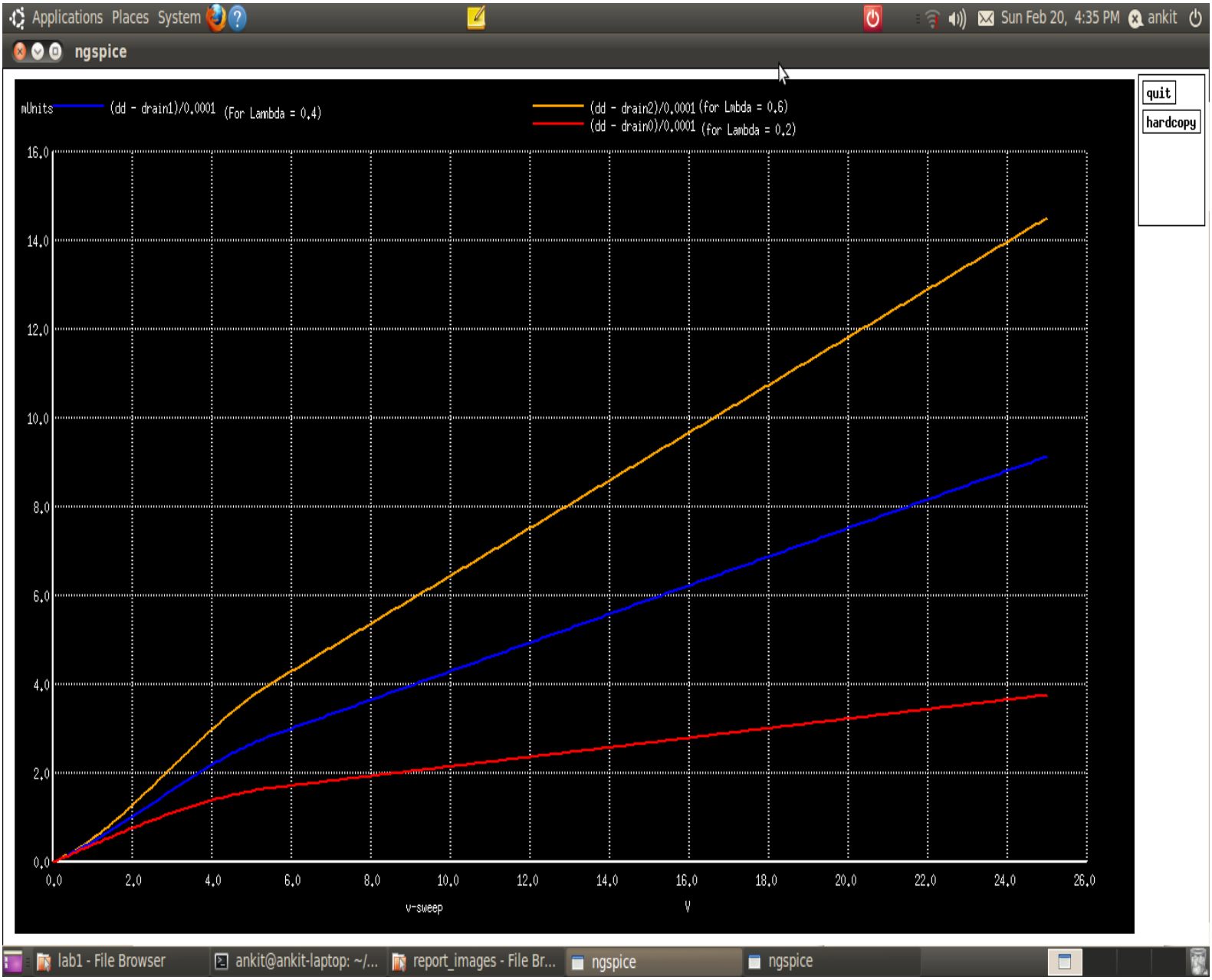
The id vs Vdd curve is at first linear then becomes varies slowly in saturation region due to channel length modulation which should be otherwise constant.

*Id vs Vgg:



Initially the current is zero as the channel is not formed. This is till Vgs crosses the threshold voltage.Then the current varies almost linearly

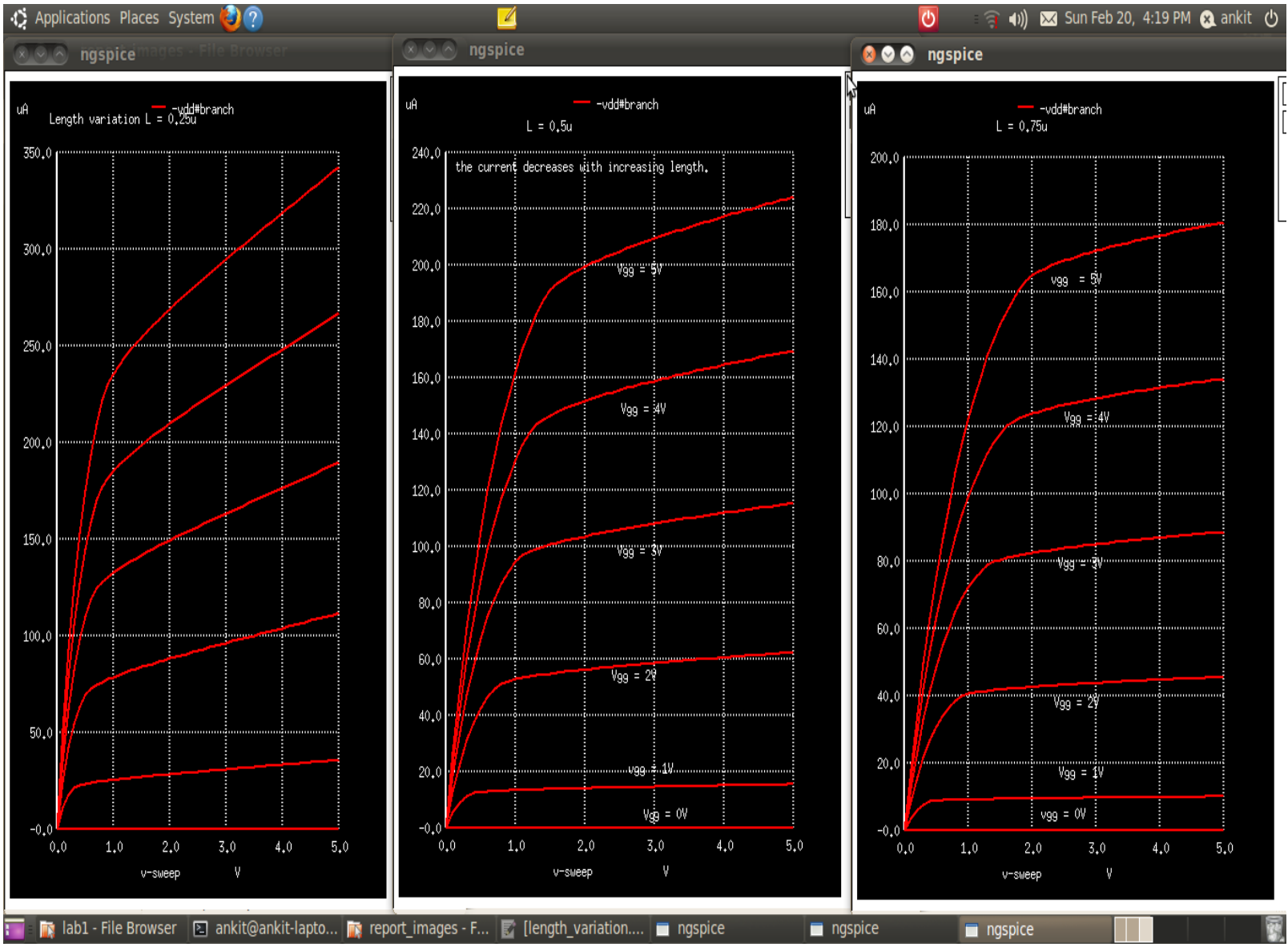
Lambda variation : Id vs Vdd



The current for different values of lambda . The variation is due to the (1 + lambda*Vds) factor in the expression of the current.

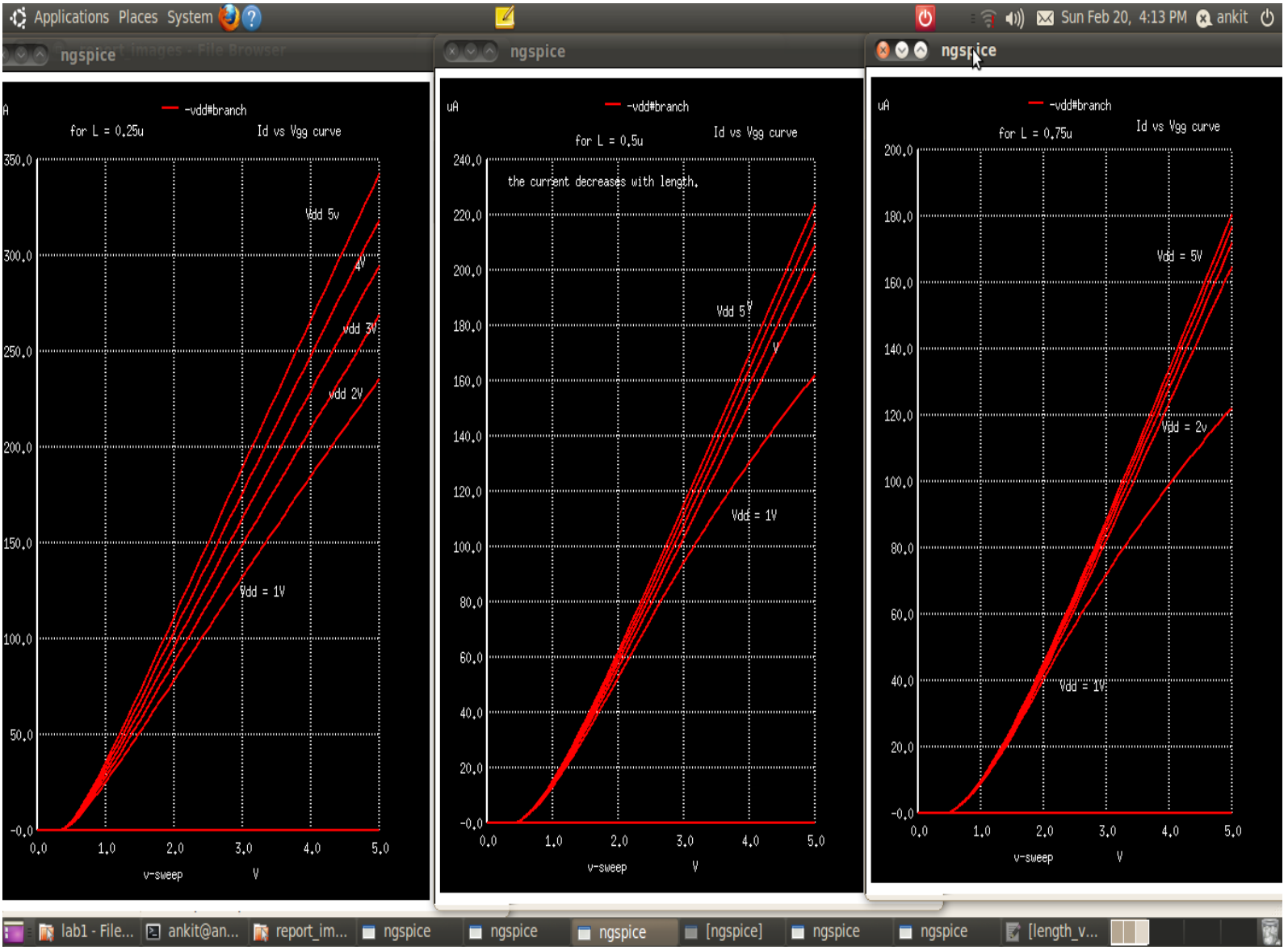
Lambda variation : Id vs Vgg

Length variation : Id vs Vdd:



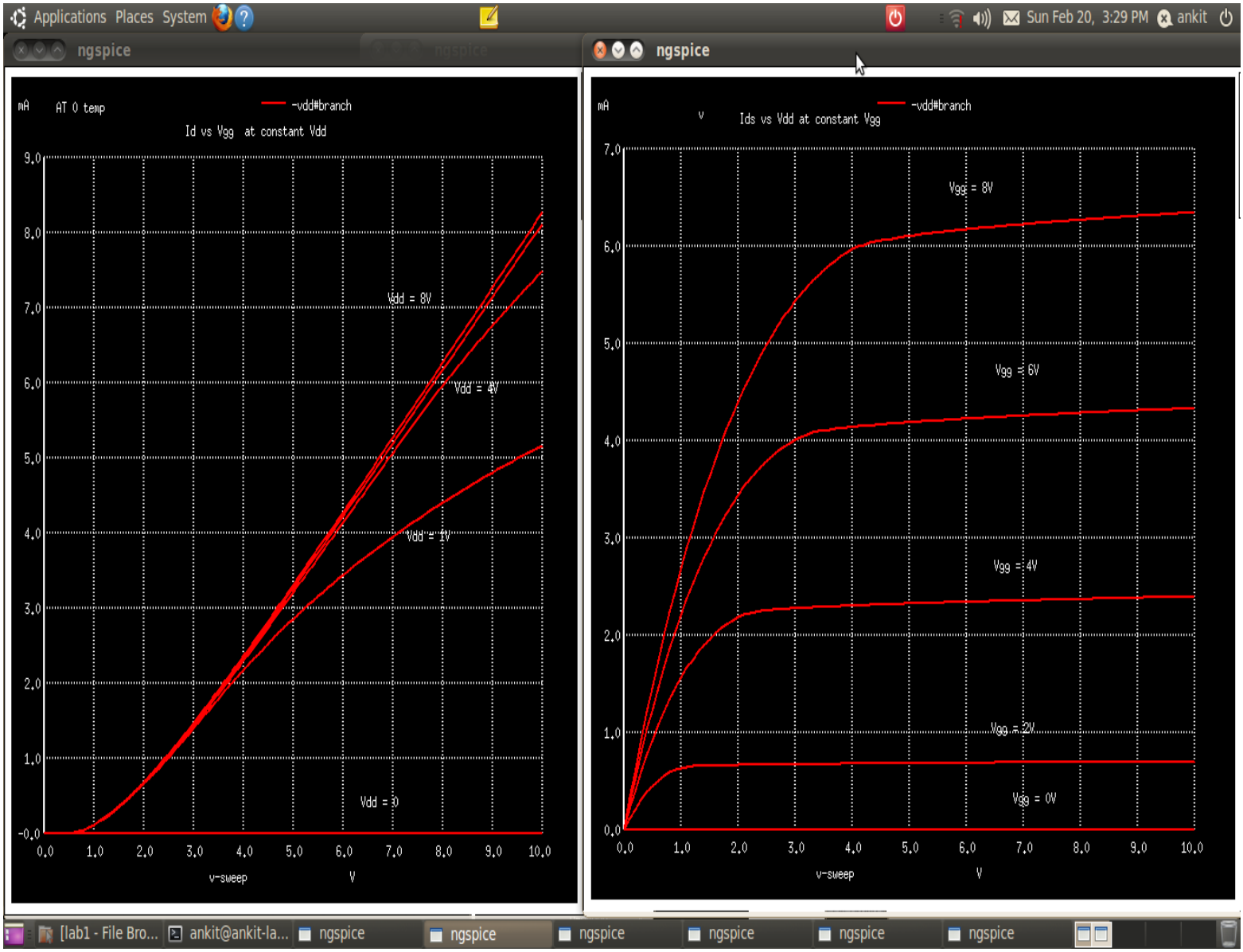
When Vgg is more than Vth, the current varies as shown above with Vdd.If the length parameter is changed then the current decreases with increase in length which can be seen by the values on y-axis.

length variation :



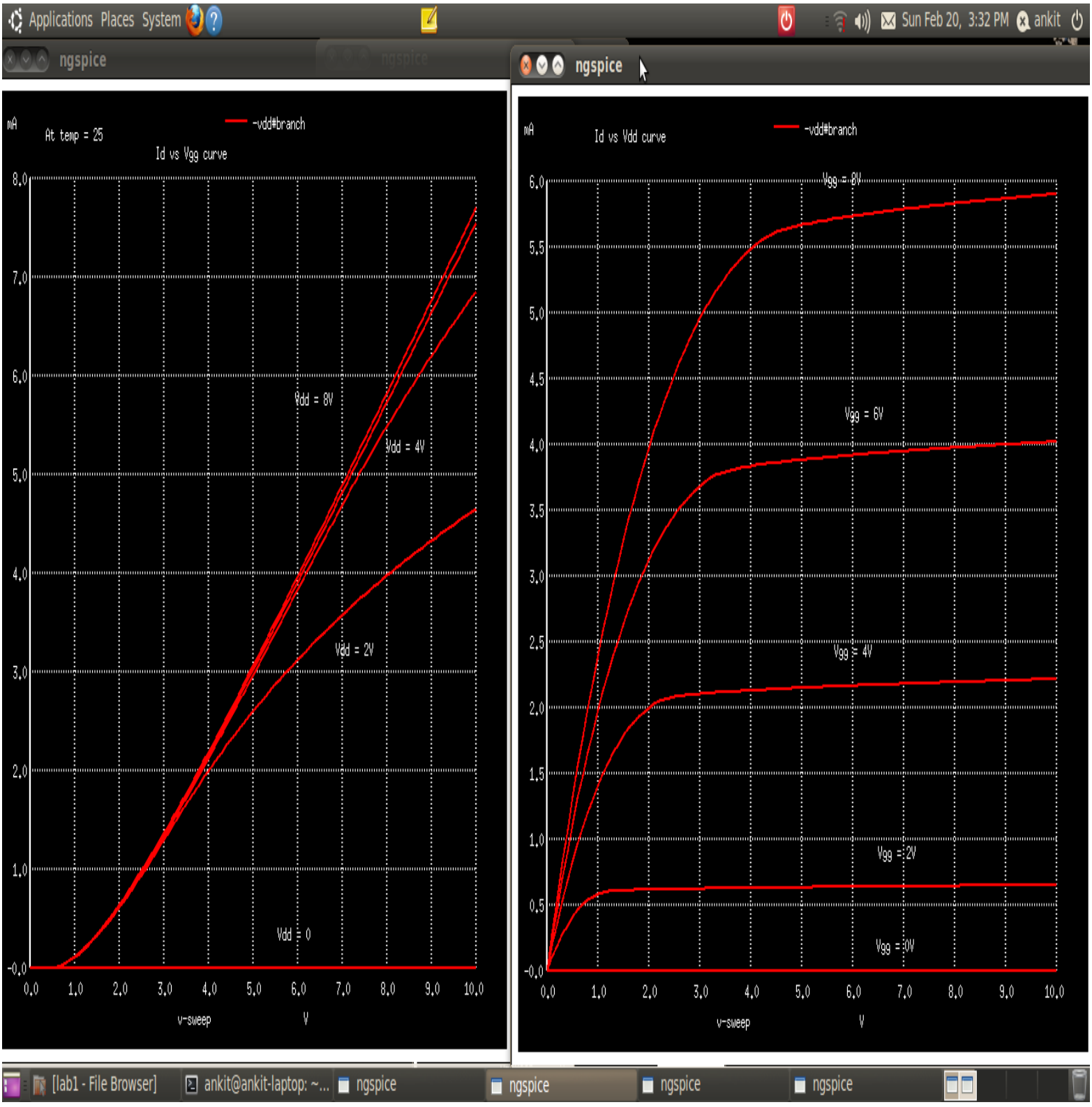
The above curve shows the effect of length variation on current with respect of Vgg for a constant value of Vdd.

Temperature variation :

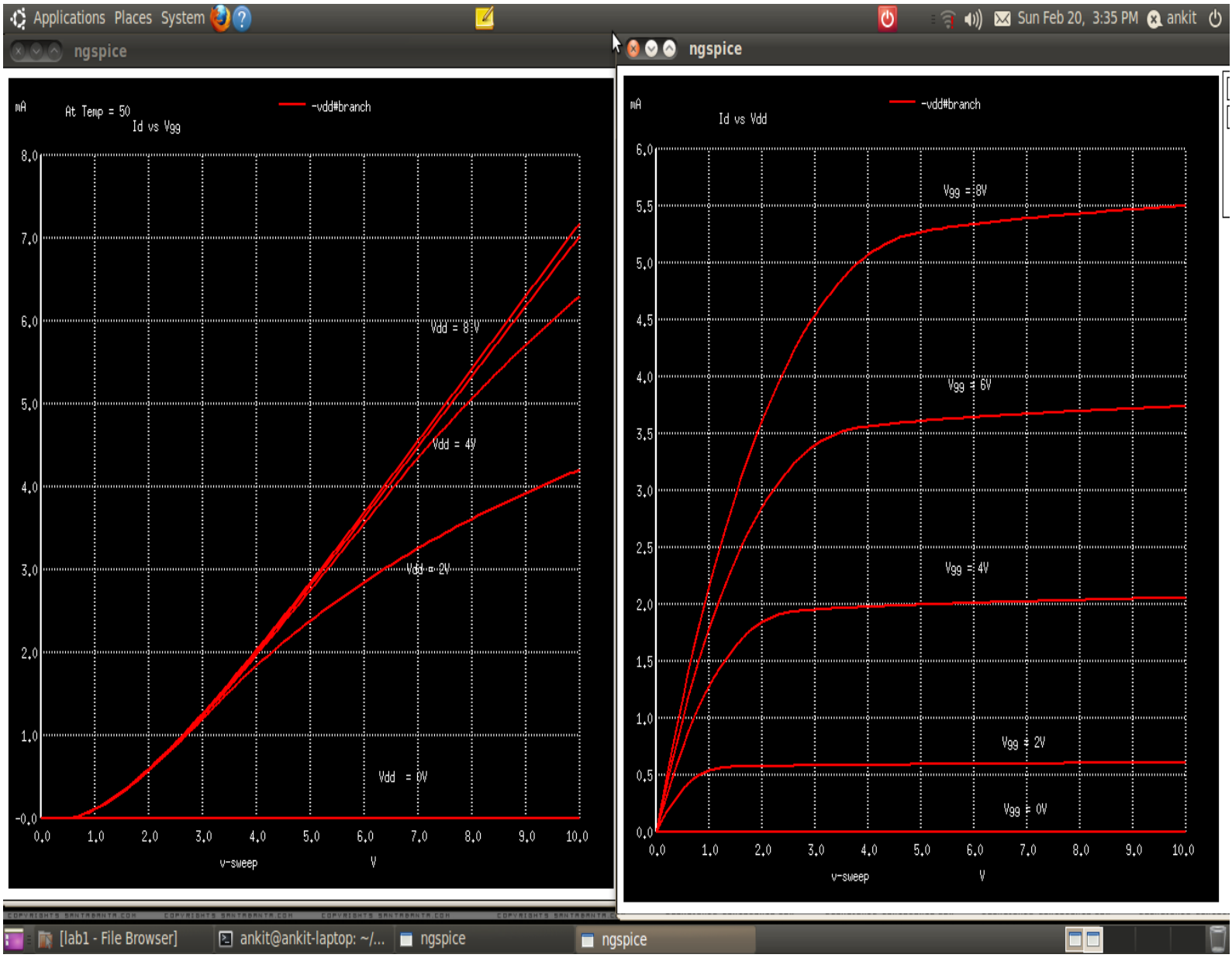


The above curve shows the variation of current with Vgg and Vdd at temperature of 0.

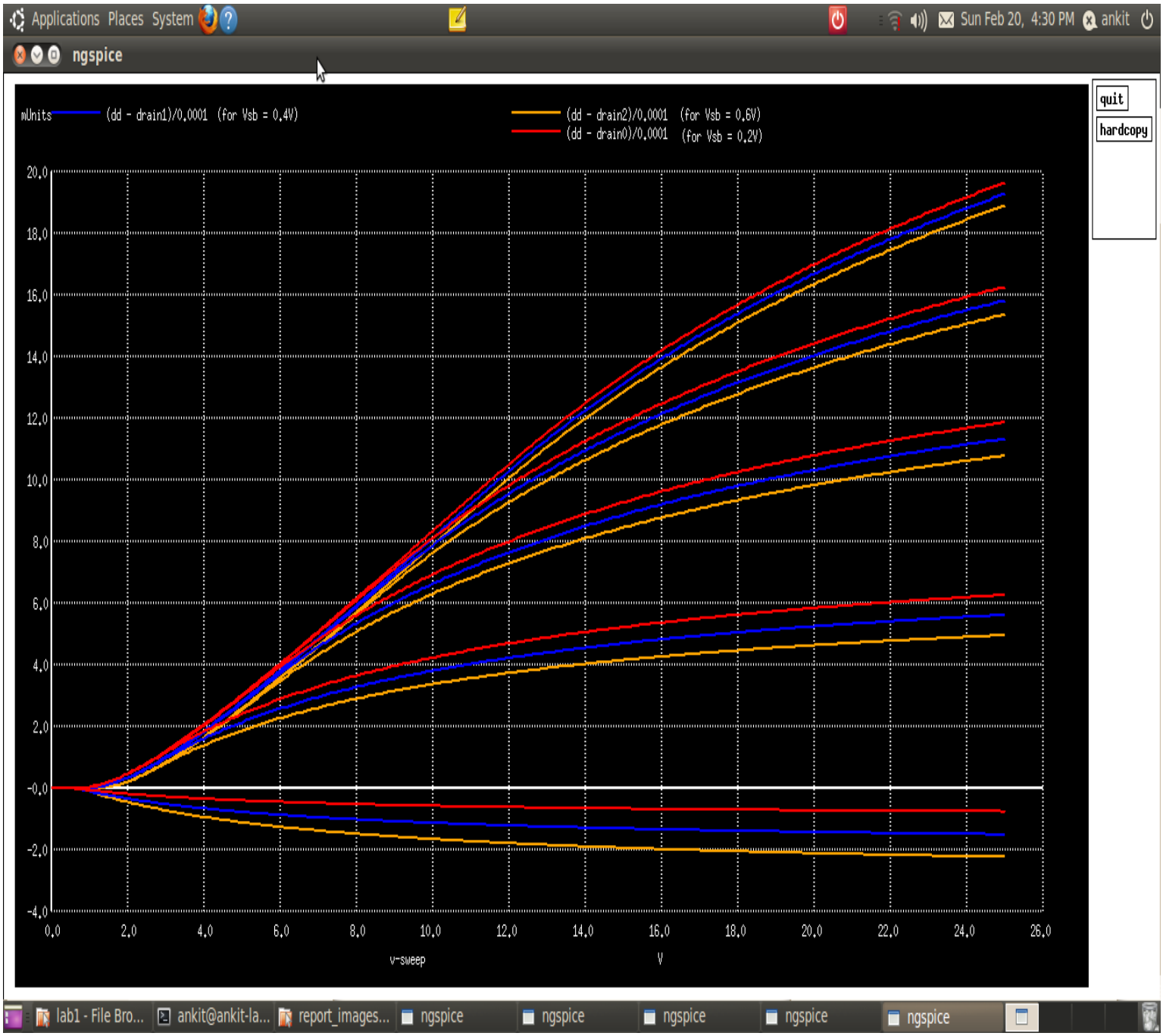
Temperature Variation: at temp = 25



Temperature variation : at temp = 50

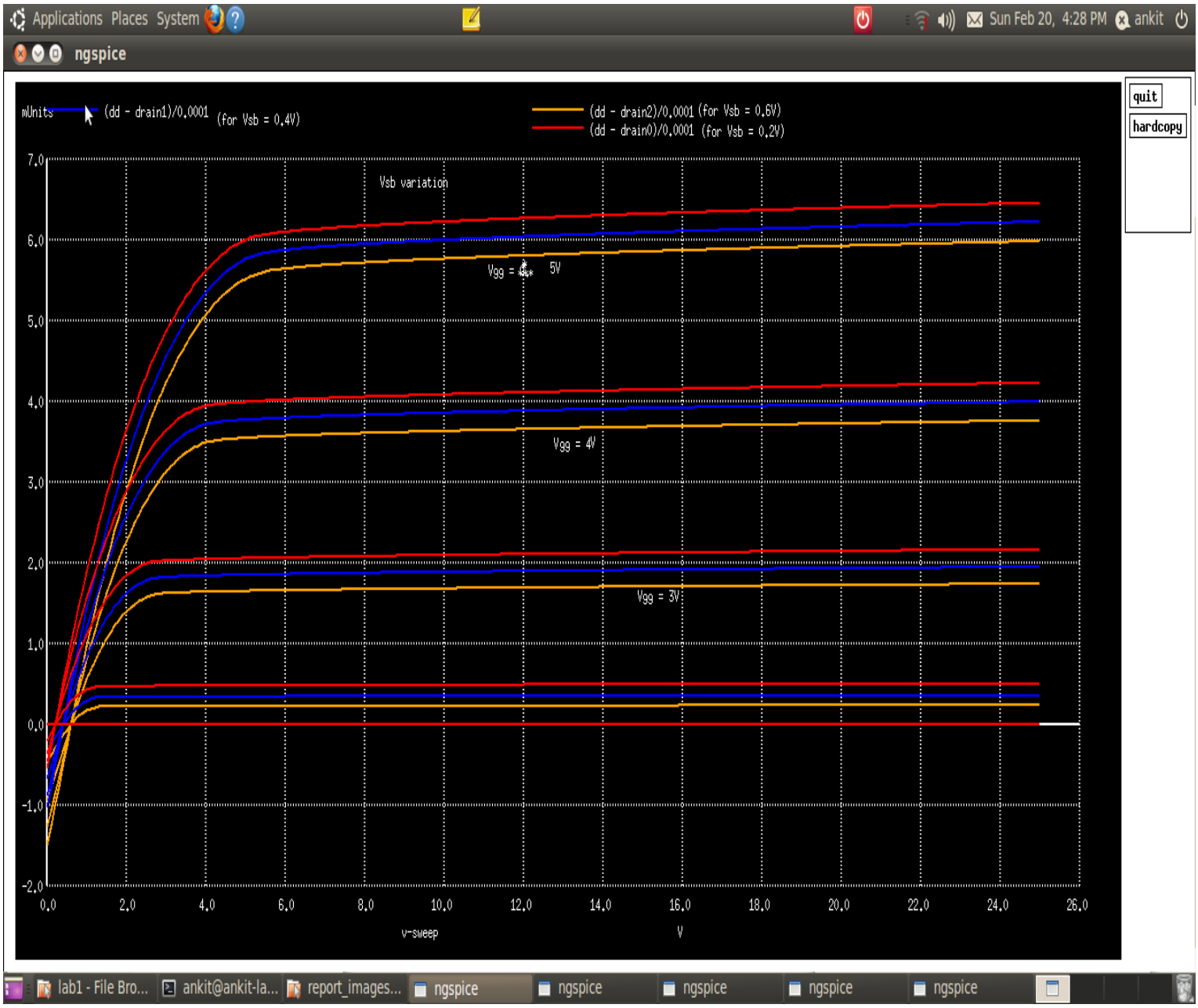


Vsb variation :



As Vsb increases the threshold voltage increases ,so initially the current is zero till the gate voltage crosses the threshold voltage.

Vsb variation

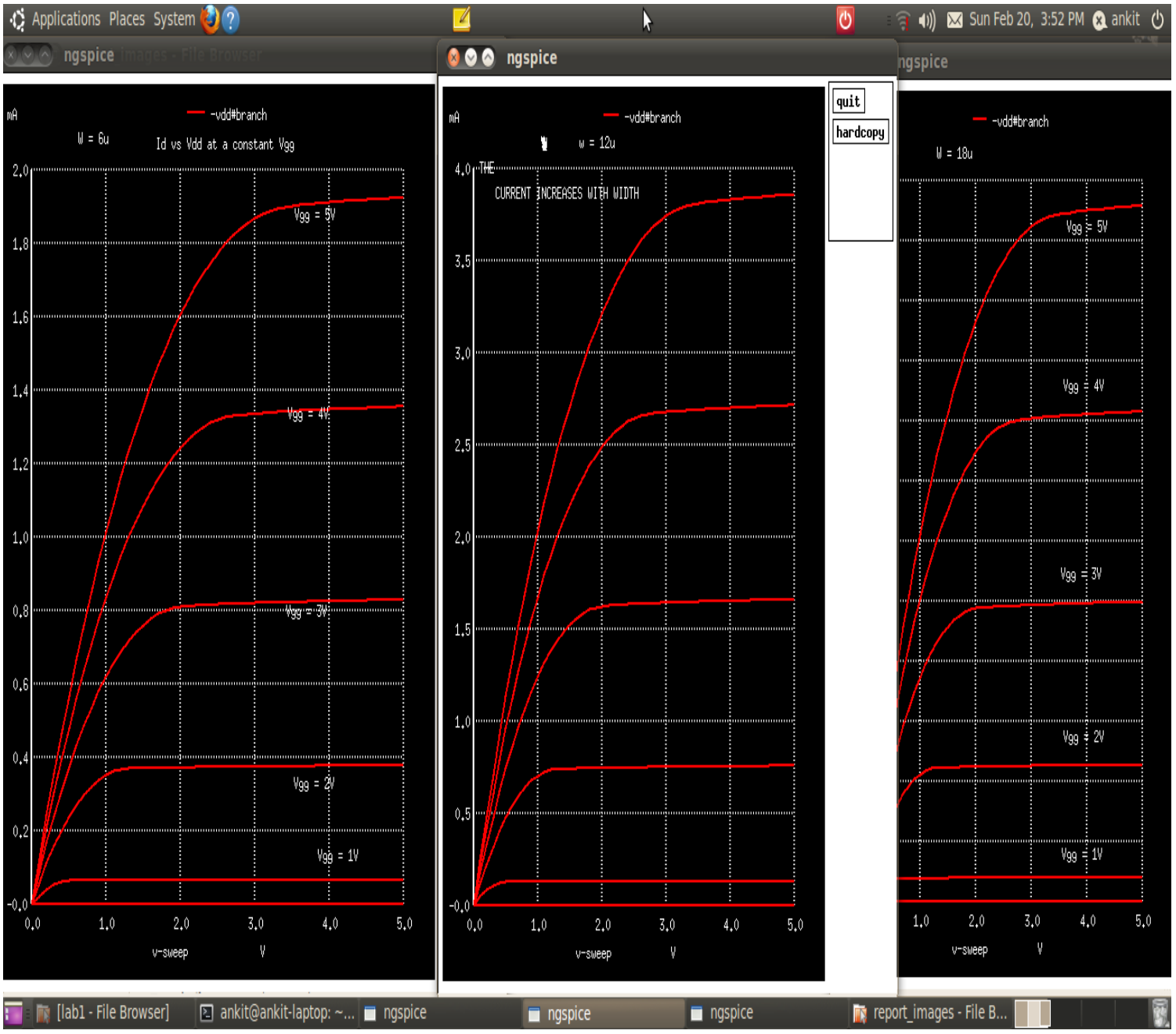


Vto variation :

Since the threshold voltage increases with the increases with the increase in the source to body voltage ,so the current also increases.

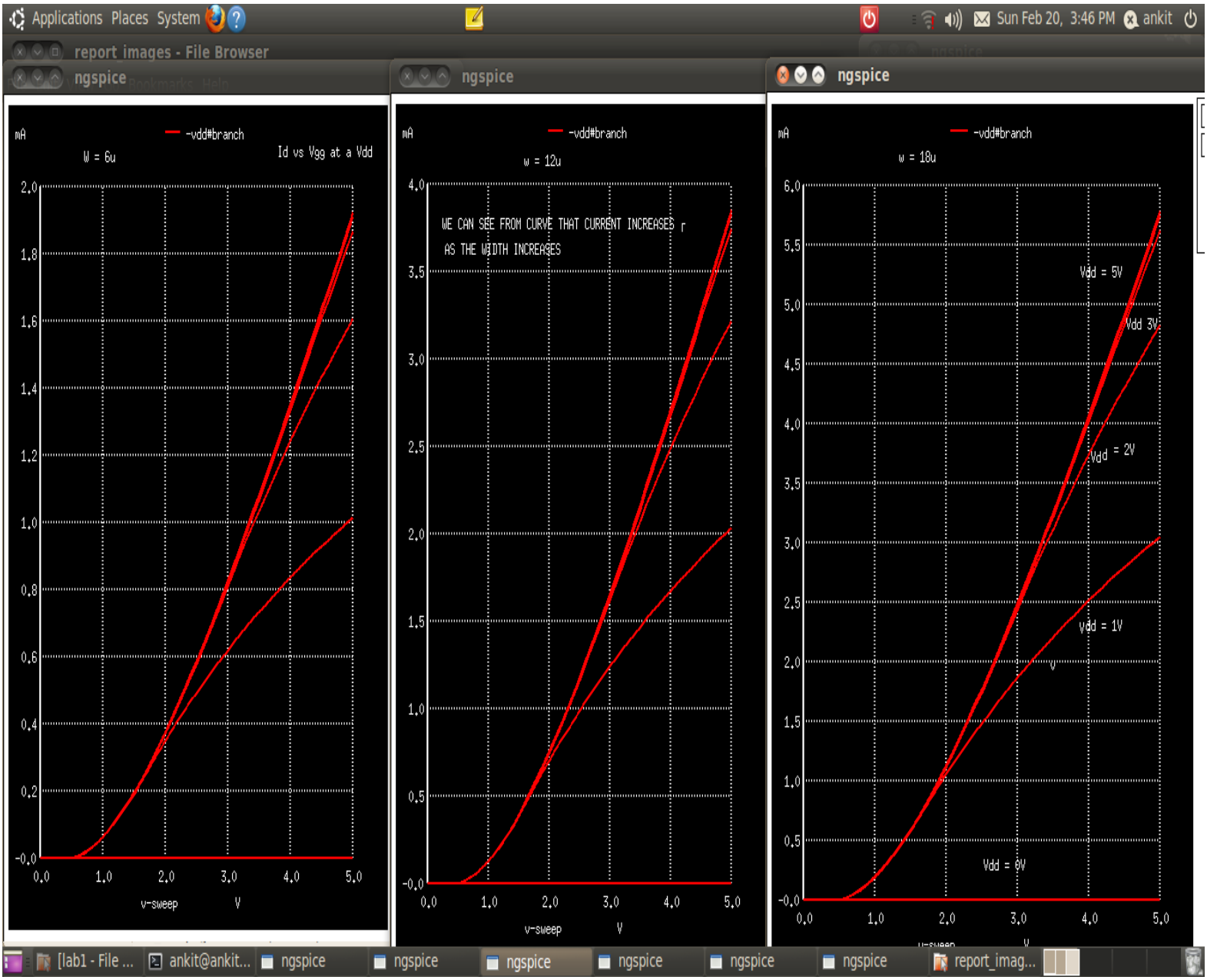
Vto variation :

Width variation :

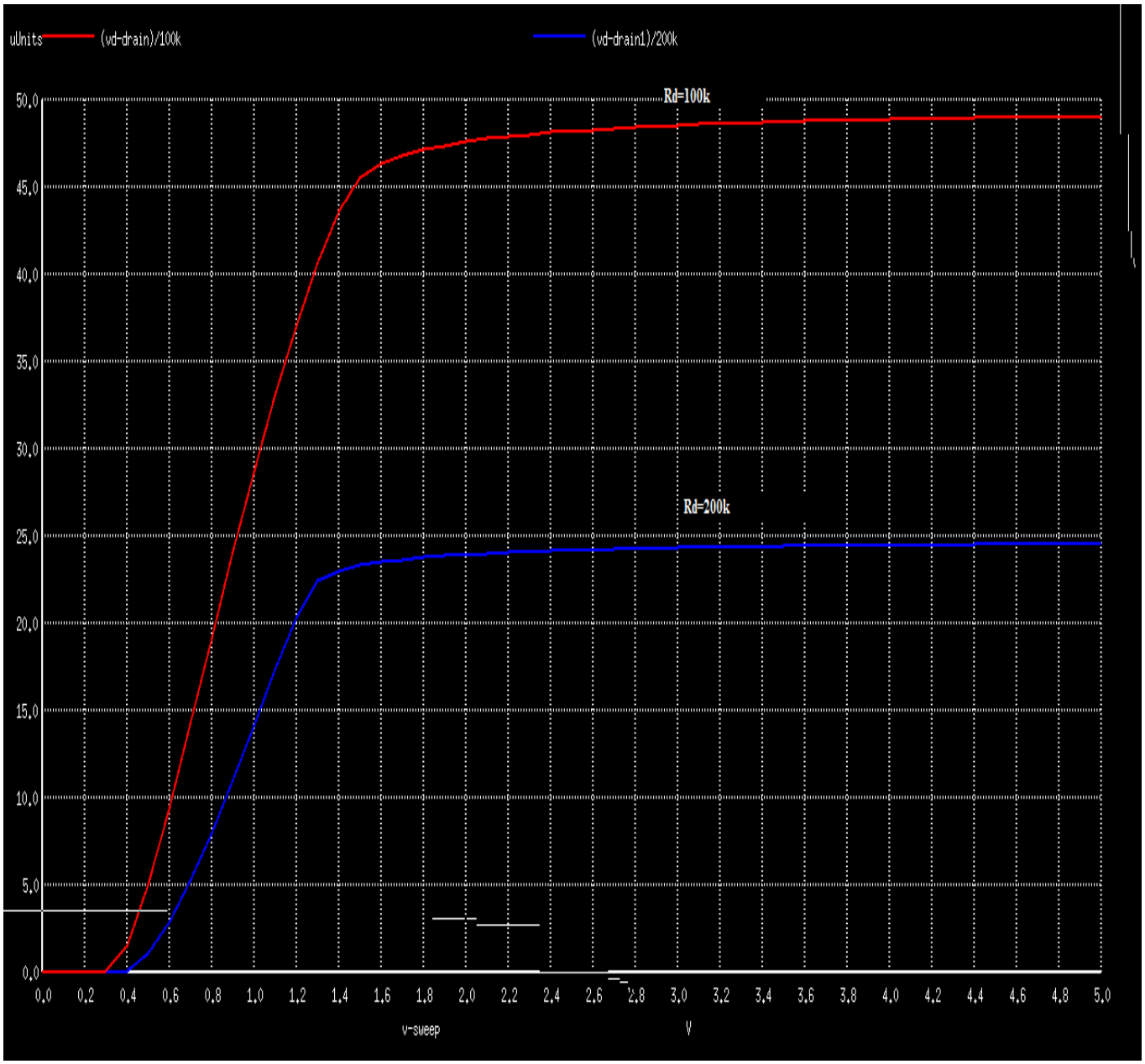


The current increases linearly with the increase in the width parameter.

Width variation :

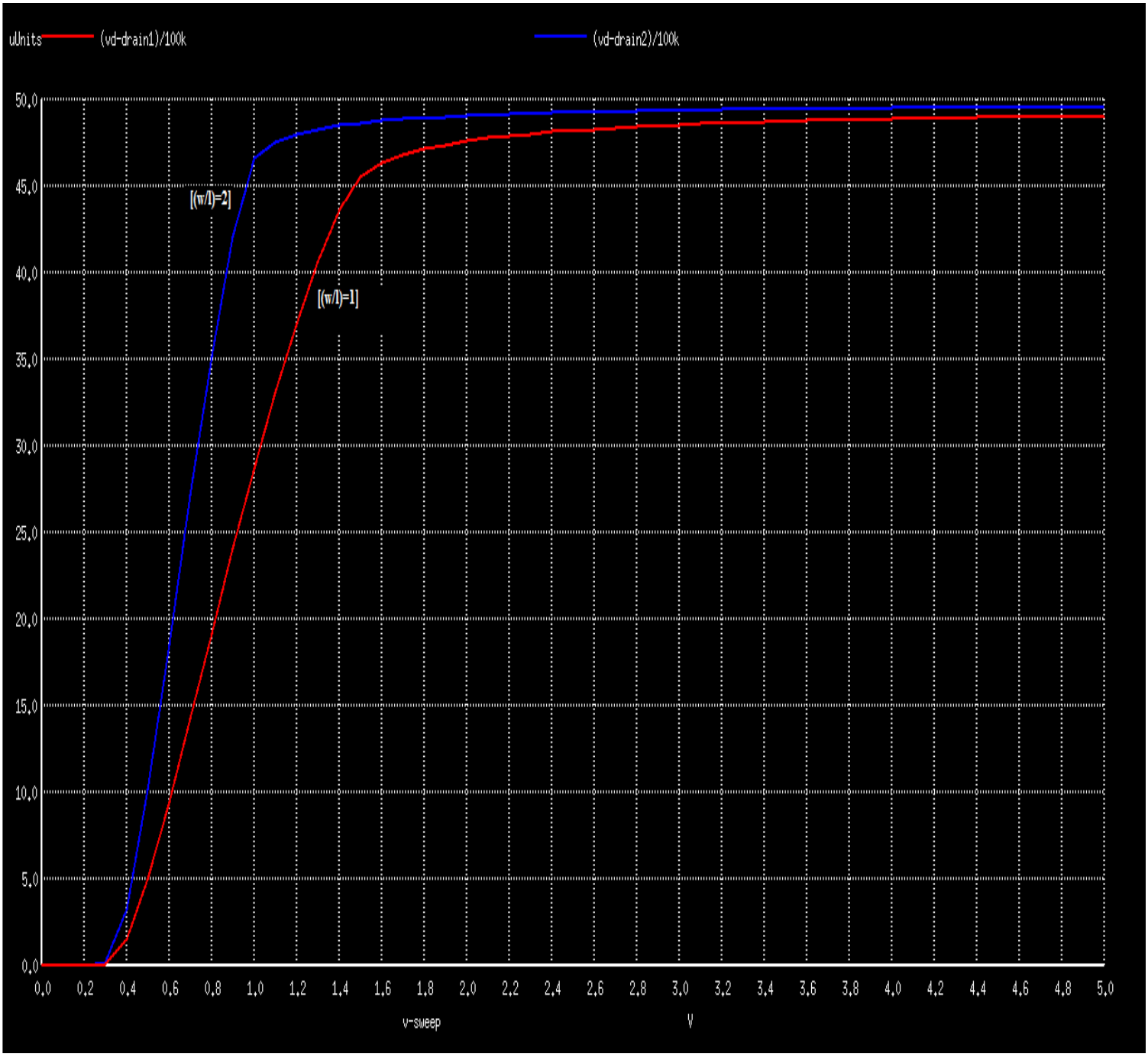


Resistive load inverter:

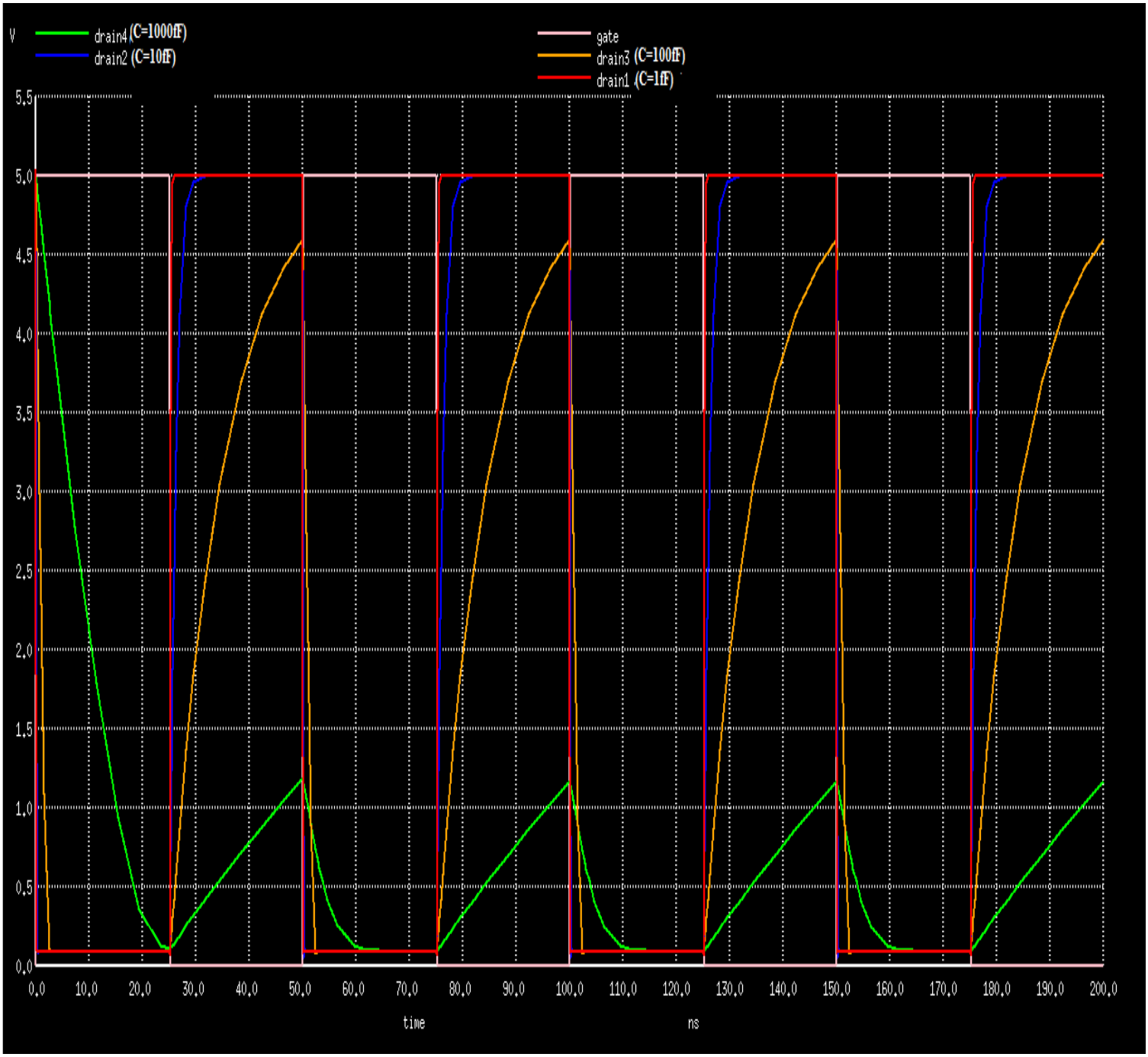


As usual the current decreases with the increase in resistance.

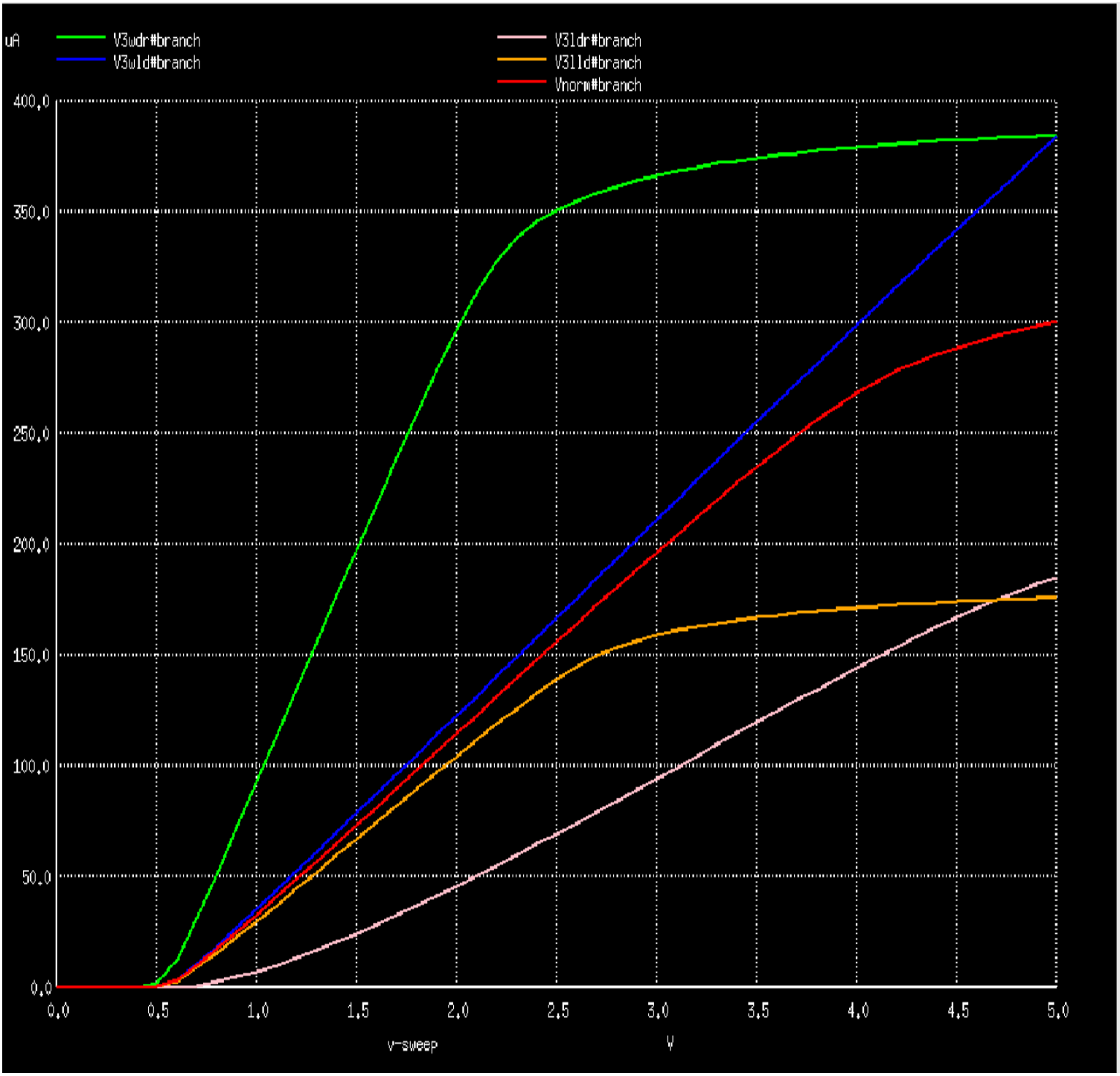
W/L variation



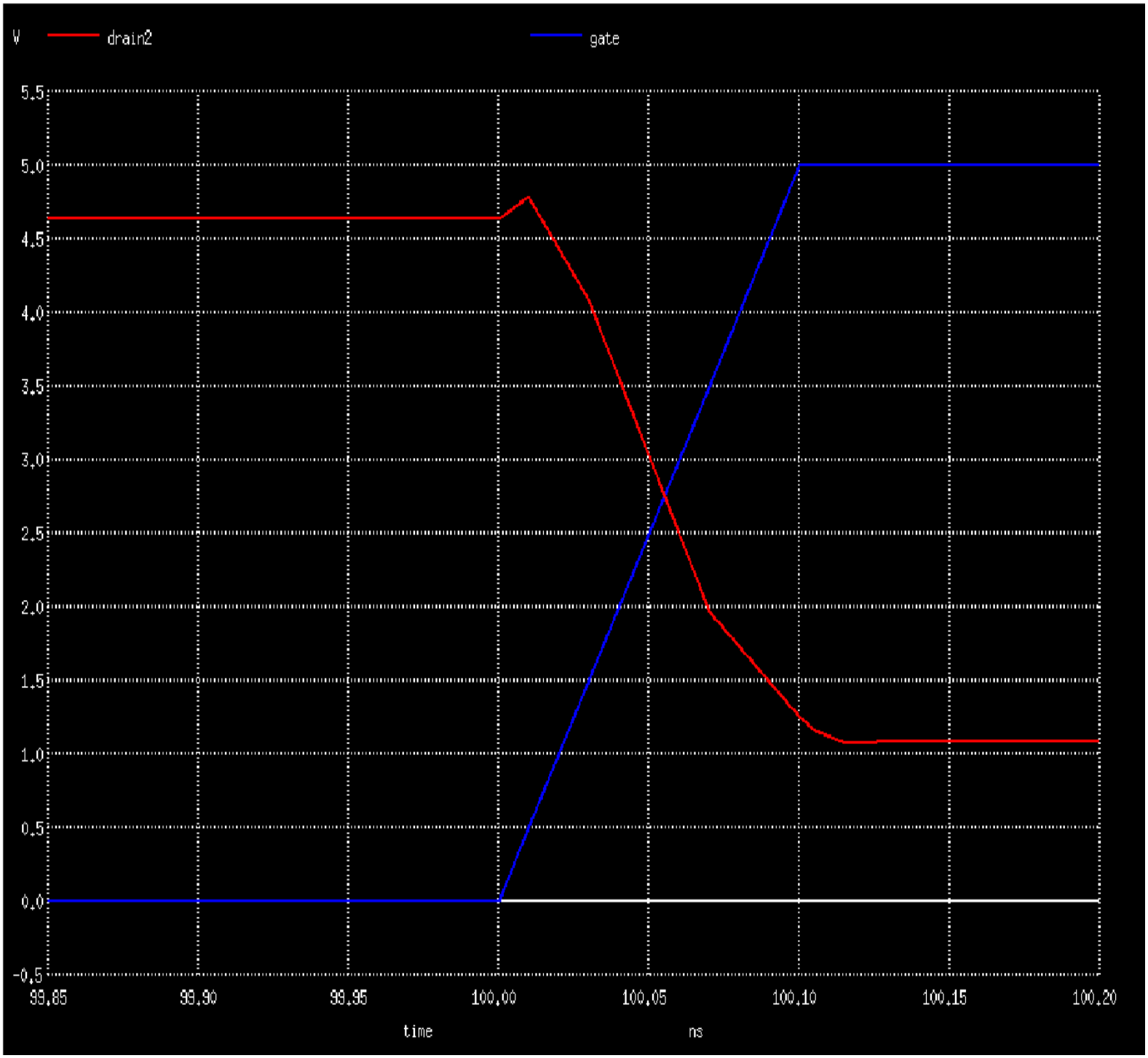
The effect of variation in the the current with respect to w/l is shown above. The current increases with the increase in the w/l.


V
drain4 (C=1000fF)
drain2 (C=10fF)
gate
drain3 (C=100fF)
drain1 (C=1fF)
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
120.0
130.0
140.0
150.0
160.0
170.0
180.0
190.0
200.0
time
ns

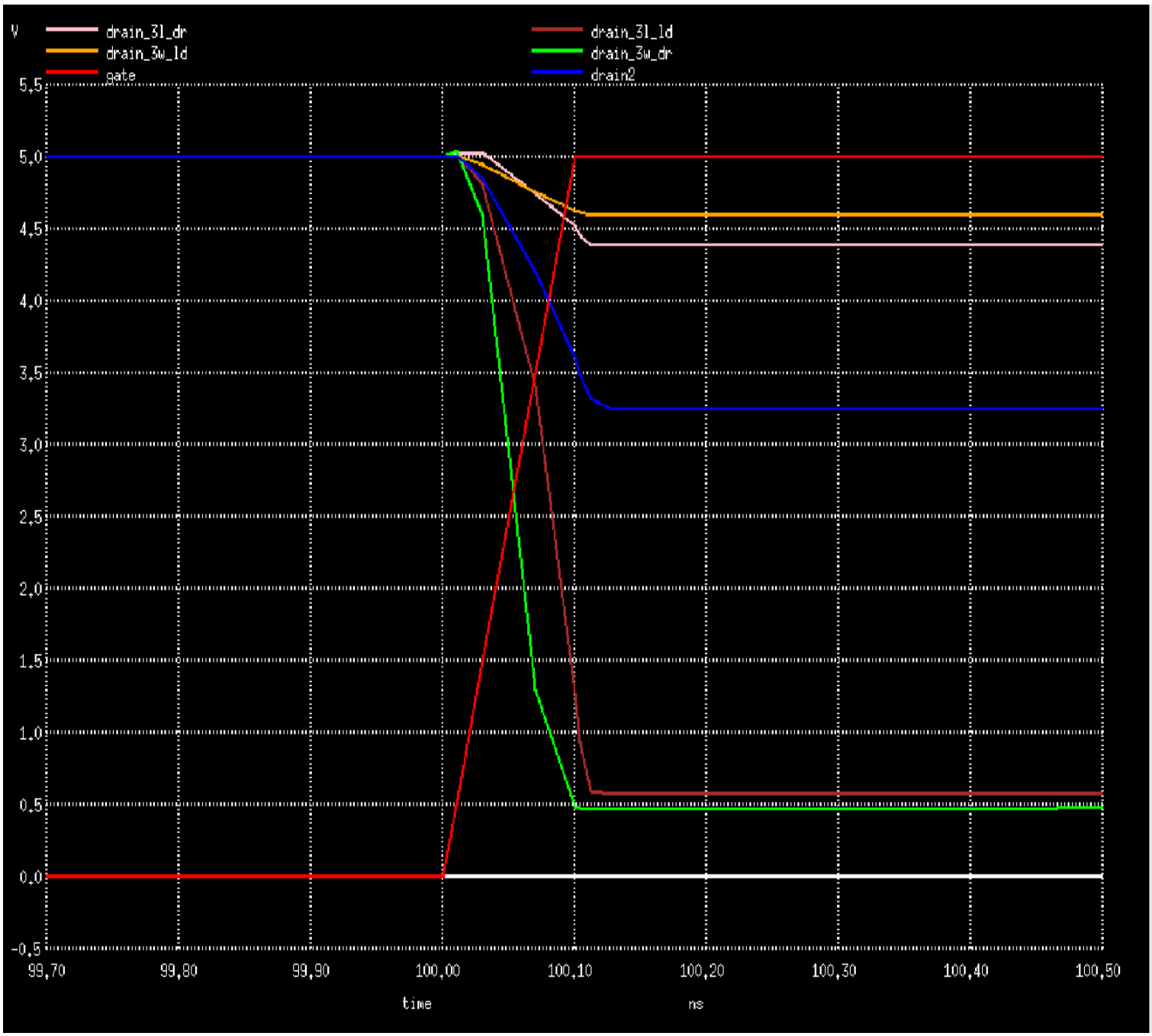
Nmos load :


uA
V3wdr#branch
V3wld#branch
V31dr#branch
V31ld#branch
Vnorm#branch
400.0
350.0
300.0
250.0
200.0
150.0
100.0
50.0
0.0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
v-sweep
V

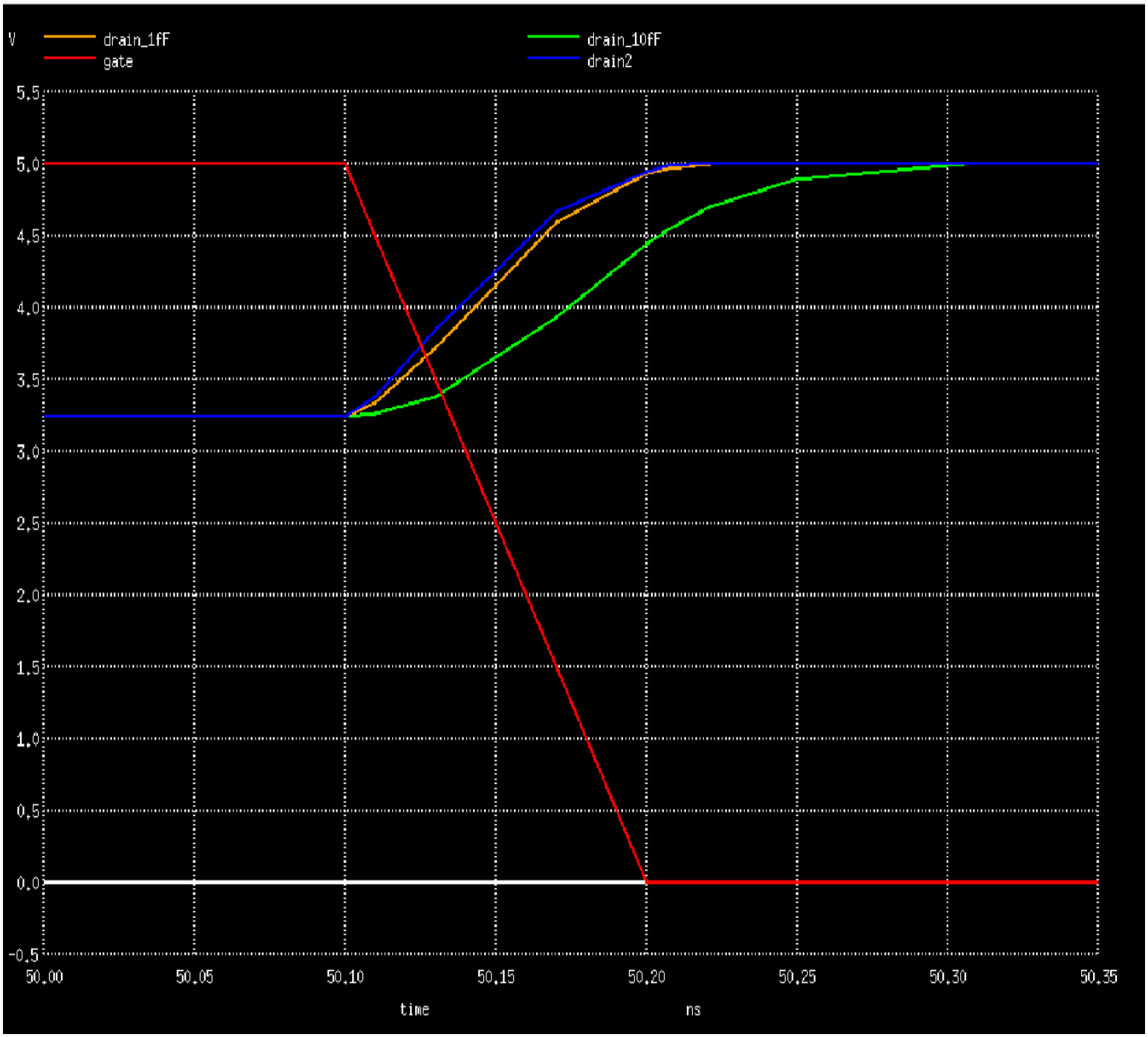
VTC of Inverter:



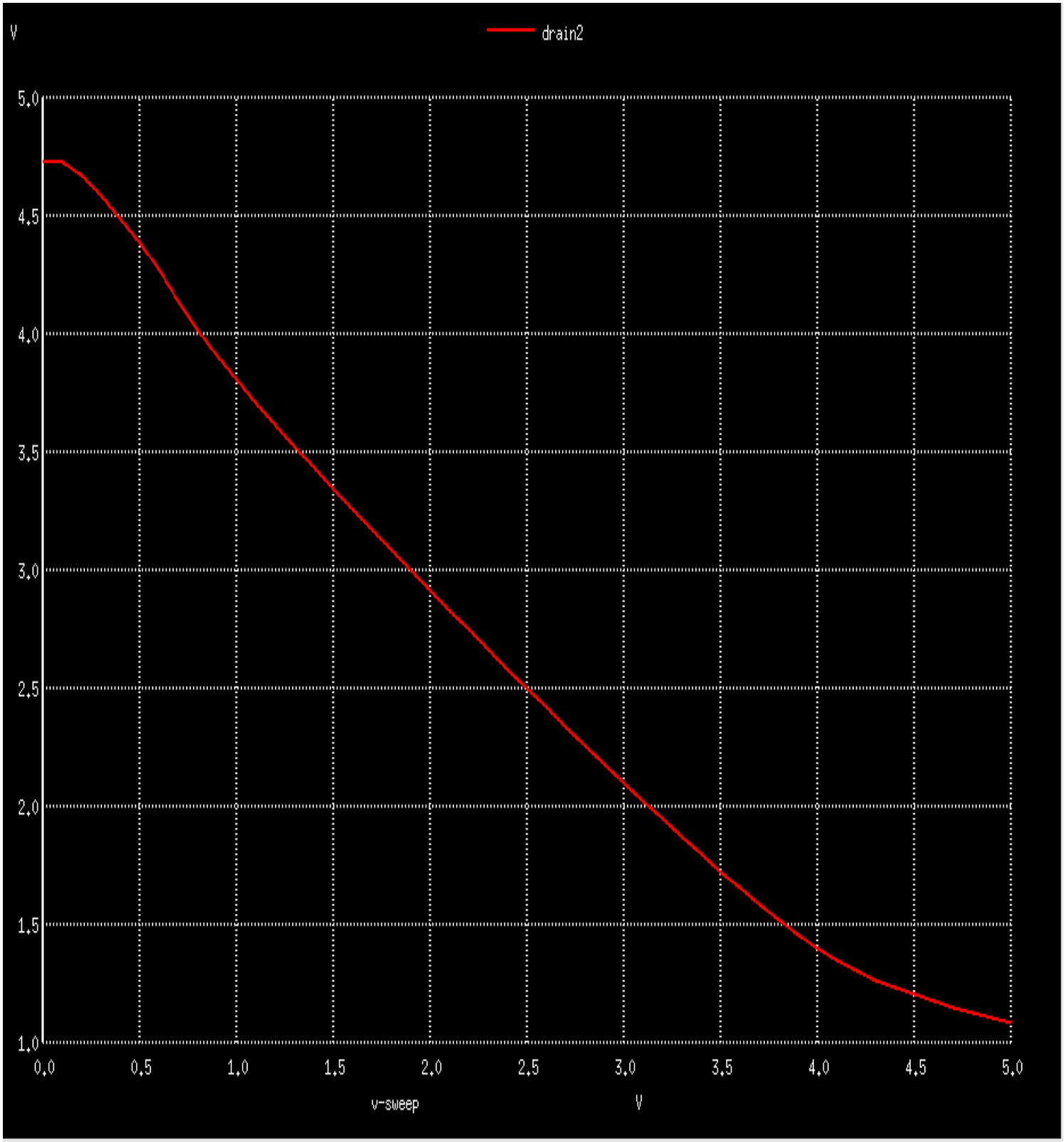
Pmos_load_tf


V
drain_3l_dr
drain_3w_ld
gate
drain_3l_ld
drain_3w_dr
drain2
5,5
5,0
4,5
4,0
3,5
3,0
2,5
2,0
1,5
1,0
0,5
0,0
-0,5
99,70
99,80
99,90
100,00
100,10
100,20
100,30
100,40
100,50
time
ns

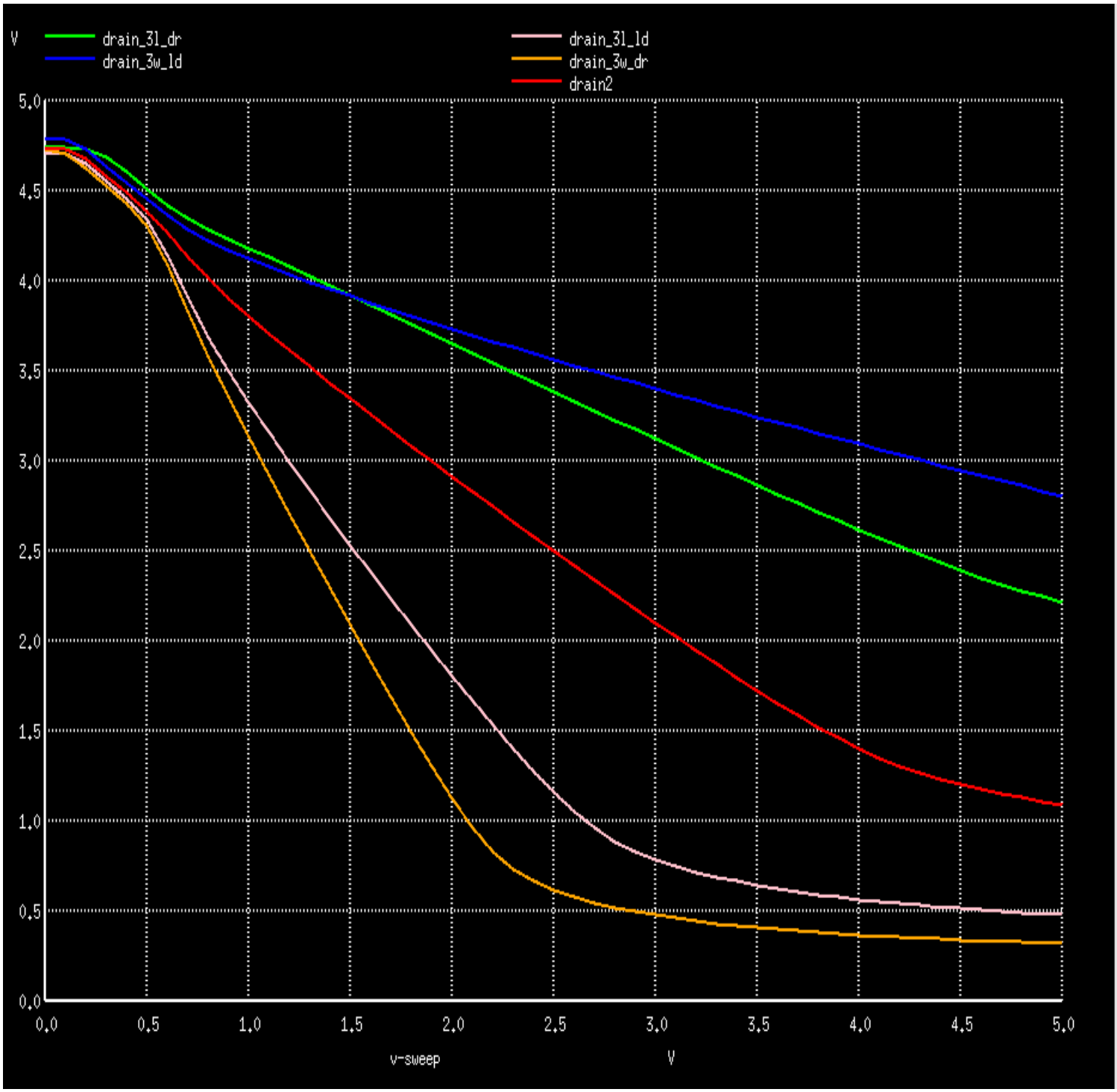
Pmosload_cap



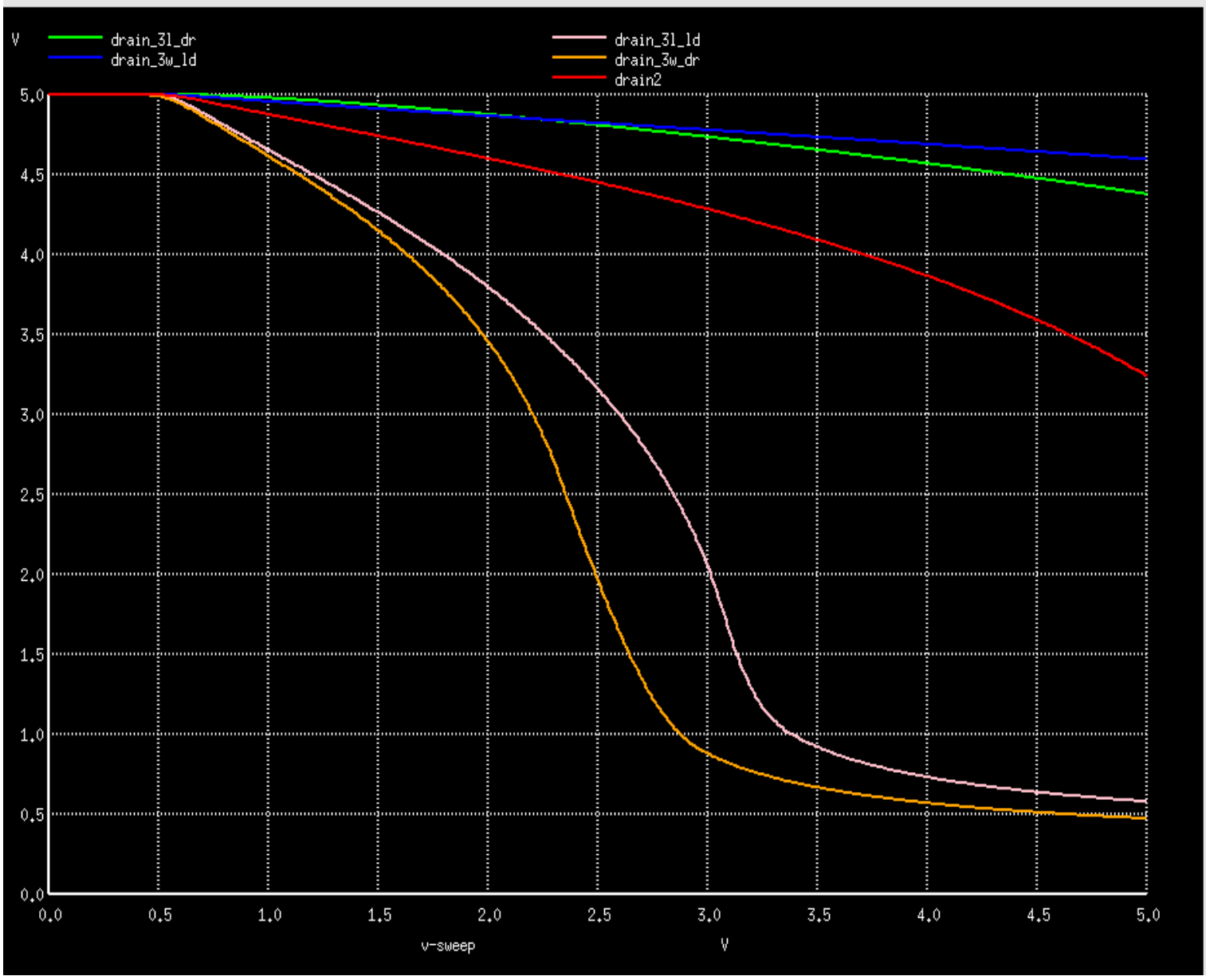
Nmos_load_tf:


V
drain2
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
v-sweep
V

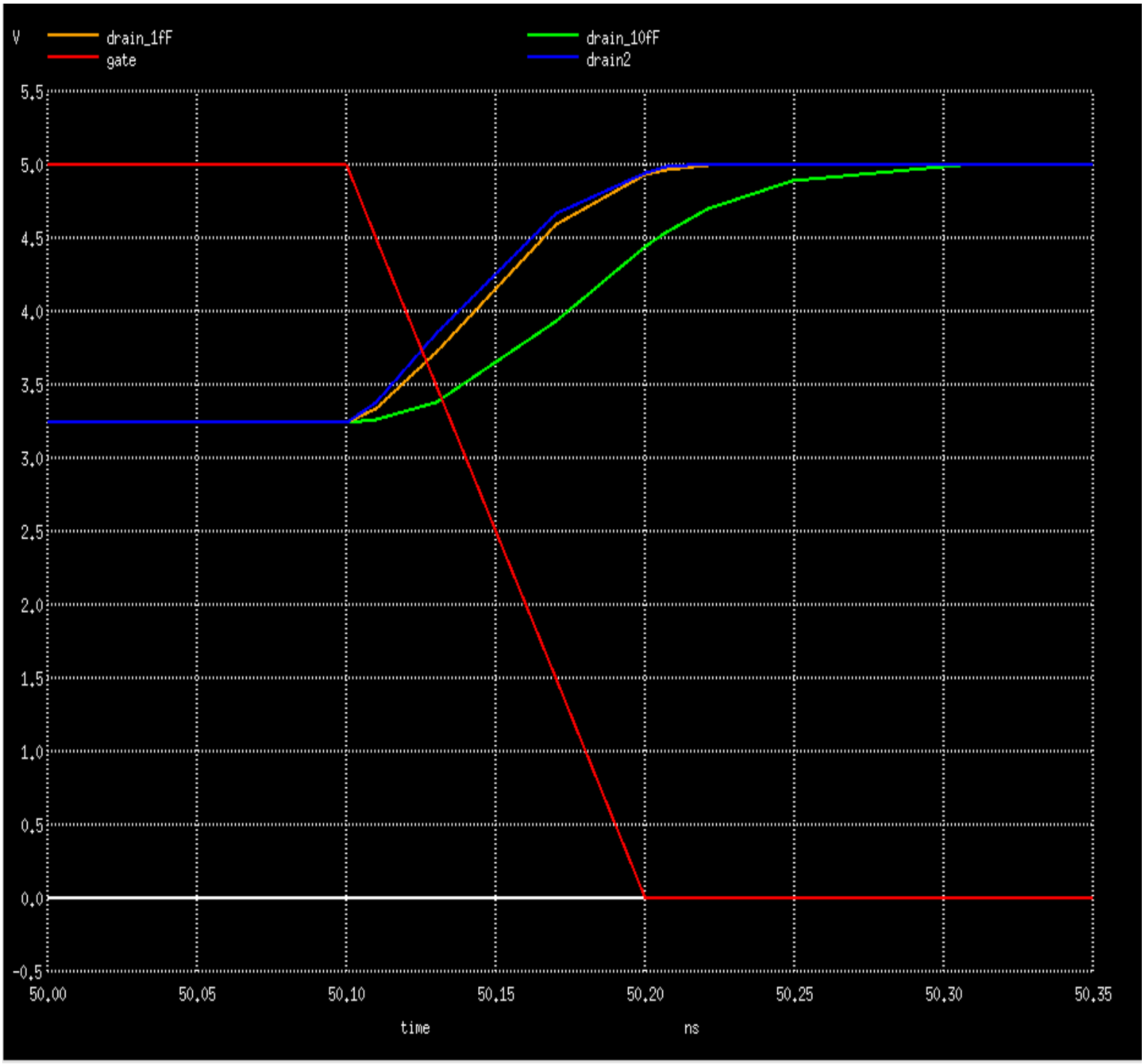
Nmos load with Various w/l:



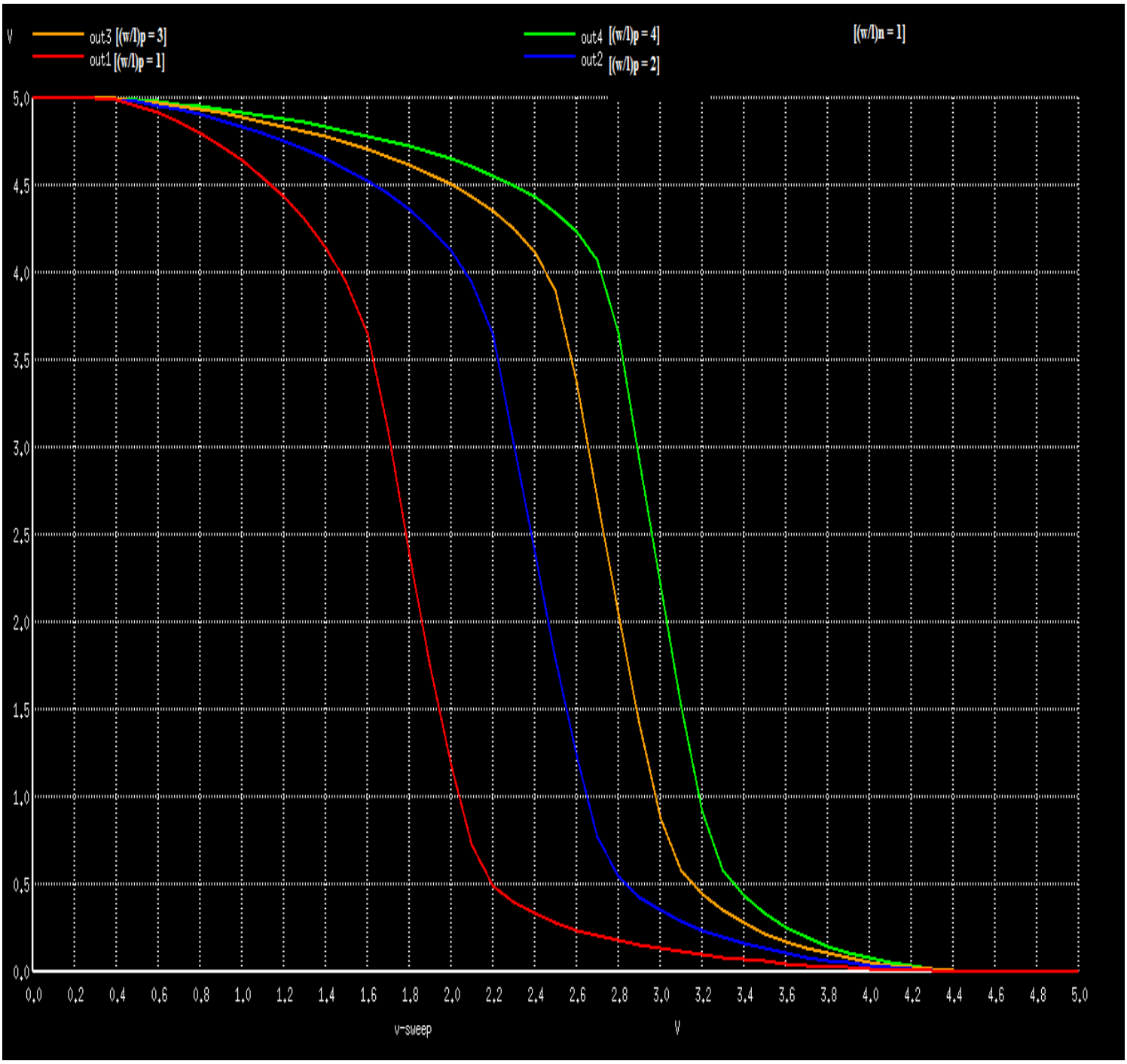
Pmos_load :


V
drain_3l_dr
drain_3w_ld
drain_3l_ld
drain_3w_dr
drain2
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
v-sweep
V

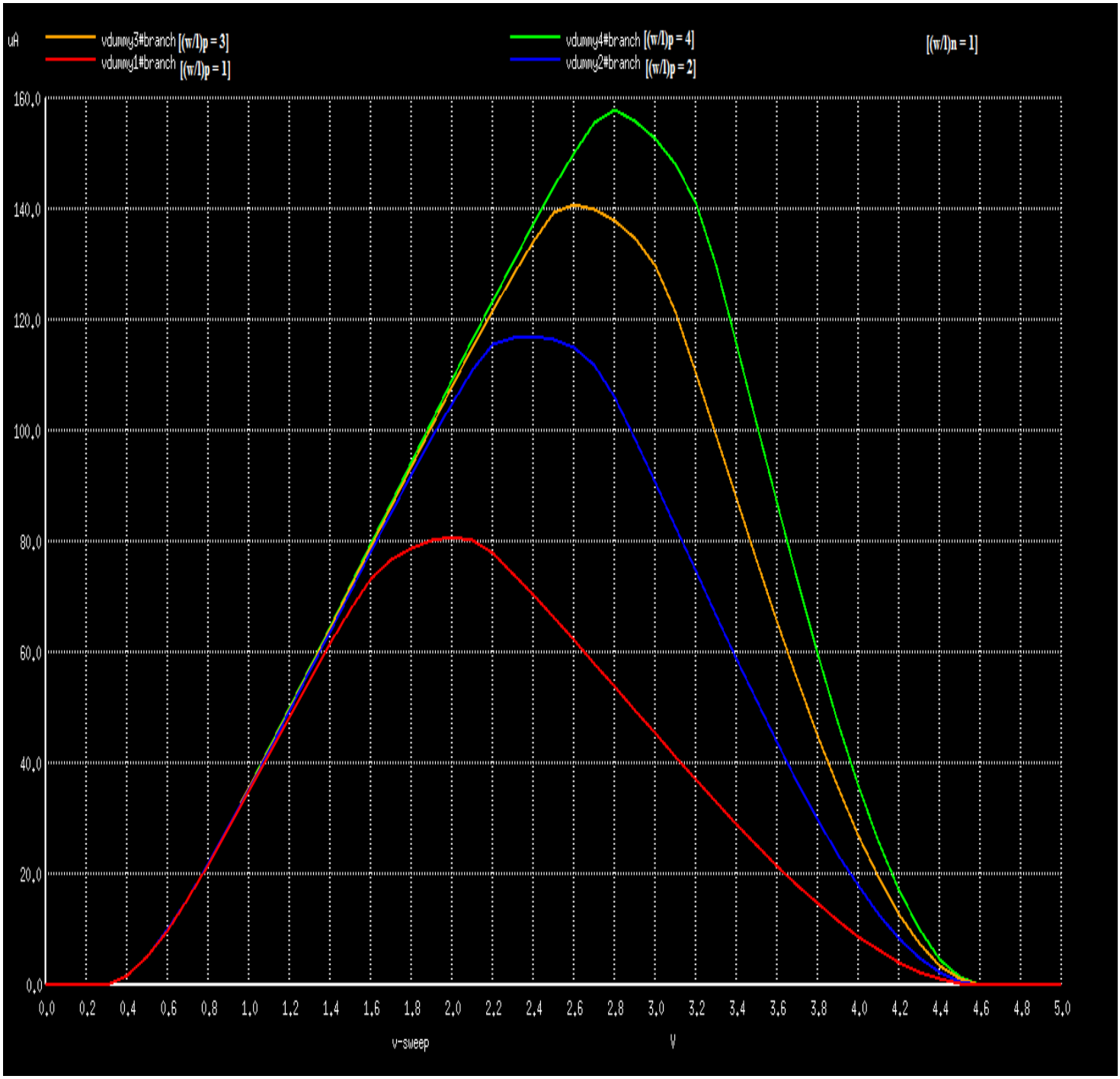
Pmos load with capacitance:



Cmosp_dc :

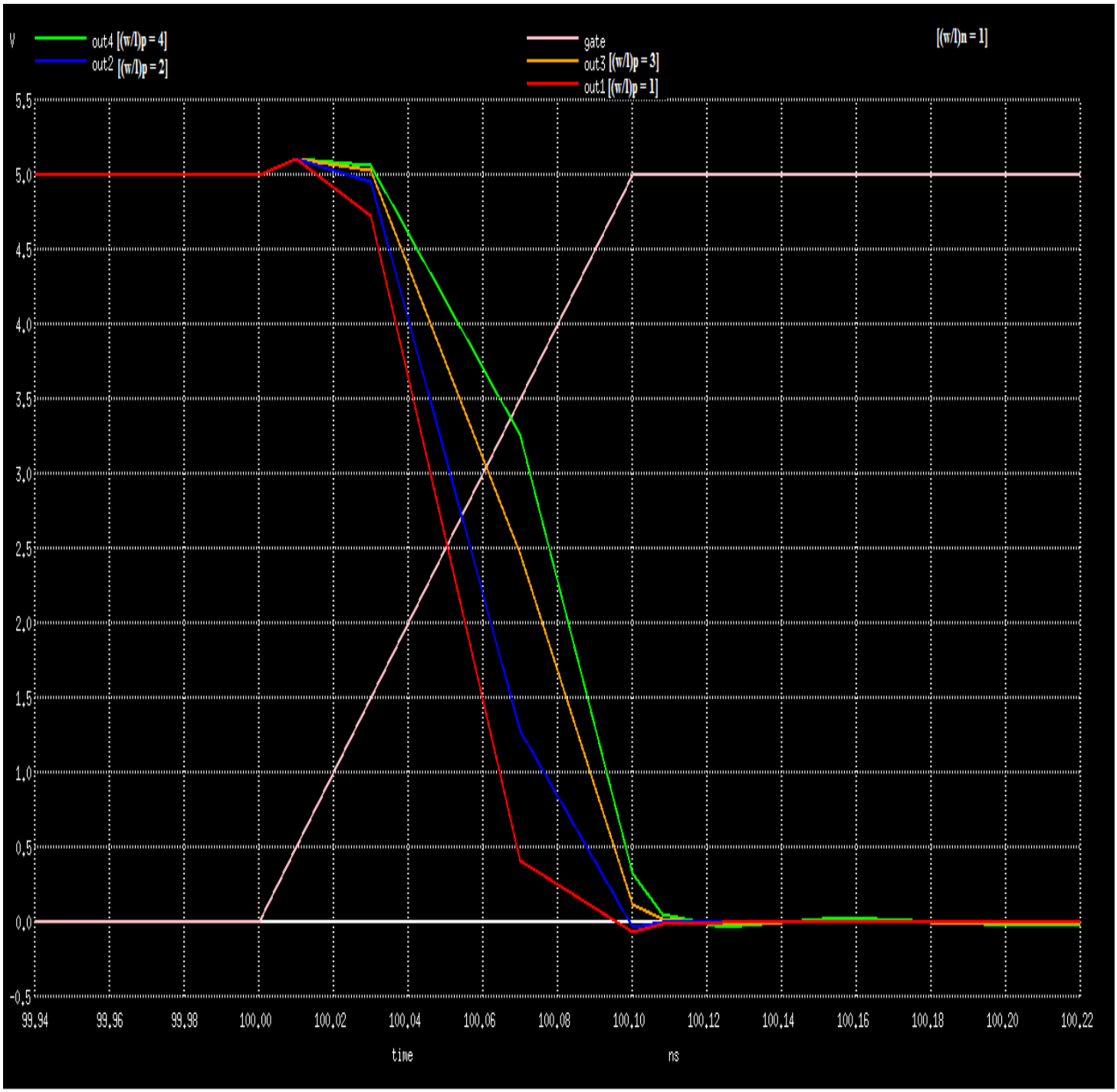

V
out3 [(w/l)p = 3]
out1 [(w/l)p = 1]
out4 [(w/l)p = 4]
out2 [(w/l)p = 2]
[(w/l)n = 1]
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8 3.0 3.2 3.4 3.6 3.8 4.0 4.2 4.4 4.6 4.8 5.0
v-sweep
V

The variation in power with different values of w/l:

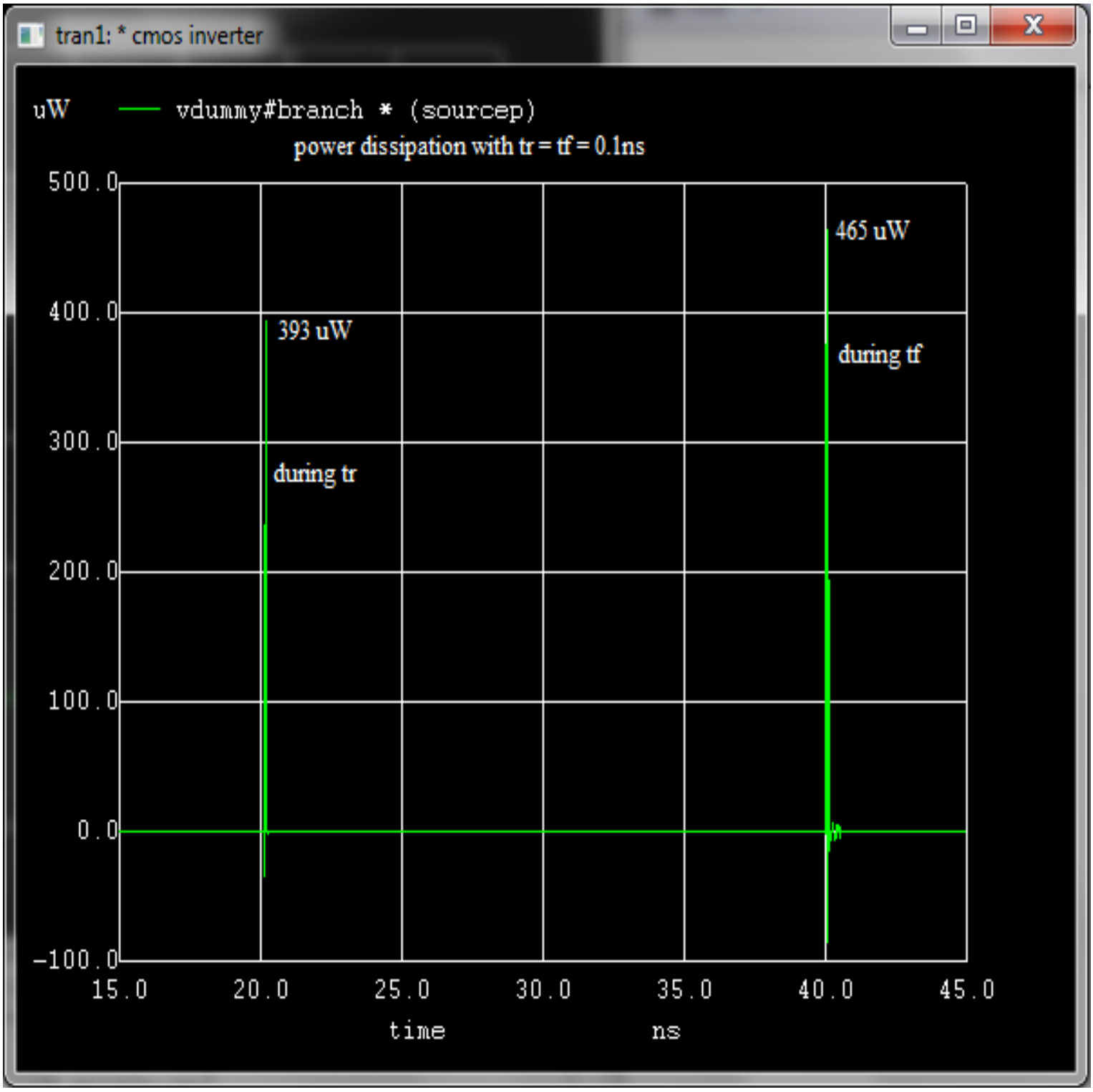


Since the current increases with increase in w/l…so the power also increases.

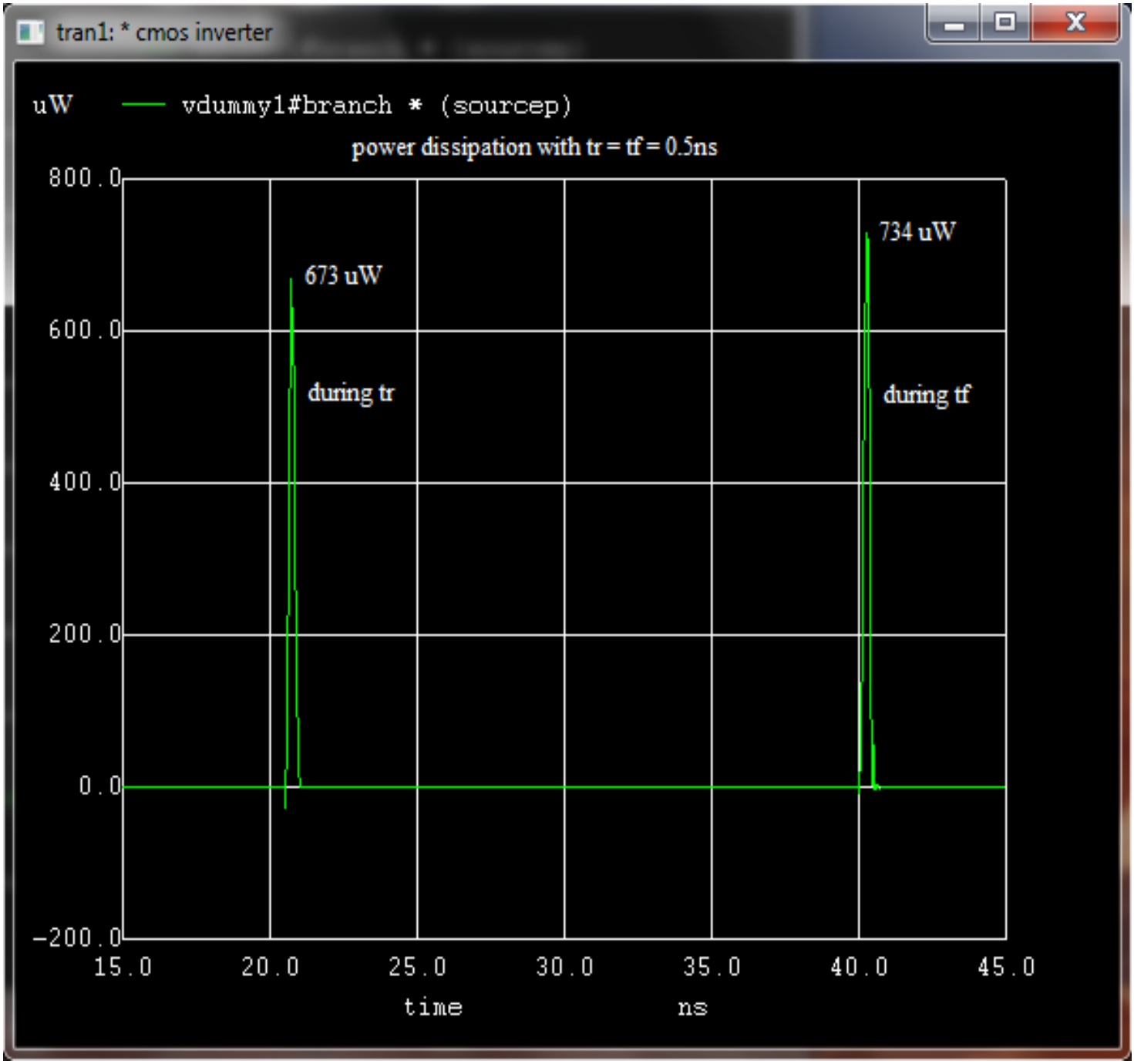
Transient analysis with various w/l values:



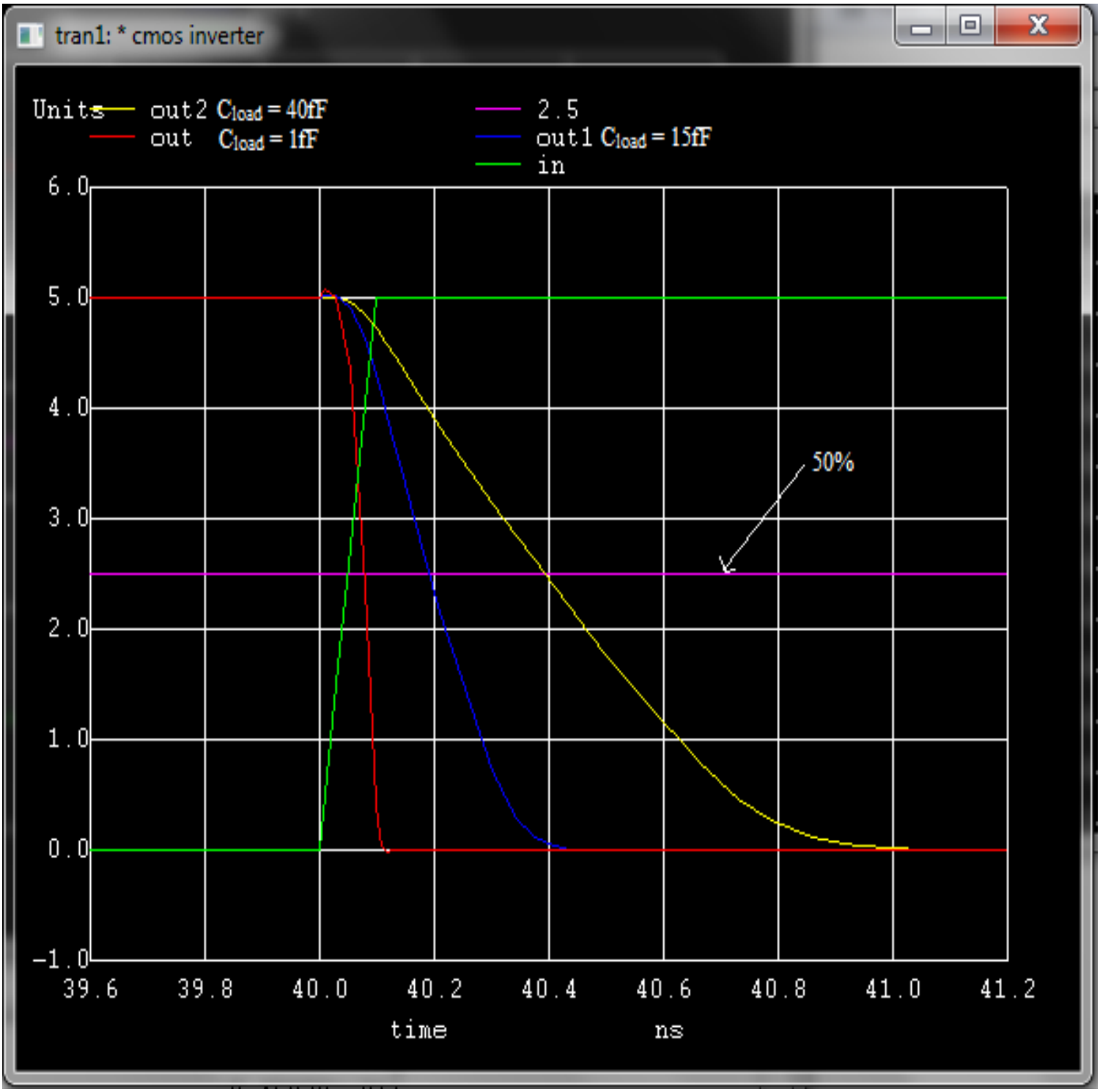
Power dissipation during rise time and fall time:



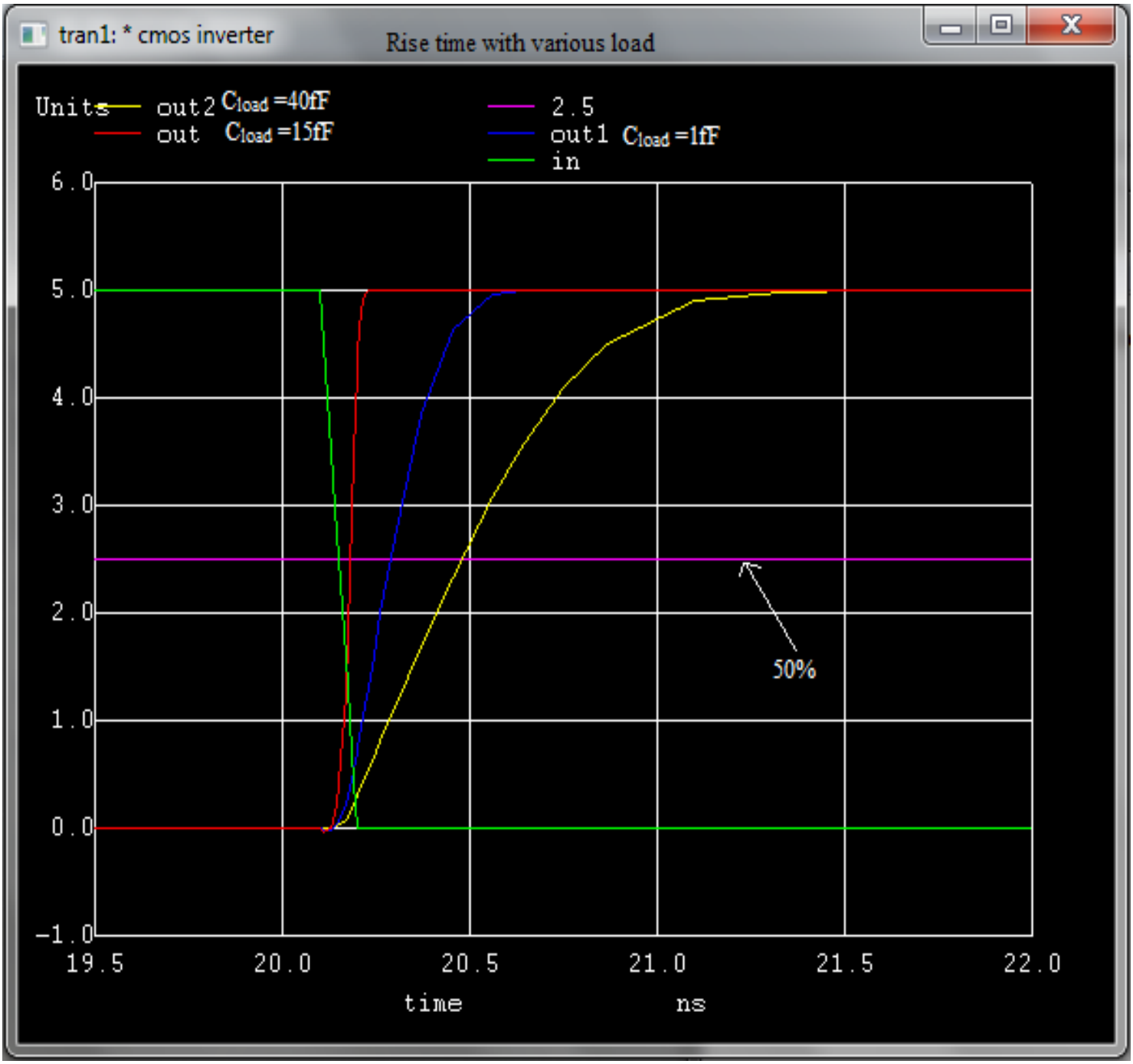
Power dissipation for tr = tf = 0.5ns:



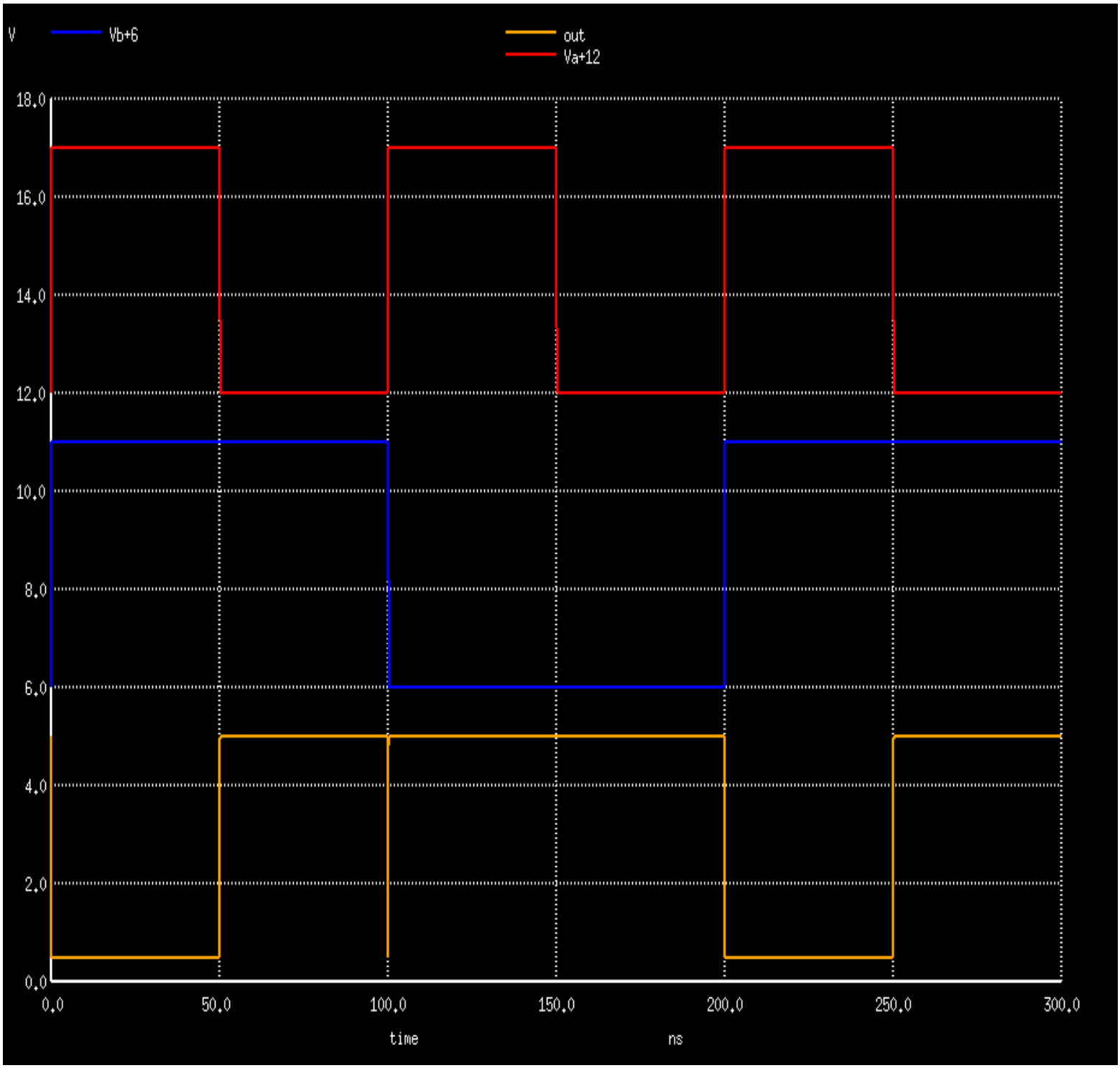
Cmos inverter with various values of output capacitance:



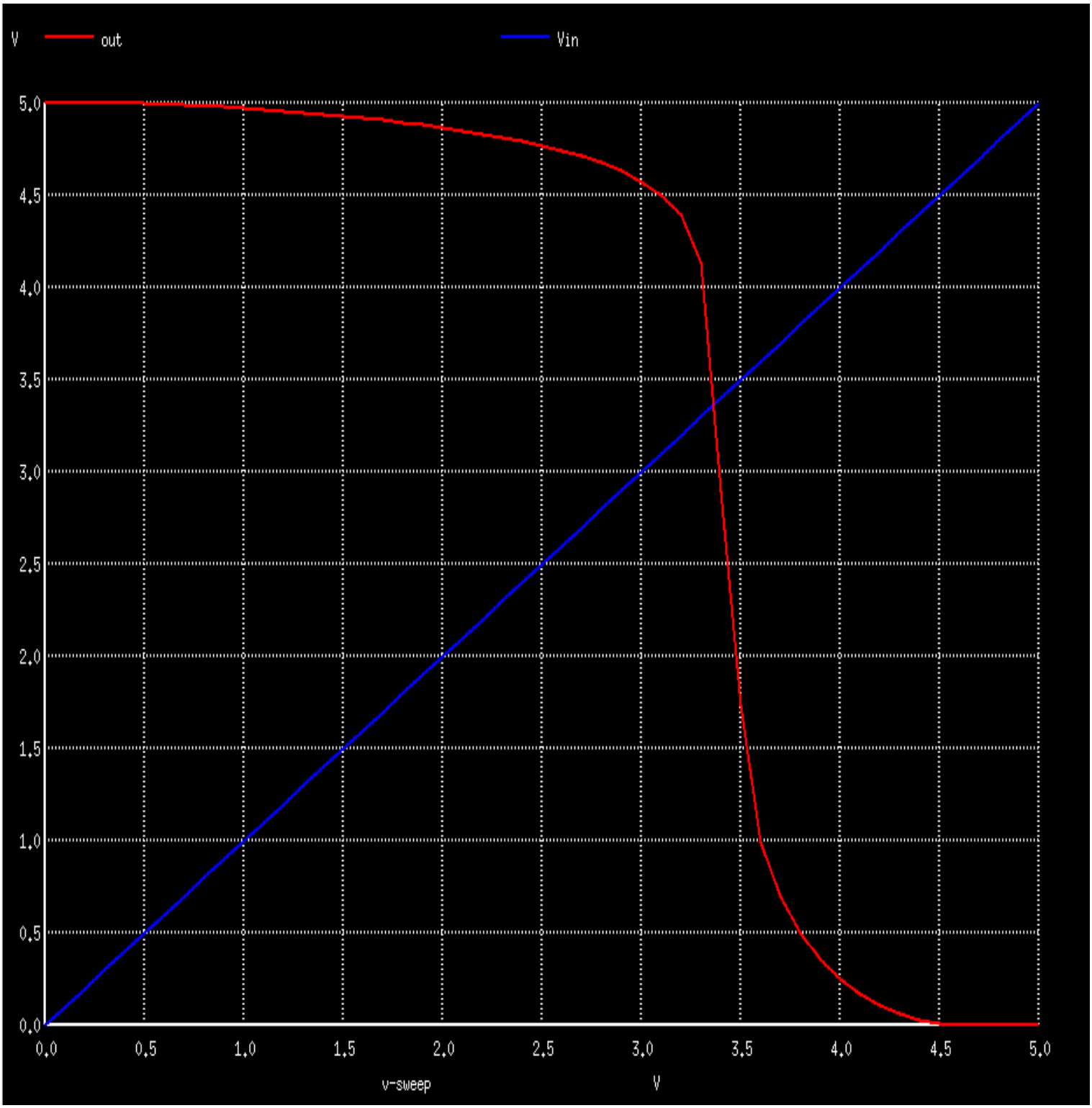
Rise time with loads :



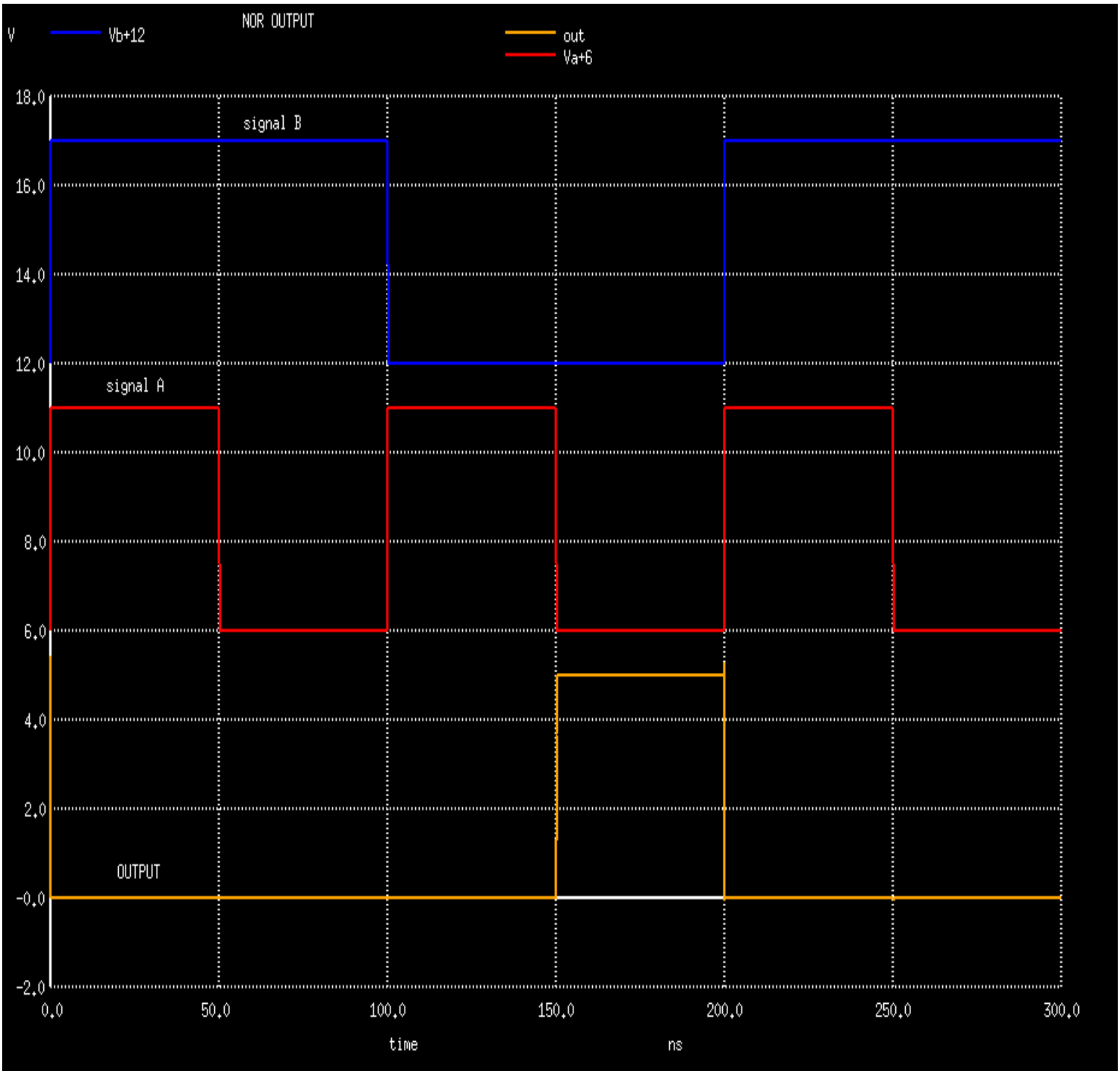
Nand :


V
Vb+6
out
Va+12
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
0.0
50.0
100.0
150.0
200.0
250.0
300.0
time
ns

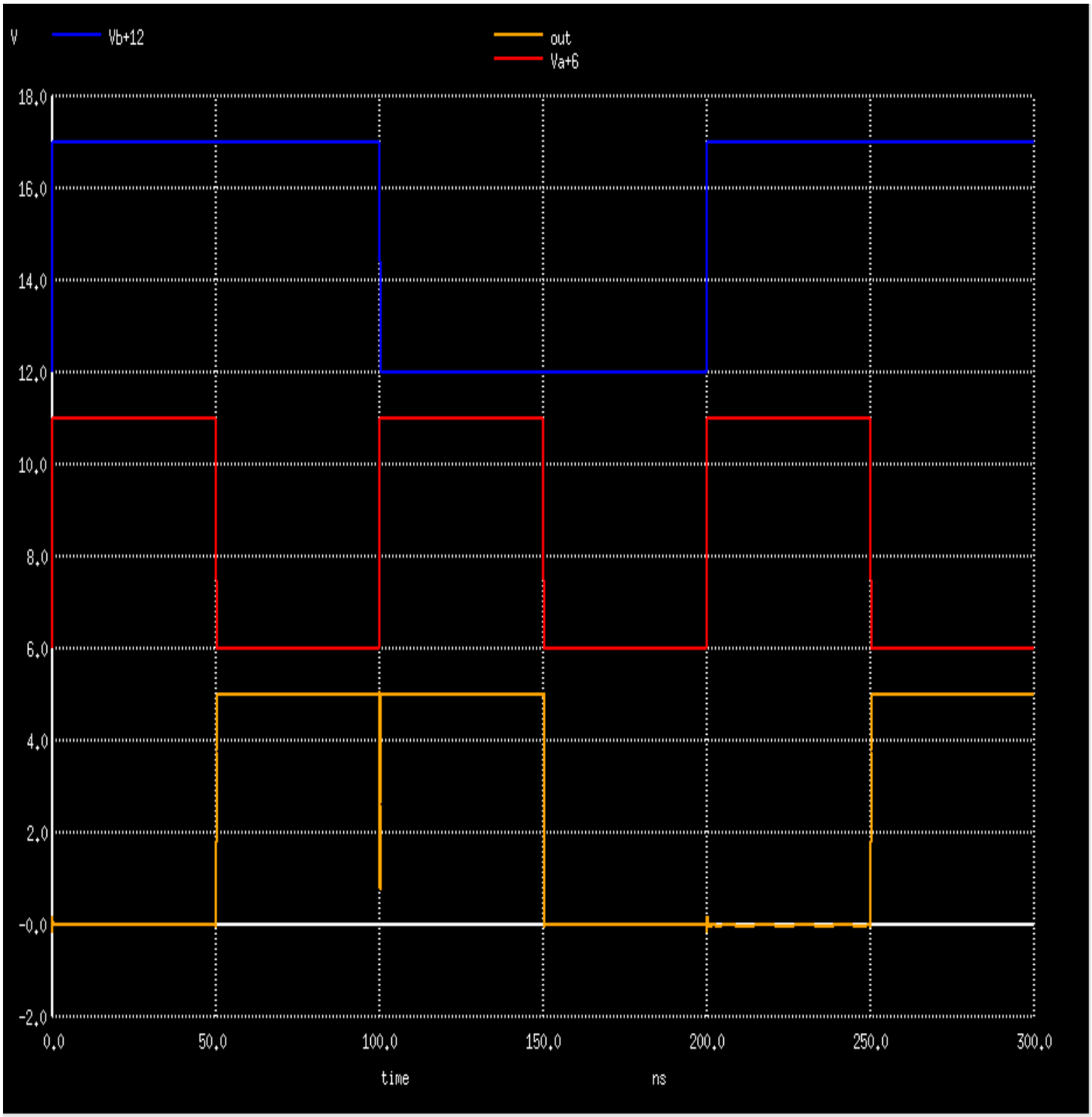
Nand dc


V
out
Vin
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
v-sweep
V

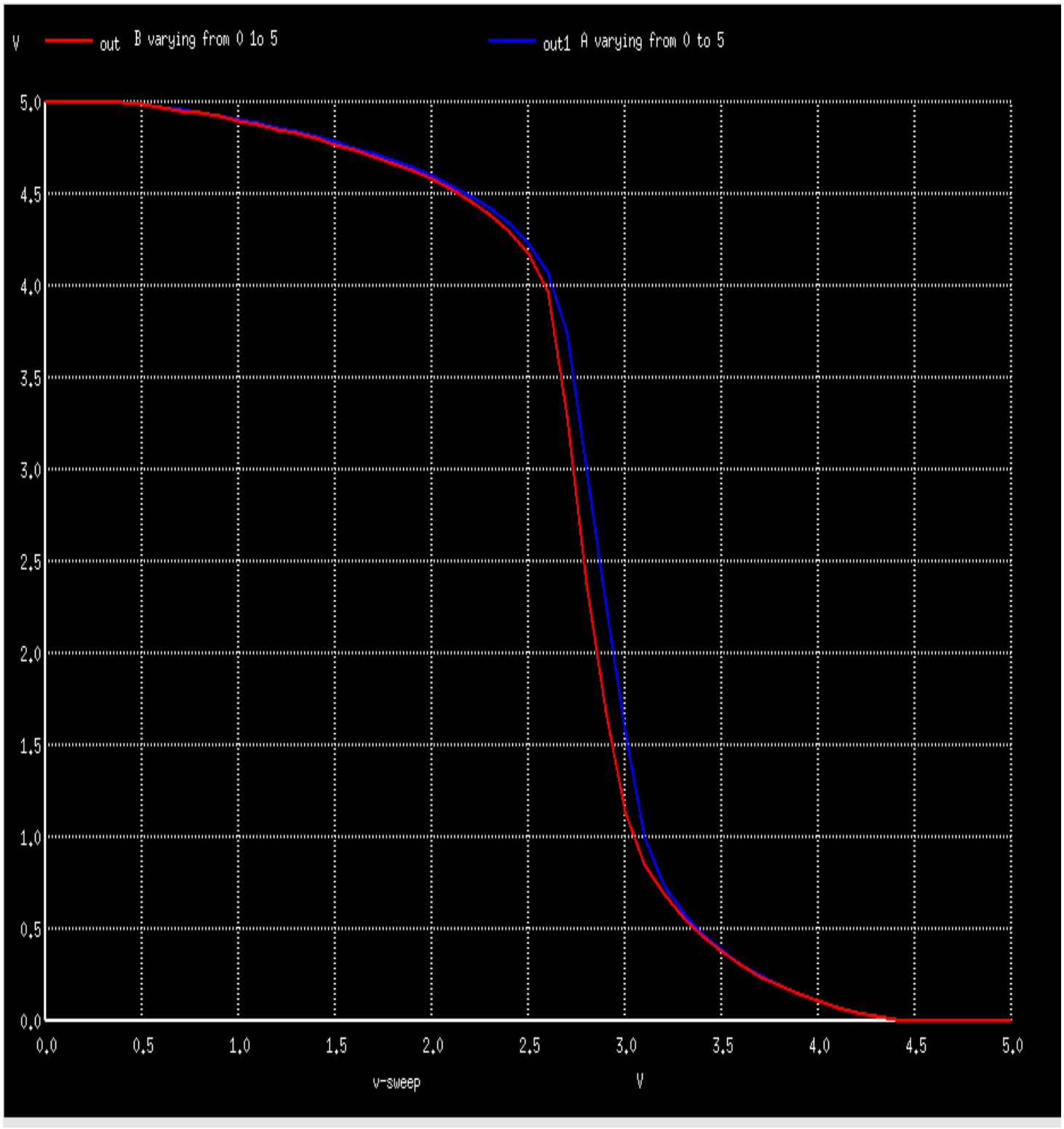
Nor


NOR OUTPUT
V
Vb+12
out
Va+6
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
-0.0
-2.0
signal B
signal A
OUTPUT
0.0
50.0
100.0
150.0
200.0
250.0
300.0
time
ns

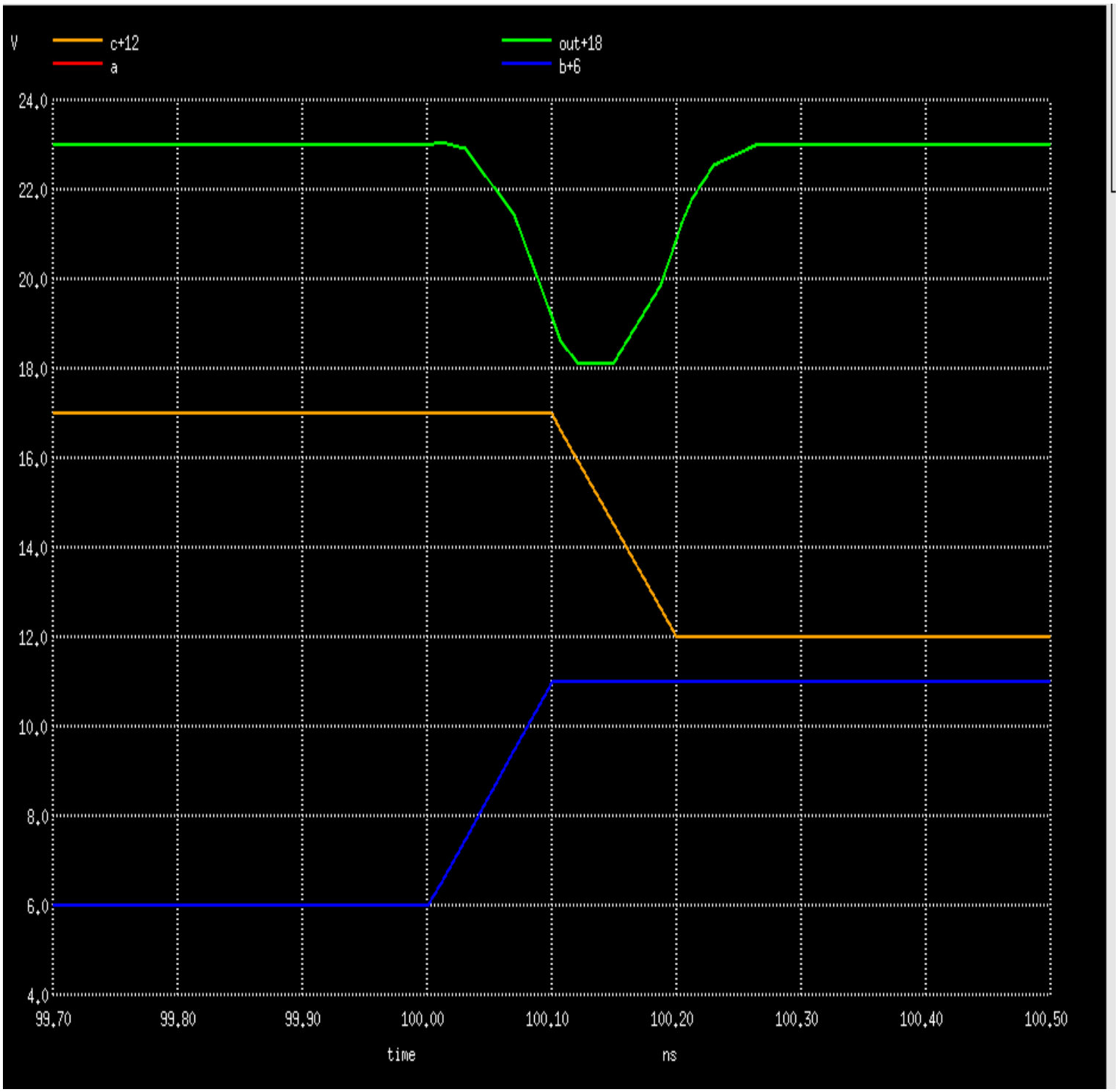
Xor:


V
Vb+12
out
Va+6
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
-0.0
-2.0
0.0
50.0
100.0
150.0
200.0
250.0
300.0
time
ns

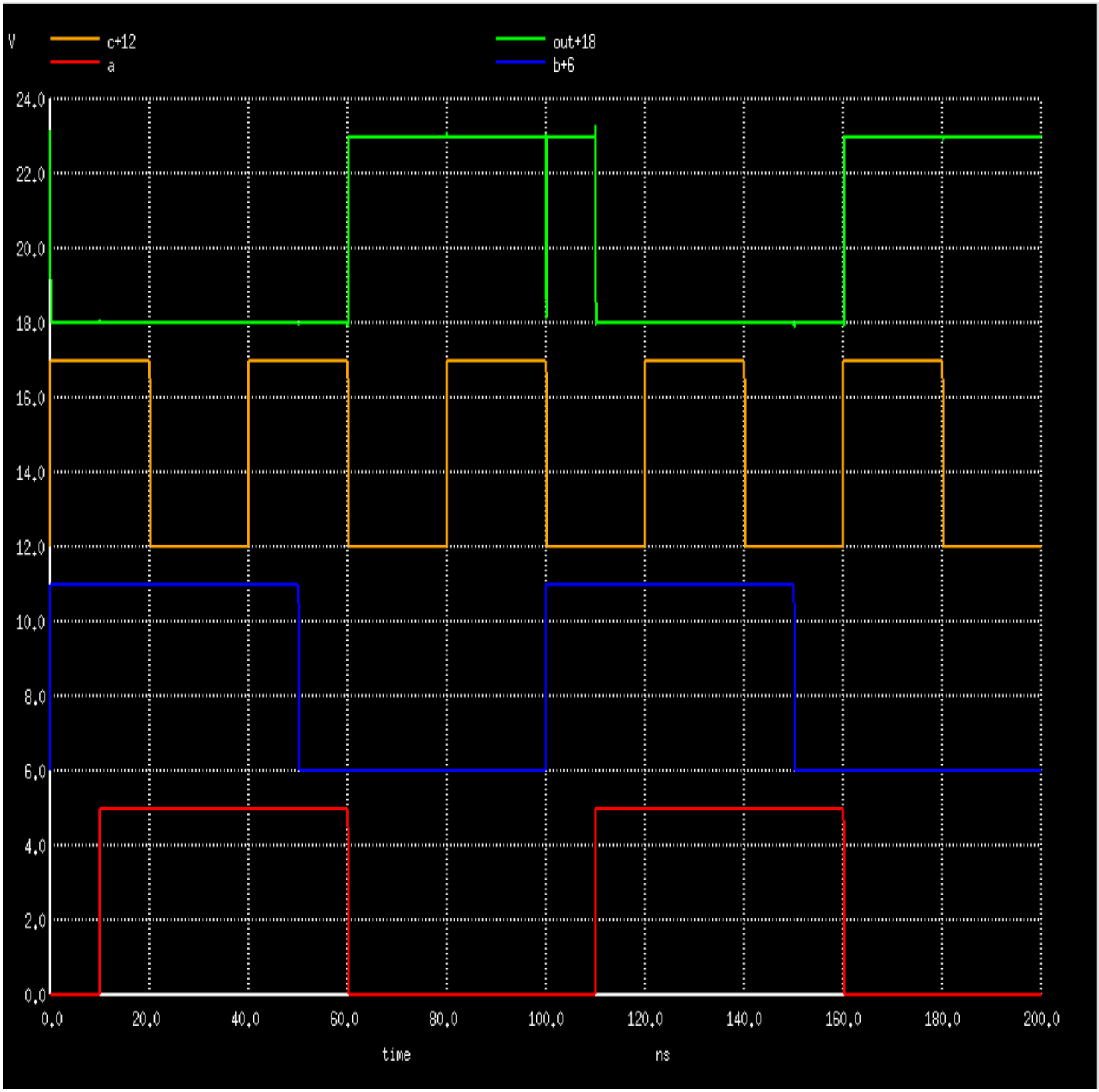
Nand Vsb effect



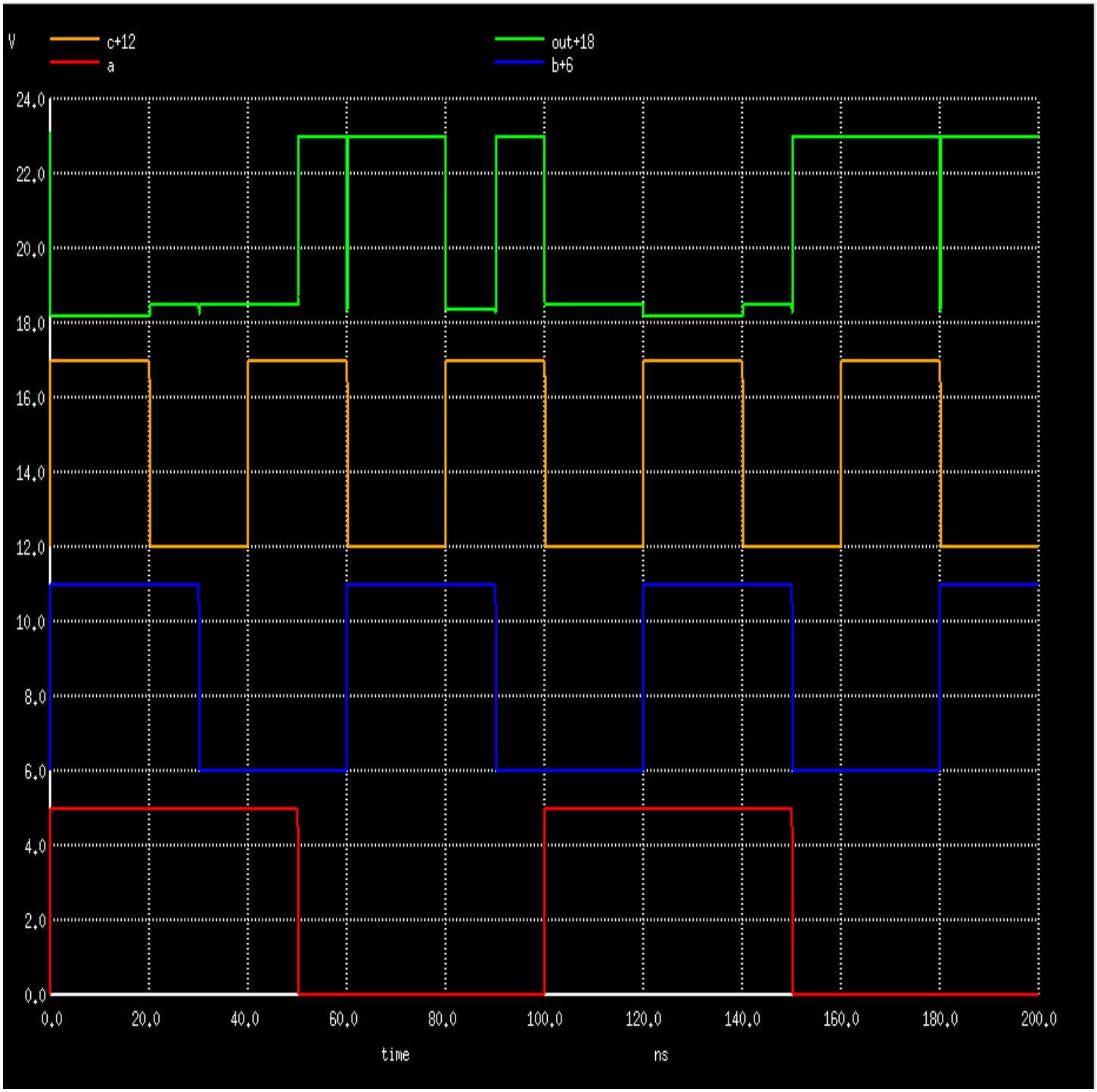
Aoi hazard


V
c+12
a
out+18
b+6
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
99.70
99.80
99.90
100.00
100.10
100.20
100.30
100.40
100.50
time
ns

Aoi out


V
c+12
a
out+18
b+6
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
time
ns

Aoi_pseudo:


V
c+12
a
out+18
b+6
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
time
ns

Aoi pulldown