VLSI LAB REPORT

MID SEMESTER

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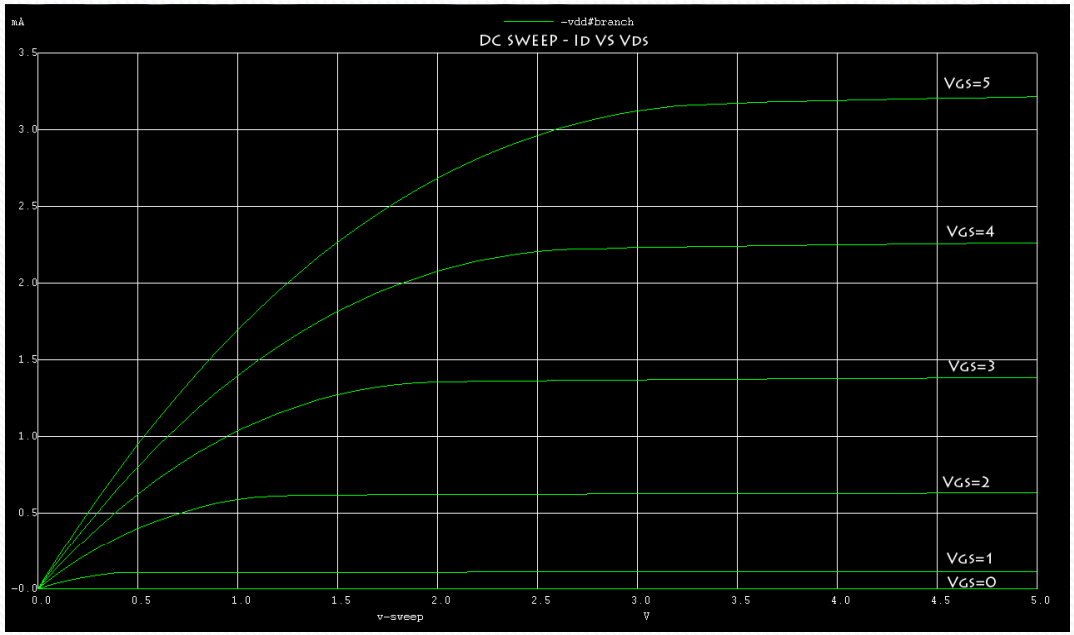
Experiment 1:

Study the V-I characteristics of NMOS Transistor

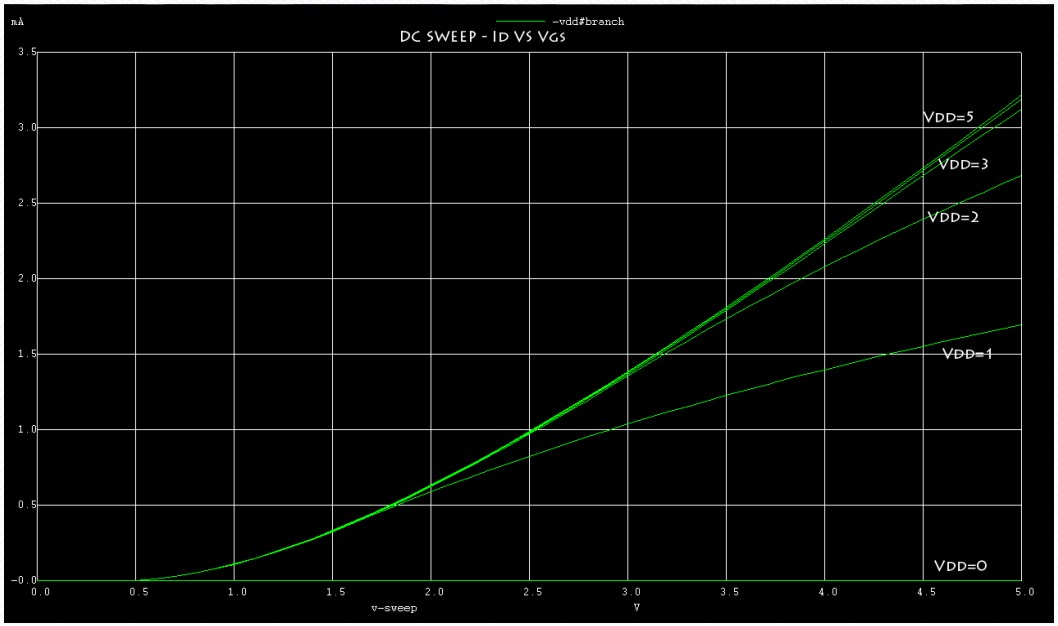
Objective:

Study the input and output characteristics of NMOS Transistor, effects of L, W, VTO, LAMBDA, VSB and temperature on the behavior of the transistor.

DC Sweep



I_d vs V_{gs}

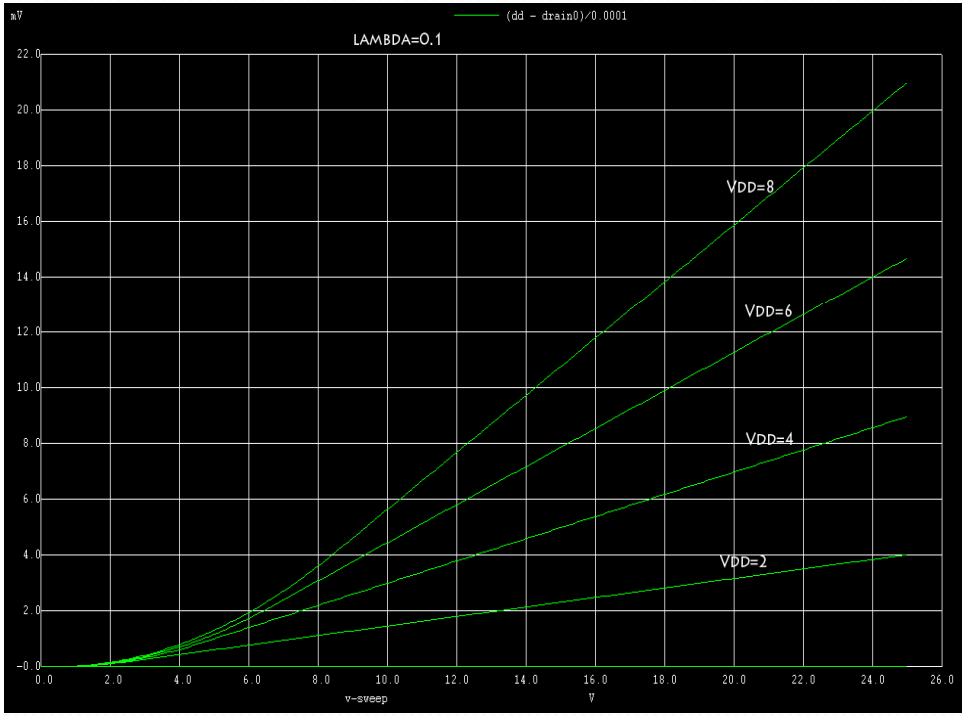


I_d vs V_{ds}

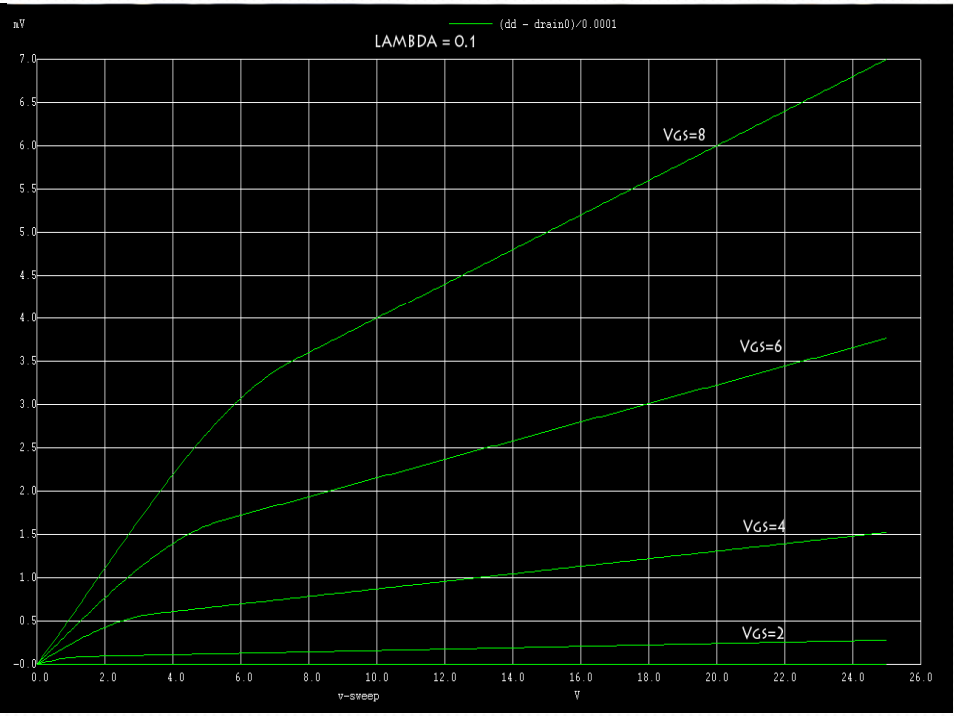
With increase in the values of V_{dd} and Vgs, the drain current increases.

Variation with Lambda

LAMBDA = 0.1



I_d vs V_{gs}

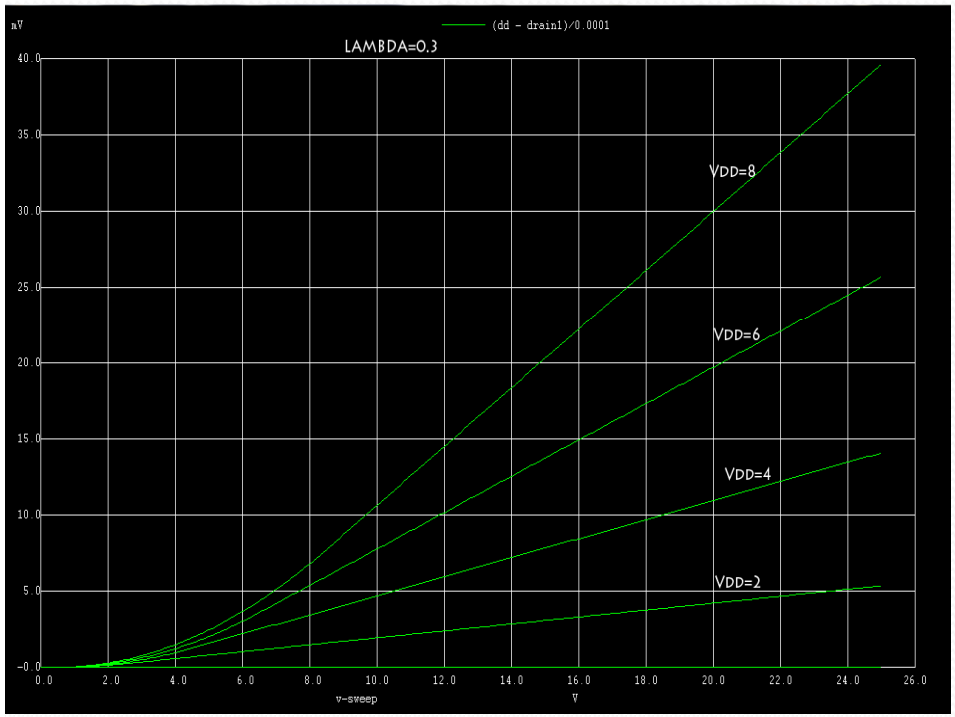


I_d vs V_{ds}

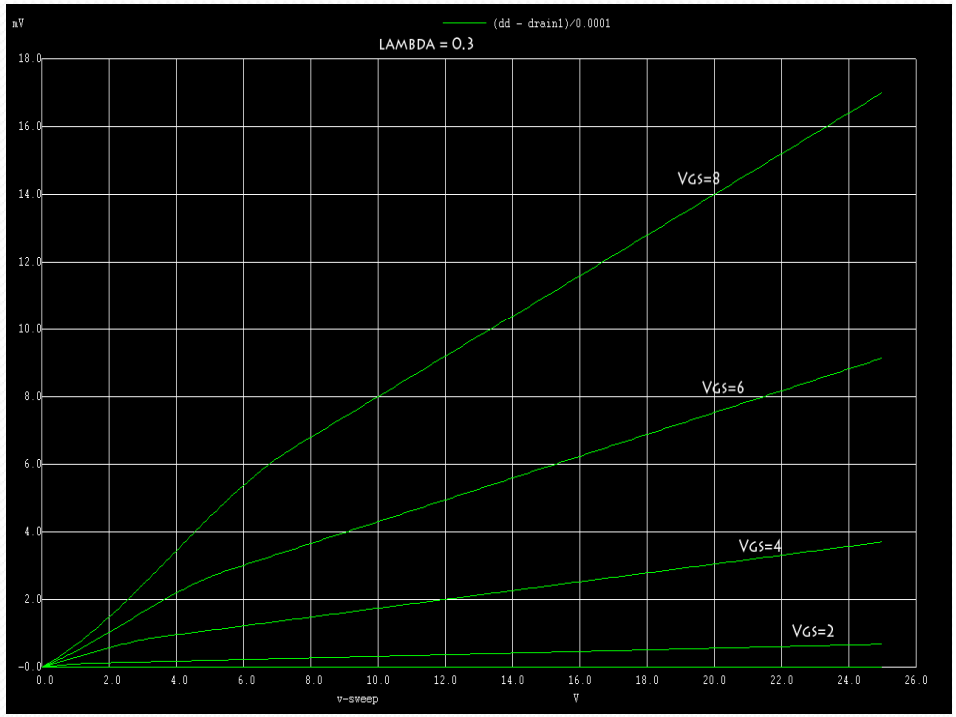
Value of current for Vgs=10V
at Vdd=8V is 6

Variation with Lambda

LAMBDA = 0.3



I_d vs V_{gs}

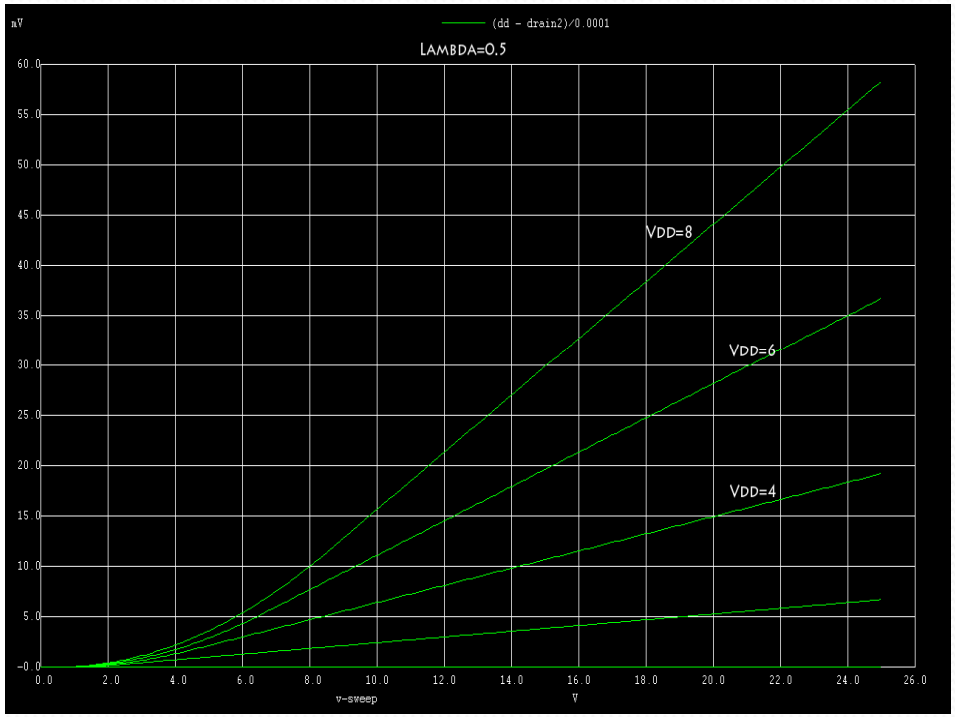


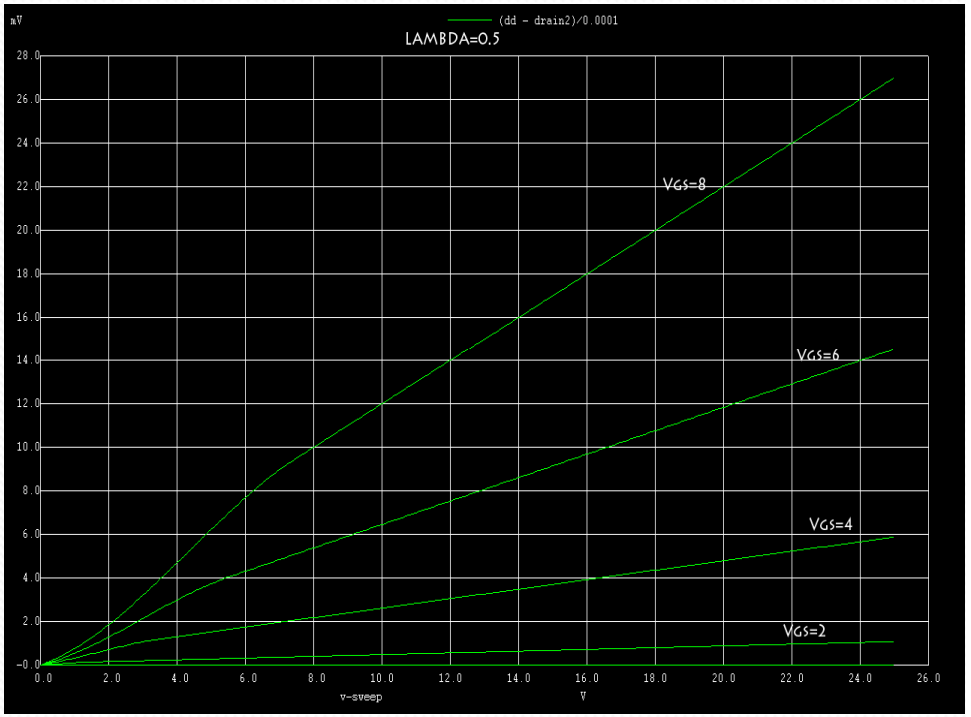
I_d vs V_{ds}

Value of current for Vgs=10V
at Vdd=8V is 11

Variation with Lambda

LAMBDA = 0.5





I_d vs V_{gs}

I_d vs V_{ds}

Value of current for Vgs=10V
at Vdd=8V is 15

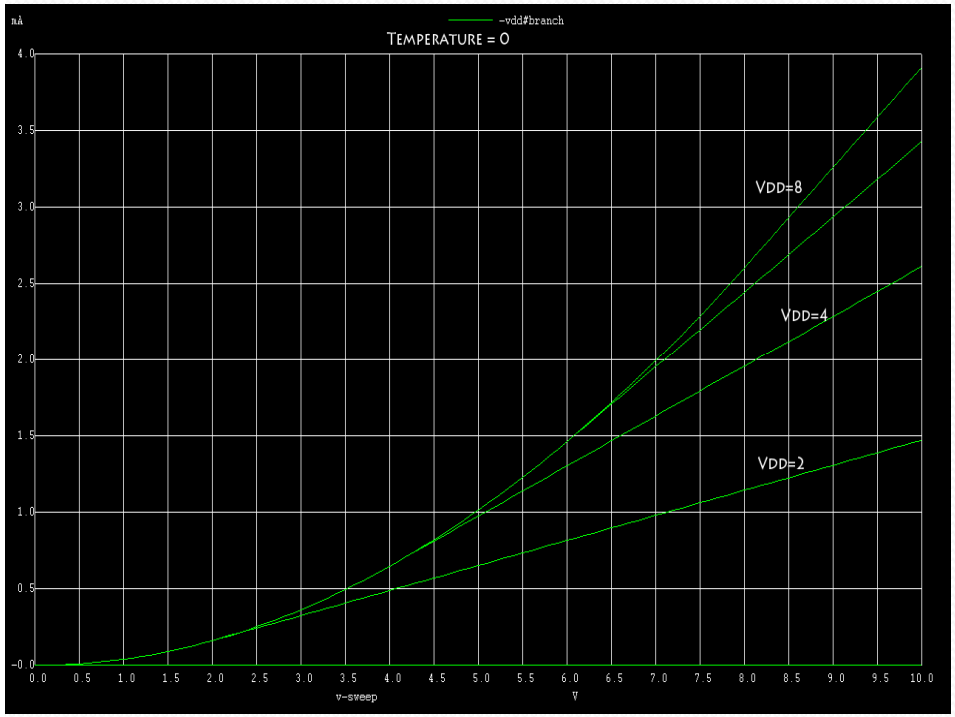
Variation with Lambda

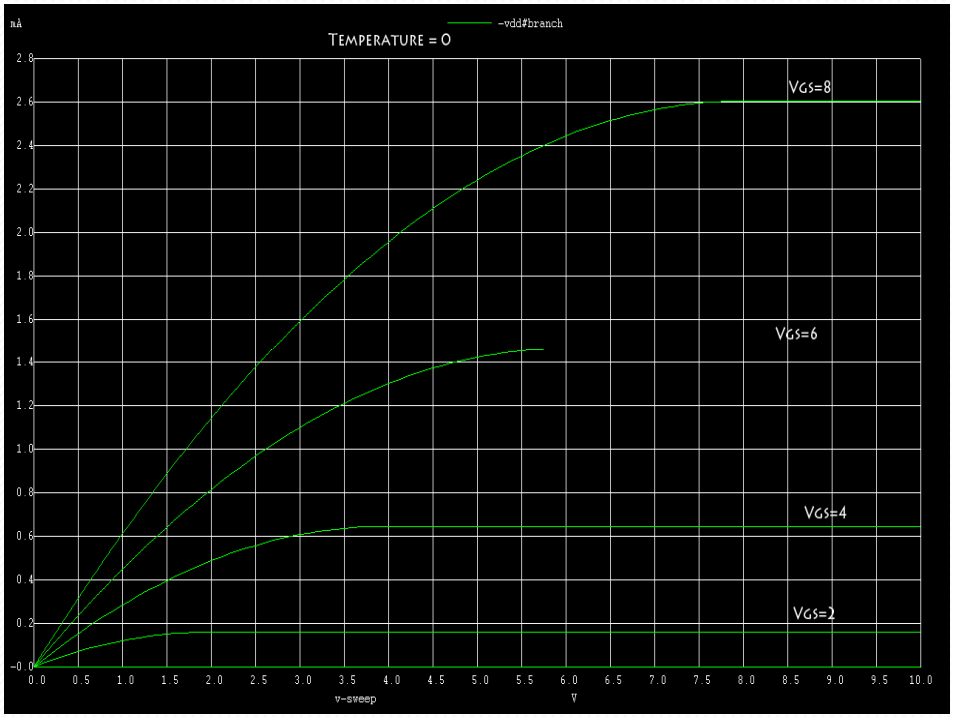
Conclusion :

As the value of Lambda increases, the current also increases. This holds true for both Vdd sweep as well as Vgg sweep.

Hence, current is directly proportional to Lambda.

Variation with Temperature



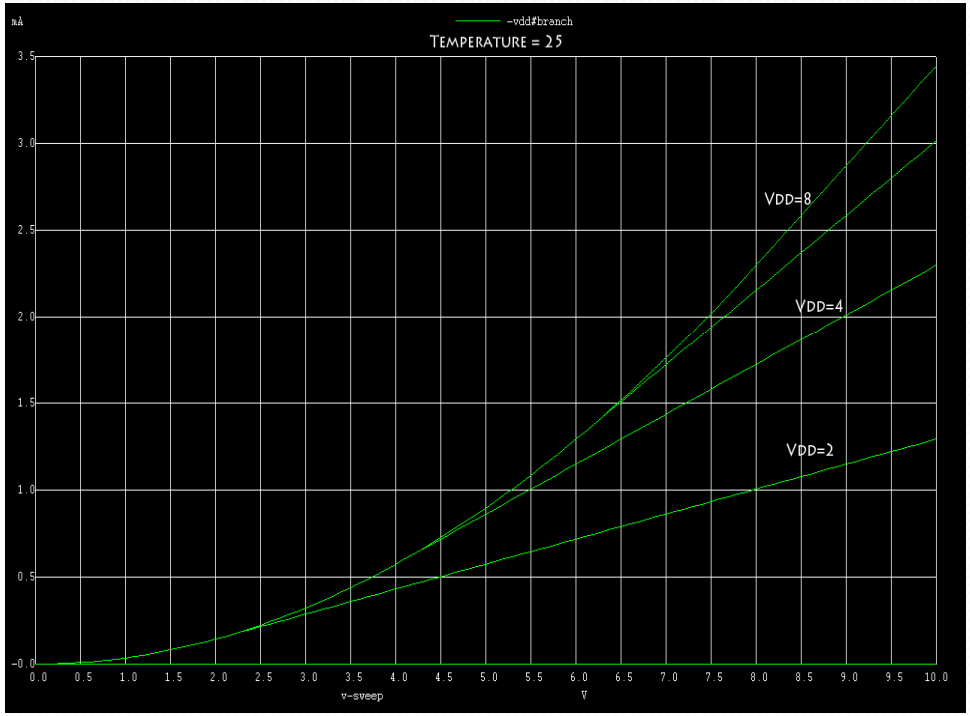


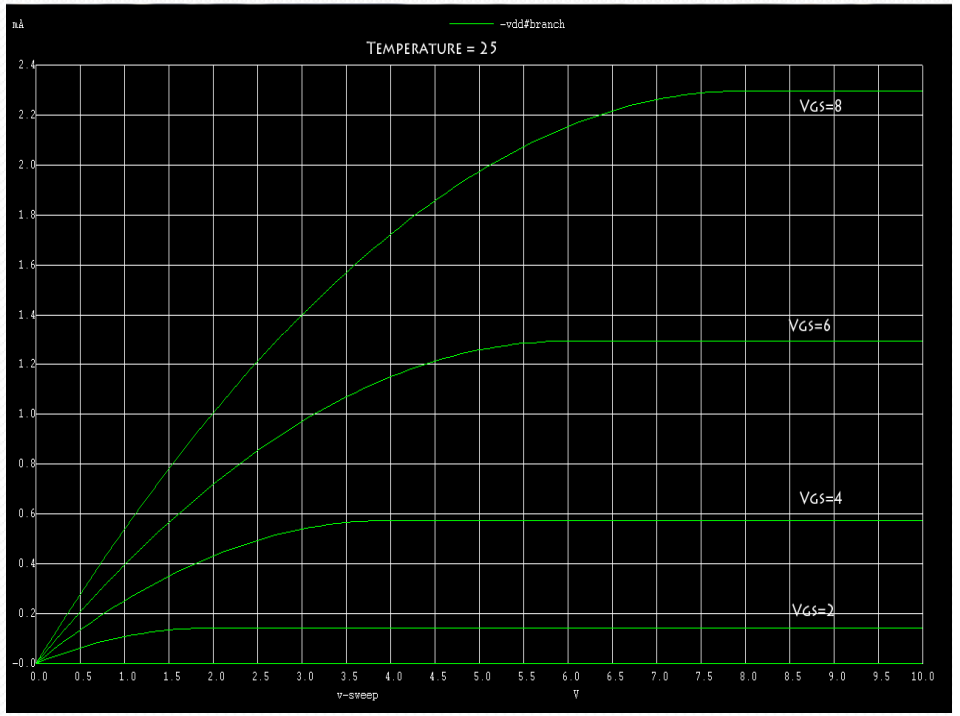
I_d vs V_{gs}

TEMP = o

I_d vs V_{ds}

Variation with Temperature



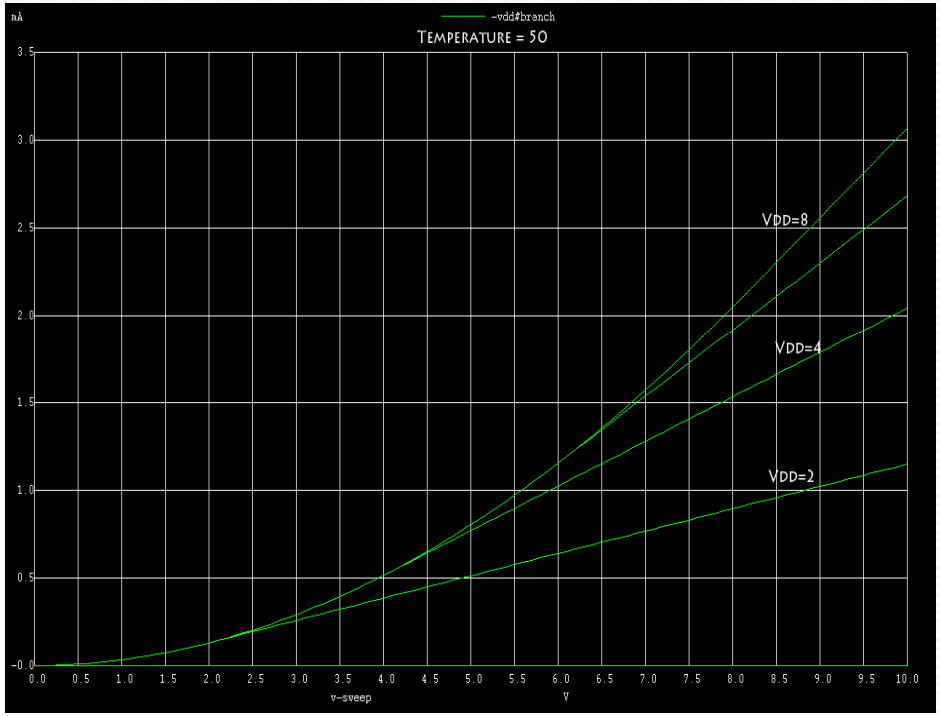


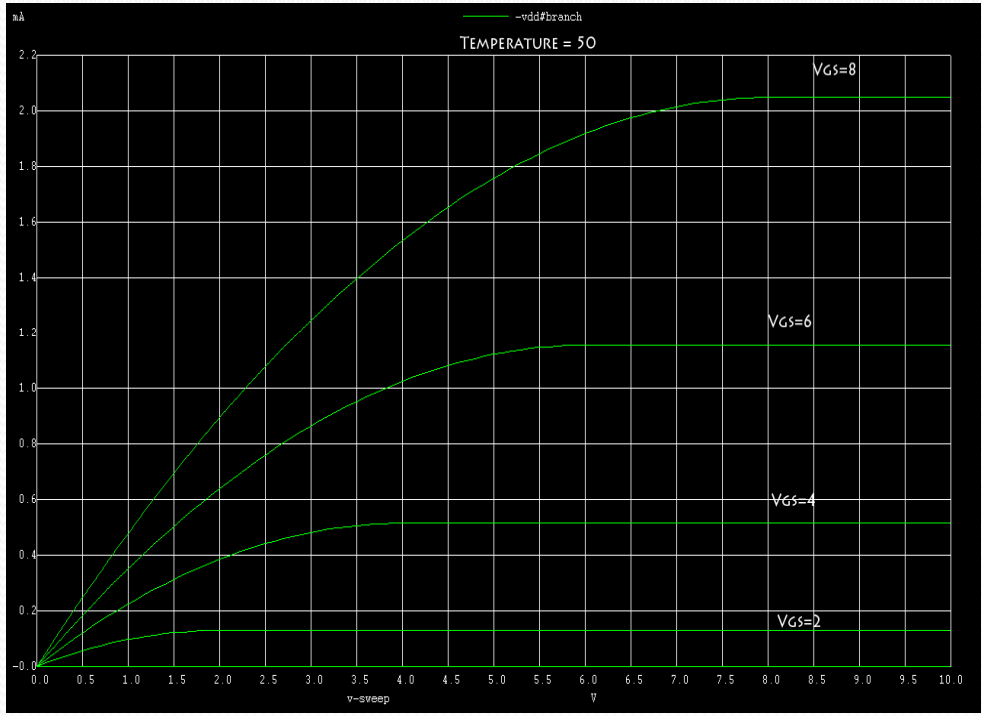
I_d vs V_{gs}

TEMP = 25

I_d vs V_{ds}

Variation with Temperature





I_d vs V_{gs}

TEMP = 50

I_d vs V_{ds}

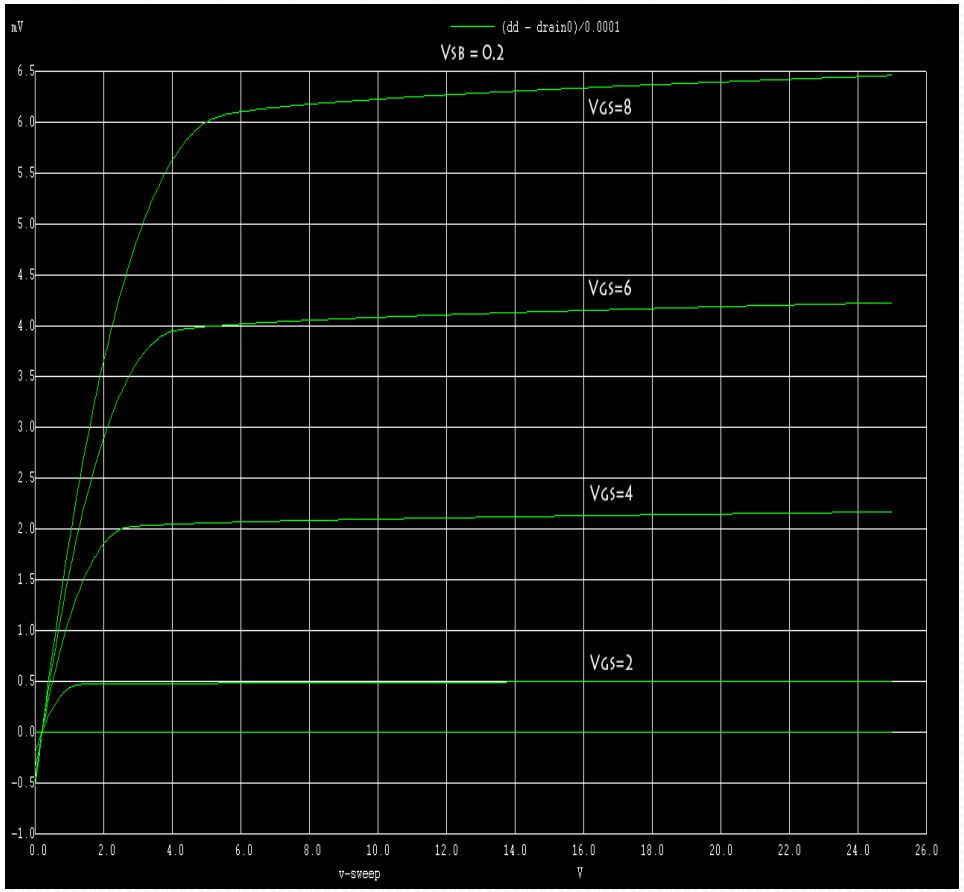
Variation with Temperature

Conclusion :

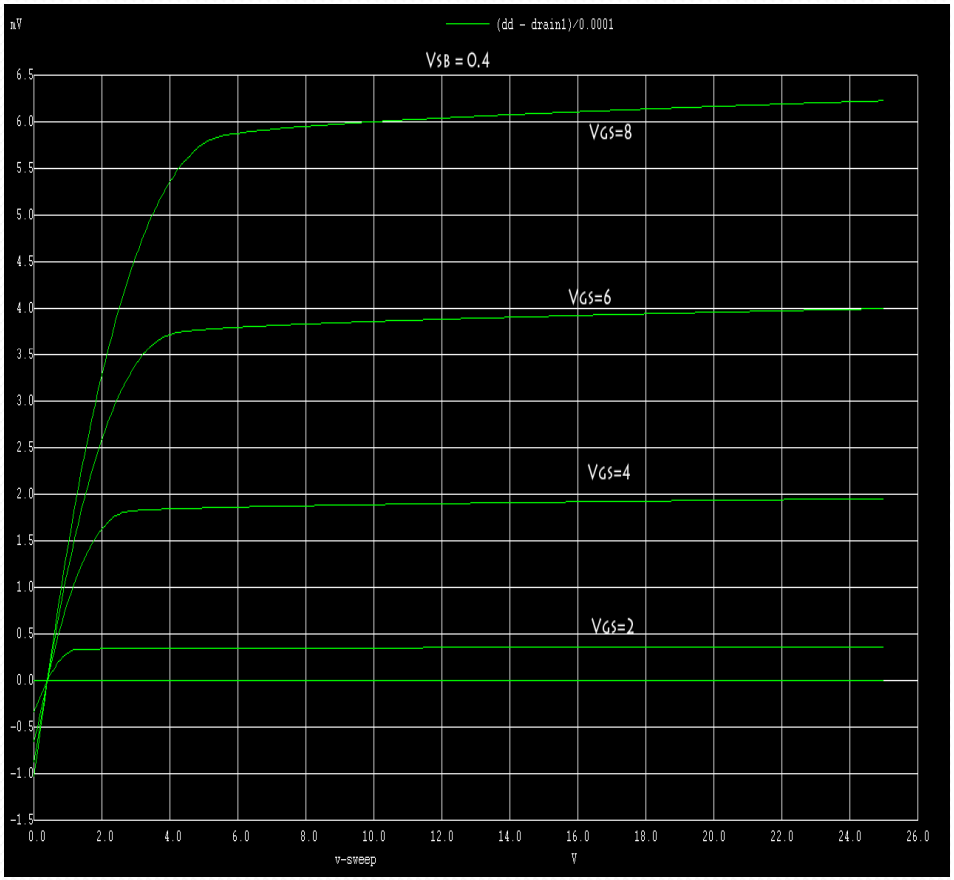
As the value of temperature increases, the current decreases. This holds true for both Vdd sweep as well as Vgg sweep.

Hence, the current is inversely proportional to the temperature.

Variation with V_{sb}

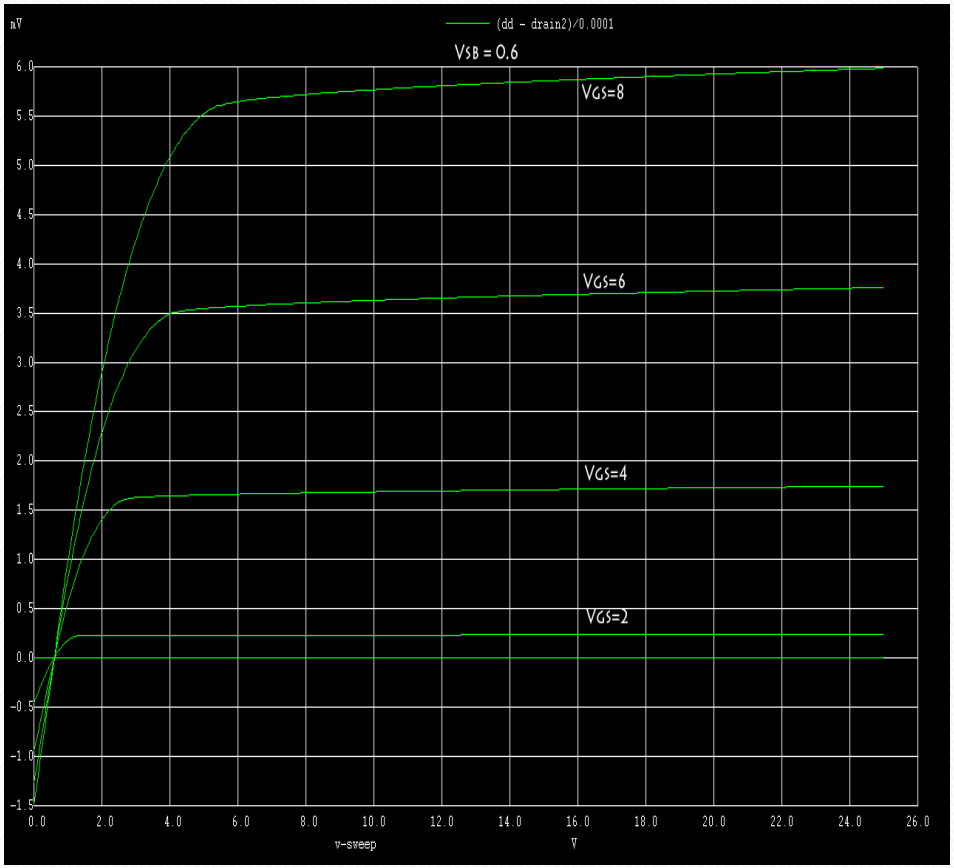


V_{sb} = 0.2 V



V_{sb} = 0.4 V

Variation with V_{sb}



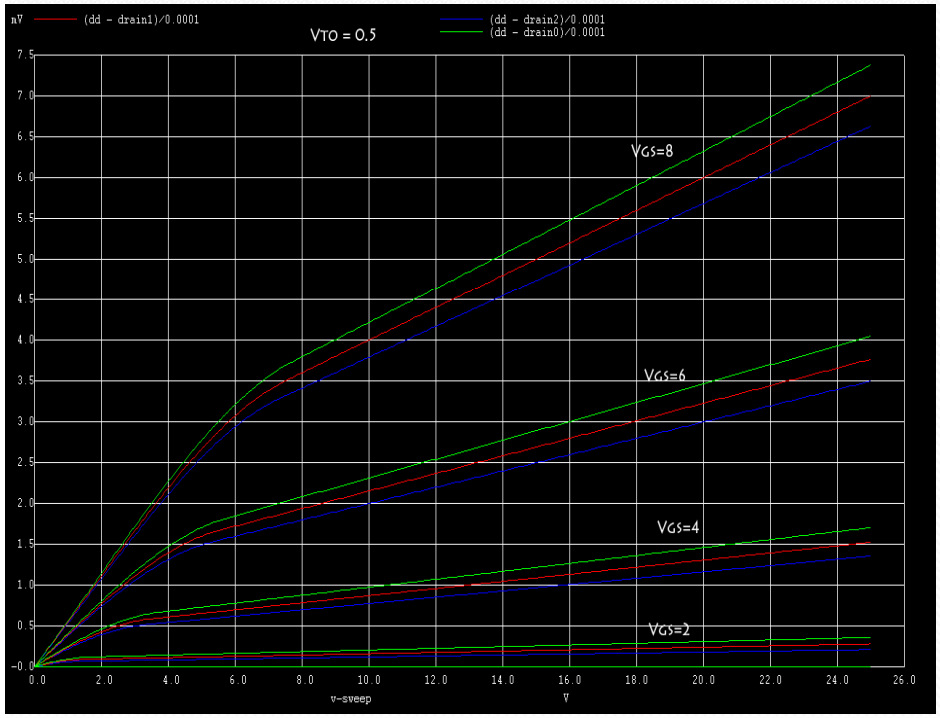
V_{sb} = 0.6 V

Conclusion :

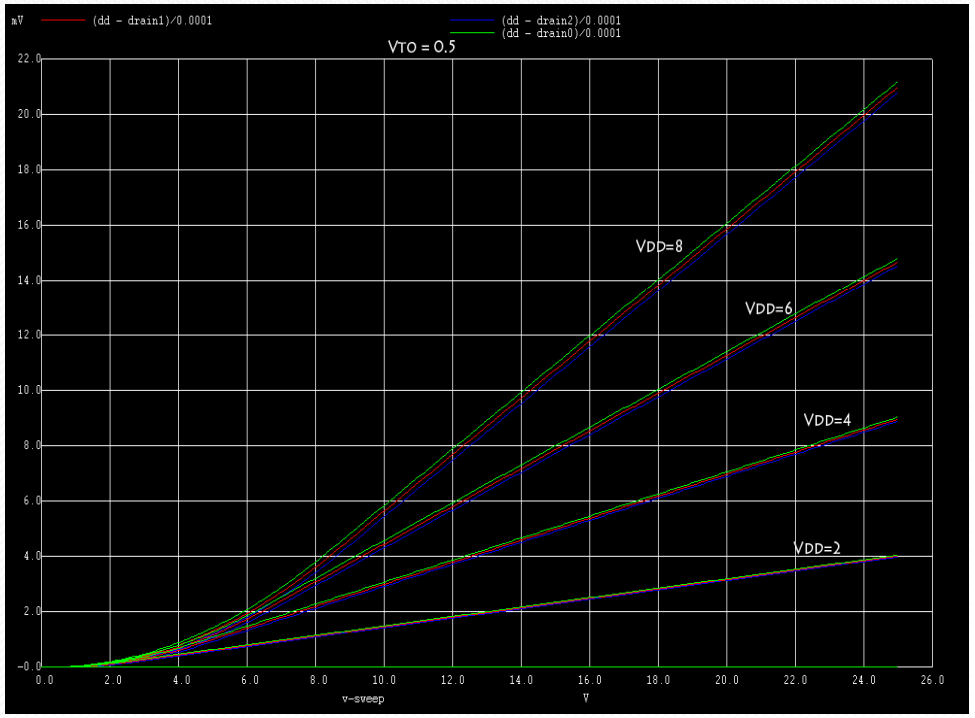
As the value of V_{sb} increases, the current decreases. This holds true for both Vdd sweep as well as Vgg sweep.

Hence, the current is inversely proportional to V_{sb}.

Variation with V_{To}



I_d vs V_{ds}



I_d vs V_{gs}

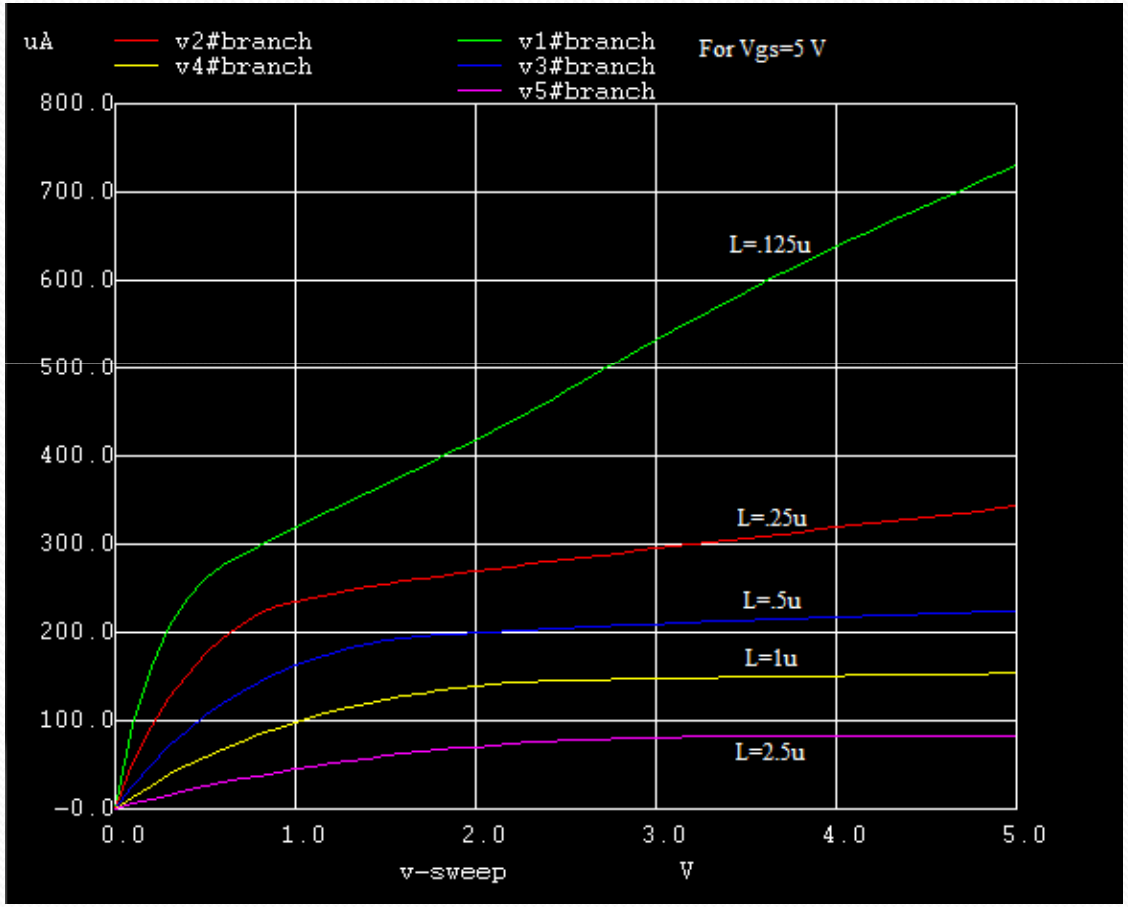
Variation with V_{To}

Conclusion :

As the value of V_{To} increases, the current decreases. This holds true for both Vdd sweep as well as Vgg sweep.

Hence, the current is inversely proportional to V_{To}.

Variation with length

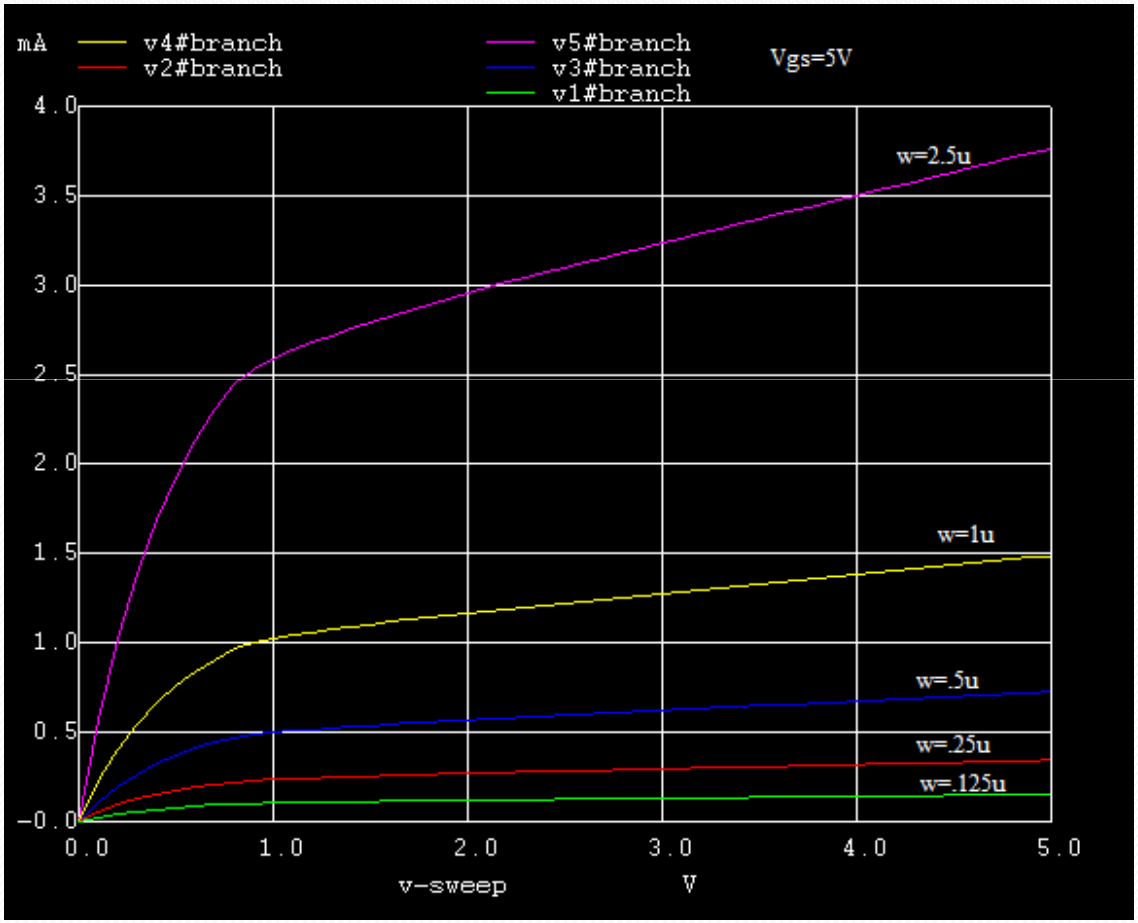


Conclusion :

As the value of length increases, the current decreases. This holds true for both Vdd sweep as well as Vgg sweep.

Hence, the current is inversely proportional to length.

Variation with width



Conclusion :

As the value of width increases, the current increases. This holds true for both Vdd sweep as well as Vgg sweep.

Hence, the current is directly proportional to width.

Experiment 2:

Study of MOS inverter with passive resistive load

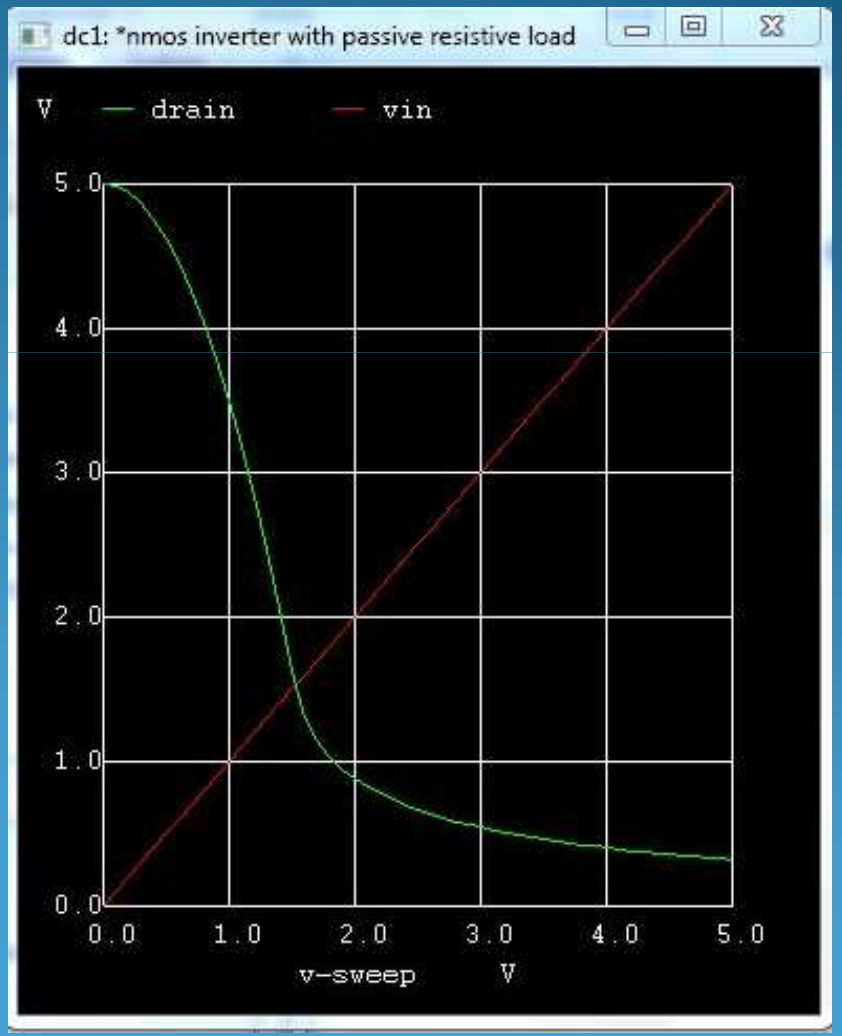
Objective:

Study the transfer function, Noise margin, effect on rise time, fall time, propagation delay, power and energy consumed of a MOS Inverter for various L, W of the transistor, load capacitance and rise/fall time of input

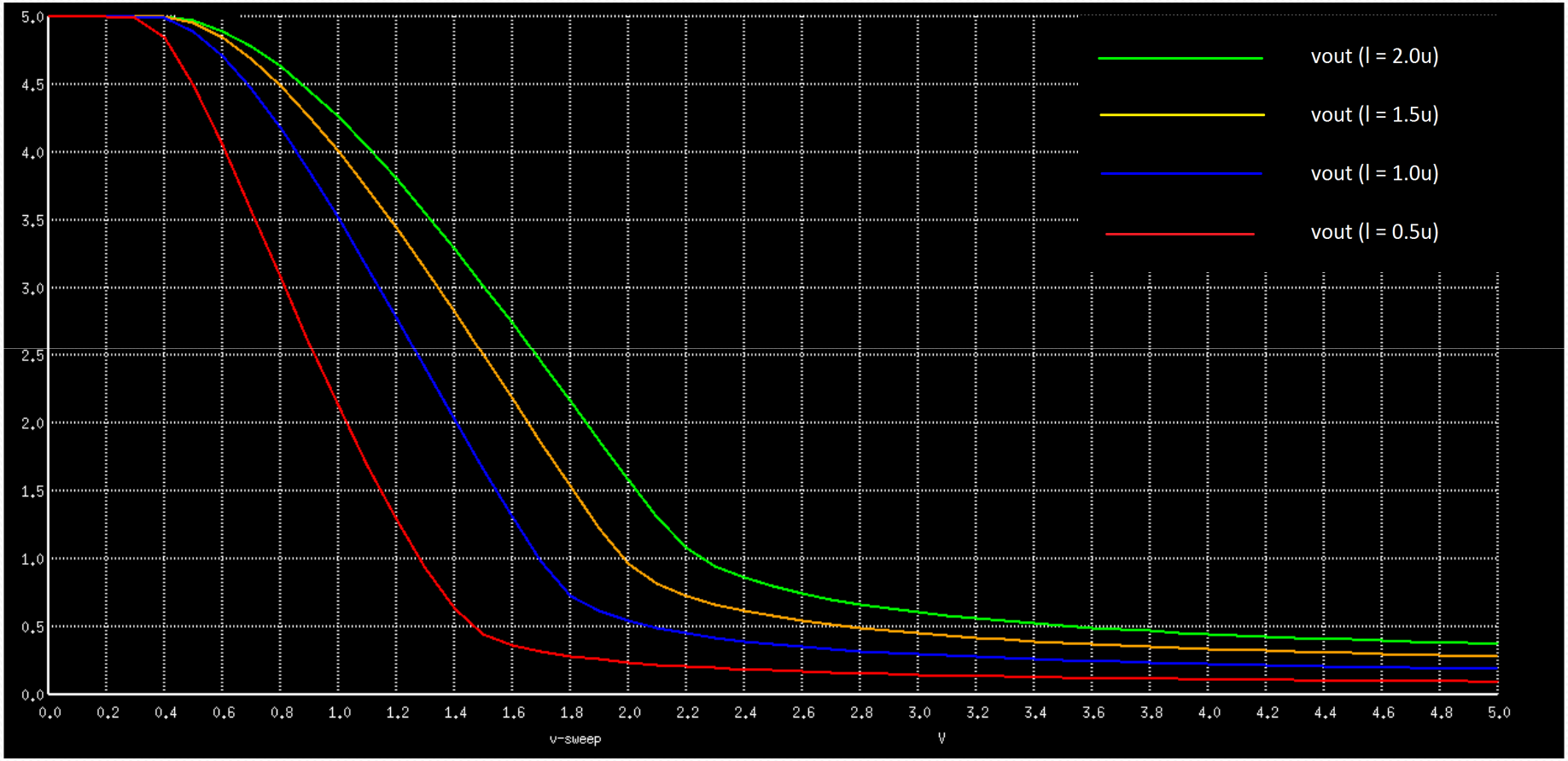
Vout vs Vin for an NMOS with resistive load

```
*nmos inverter with passive resistive load
.include tsmc_025_level3.model
*spice netlist
m1 drain vin 0  0  cmosn l=.25u w= .75u
*resistance
r1 drain vd 20k
*supply source
vdd vd 0 dc 5
vgg vin 0 dc 5
*responses
.dc vgg 0 5 0.1
*vgg pulse (0 5 0 0.1ns 0.1ns 50ns 100ns)

.control
run
Setplot dc1
Plot drain vin
.endc
.end
```

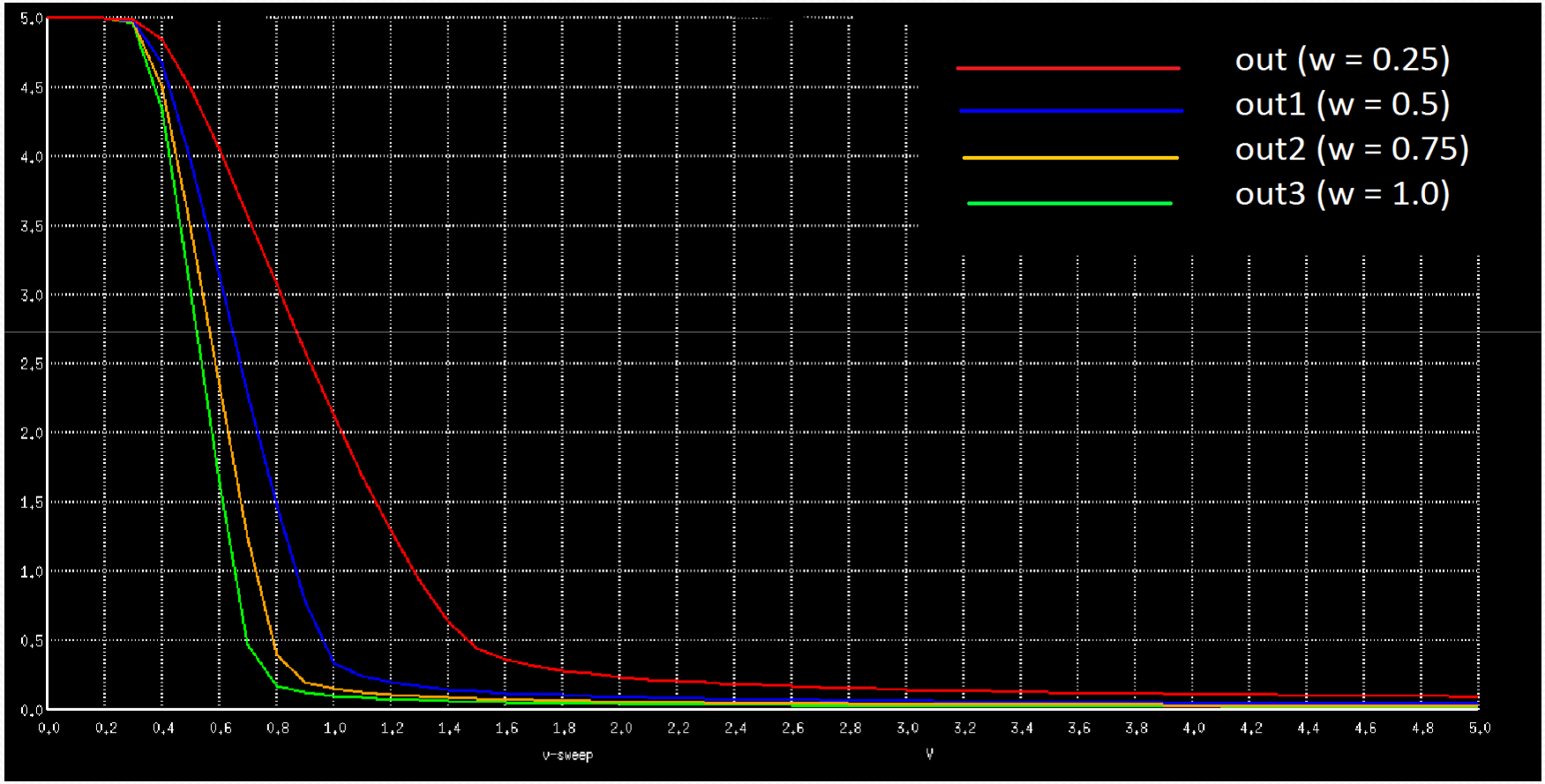


Transient response for inverter with variation in length



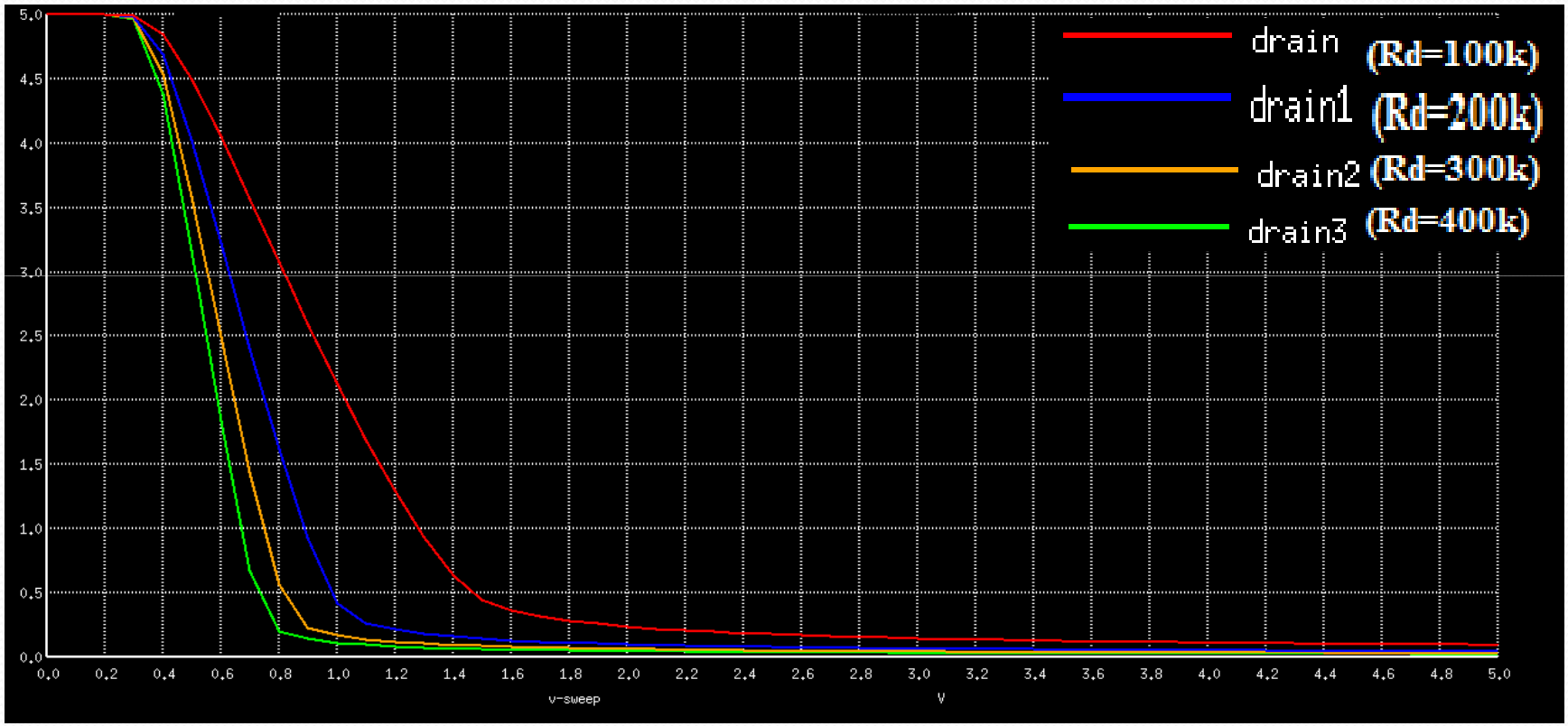
With decrease in length we have stronger ON

Transient response for NMOS with varying length



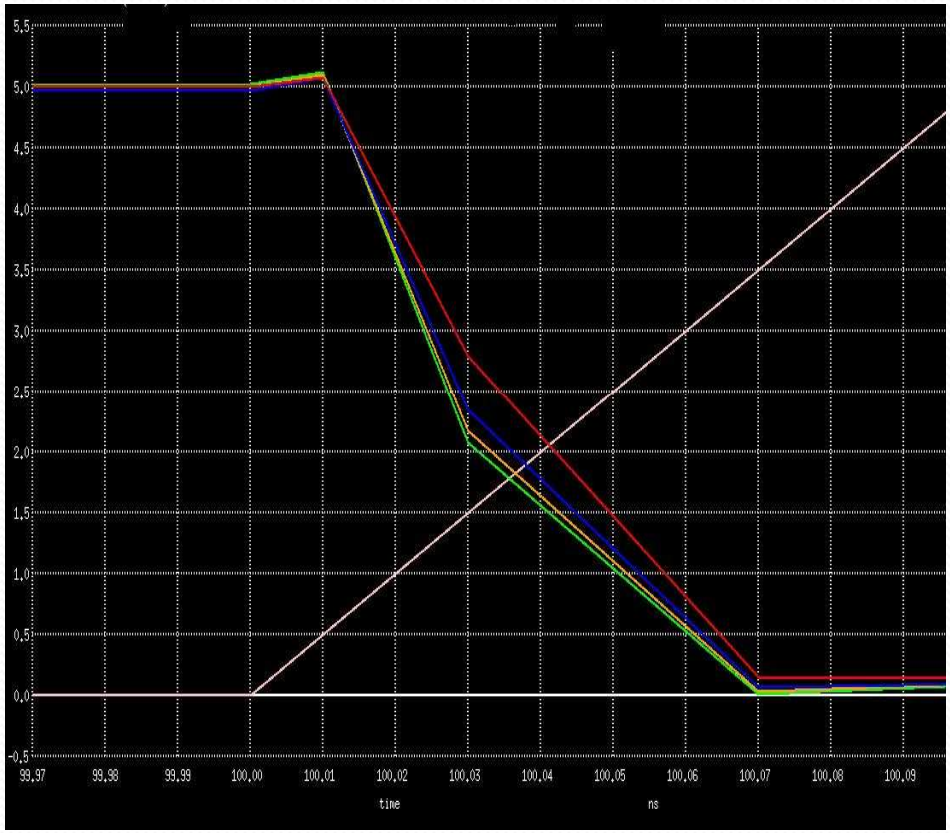
- Graph shows that V_{ih} increases with increase in width

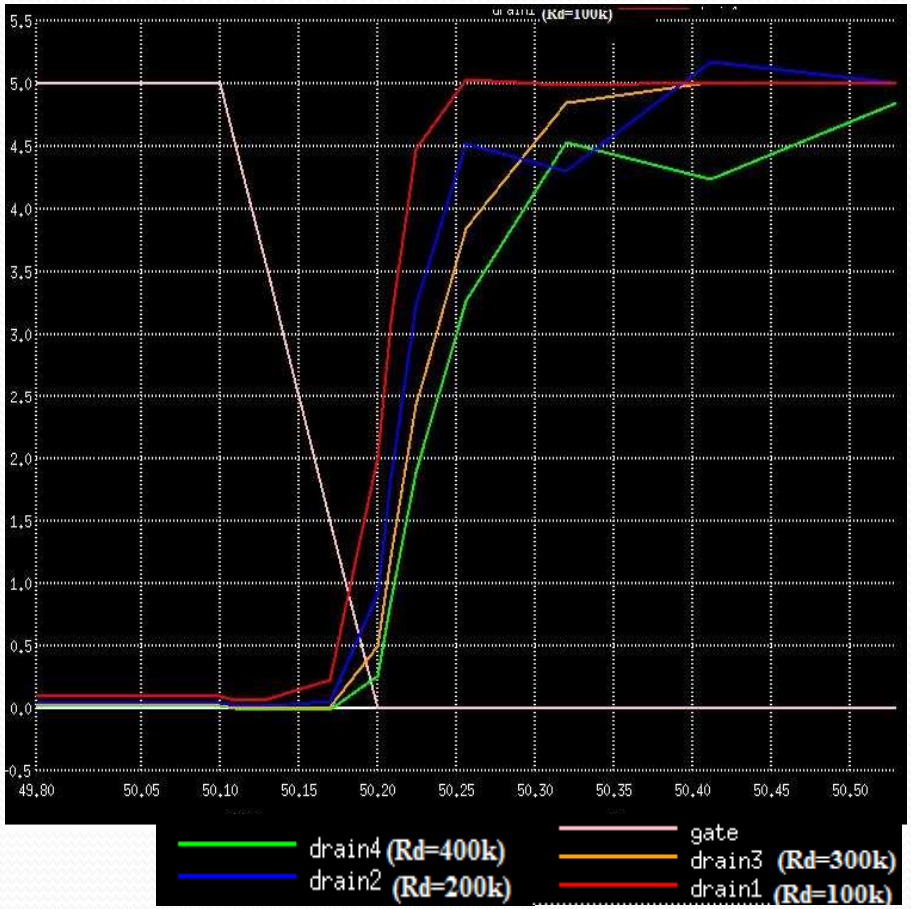
Transient response with varying resistance



- With increase in resistance Noise Margin Low also decreases
- But gain increases

Effect of change resistance on rise time and fall time

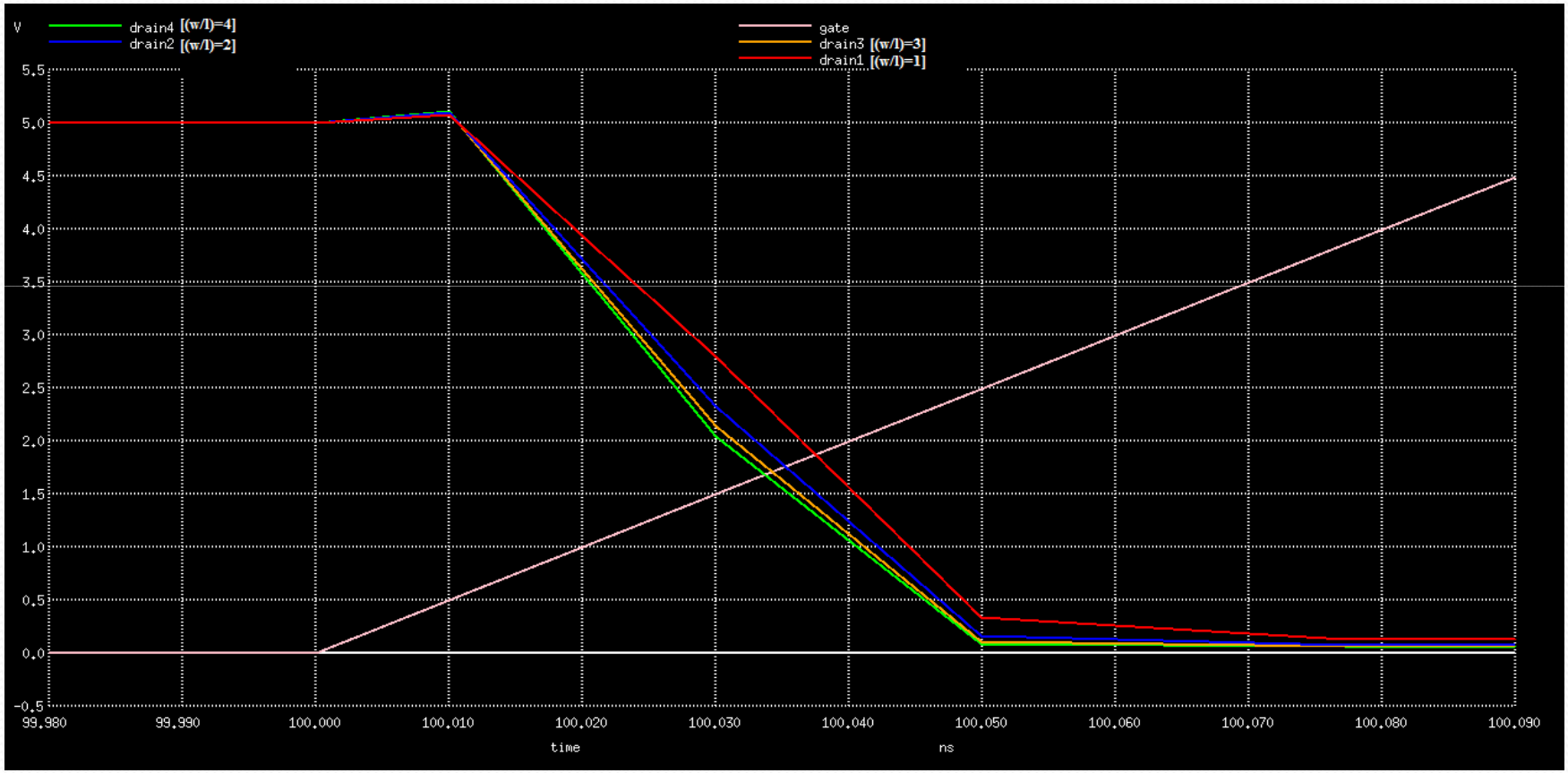




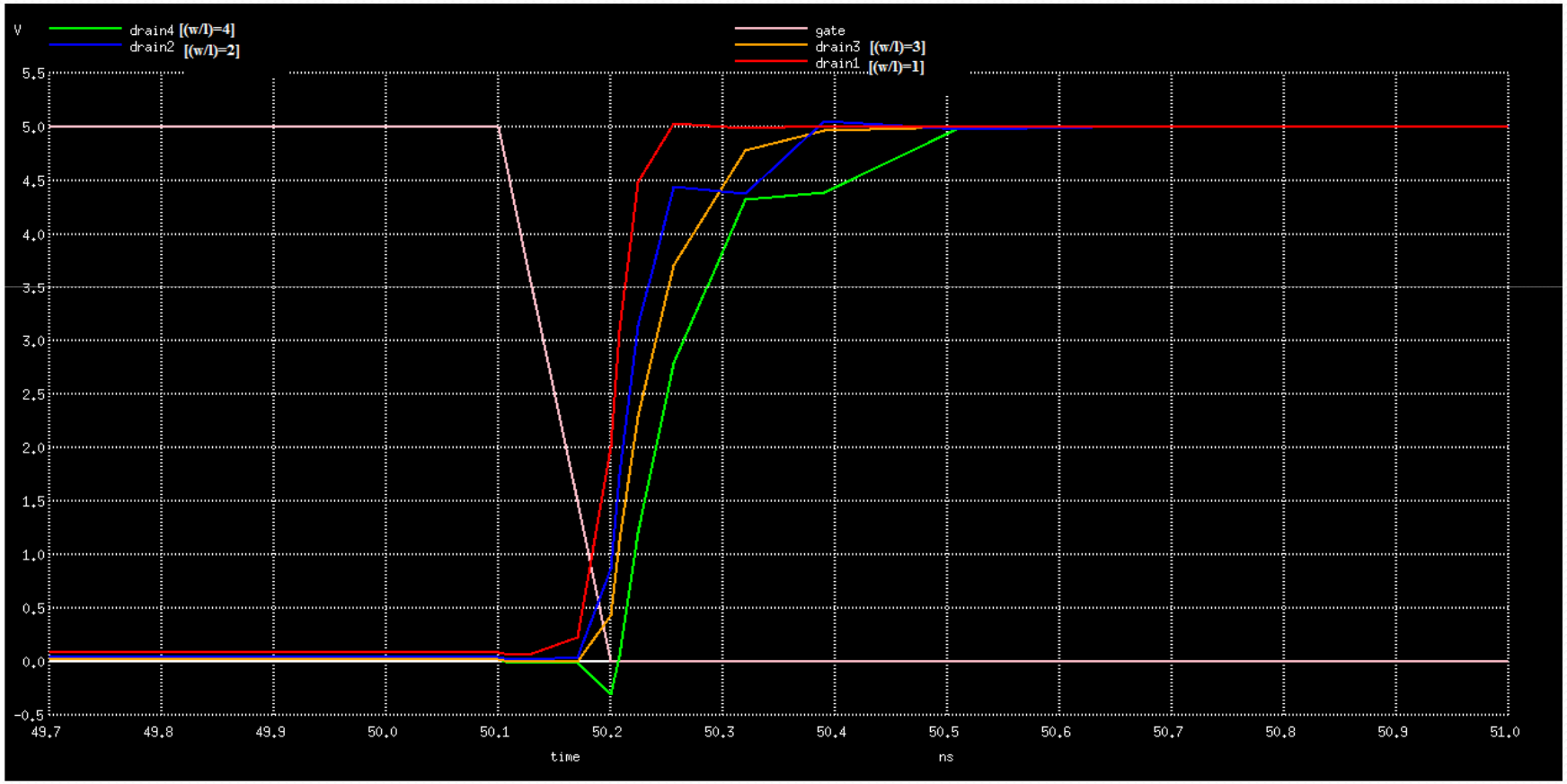
- Fall time decreases with increase in Resistance
- Rise time decreases with increase in Resistance

Effect of change in W/L ratio on rise time and fall time

1. Fall time

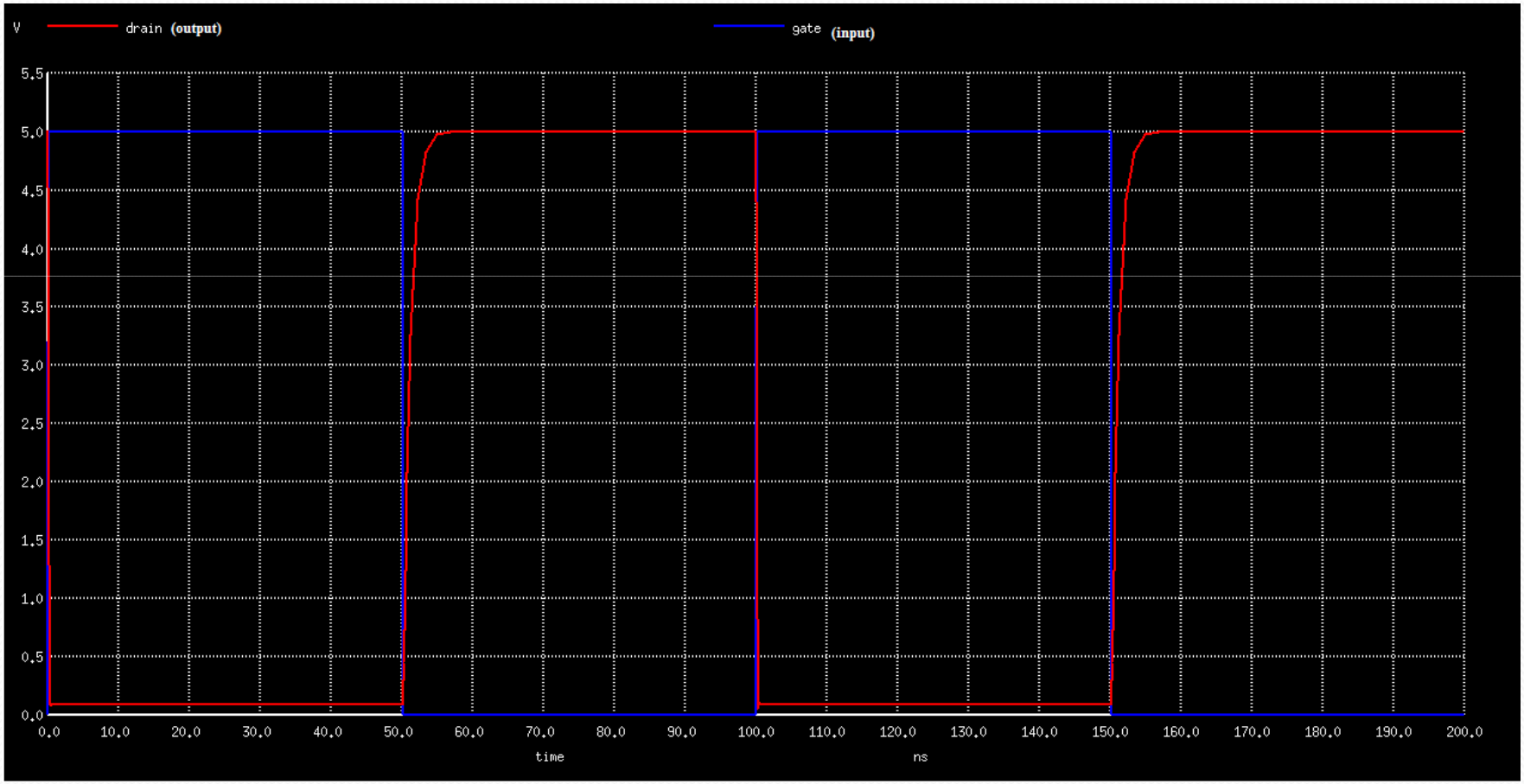


2. Rise time

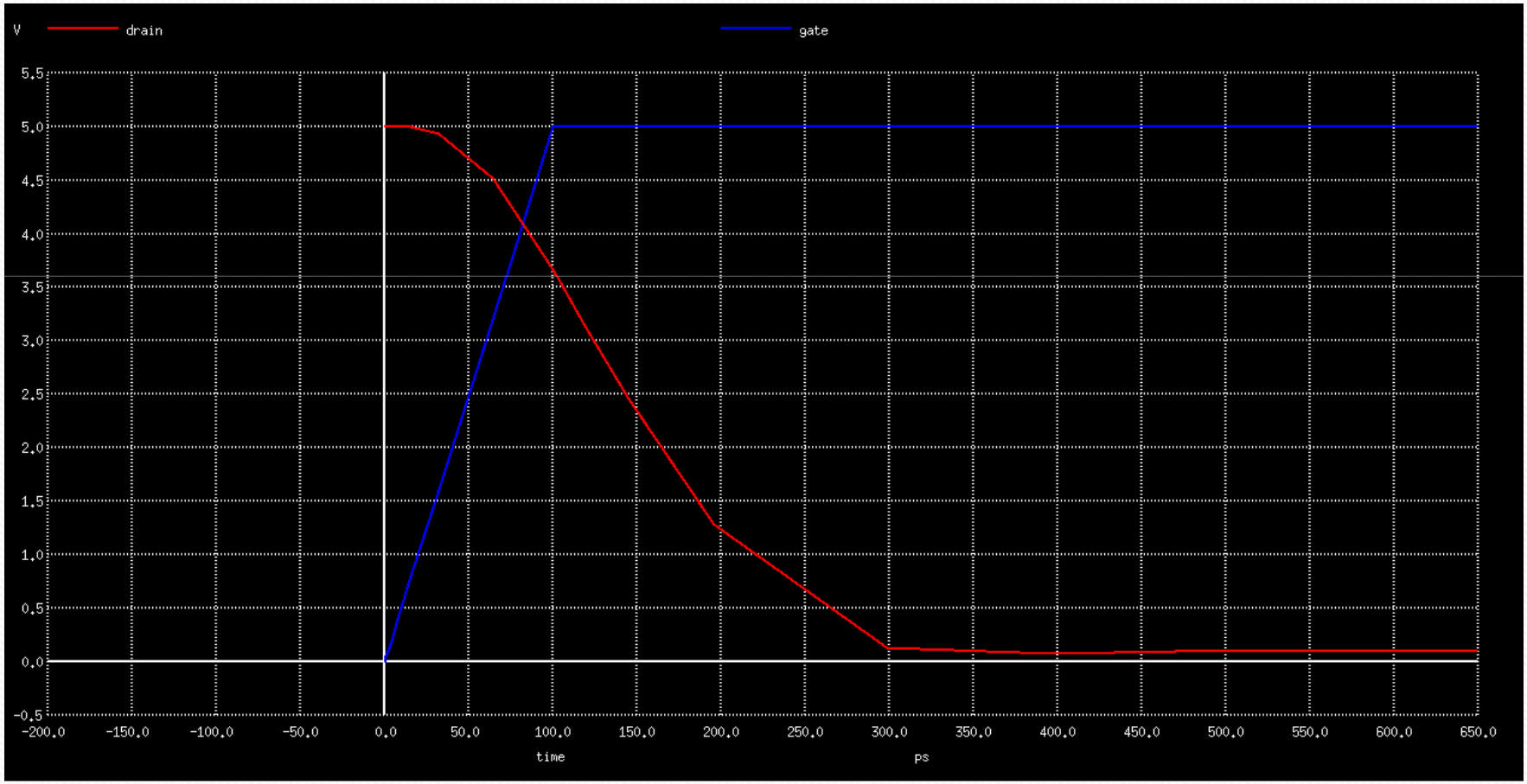

V
drain4 [(w/l)=4]
drain2 [(w/l)=2]
gate
drain3 [(w/l)=3]
drain1 [(w/l)=1]
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-0.5
49.7
49.8
49.9
50.0
50.1
50.2
50.3
50.4
50.5
50.6
50.7
50.8
50.9
51.0
time
ns

Output capacitance

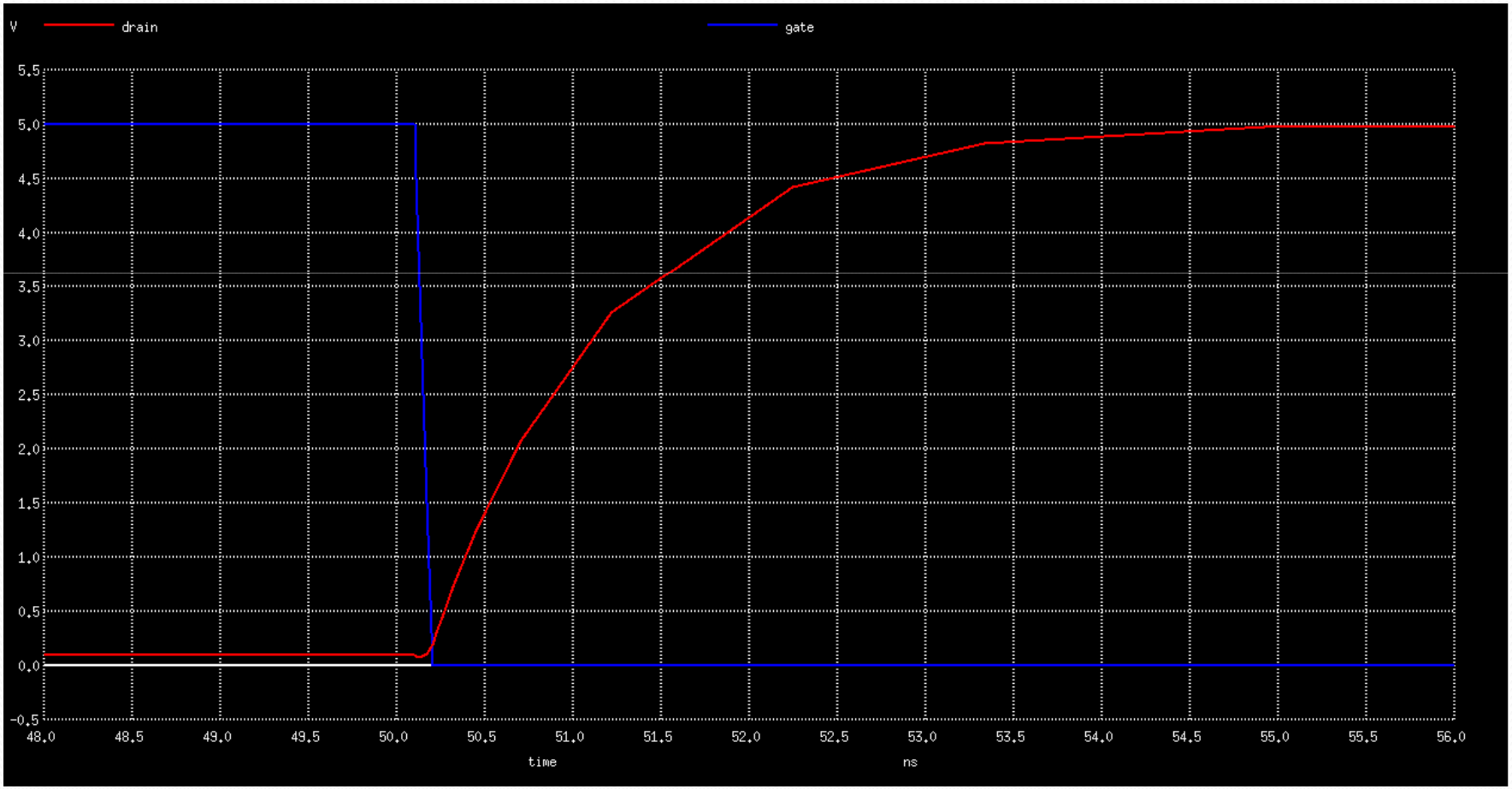
1. Vout across capacitance for square wave input



2.Vout across capacitance for low to high input



3.Vout across capacitance for high to low input



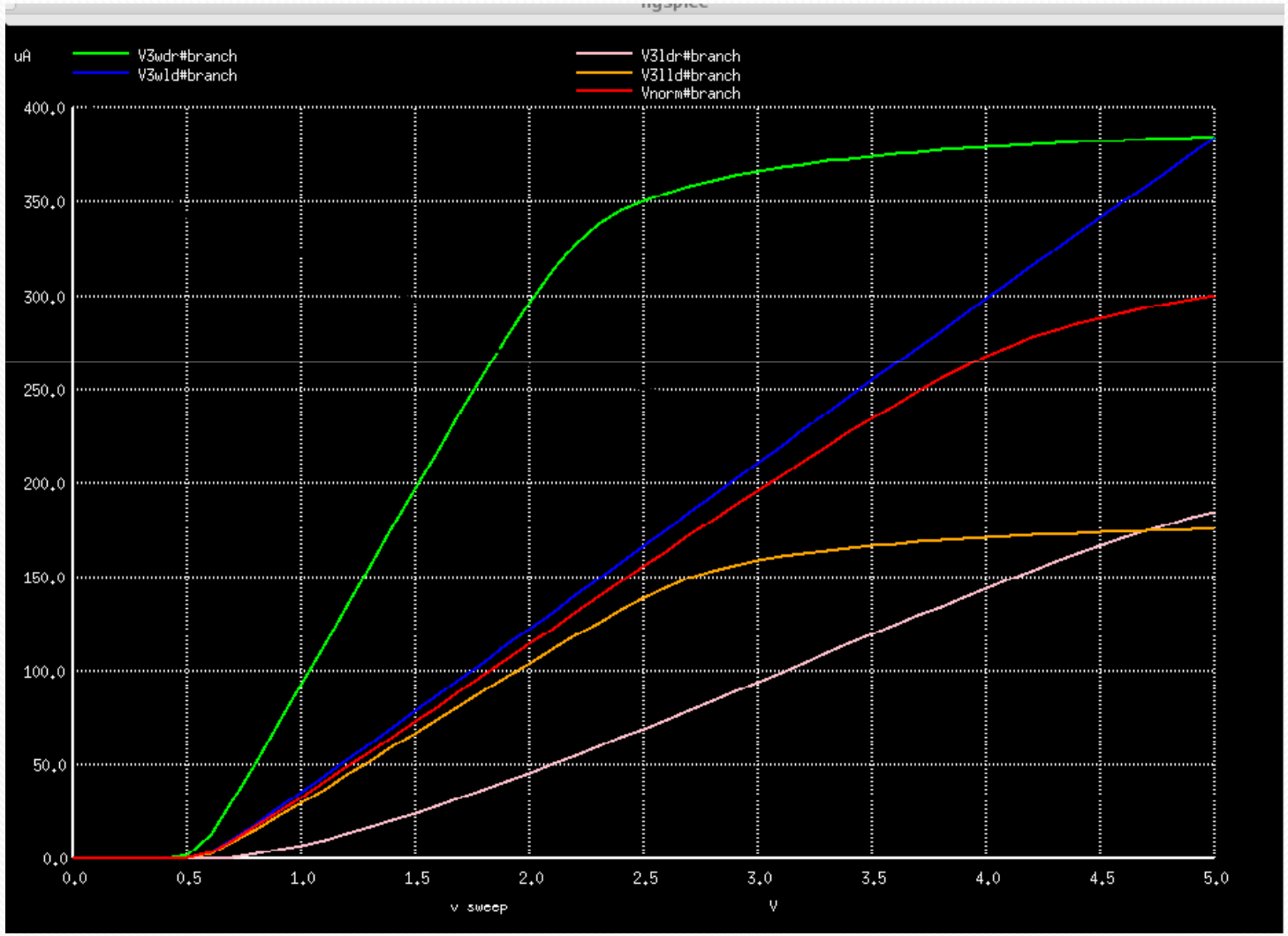
Experiment 3:

Study of MOS Inverter with active load – NMOS and PMOS

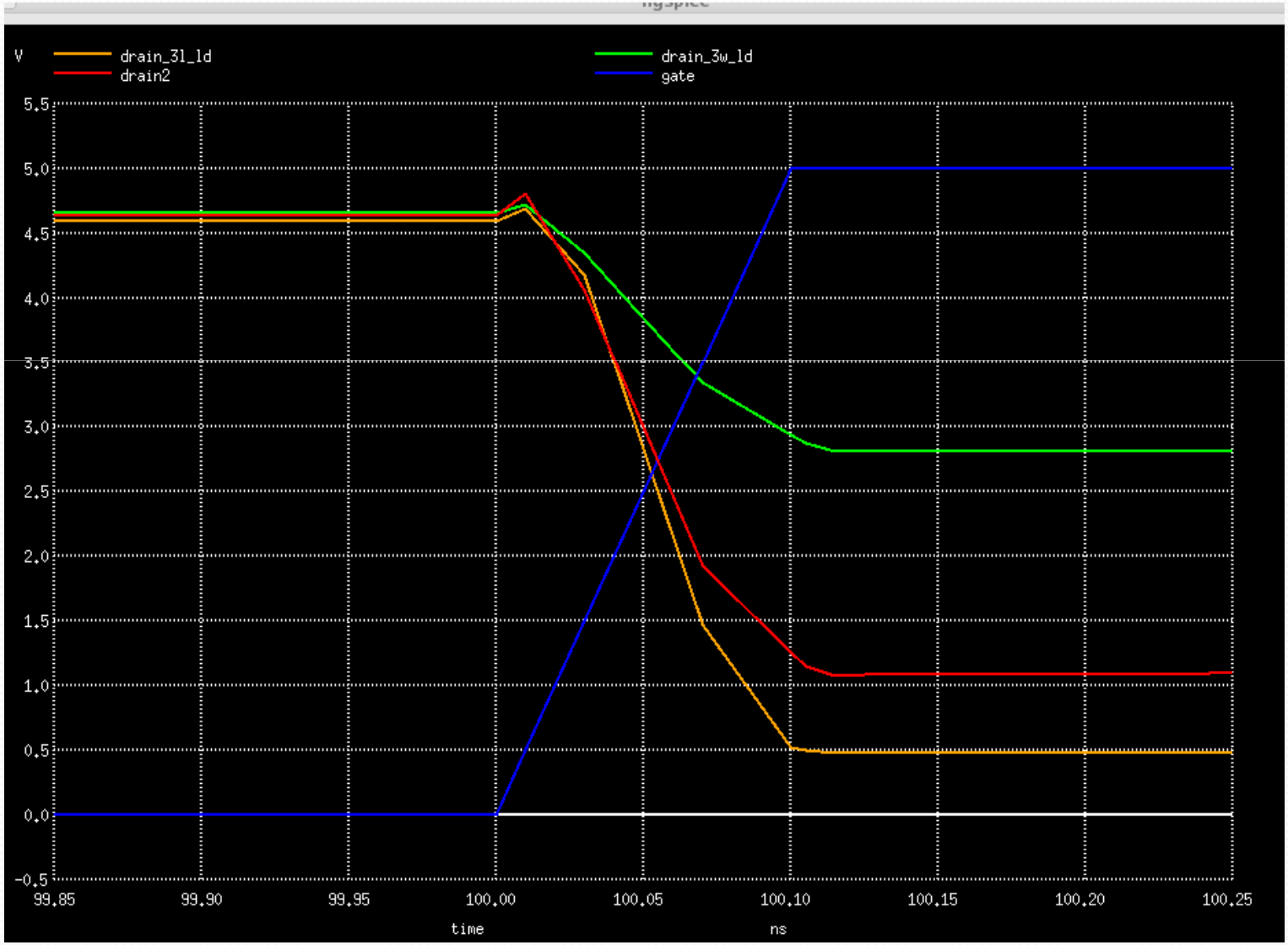
Objective:

For a MOS Inverter with active load – NMOS and PMOS, study the Noise Margin, effect on rise time, fall time, propagation delay, power and energy consumed with variation in L and W.

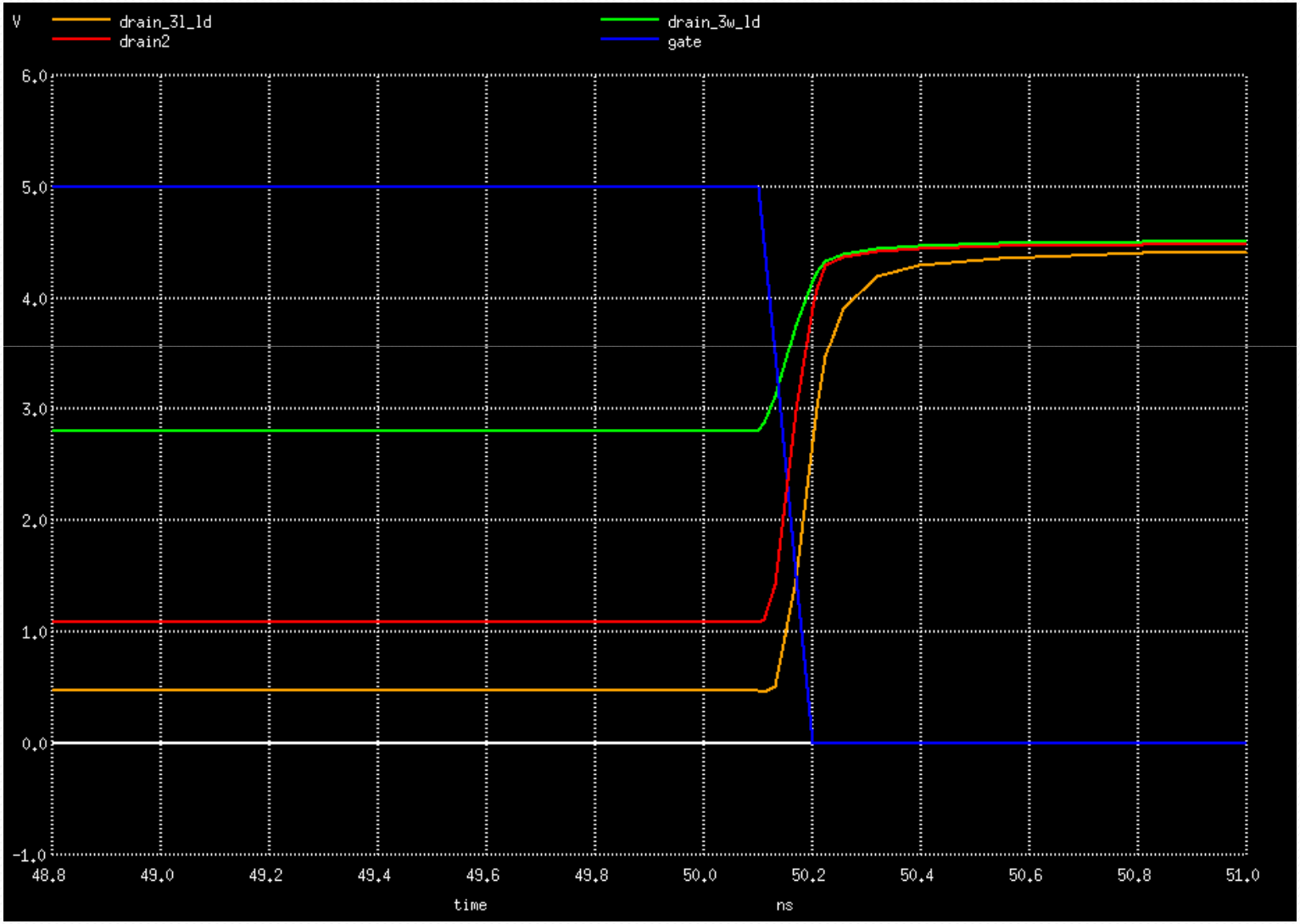
Current Variation with NMOS Load



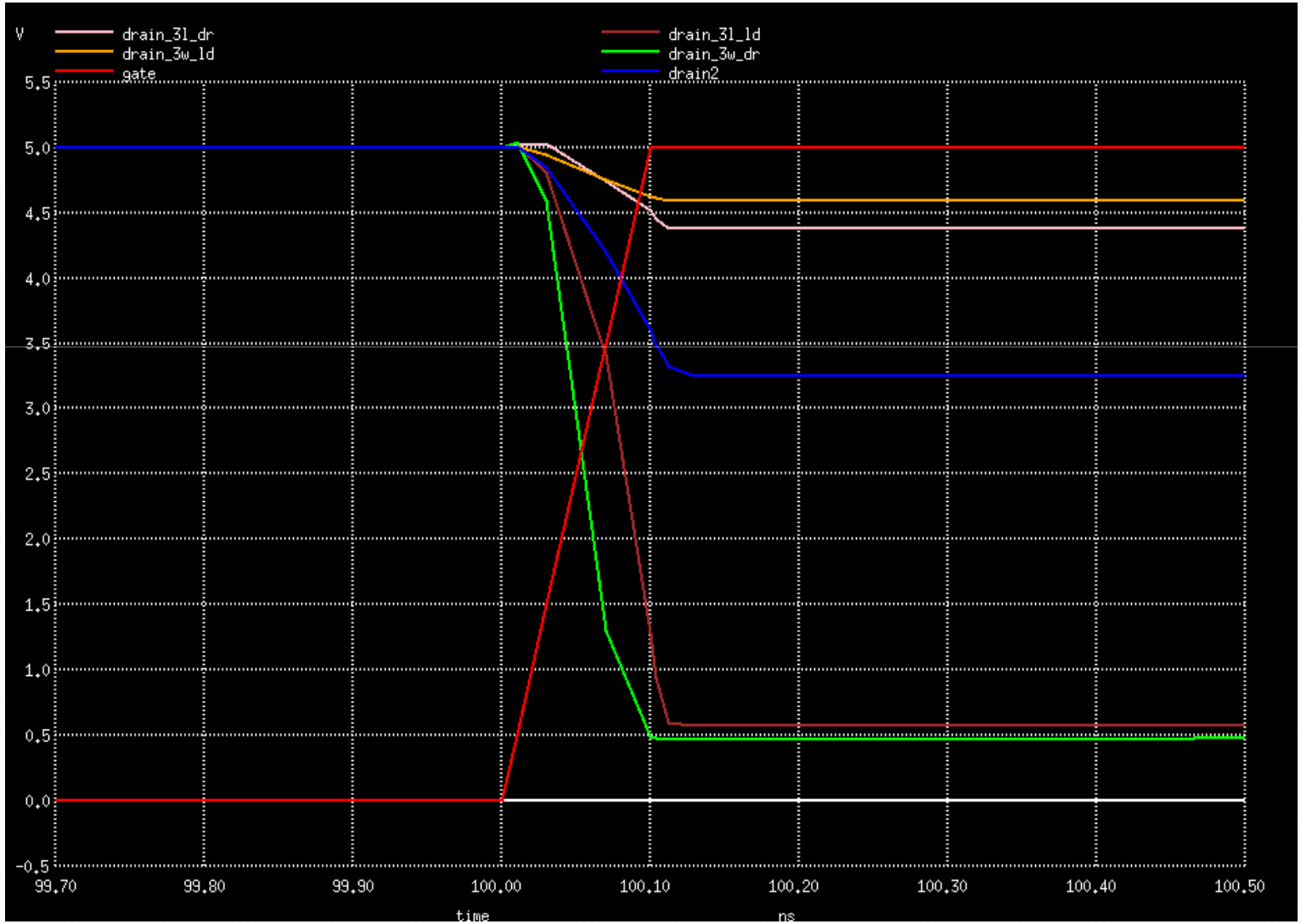
Transient Analysis with NMOS Load (Fall)



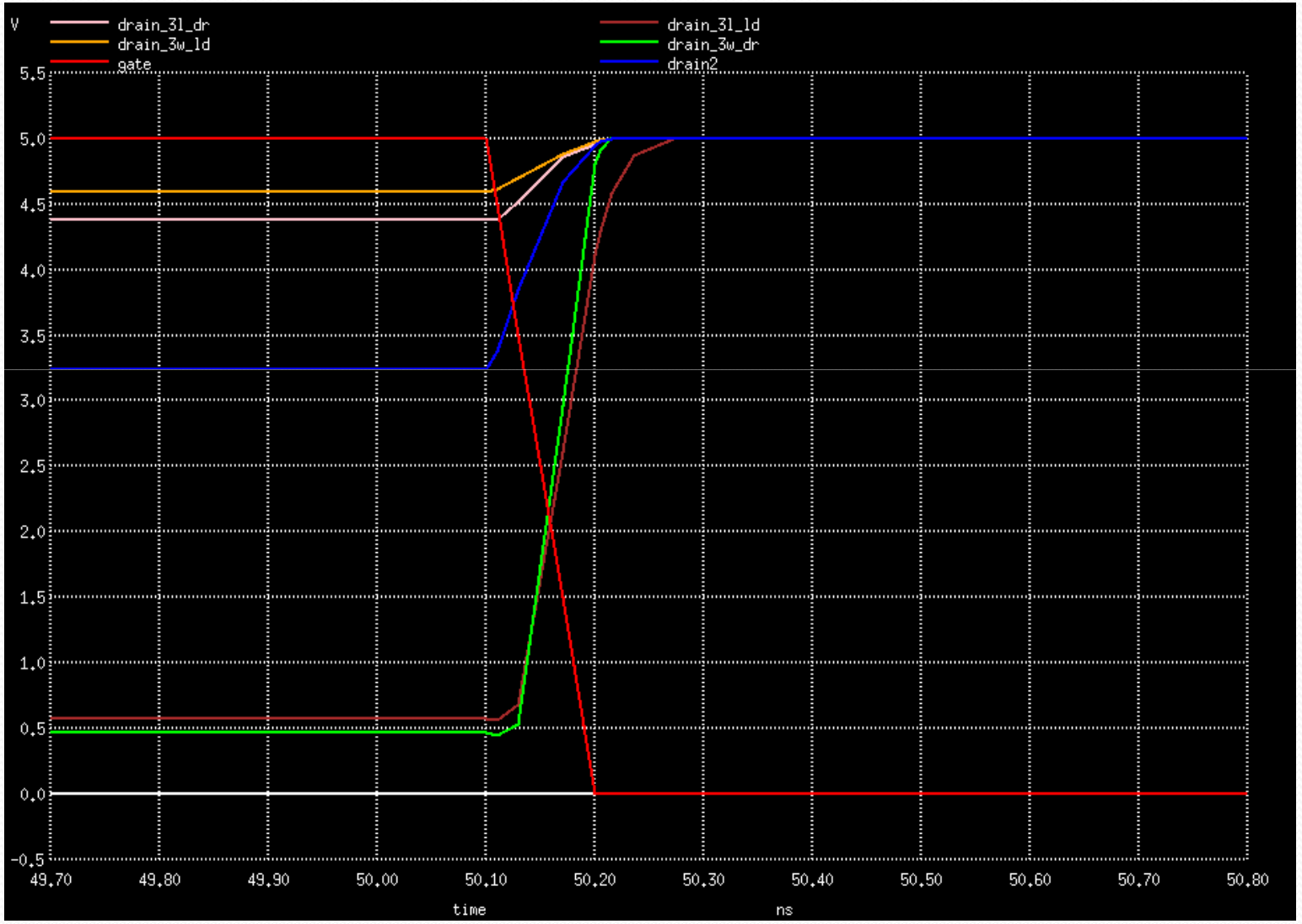
Transient Analysis with NMOS Load (Rise)



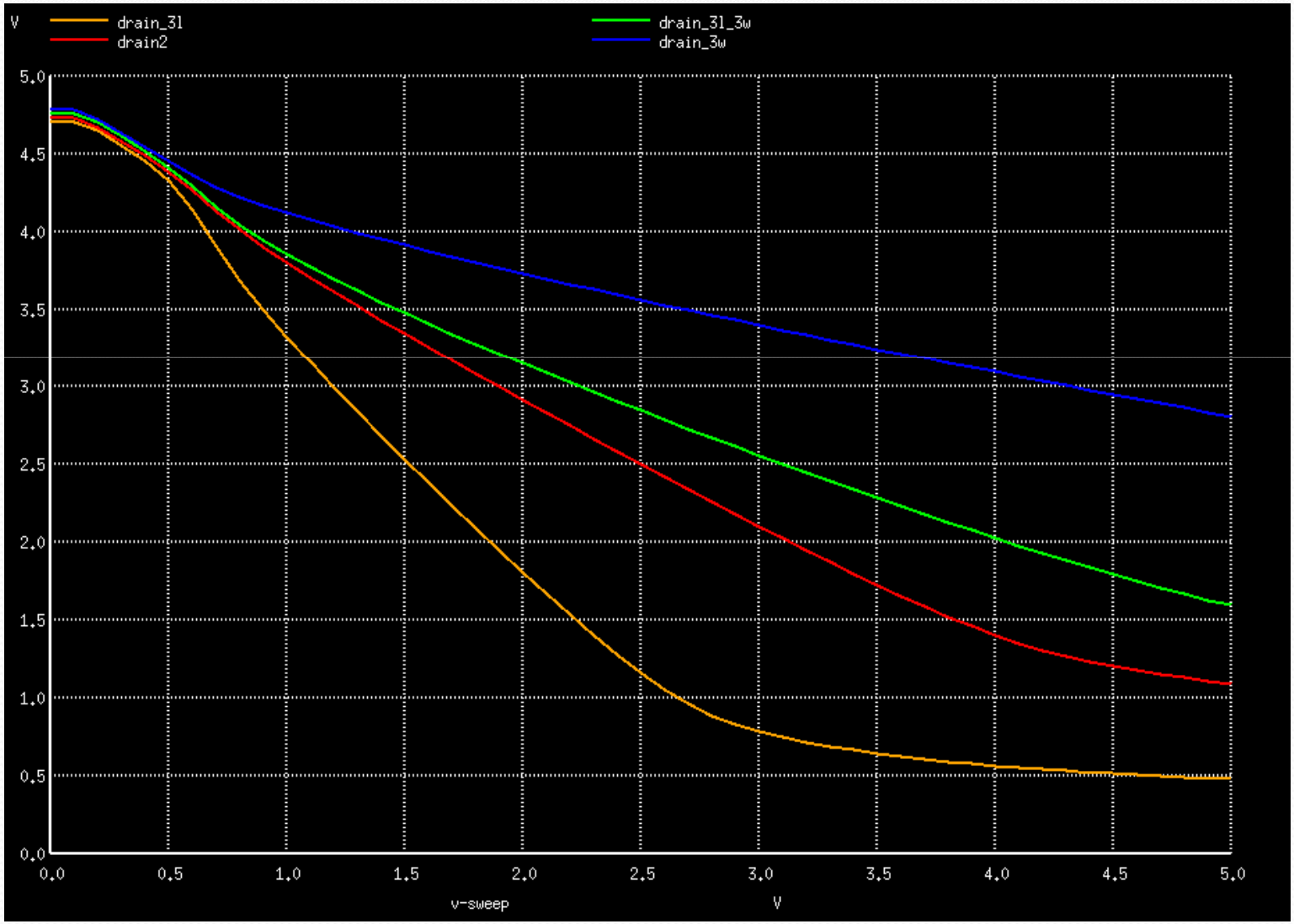
Transient Analysis with PMOS Load (Fall)



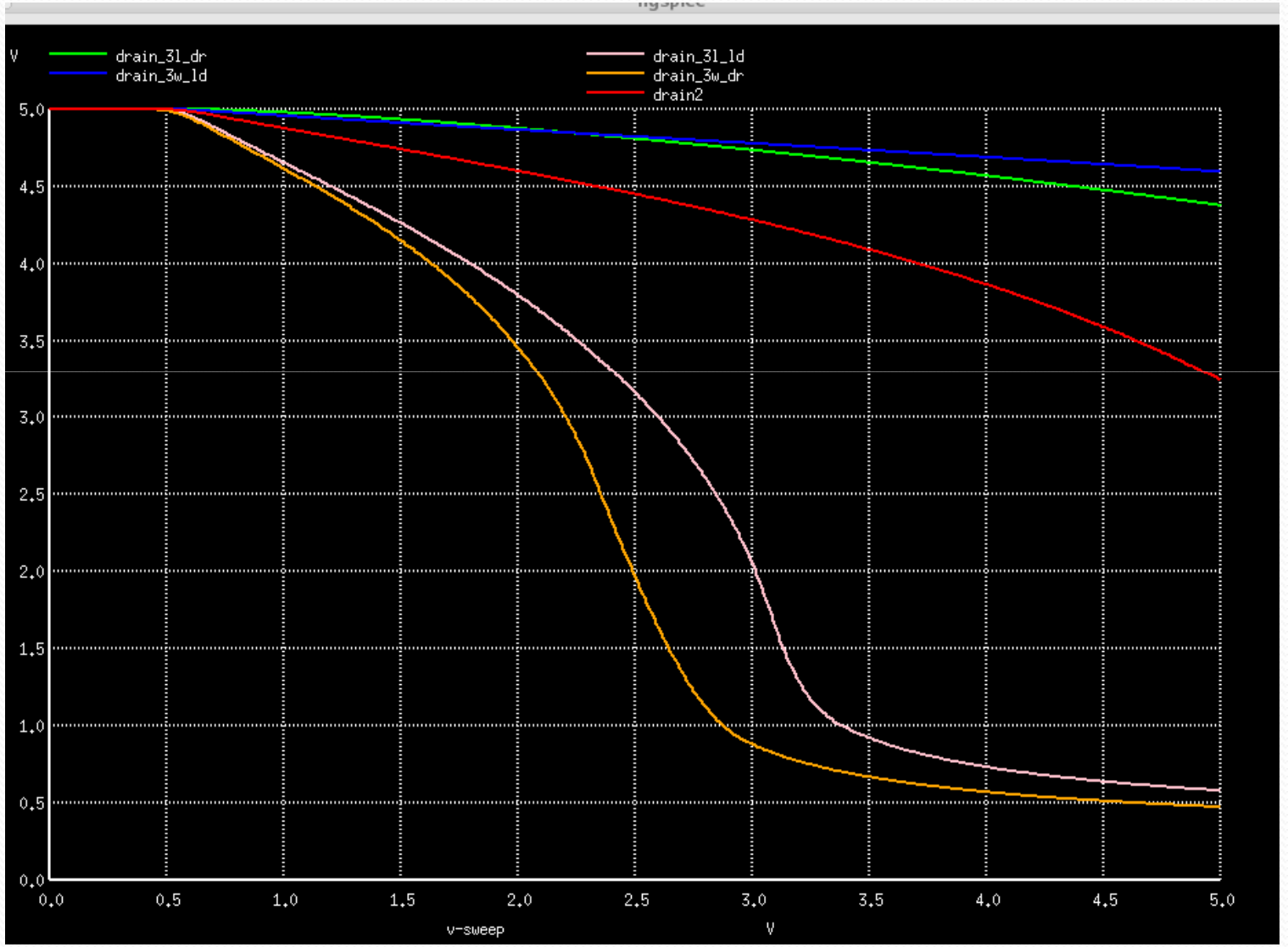
Transient Analysis with PMOS Load (Rise)



VTC for NMOS Load



VTC for PMOS Load



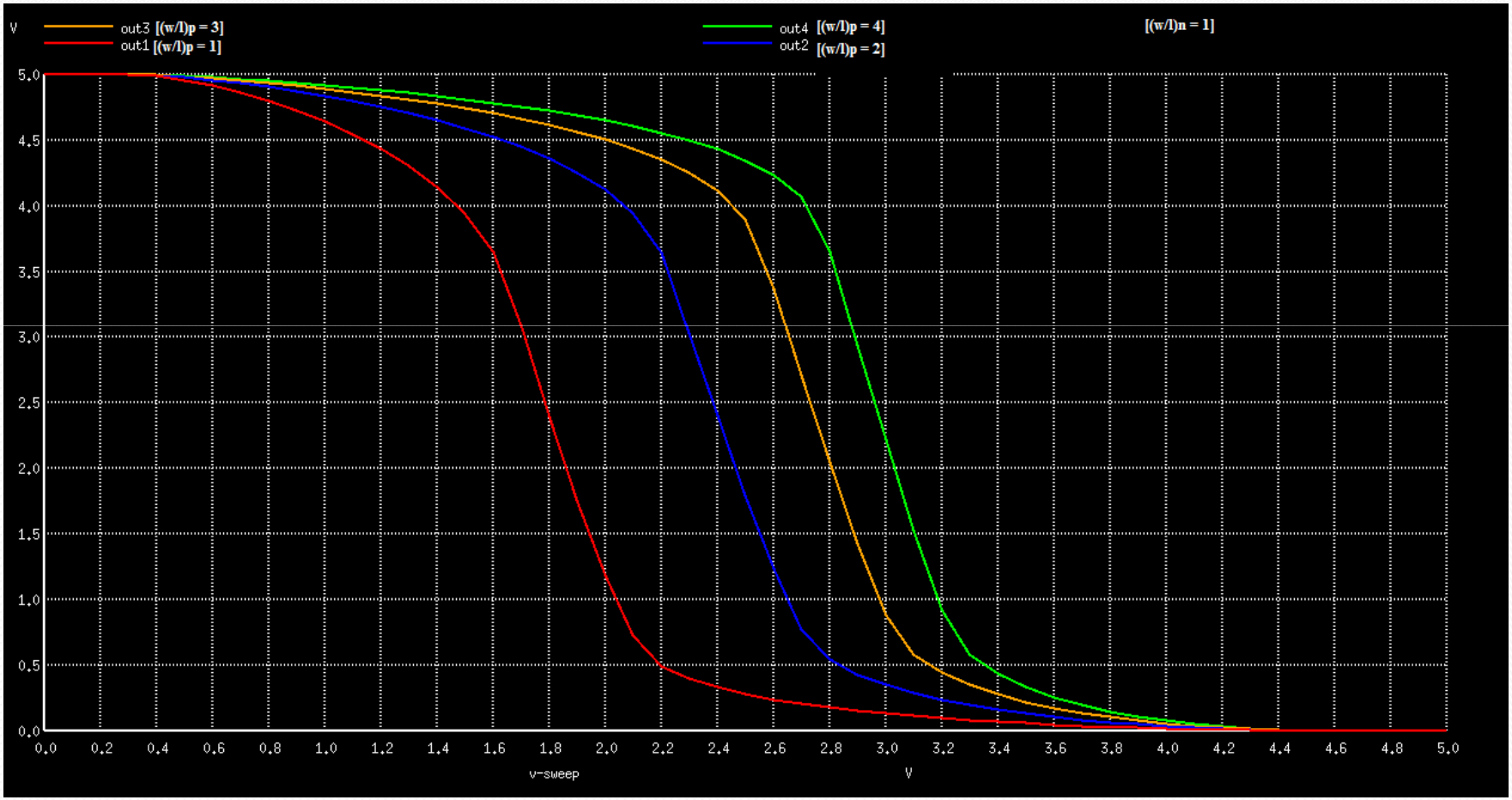
Experiment 4:

Study of CMOS Inverter

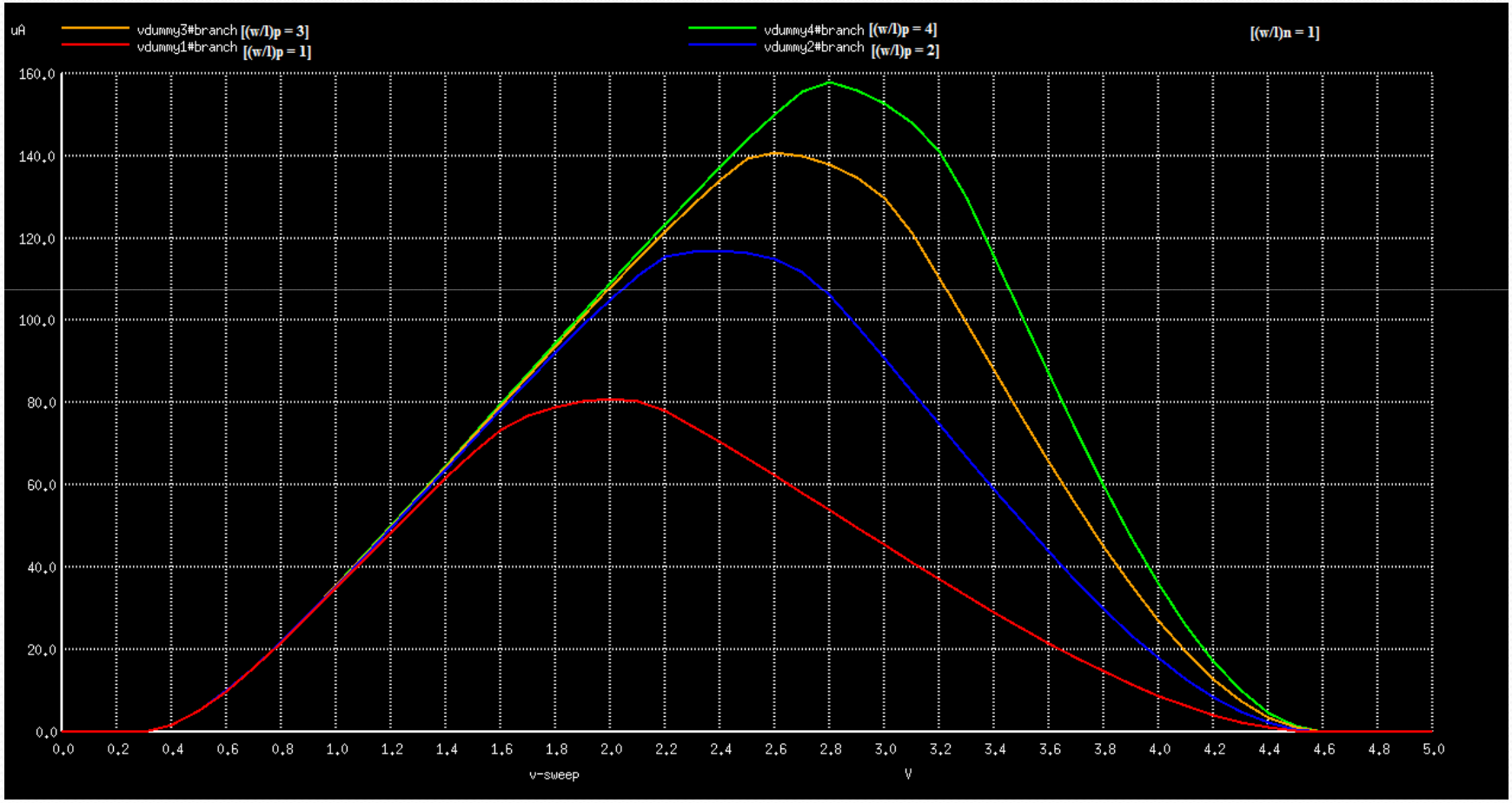
Objective:

Study the Transfer function, Noise Margin, effect on rise time, fall time, propagation delay, power and energy consumed of a CMOS inverter with variation in L and W.

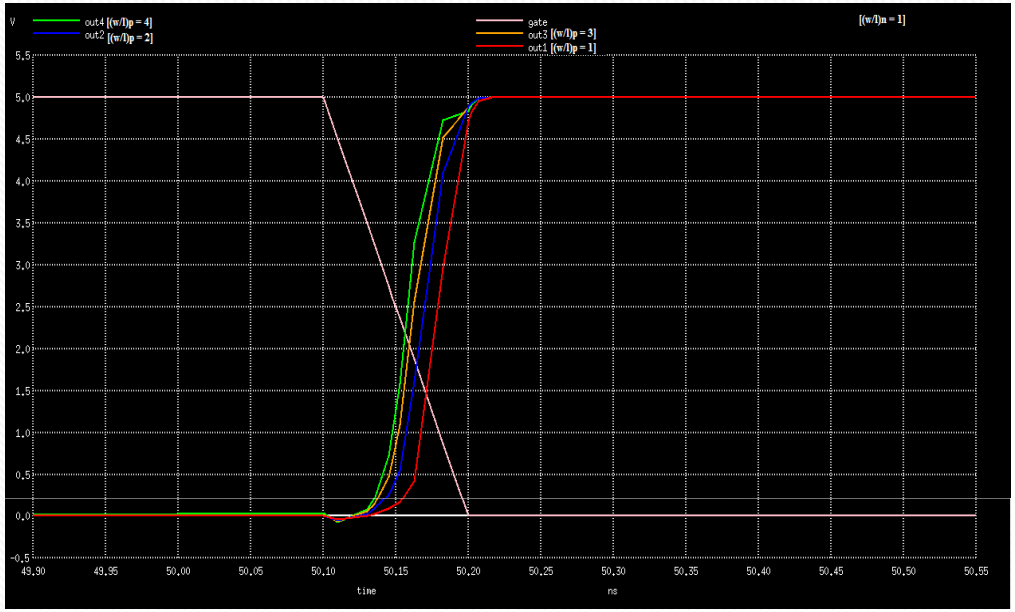
Transfer Function

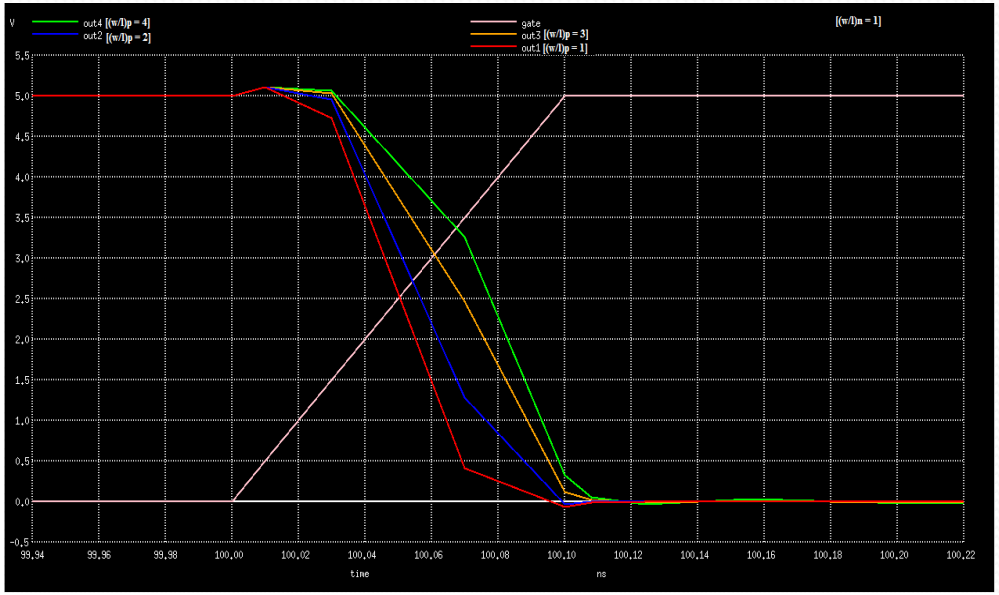


Variation in current with W/L



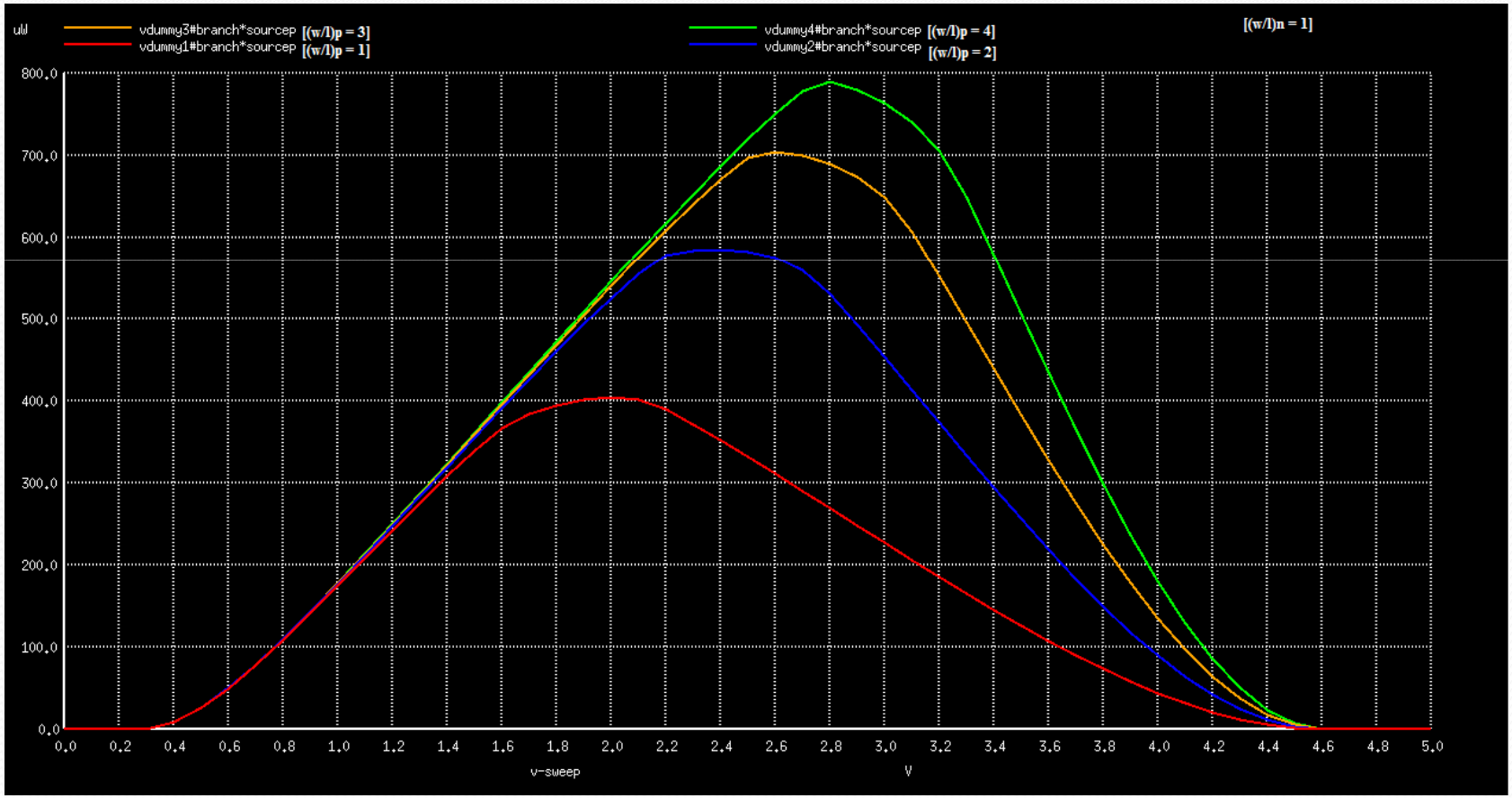
Rise time



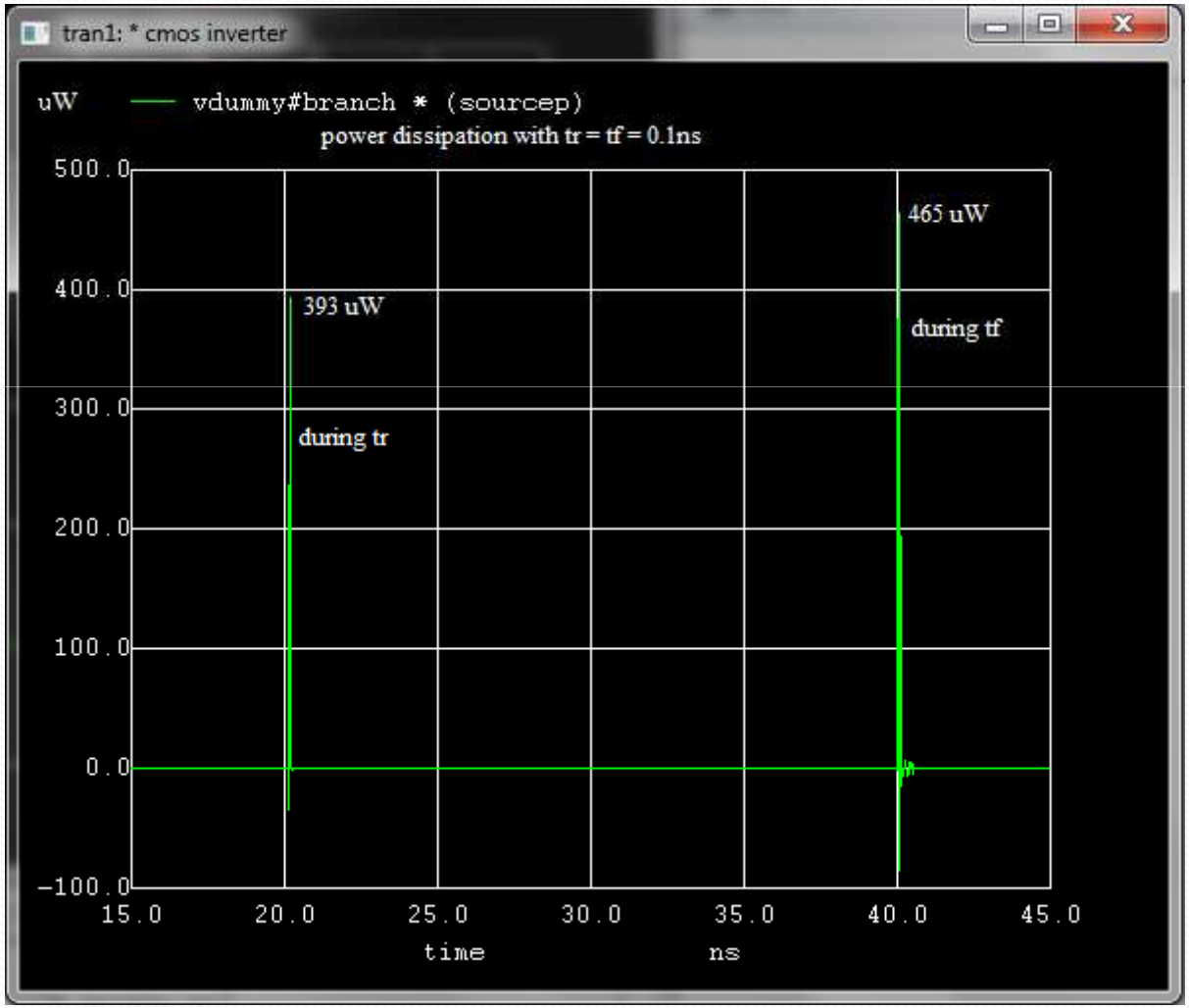


Fall time

Variation in power with W/L



Power Dissipation for pulse input



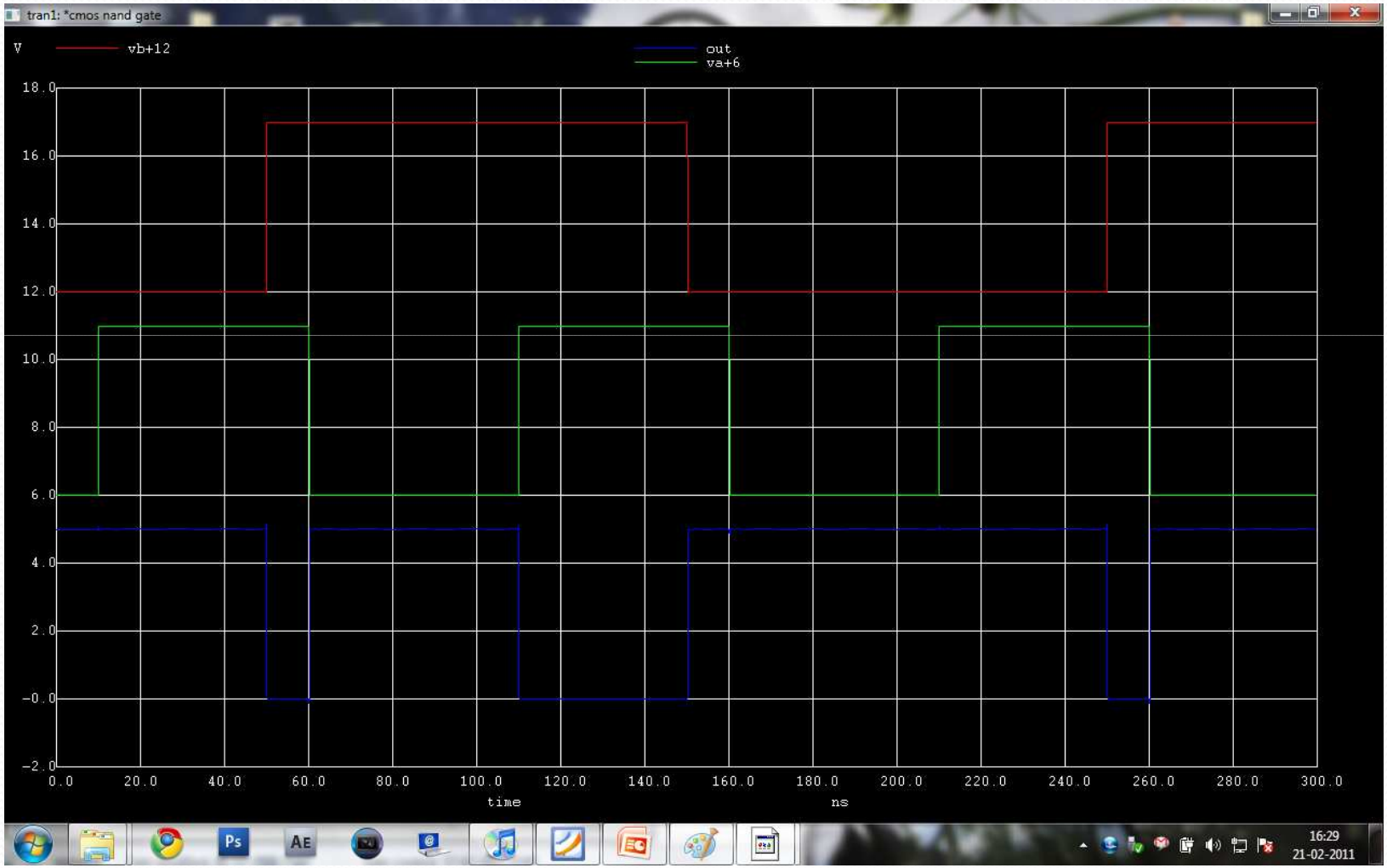
Experiment 5:

Study of CMOS Gates

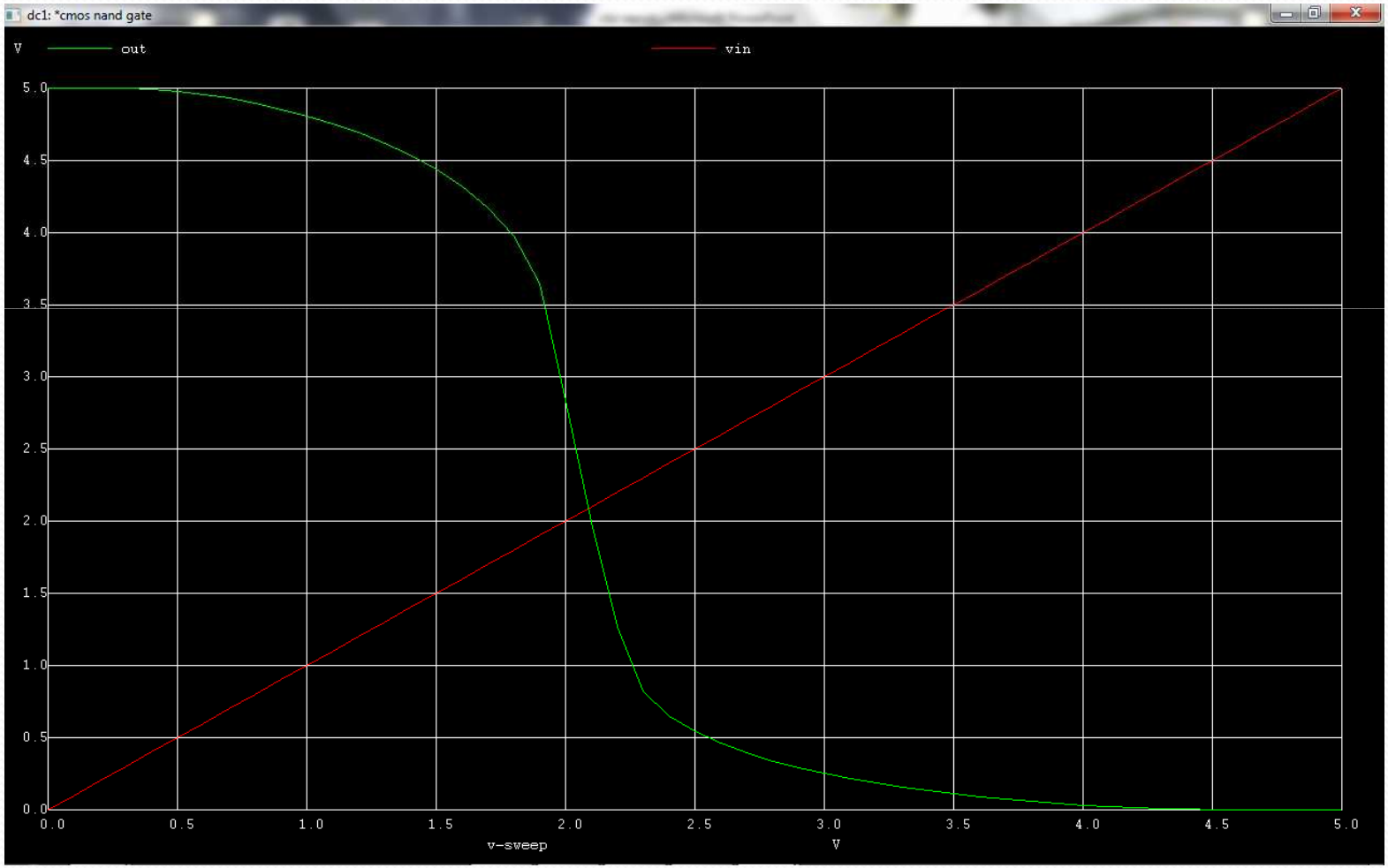
Objective:

Study the Behavior Transfer function, Noise Margin, effect on rise time, fall time, propagation delay, power and energy consumed of CMOS gates like NAND, NOR functions like AOI and XOR with variation in L and W.

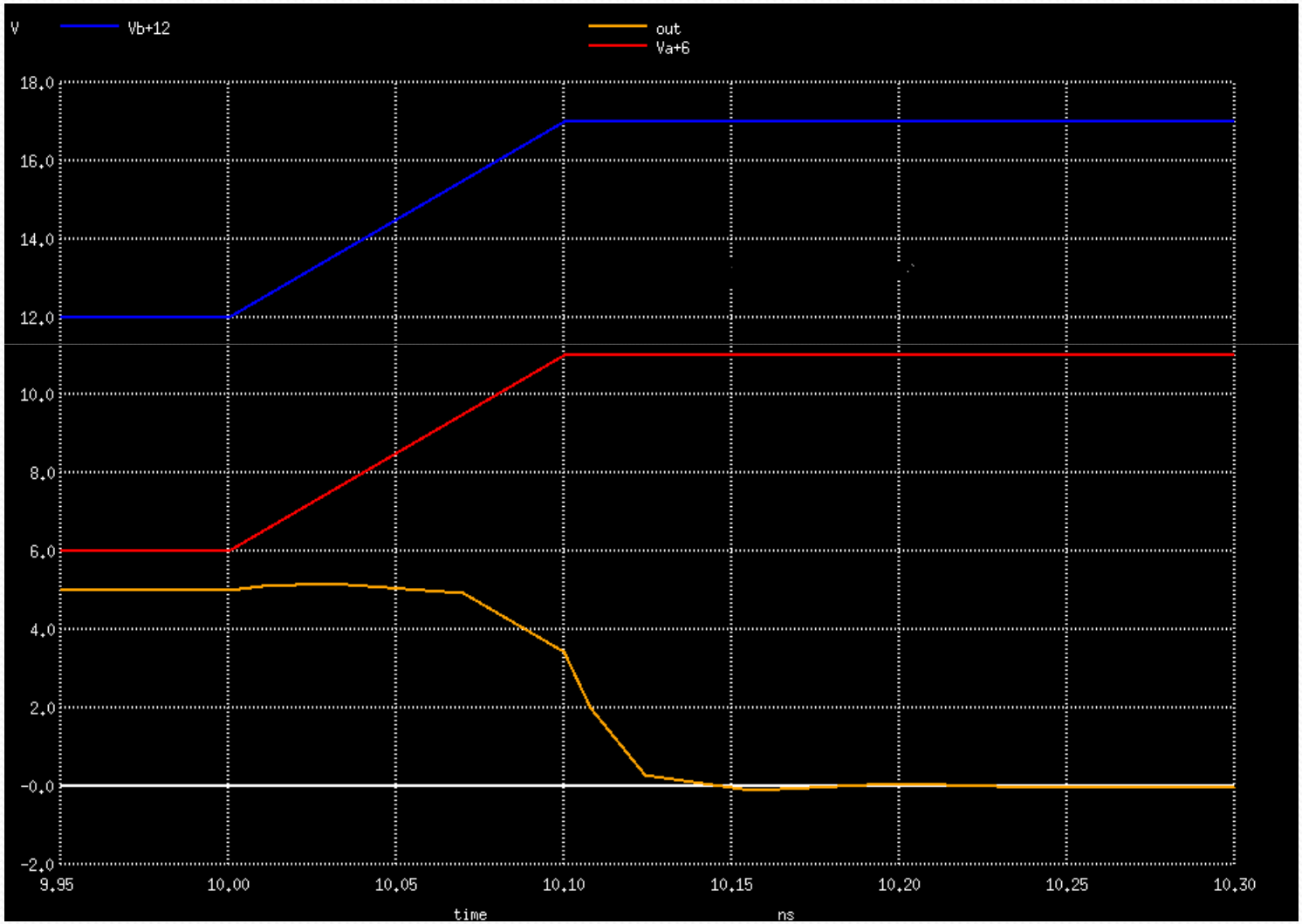
NAND Output


tran1: *cmos nand gate
V
vb+12
out
va+6
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
-0.0
-2.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
280.0
300.0
time
ns
16:29
21-02-2011

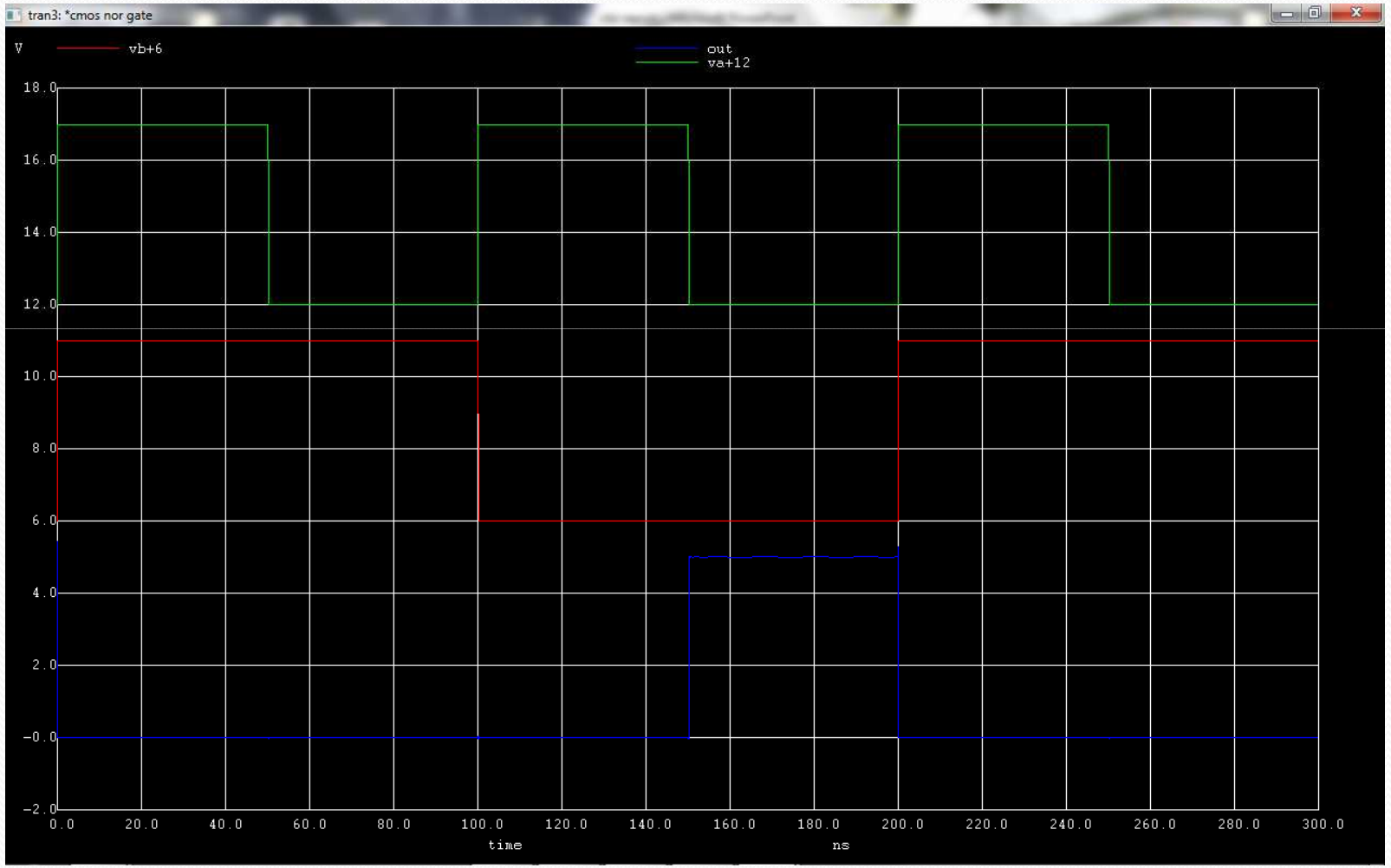
NAND DC Analysis



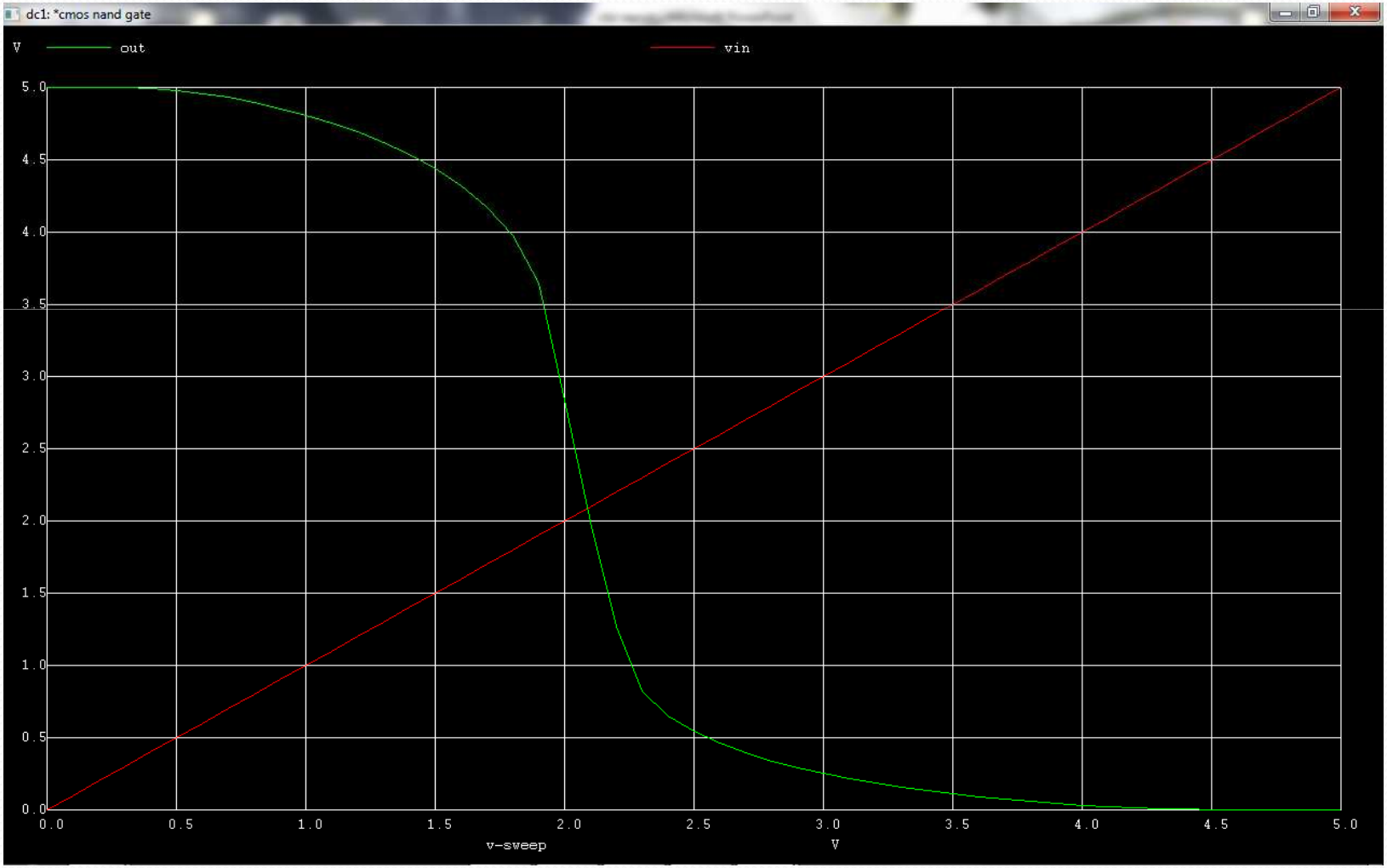
NAND Propagation Delay



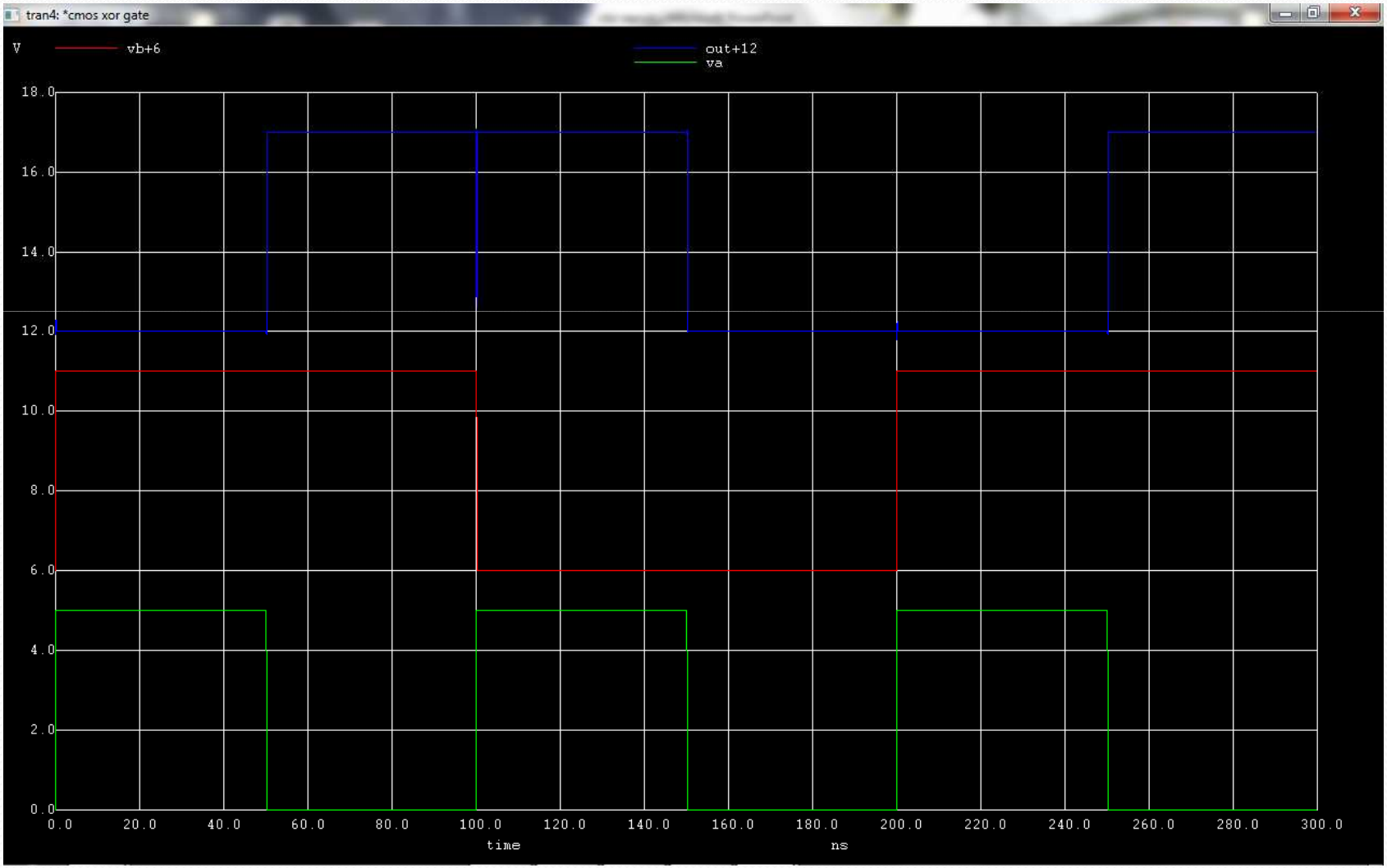
NOR Output


tran3: *cmos nor gate
V
vb+6
out
va+12
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
-0.0
-2.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
280.0
300.0
time
ns

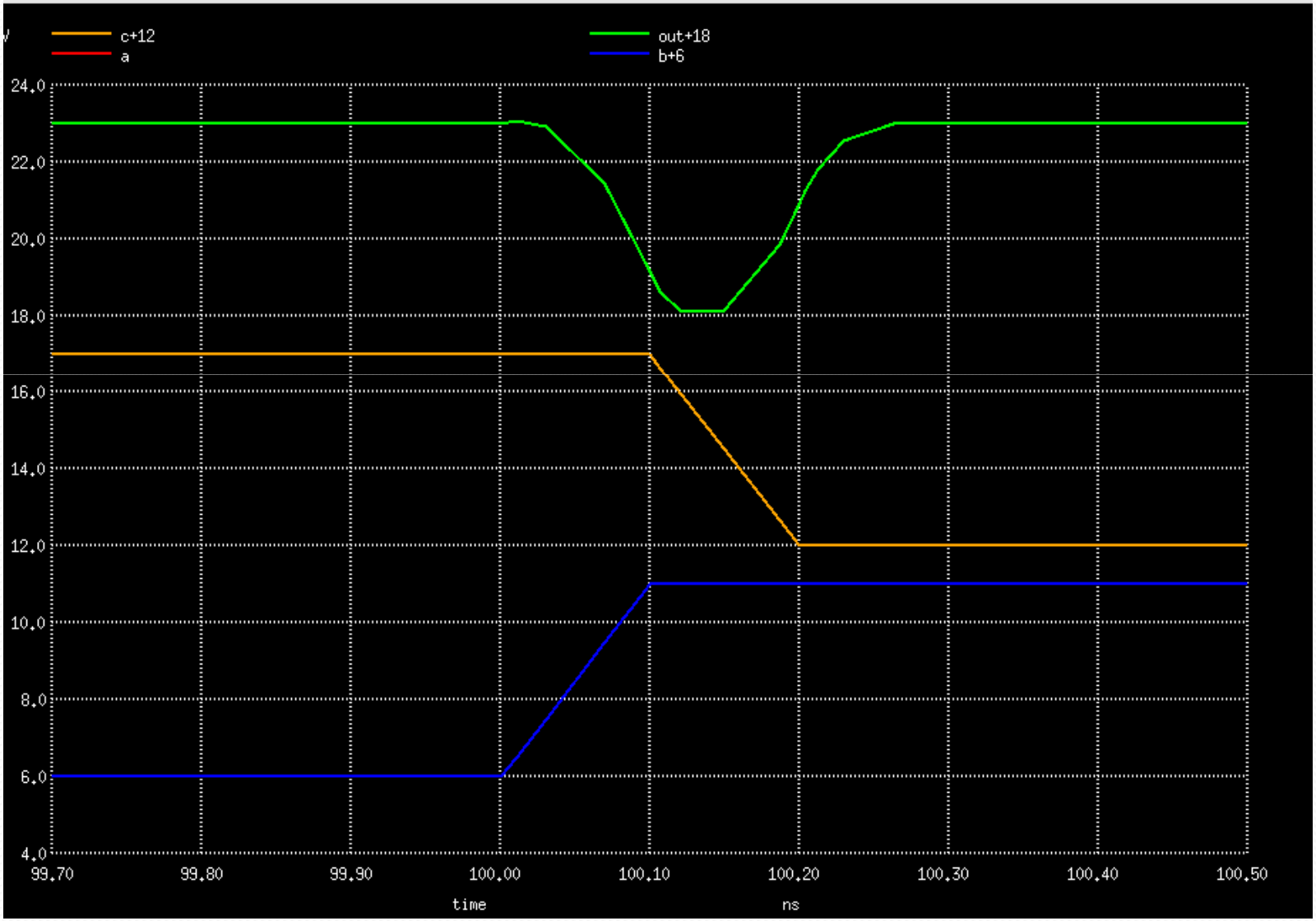
NOR DC Analysis



XOR Output


tran4: *cmos xor gate
V
vb+6
out+12
va
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
2.0
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
220.0
240.0
260.0
280.0
300.0
time
ns

AOI Hazard


c+12
a
out+18
b+6
24.0
22.0
20.0
18.0
16.0
14.0
12.0
10.0
8.0
6.0
4.0
99.70
99.80
99.90
100.00
100.10
100.20
100.30
100.40
100.50
time
ns