

(2-stage Op-Amp) Instrumentation Amplifier using 2 stage OP-AMP in gpdk 180nm



Ankit Kumar(BT23ECE008) and Abhishek Chaudhary(BT23ECE010)

ABSTRACT

- ✓ Designed a 2-opamp instrumentation amplifier using a two-stage CMOS opamp in 180nm technology, achieving gain >60 dB with CMRR & PSRR >60 dB.
- ✓ Verified through simulations and layout checks (DRC & LVS), making it suitable for precision analog and biomedical applications.

DEVICE STRUCTURE AND CALIBRATION

This is the two-stage CMOS opamp schematic used in our instrumentation amplifier. It achieves high gain with Miller compensation, ensuring stable operation and excellent CMRR/PSRR for precision analog use.

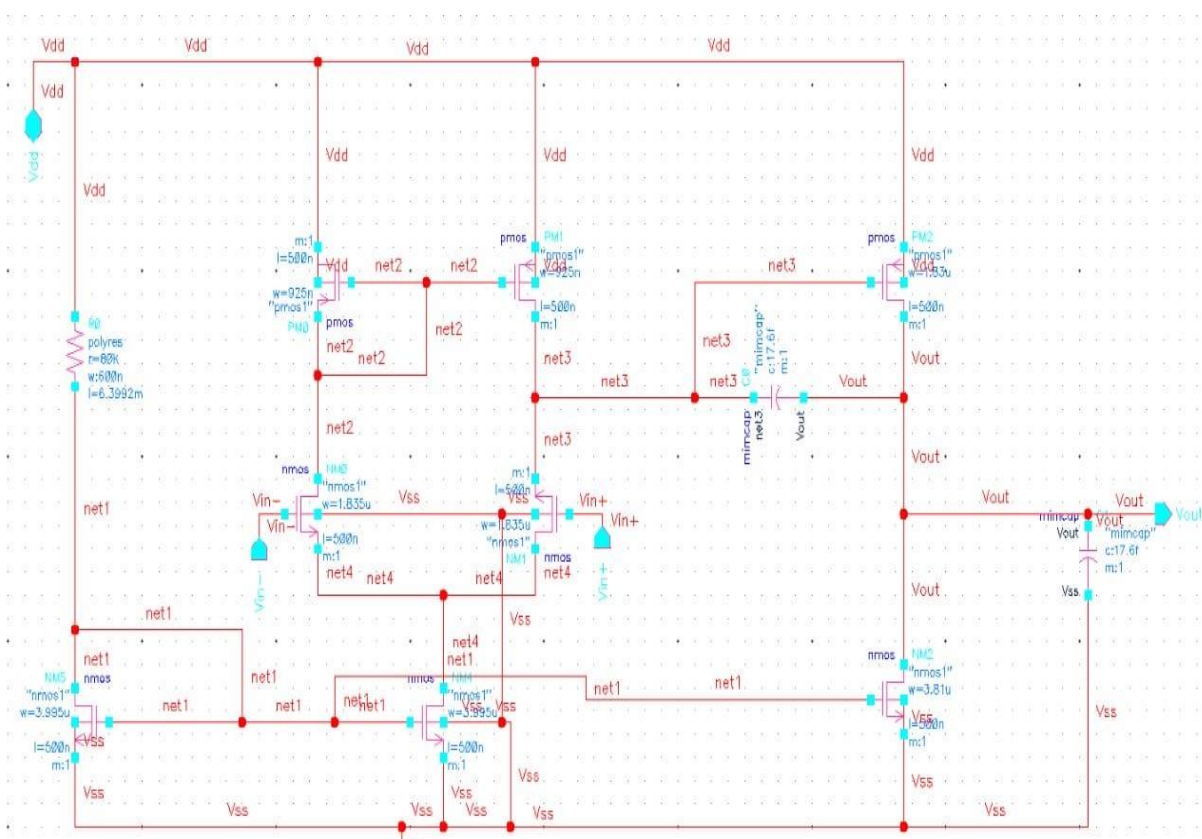


Fig: A Schematic 2 Stage Op-Amp

Parameter	w/L
M1, M2	1.835/0.5
M3, M4	0.925/0.5
M5	3.81/0.5
M6, M7	3.995/0.5

Table 1: Parameter Table

DEVICE CONFIGURATIONS

Technology Node: GPDK 180nm CMOS, Supply Voltage (VDD): 1.8 V, Gain Target: > 60 dB, CMRR & PSRR Target: > 60 dB, Load Capacitance: 1–5 pF, Input Common Mode Range: Rail-to-Rail (approx.), Compensation Capacitance: 1.77 pF (Miller Cap), Simulation Tools: Cadence Virtuoso, Spectre

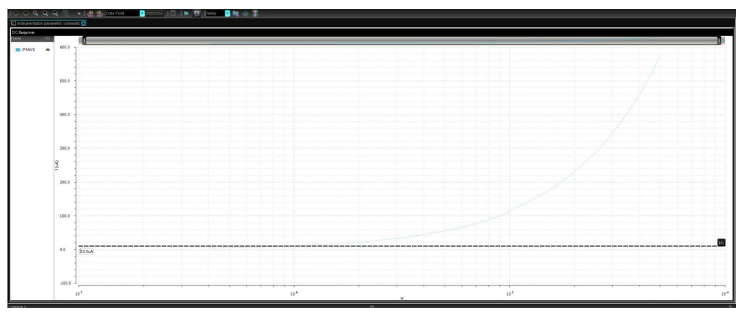


Fig: Parametric Extraction graph

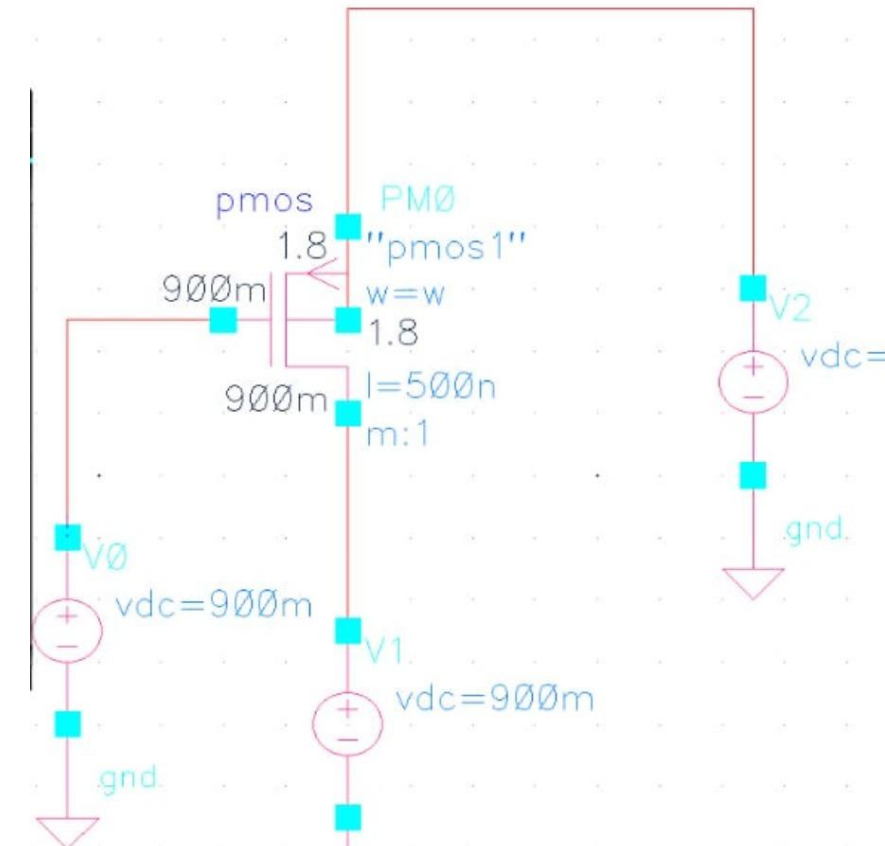


Fig: Schematic View

2 STAGE OP-AMP GAIN

The two-stage CMOS op-amp achieves a gain of 72.4 dB using a differential input stage followed by a common-source gain stage. Optimized W/L ratios and Miller compensation ensure high gain and stable operation for precision analog applications.

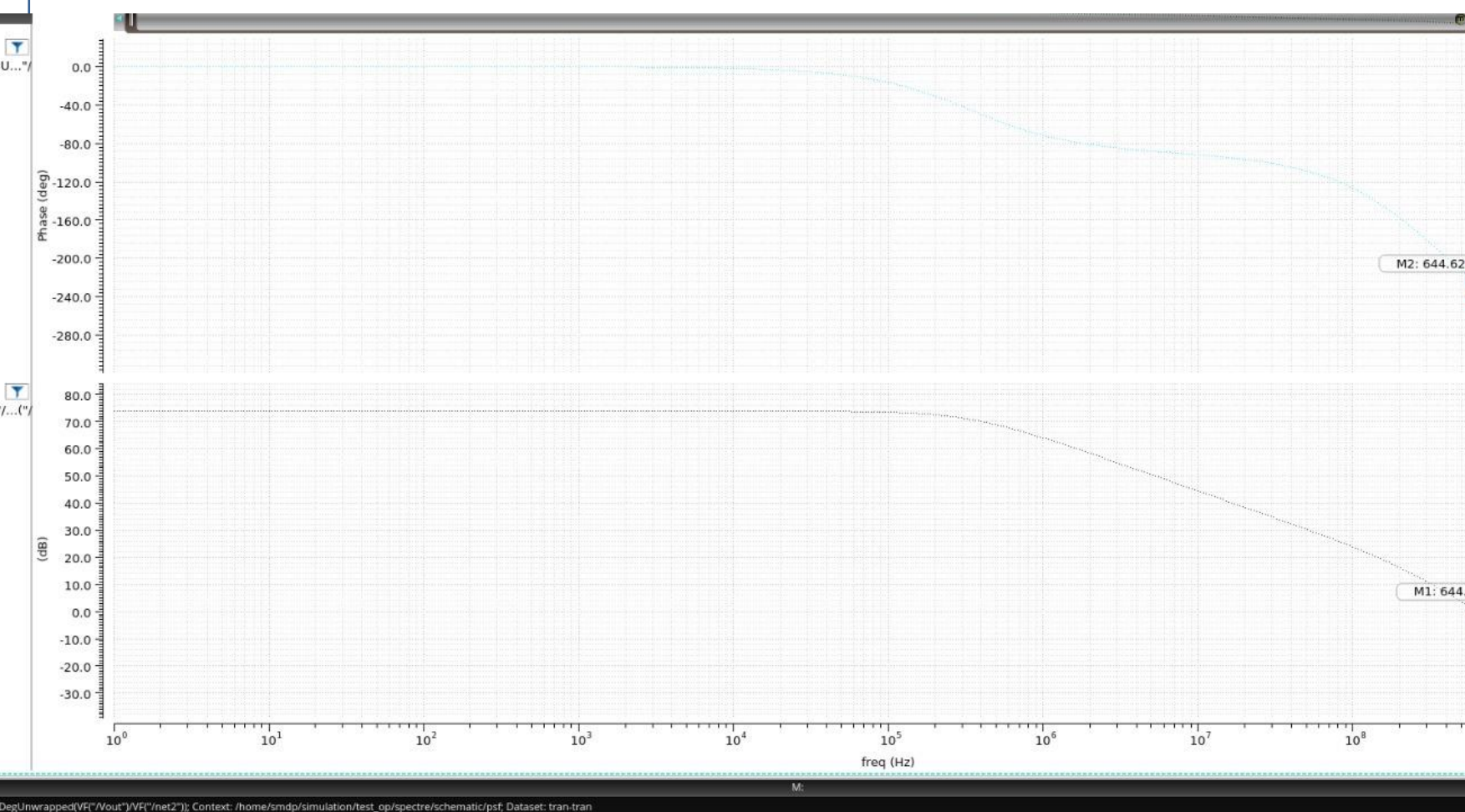


Fig: A gain Graph

SLEW RATE, PSRR AND CMRR

The op-amp demonstrates a slew rate of 0.211 V/μs, ensuring moderate speed for signal transitions. It achieves a CMRR of 80.2 dB and a PSRR of 77.9 dB, reflecting strong rejection of common-mode and supply noise. These characteristics support stable and accurate operation in precision analog systems.

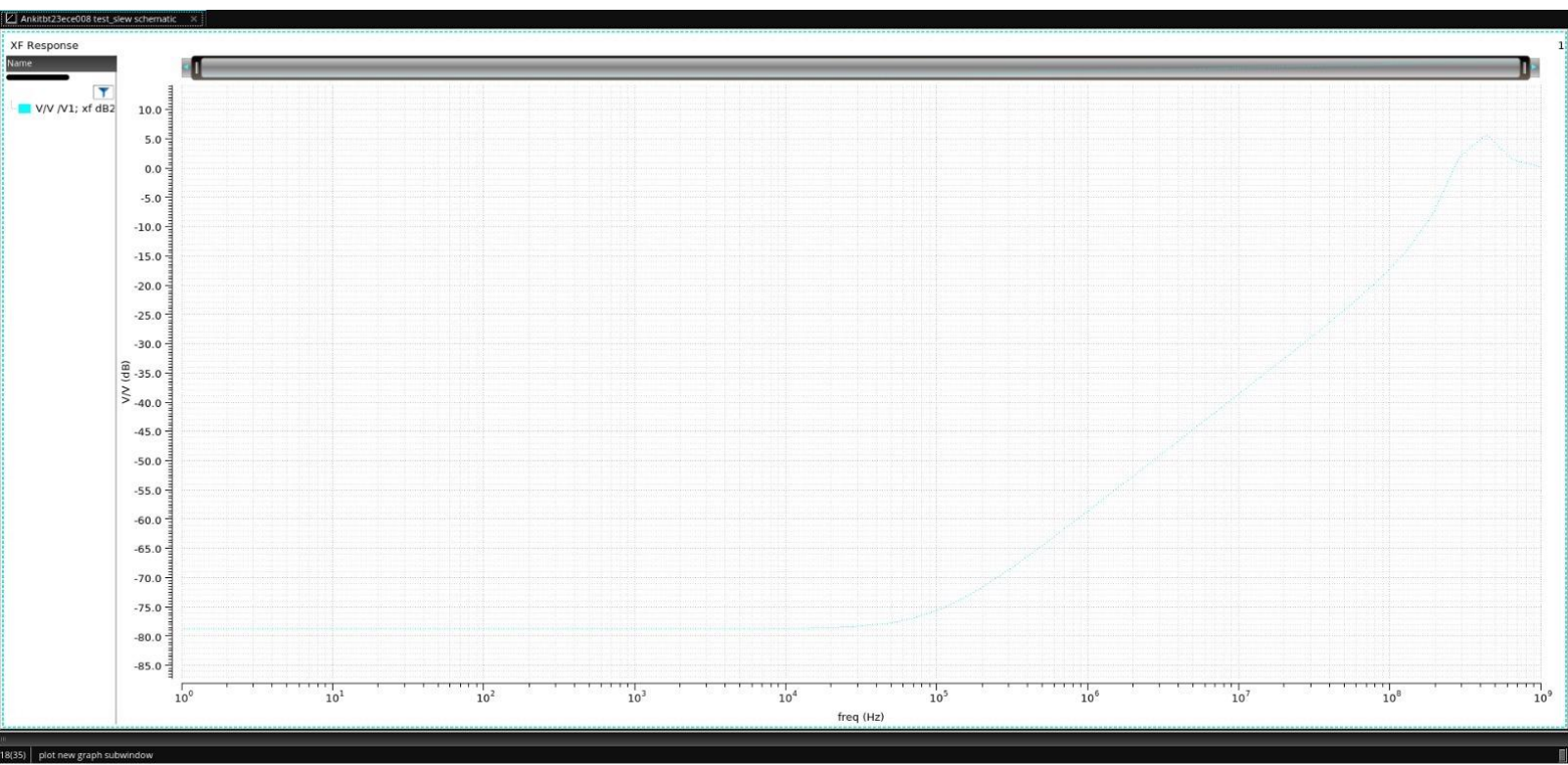


Fig: A PSRR Graph

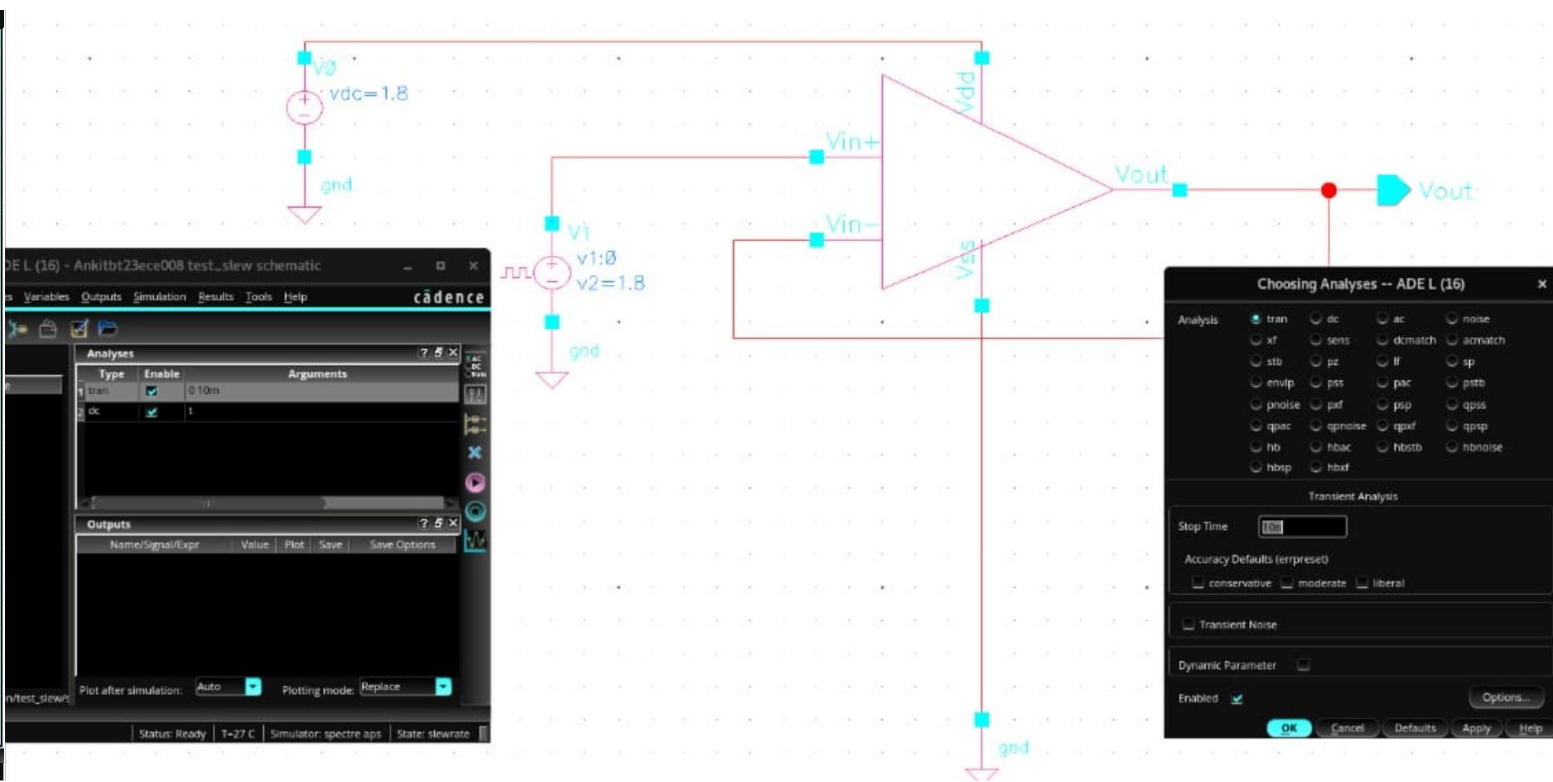


Fig: A Schematic View of PSRR Circuit

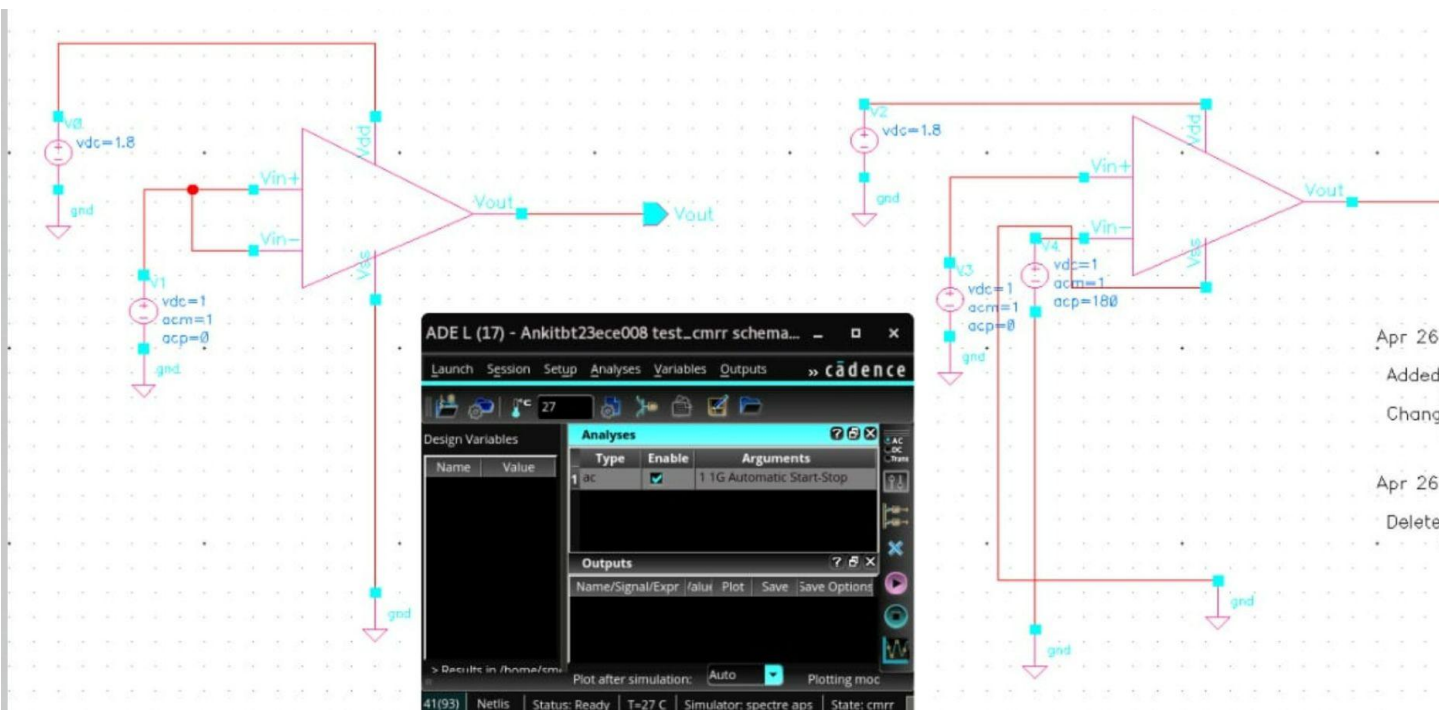


Fig: A Schematic View of CMRR Circuit

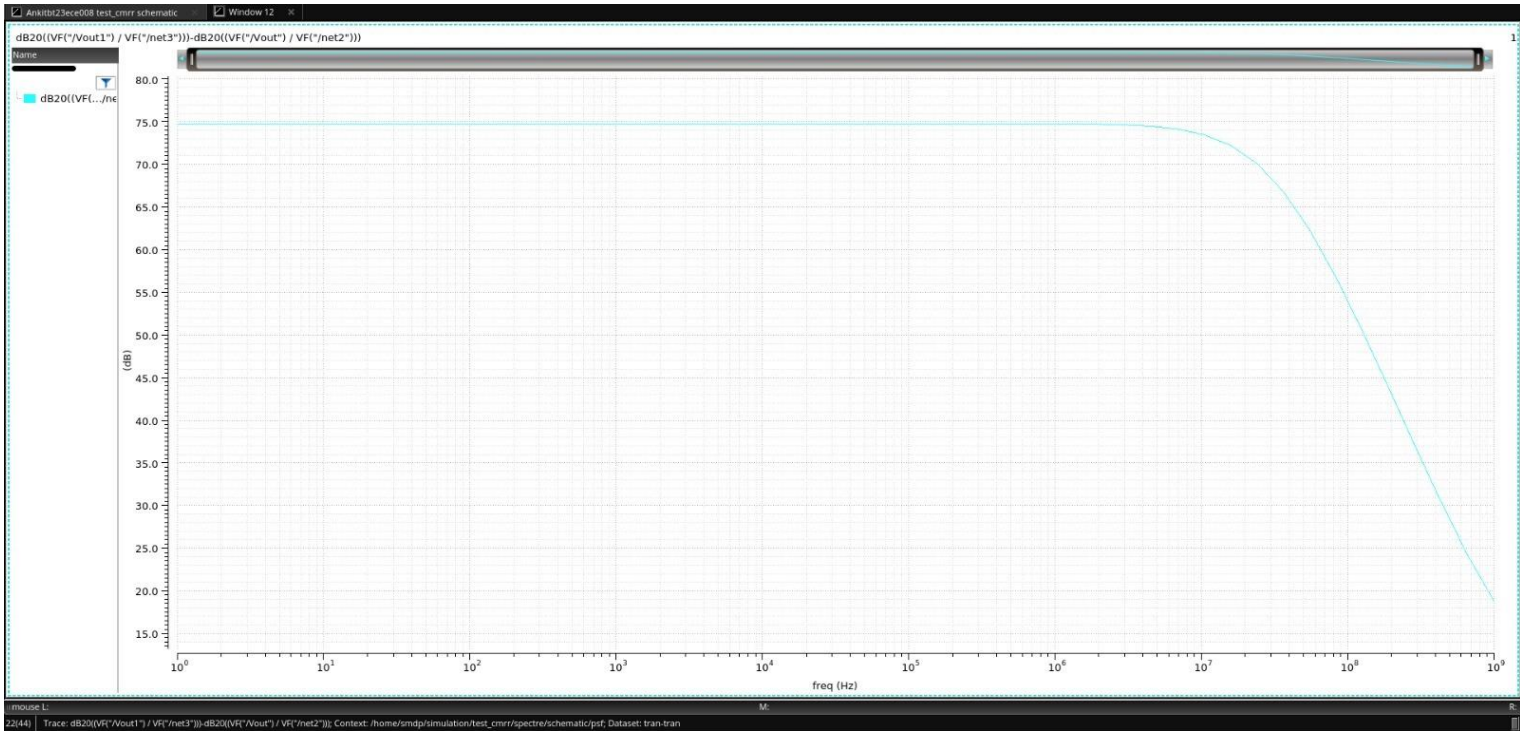


Fig: A CMRR Graph

INSTRUMENTATION AMPLIFIER

(The instrumentation amplifier is built using two identical two-stage CMOS op-amps to achieve high gain and precision. It is designed to amplify low-level differential signals while rejecting common-mode noise, making it ideal for sensor and biomedical applications. The amplifier achieves a gain greater than 60 dB, with high CMRR and PSRR ensured by careful matching and layout symmetry. This configuration enables accurate signal processing in noisy environments.

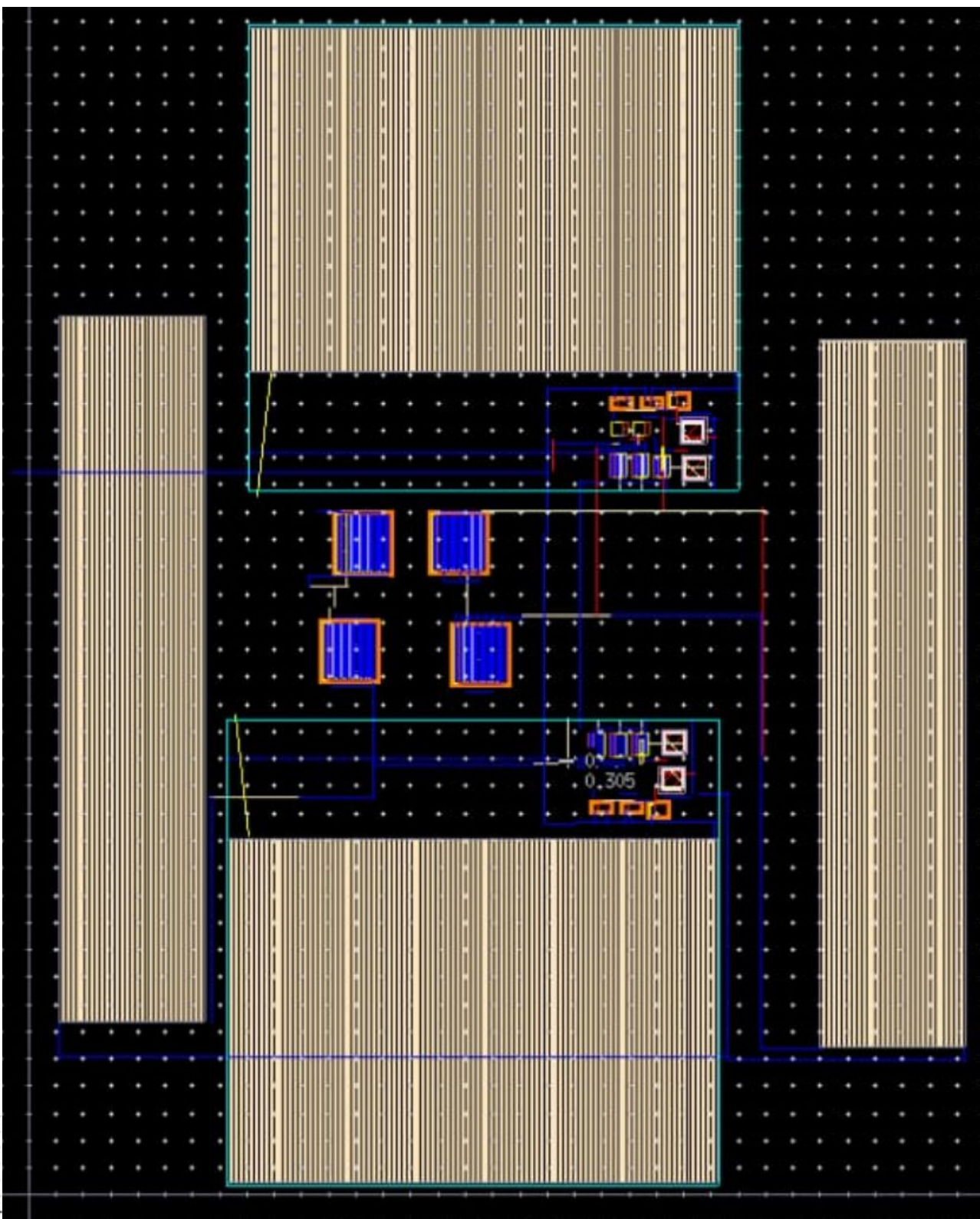


Fig: A Layout View of Instrumentation Amplifier

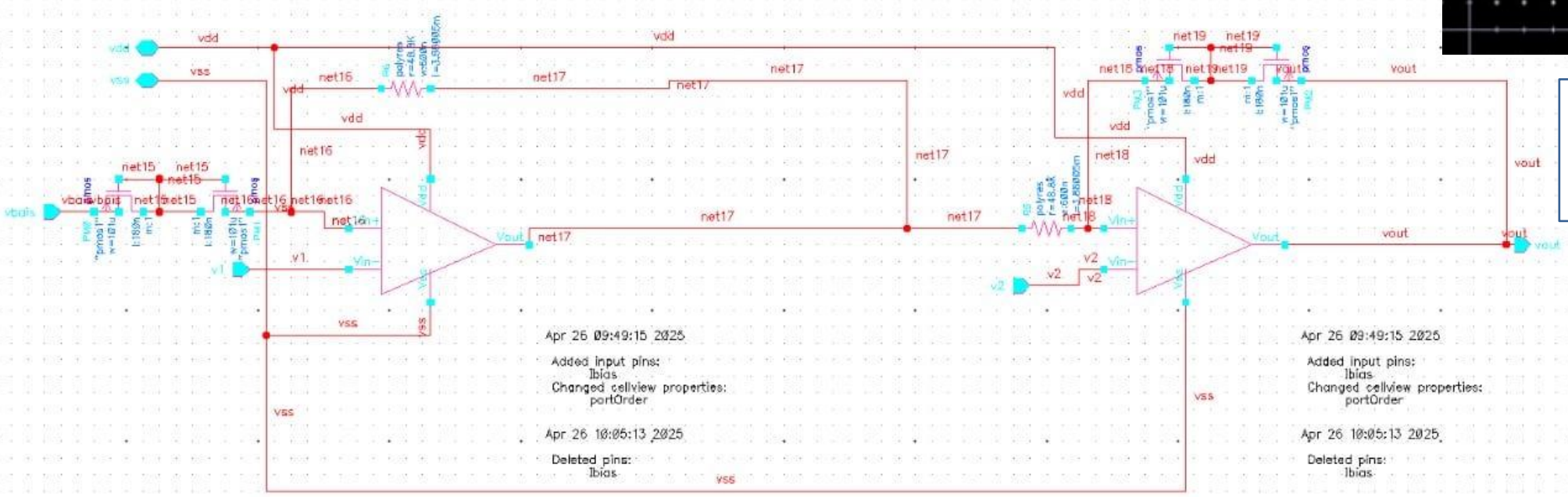


Fig: A Schematic view of Instrumentation Amplifier

CMRR AND PSRR OF INSTRUMENTATION AMPLIFIER

The instrumentation amplifier boasts a high Common Mode Rejection Ratio (CMRR) of 85.3 dB for excellent noise immunity and a Power Supply Rejection Ratio (PSRR) of 78.6 dB for stable operation despite power fluctuations, ensuring reliability and precision.

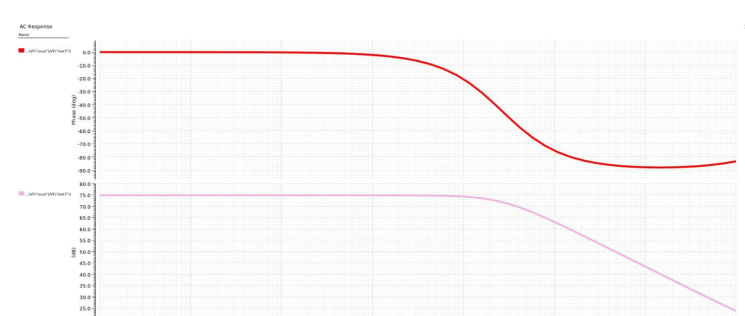


Fig: A Gain Graph (IA)

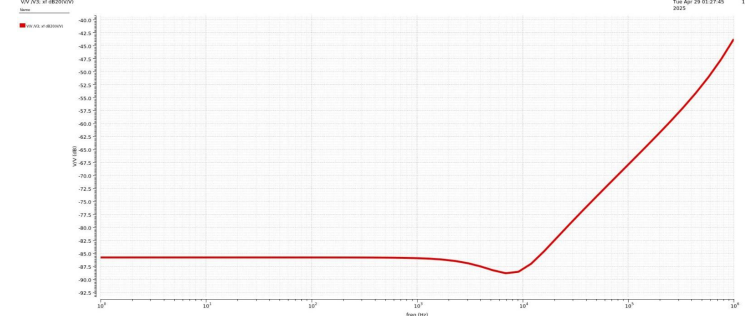


Fig: PSRR of IA

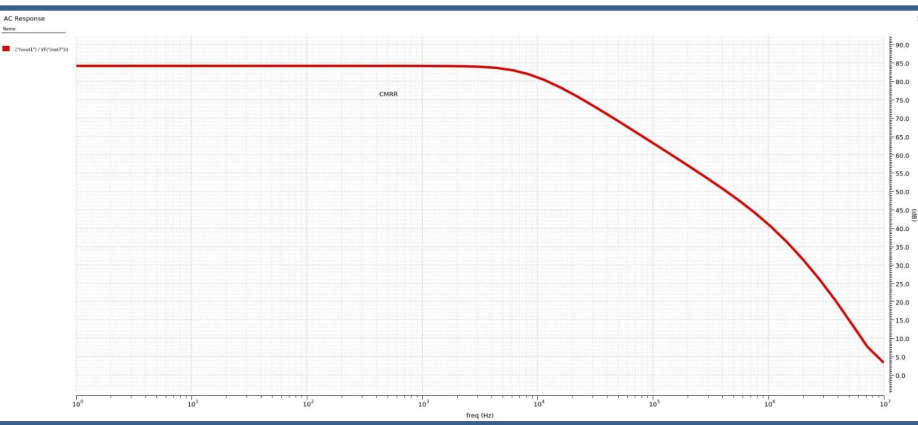


Fig: CMRR of IA

CONCLUSION

- ✓ The 2-opamp instrumentation amplifier met the target gain of over 60 dB.
- ✓ Simulations confirmed CMRR and PSRR above 60 dB.
- ✓ The layout passed DRC and LVS checks, ensuring design accuracy.
- ✓ The design is suitable for precision analog applications requiring high gain and noise rejection.

Acknowledgement

I would like to express my sincere gratitude to our Analog Circuit Faculty Dr. Vivek Kumar, our instructor and lab assistants for their valuable guidance and support throughout this project. I also thank my peers for their collaboration and the institution for providing access to the Cadence tools and resources necessary to complete this design successfully.

Reference

Sedra, A. S., & Smith, K. C. (2020). Microelectronic Circuits (7th ed.). Oxford University Press.
Razavi, B. (2001). Design of Analog CMOS Integrated Circuits. McGraw-Hill Education.,
Cadence Design Systems. (2023). Virtuoso Analog Design Environment User Guide., R. J. Baker, CMOS: Circuit Design, Layout, and Simulation, 4th ed. Hoboken, NJ: Wiley-IEEE Press, 2019.