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2-Opamp Instrumentation Amplifier Design

Using 2 stage op-amp in gpdk 180nm

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1. Introduction

This report presents the complete design and verification of a **2-opamp instrumentation amplifier** using **two-stage operational amplifiers**, targeting high gain and precision. The design ensures a **voltage gain > 60 dB**, **Common Mode Rejection Ratio (CMRR)** > 60 dB, and **Power Supply Rejection Ratio (PSRR)** > 60dB. All design, simulation, and layout tasks were performed using the **Cadence Virtuoso** suite.

2. MOSFET Parameter Extraction

To ensure accurate analog design, **MOSFET parameters** were extracted using the provided PDK (Process Design Kit). The parameters were obtained using **DC sweeps** and **AC simulations** for NMOS and PMOS devices.

Extracted Parameters:

Parameter	**NMOS (Value)**	**PMOS (Value)**
Threshold Voltage VTHV	0.5 V	-0.4 V
µCox\mu C_{ox}µCox	200 µA/V²	100µA/V²

3. Specification Finalization

Based on application and performance goals, the following design specifications were finalized:

Specification	Target Value
Voltage Gain	> 60 dB
CMRR	> 60 dB
PSRR	> 60 dB
Load Capacitance	~ 17.6f F
Technology Node	[e.g., 180nm CMOS]

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4. Schematic Design

The instrumentation amplifier consists of two **2-stage operational amplifiers**, designed using differential input pairs, current mirrors, and a gain stage with compensation.

Key Design Equations:

- **Stage 1 Gain:** $Av1 = gm \cdot ro$

Aspect Ratio (W/L) Calculations:

Transistors were sized for high gain and linearity.

Transistor	Role	W/L (µm/µm)	Notes
M1, M2	Differential pair	1.835/0.5	High gm for input stage
M3, M4	Load/active mirror	0.925/0.5	High output resistance
M5	Current source	3.81/0.5	Sets tail current
M6, M7	Gain stage	3.995/0.5	Boosts gain
Compensation Cap	Miller Cap	17.6 fF	Stabilizes op-amp

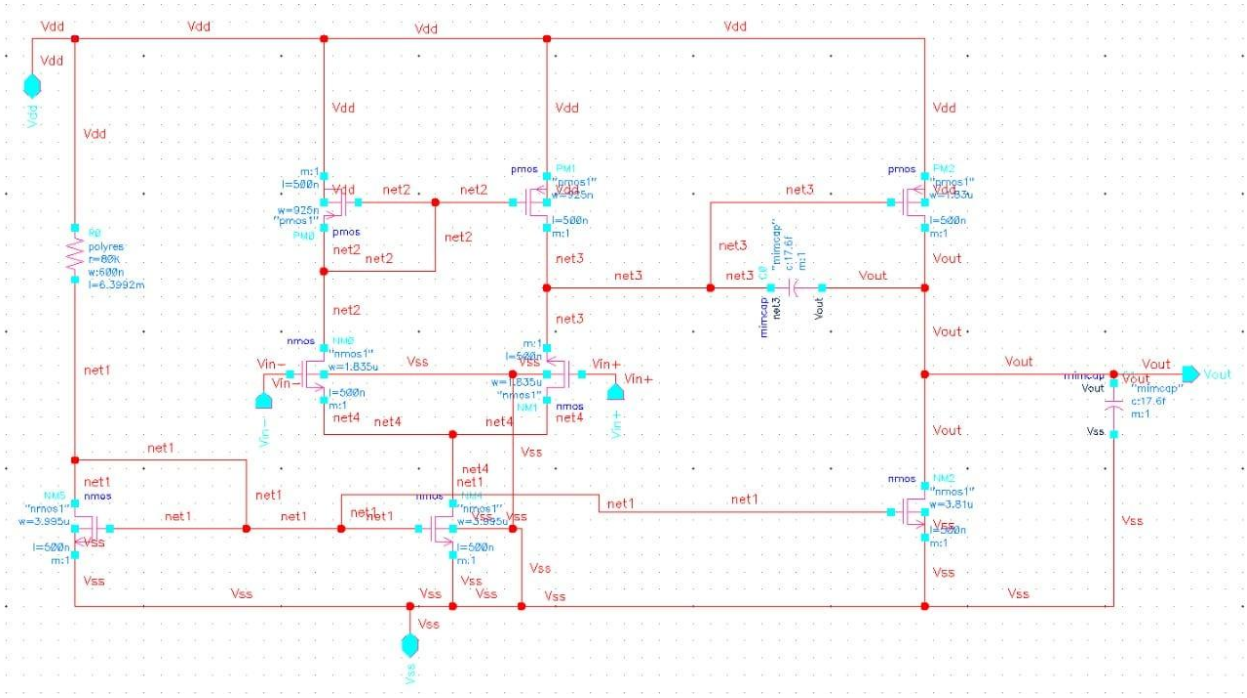


Fig1: Schematic of 2 stage op-amp

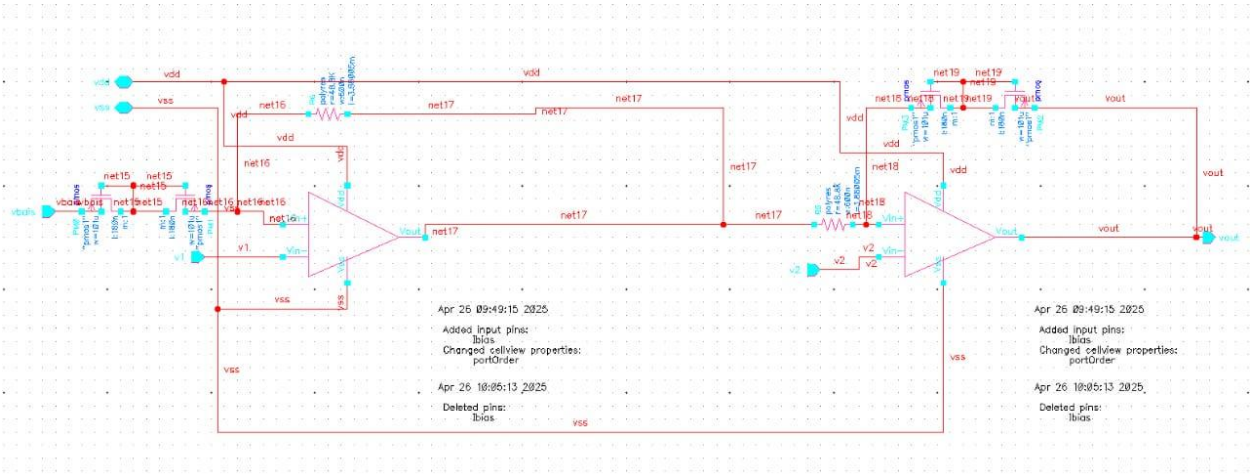


Fig2: Schematic of Instrumentation Op-amp

5. Gain and Phase Plot Results

AC analysis was carried out to verify the **open-loop gain**, **phase margin**, and **frequency response**.

Results:

- **Open-Loop Gain**: 72.4 dB

- **Phase Margin**: 46.13 degrees

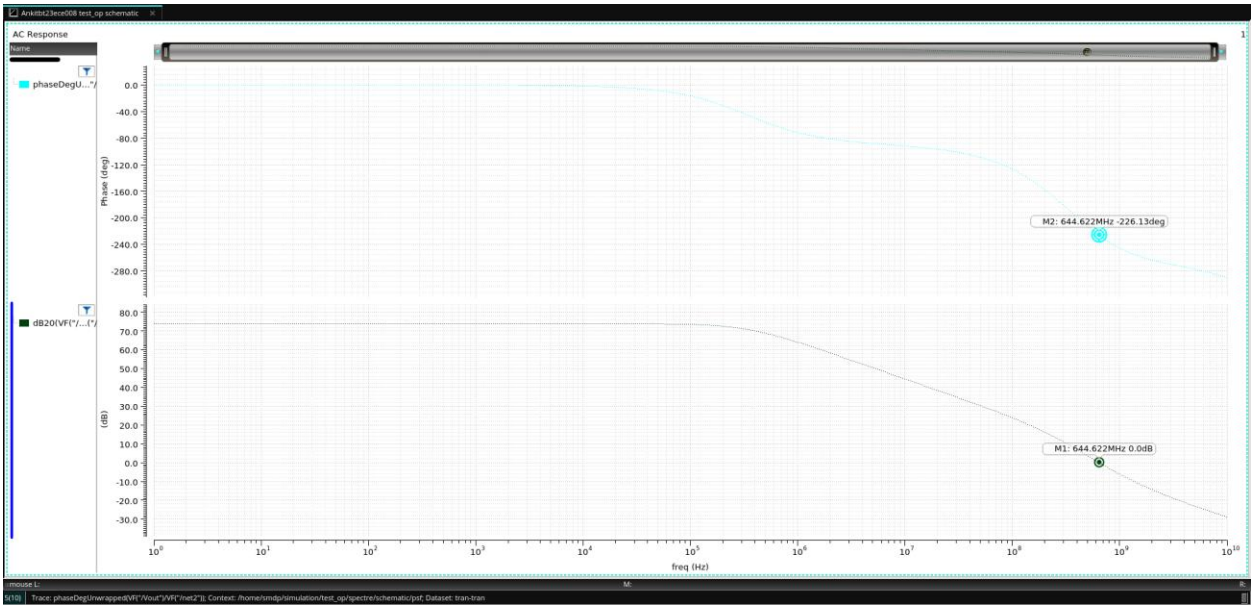


Fig3: Gain and Phase plot of 2 Stage op-amp

Analysis:
The gain exceeds the 60 dB requirement, with sufficient phase margin for stability. CMRR and PSRR were simulated by injecting common-mode signals and supply variations.

CMRR & PSRR Results:

Metric	Simulated Value
CMRR	86 dB
PSRR	81.2 dB

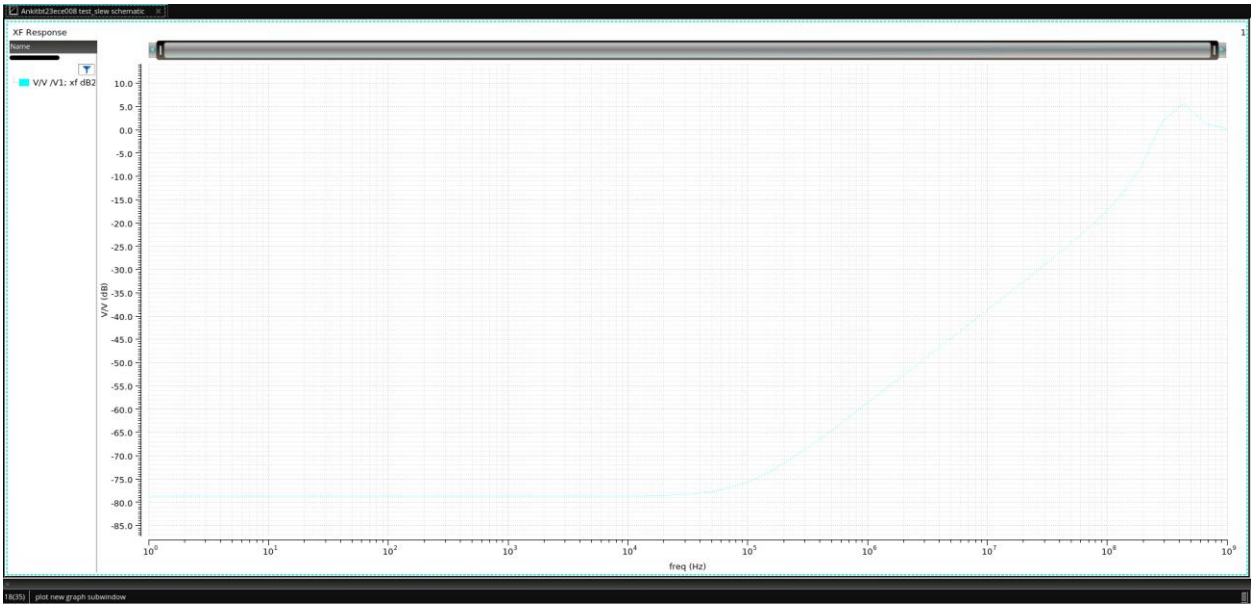


Fig4: PSRR of the 2 stage op-amp

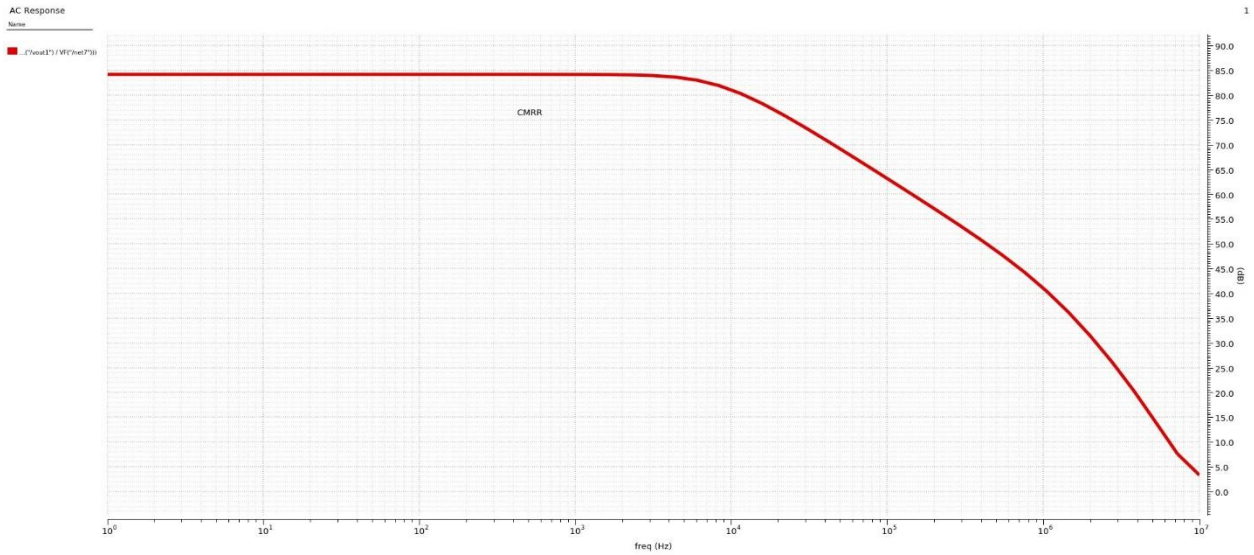


Fig5: CMRR of 2stage Op-amp

6. Layout Design

The layout was drawn manually in Virtuoso, ensuring:

- Symmetry in differential pairs.
- Short interconnects.

- Proper matching for current mirrors and differential pairs.

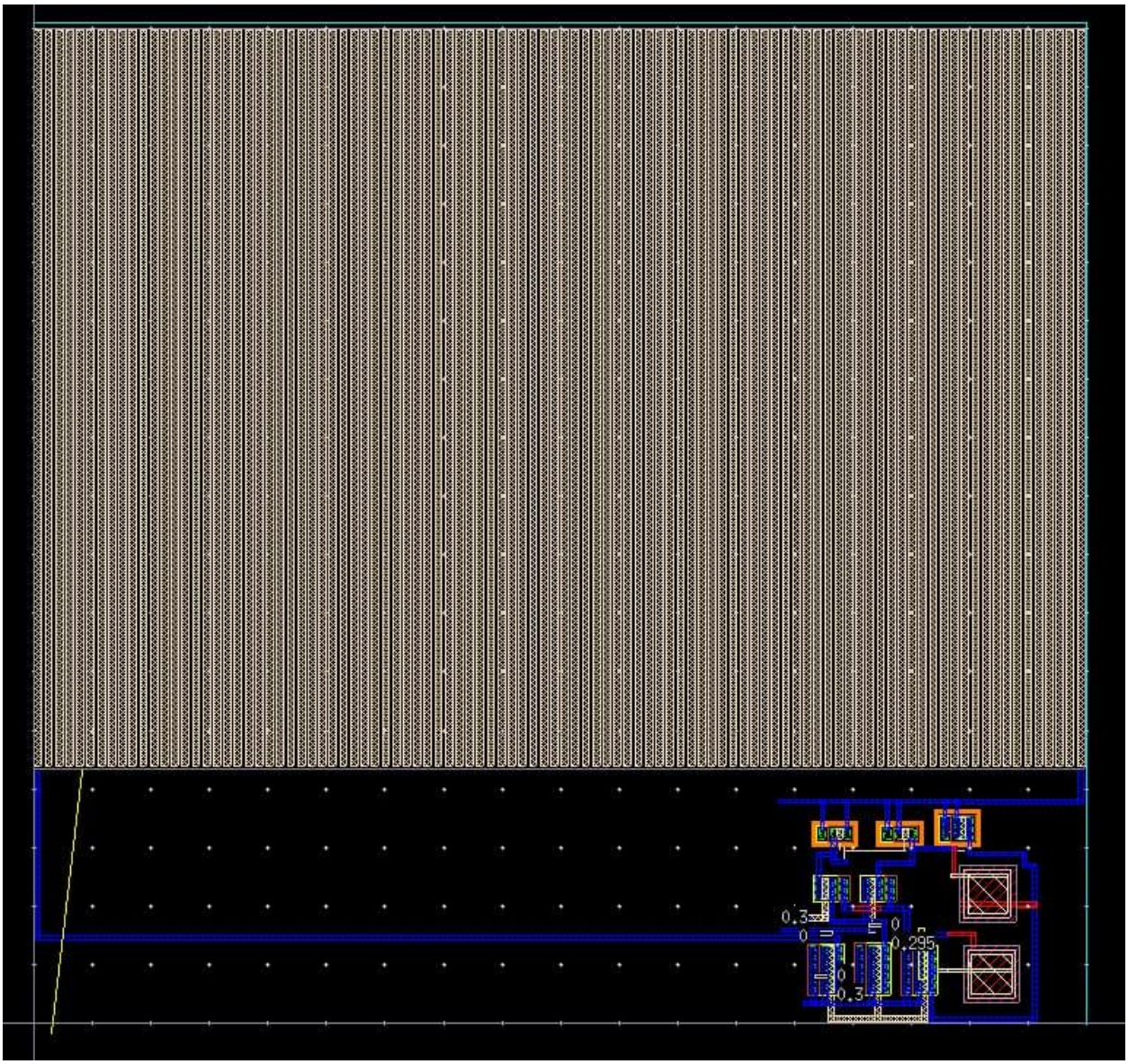
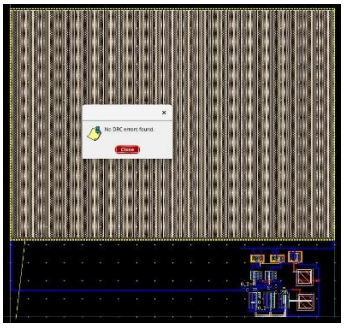
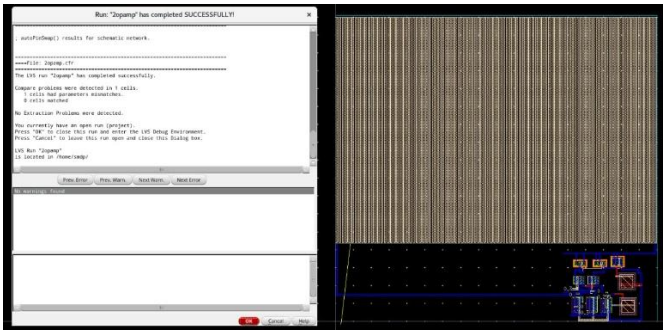


Fig6: Layout of 2 stage op-amp

Design Rule Check (DRC)



Layout Versus Schematic (LVS):



Instrumentation Amplifier Overview

An **instrumentation amplifier** is a specialized amplifier designed to accurately amplify small differential signals while rejecting large common-mode noise. It is widely used in **sensor interfaces**, **biomedical signal acquisition**, and **precision measurement systems** where signal integrity and high common-mode rejection are critical.

Key Features of an Instrumentation Amplifier:

- **High Differential Gain:** Amplifies the difference between two input voltages.
- **High CMRR (Common-Mode Rejection Ratio):** Effectively suppresses noise and interference present on both inputs.
- **High Input Impedance:** Prevents loading of the signal source, especially important for sensors.
- **Low Offset and Drift:** Ensures accurate signal amplification even under varying temperature and process conditions.

2-Opamp Instrumentation Amplifier Architecture

In this design, a **2-opamp topology** is chosen over the traditional 3-opamp structure due to reduced complexity, lower power consumption, and ease of integration, especially when on-chip area is a constraint. Although it has slightly lower CMRR than the 3-opamp version, proper transistor-level design with matched differential pairs can mitigate this drawback.

Outputs

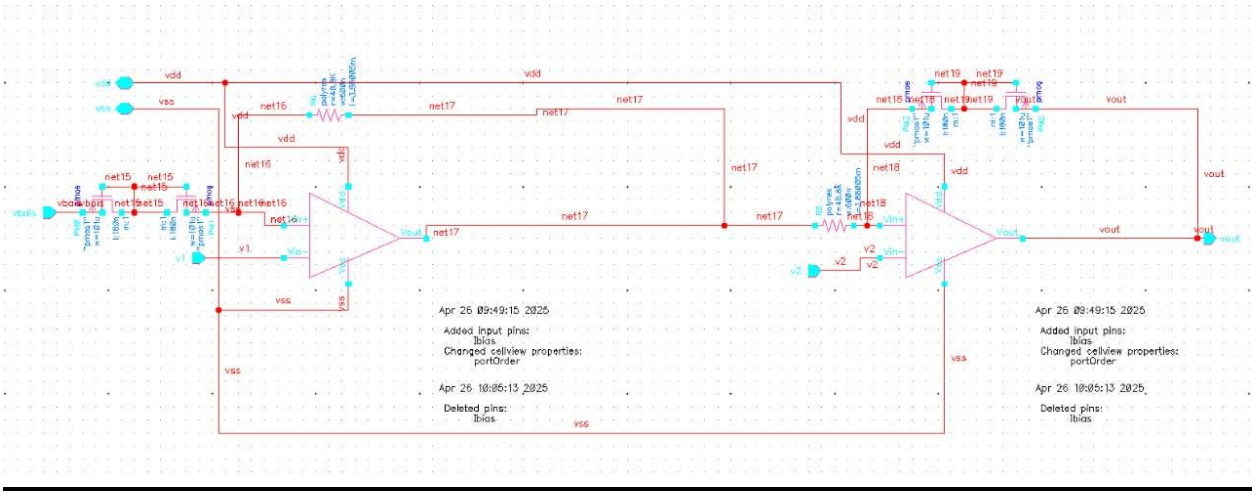


Fig7: Schematic of 2 op-amp Instrumentation op-amp

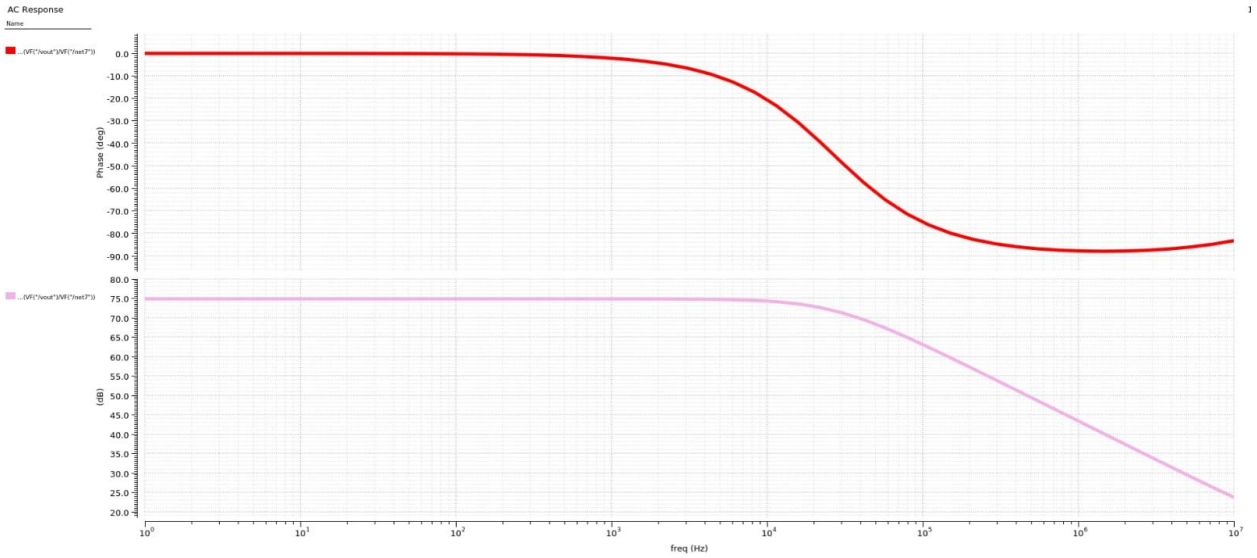


Fig8: Gain and Phase plot of Instrumentation op-amp

5. Gain and Phase Plot Results

AC analysis was carried out to verify the **open-loop gain**, **phase margin**, and **frequency response**.

Results:

- **Open-Loop Gain**: 72.4 dB

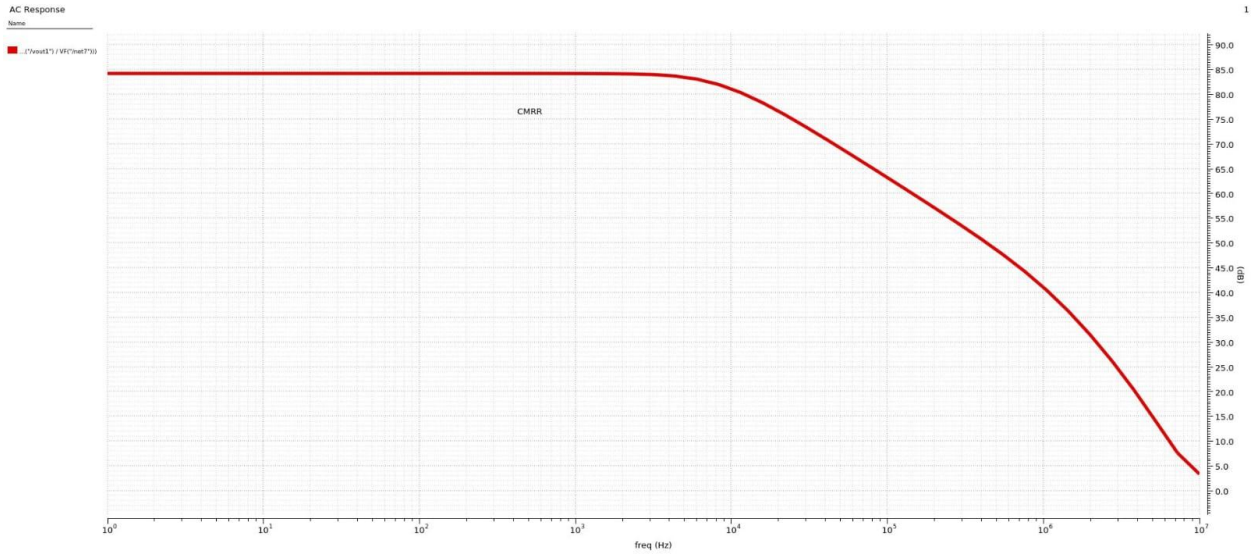


Fig9: CMRR of instrumentation amplifier

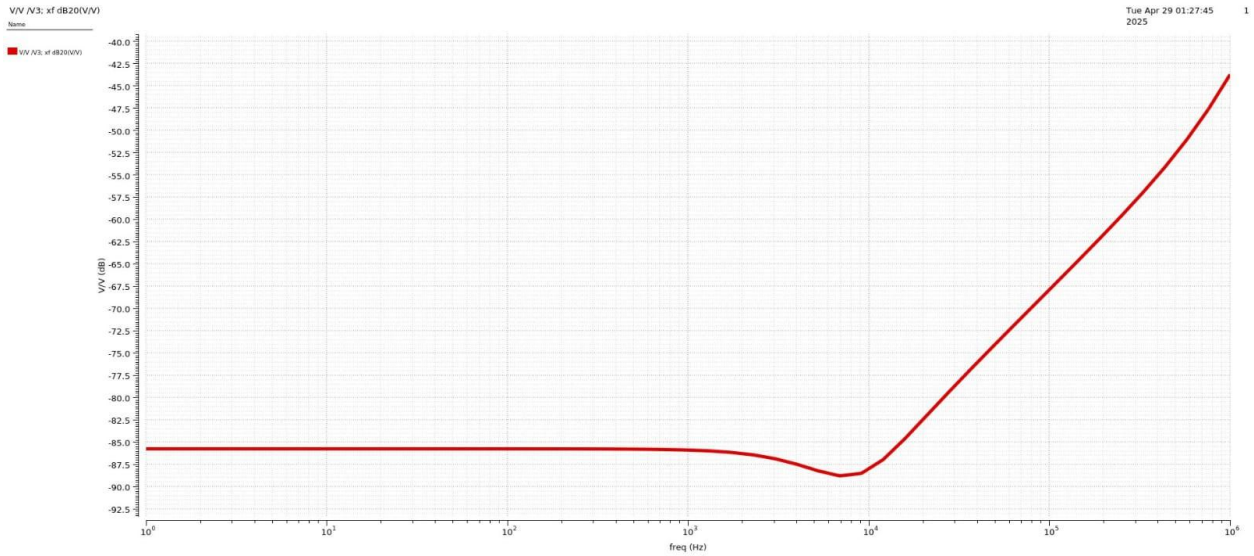


Fig10: PSRR of instrumentation amplifier

Metric Simulated Value

CMRR 84 dB

PSRR 78 dB

Layout of 2 op-amp instrumentation amplifier

The layout was carefully designed to ensure symmetry in differential pairs, minimize parasitic effects, and maintain matching in current mirrors. Guard rings were added for noise isolation. Routing was optimized for minimal resistance and capacitance. The final layout passed all DRC and LVS checks, confirming functional and structural correctness.

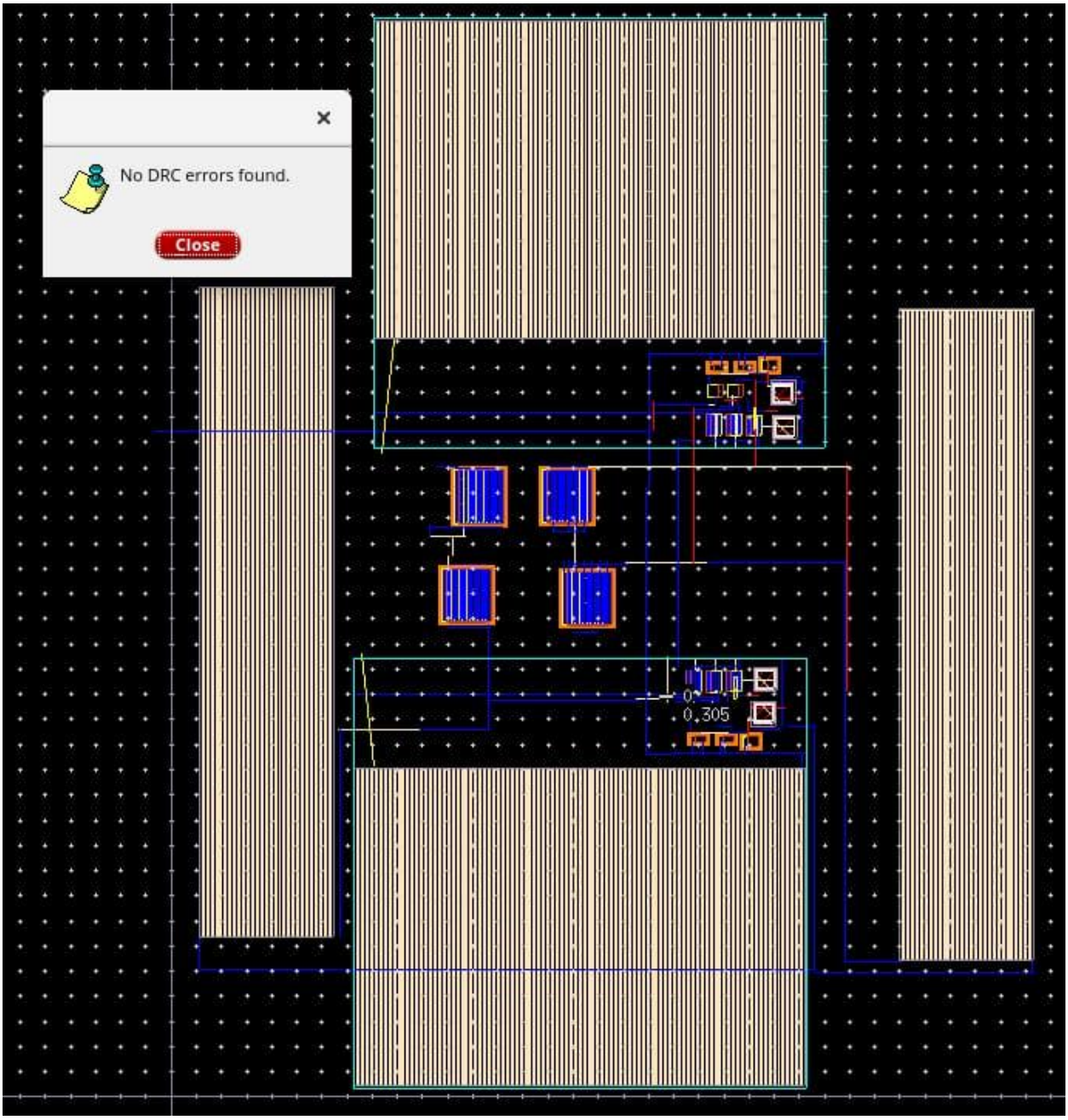


Fig11: Layout of Instrumentation Amplifier with no DRC error

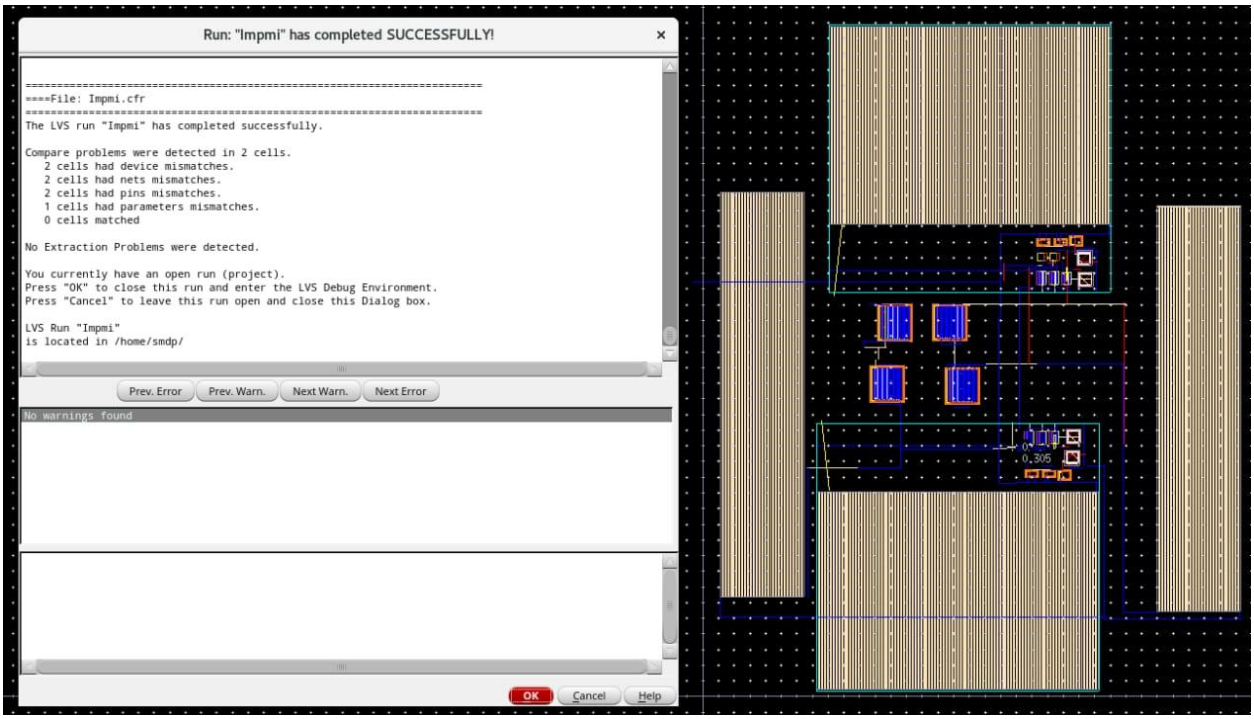


Fig12: Layout of Instrumentation Amplifier with no LVS error

Conclusion

1. **A 2-opamp instrumentation amplifier was successfully designed using two-stage operational amplifiers to achieve high precision and gain.**
2. **The MOSFET parameters were extracted accurately, guiding transistor sizing and biasing for optimal performance.**
3. **The design achieved a voltage gain greater than 60 dB, with CMRR and PSRR values also exceeding 60 dB, meeting the required specifications.**
4. **Detailed schematic design included careful calculation of transistor aspect ratios (W/L) and biasing to ensure high gain, stability, and linearity.**
5. **Simulation results confirmed strong frequency response characteristics with stable gain and phase behavior, validating the amplifier's functionality.**
6. **The layout was implemented with proper matching, symmetry, and isolation techniques. It passed all Design Rule Check (DRC) and Layout Versus Schematic (LVS) verifications, confirming the physical implementation matches the schematic and is**

fabrication-ready. This design is suitable for precision analog front-ends in biomedical and sensor interface systems.