Department of Computer Science and Engineering
Motilal Nehru National Institute of Technology
End Semester Exam, Computer Organization(CS1403)
BTech (IT) IV Semester
Time: 3 Hour, MM:60

Note: There are 4 questions. Attempt all.

1. **Cache Memory**

   (a) Suppose a computer has 4-way set associative cache with 64 one word (4 byte) blocks. Given the sequesnce of byte addresses 8, 64, 96, 128, 64, 96, 256, 192, 24 show the final cache contents and state the numbers of cache hit and miss.

   (b) Assuming a cache of 16K blocks and a 32 bit address, find the total number of sets and the total number of tag bits for caches that are direct mapped, two-way and four-way set associative, and fully associative.

   (c) Draw a picture showing the organization of a 4-way set associative cache having 1K one word blocks. Show any multiplexers, comparators, gates etc. needed. Show how a 32 bit address is mapped to a cache block.

   (d) Differentiate between write-through and write-back policies.

2. **Pipelined Datapath**

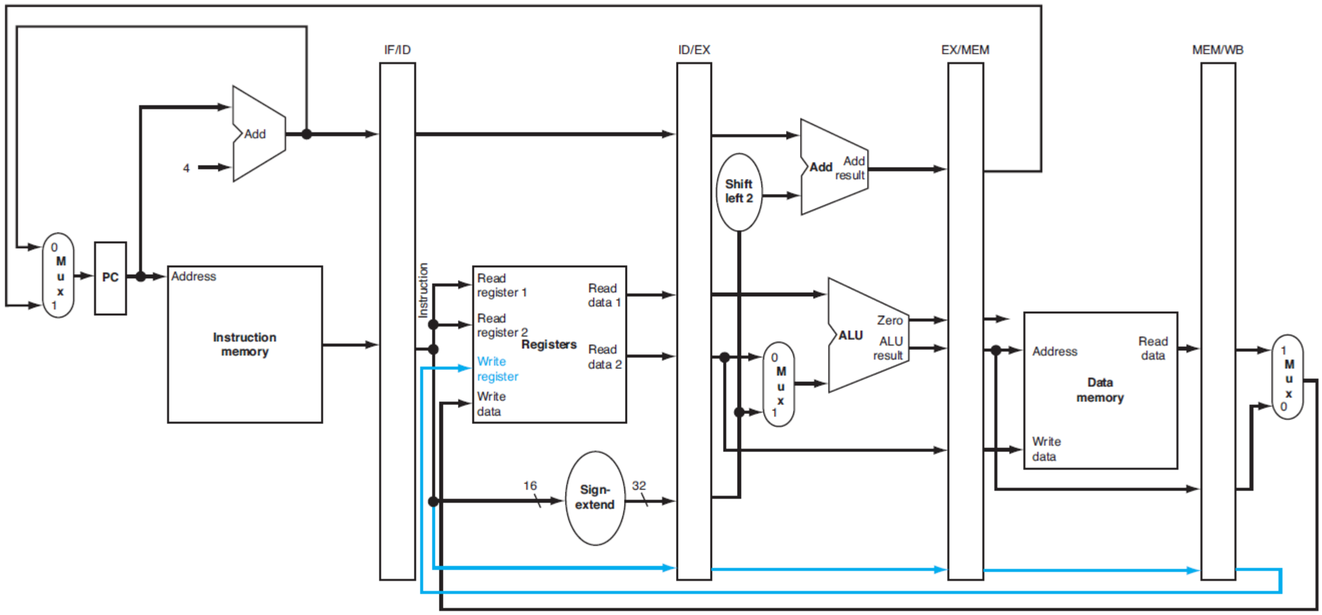

Figure 1: Figure for Question 2

   (a) Consider the execution of following instruction sequence over datapath given in Figure.1:

```
lw  $t0,  10($t1)
sw  $t3, 20($t4)
add $t5,  $t6,  $t7
sub $t8,  $t9,  $t10
```

   Show and explain explicitly the contents of Pipeline Registers (IF/ID, ID/EX, EX/MEM, MEM/WB) after every clock cycle starting from clock cycle 1 to clock cycle 6.

(b) For each of the following sequences of instructions, state: (1) Whether a data hazard exists in the pipelined datapath of Figure.1 (2) If that data hazard necessarily results in a stall, and (3) Which forwarding paths (from the output of which stage to the input of which stage) are necessary to eliminate or minimize the stall.

-
  ```
  lw $s0, 4($s1)
  addi $s2,$s0,10
  ```

-
  ```
  slt $s1,$s2,$s3
  sw $s1,4(4$t0)
  ```

3. **Arithmetic**

(a) Draw the optimized Multiplier and Divider hardware discussed in class with appropriate control signals. Observe and write the similarities between these two hardwares. How can we use the same hardware both for multiplication and division. Explain. (Hint: in these hardwares only four elements are there: two registers, one ALU and one abstract control test unit)

(b) Show step by step implementation of dividing 7 by 2 on the above hardware.

4. **MIPS**

(a) Consider the following Array code in C:

```
void shift(int a[], int n){
int i;
for(i=0;i!=n-1;i++)
a[i]=a[i+1];
}
```

i. Translate this function into MIPS assembly.

ii. Convert this function into pointer-based code (in C).

iii. Translate your pointer-based C code from (b) into MIPS assembly.

iv. Compare the number of temporary registers (t-registers) needed for your array-based code from (i) and for your pointer-based code from (ii).

v. What other merits or demerits you can think of in pointer based assembly code compared to array based assembly code.

(b) Provide example instructions for the following MIPS addressing modes:

- Immediate addressing mode
- Base addressing mode for byte, half word and word
- PC-relative addressing mode
- Pseudo direct addressing mode