**BTECH\CSE\2nd Year\Sem-4\2018**
**Computer Organization - CSEN2203**
**Class Test-II**

**Time Allotted: 1hr** **Full Marks: 30**

*Answer any 3 questions(10X3=30)*

1 a) Consider a 4 way set associative cache with 128 blocks and a block size of 16 bytes. Find out cache block number which will contain the main memory address 1200.

b) A hierarchical Cache-MS memory has the following specifications:

i) Cache access time of 90 ns;
ii) Main memory access time of 500 ns;
iii) 80% of memory references are for read and 20% for writes;
iv) The hit ration of 0.9 for read accesses and 0.80 for write access.
v) Probability of setting flag bit is 0.5.

Compute Average access time for read (considering both write through and write back).

Average access times for both read and write (considering both write through and write back). (3+7)

2 a) How many 512K X 8 RAM chips are needed to provide a memory capacity of 8M X 32? Show also the corresponding interconnection diagram.

b) A system has 48 bit virtual address, 36 bit physical address. How many virtual pages and physical frames can the address space support if the page size is 4KB? (8+2)

3 a) Differentiate between I/O mapped I/O and memory mapped I/O.

b) Draw the block diagram of control memory (4096 words of 24 bits each) and the associated hardware for selecting the next microinstruction address.

i) How many bits are there in the control address register?
ii) How many bits are there in each of the four inputs of multiplexer?

(4+6)

4 a) Consider a 4 segments pipeline with 20 ns clock period. Find out speedup for 100 tasks.

b) Discuss different types of data hazards.

c) Find out the CPI in a multi cycle CPU having different instruction classes (22% load, 11% stores, 49% register format operation, 16 % branch and 2% are the jump instruction). The numbers of clock cycles for each instruction class are Load-5, Stores-4, R-format-4, Branch- 3, Jumps-3. (3+3+4)

# HERITAGE INSTITUTE OF TECHNOLOGY

**BTECH\CSE\2nd Year\Sem-4\2018**
**Computer Organization - CSEN2203**
**Class Test-I**

**Time Allotted: 50 mins** **Full Marks: 30**

***Answer any 3 questions (10X3=30)***

1. a) Represent the following floating point numbers using **IEEE (single precision)** format 5

   i) -0.75
   ii) 2.15

   b) Explain the use of the following registers- 5
   - ***i.*** Program counter
   - ***ii.*** Instruction register
   - ***iii.*** Memory address register
   - ***iv.*** Memory data register
   - ***v.*** Accumulator
   - ***vi.*** Stack Pointer

2. a) Perform arithmetic operation (+70) + (+80) in binary using 2's complement representation using 8 bit numbers to accommodate each number with its sign. Indicate whether overflow occurs or not. 3
   b) What is the largest possible value for n bit 2's complement binary number? 1
   c) Apply Booth's algorithm to multiply two numbers (+12) and (-10) 6

3. a) The two word instruction" LOAD AC" is stored at location 200 with its address field at location 201. The address field has the value 500. A processor register R1 contains the number 400. The content of memory locations 400, 500, 600, 700, 702, 900 are 60, 70, 50, 80, 90, 100 respectively.
   Evaluate the effective address and the content of accumulator after the execution of this statement if the following addressing modes are used.
   **i)** direct **ii)** immediate **iii)** relative **iv)** register indirect (use register R1) v) index with R1 as index register 10
4. Evaluate the arithmetic statement X=(A+B)/(C-D) in zero, one, two, three addresses machine instructions. A,B,C,D are variables/memory address. 10