S. No.	**Topic**	(Along with the reference presentations I have sent**)** **Reference Books and Chapters**
1.	Basic organization of the stored program computer and operation sequence for execution of a program- Fetch, decode and execute cycle	Computer Organization, 5th Edition, Carl **Hamacher**, Zvonko Vranesic, Safwat Zaky, MGH- Chapter 1 to 1.5, 1.6.4,1.6.5
2.	Concept of registers and storage, Instruction format, Instruction sets and addressing modes	**Hamacher :-** 2.2 to 2.6 Computer System Architecture, 3rd Edition, **Morris M. Mano**, Pearson:- 8.4 to8.5 upto page 268 Pay attention to : Addressing Mode and Instruction format numericals
3.	Von Neumann & Harvard Architecture RISC vs. CISC based architecture	**Morris M. Mano:-** 8.8 uptp page28 Done in class :- See presentation
4.	Binary number representation; Fixed and Floating point representation of numbers	**Hamacher :-Chapter 6 , 6.1 ,6.7 to 6.7.2** **Morris M. Mano** :- 3.3 Conversions related to IEEE754 floating point numbers
5.	Adders: Serial and Parallel adders, Ripple Carry / Carry Lookahead / Carry Save; Multipliers & Divider Circuits: Multiplication of signed binary numbers Booth Multipliers	**Hamacher :-** 6.1.1 to 6.6
6	Datapath for : Data Movement Instructions / Control Unit Design	**Hamacher :-**Chapter 7 to 7.2
7.	Hardwired and Microprogrammed control. The state machine	**Hamacher :-** 7.4,7.5 **Morris M. Mano** :- **Microprogram sequencer page 234 to 237,** for rest of it use presentation
S. No.	**Topic**	(Along with the reference presentations I have sent**)** **Reference Books and Chapters**

8.	Basic concepts, Instruction pipeline; Concepts of hazards in pipeline and techniques for their removal	**Hamacher :-** Chapter 8 upto page 470: (Delayed branching technique to remove control hazard)
9.	Memory system overview, Cache memory organizations, Techniques for reducing cache misses	**Hamacher :-** Chapter 5 to page 299, 5.2.5 to page 307, 5.3 to 5.5.2 page 322 **Morris M. Mano** :- 12.2 and Table 12.1memory address map for microcomputer using Hexadecimal address, and Figure 12.4 on page 455 memory address map and memory connection to CPU (these are given in reference presentation on memory sent to you.)
10.	Memory mapped IO. Introduction to I/O interfaces. Interrupts, Interrupt hardware, Enabling and Disabling interrupts, , Polled I/O, Priorities, Daisy Chaining. Vectored interrupts;	**Hamacher :-**Chapter 4 to 4.2.3 page 217 **Morris M. Mano** :-page 408 for **Vectored interrupts;**
11	Direct memory access, DMA controller. Instruction sequencing with examples	**Morris M. Mano** :- 11.6 upto page 422 **Hamacher :-**4.4
		https://nptel.ac.in/courses/106103068/

Revision References