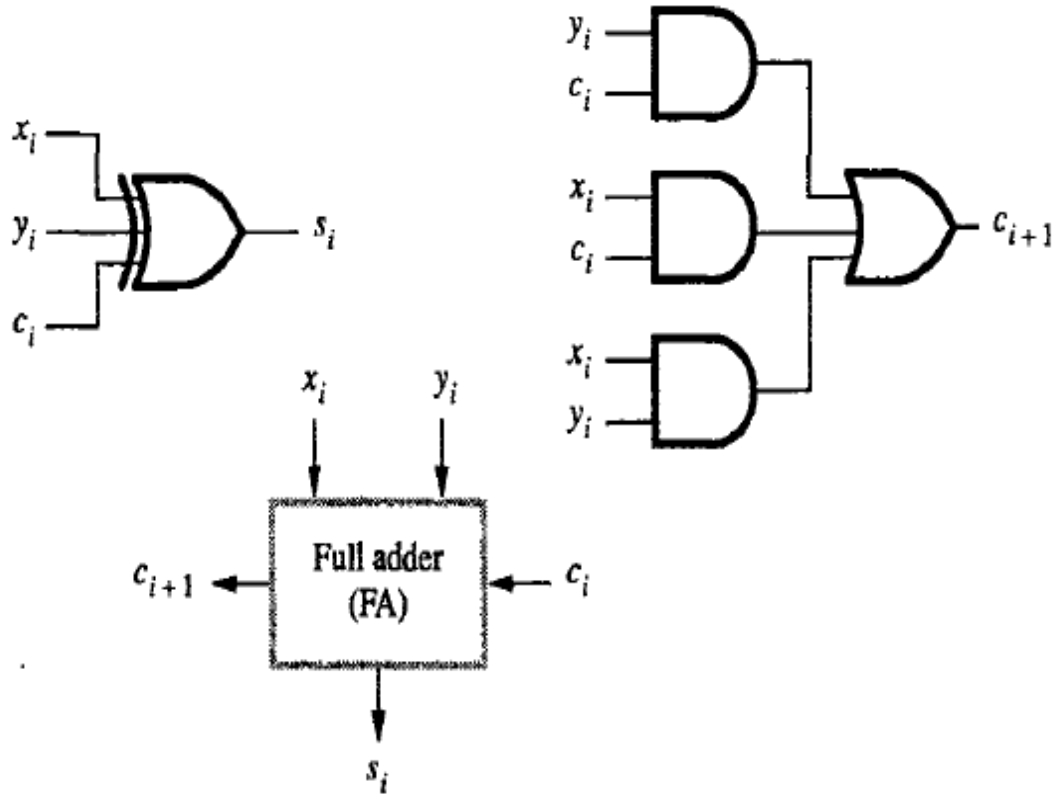
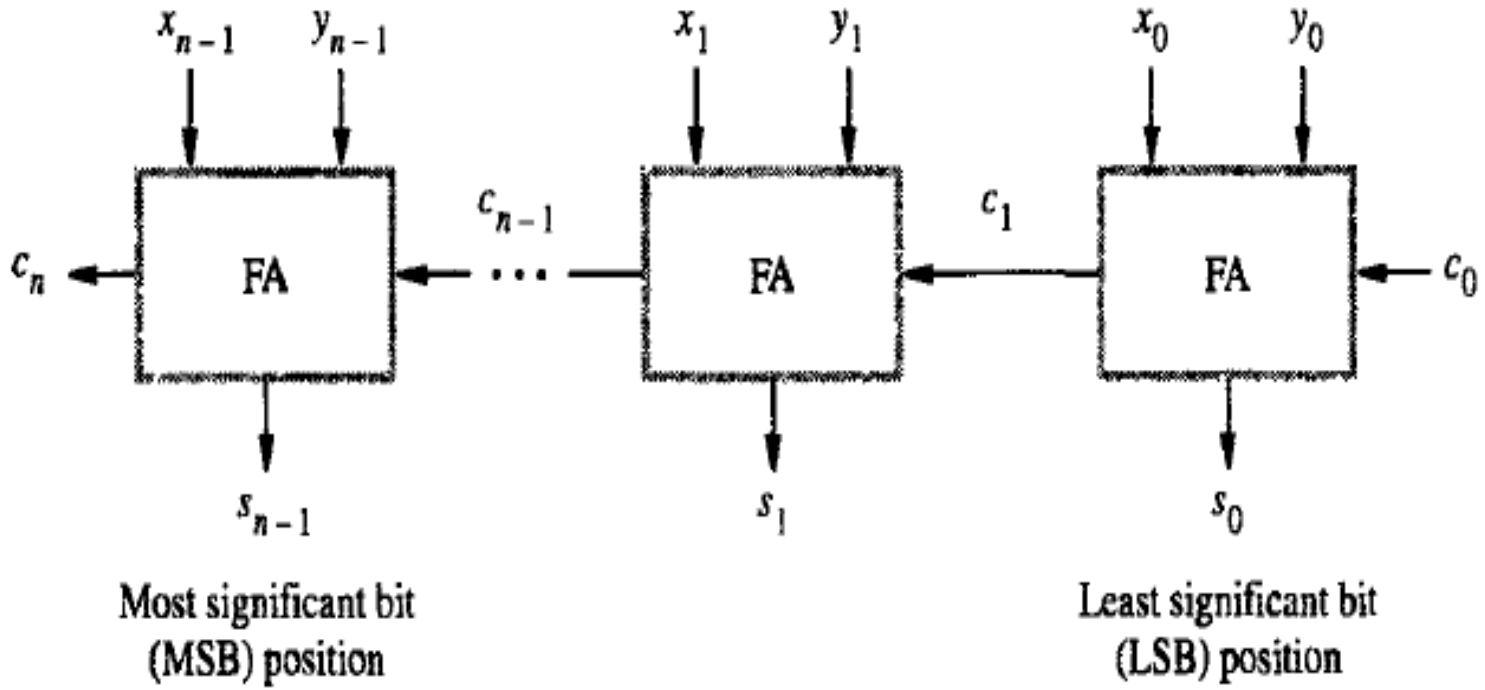
Ripple Carry Adder Gate Delay



(a) Logic for a single stage

elay in getting Ci+1 from time when Ci enters is 2 gate delay
available after 1 gate delay



(b) An *n*-bit ripple-carry adder

Cn got after 2n gate delays
Sn-1 got after 2n-1 gate delays from time when C_0 enters RCA

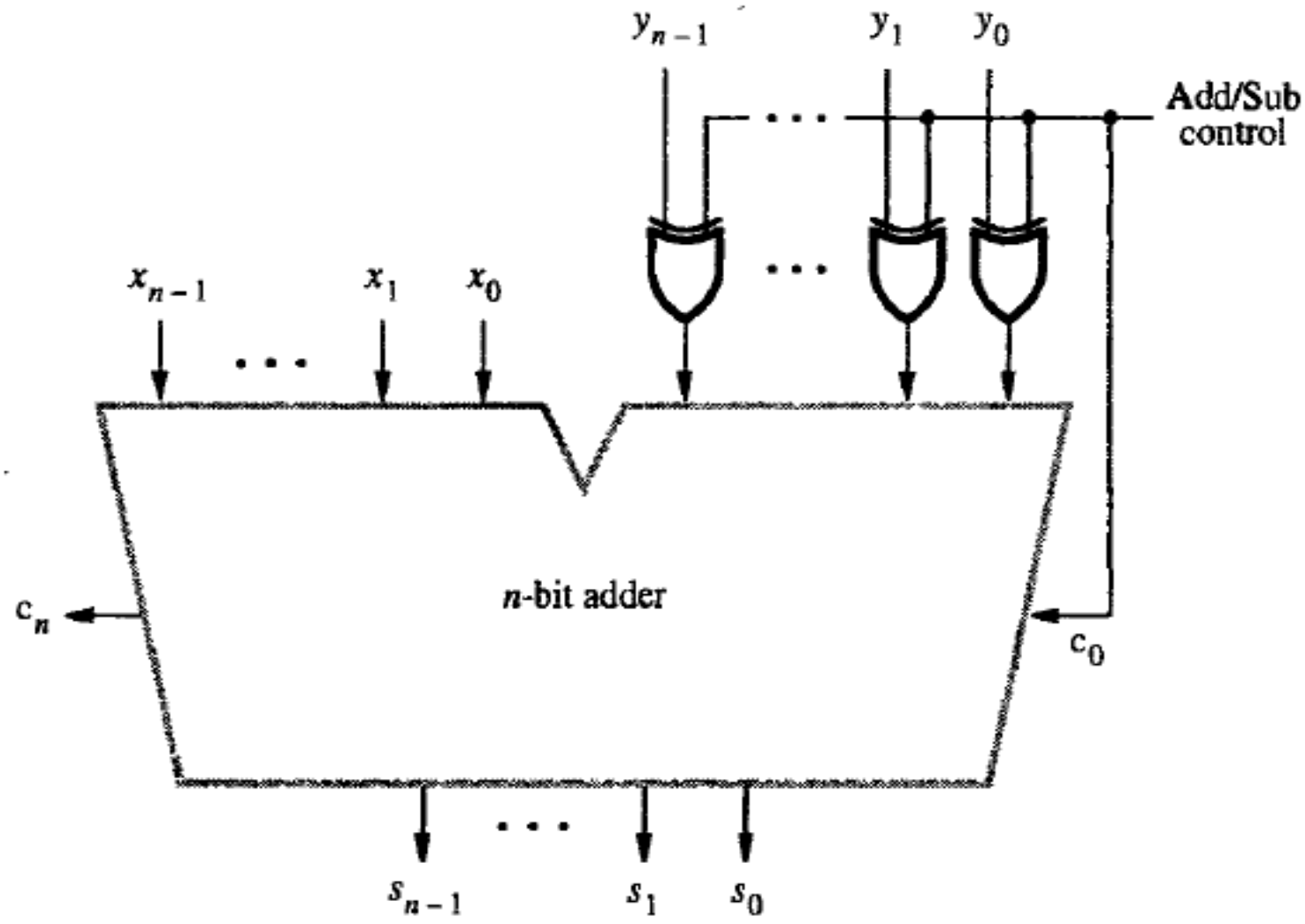


Figure 6.3 Binary addition-subtraction logic network.

Gate Delays in Ripple Carry Adder/Subtractor

- In adder/subtractor
  - Sum/difference available after 2n-1 +1(for the xor gate used in add/sub control= 2n gate delays

    and Cn after 2n +1 gate delays
  - Plus another xor gate checks for overflow to detect the overflow condition $c_n \oplus c_{n-1}$.
  - So Cn available after 2n+2 gate delays
    - For 8 bit adding C8 available after 18 gate delays!!