RAM Chip(Memory)

- Random Access Memory (**RAM**)
  - Initially contains no data
  - Digital circuit can retrieve and store data at various locations on a RAM chip
  - Data pins are bidirectional (into or out of the chip)
  - **Volatile**: loses data when power is removed

RAM

- static RAM (SRAM).
  - cells take more space; cannot be made as dense as DRAM
  - result: SRAM is more expensive than DRAM
  - used where high speed is necessary (e.g., cache)
  - The contents stay valid and does not have to be refreshed.
- dynamic RAM (DRAM)
  - Leaky capacitors. DRAM needs to be refreshed after several milliseconds
  - results in longer *cycle time*, the minimum time between consecutive memory accesses
  - simpler internally
  - Cheaper. Used for Computer Primary memory
- normally DRAM is a generation ahead of SRAM in terms of size

Memory

- Reading a memory:
  - place address code of the desired locations on the address pins of the RAMs/ROMs
  - internal circuit must read address and enable the correct bit cells
  - places contents of the locations on the output lines
  - Each RAM chip has 2^n * m bit cells. n address inputs and m bidirectional data pins

The following slides give details of the above read process for DRAM chip

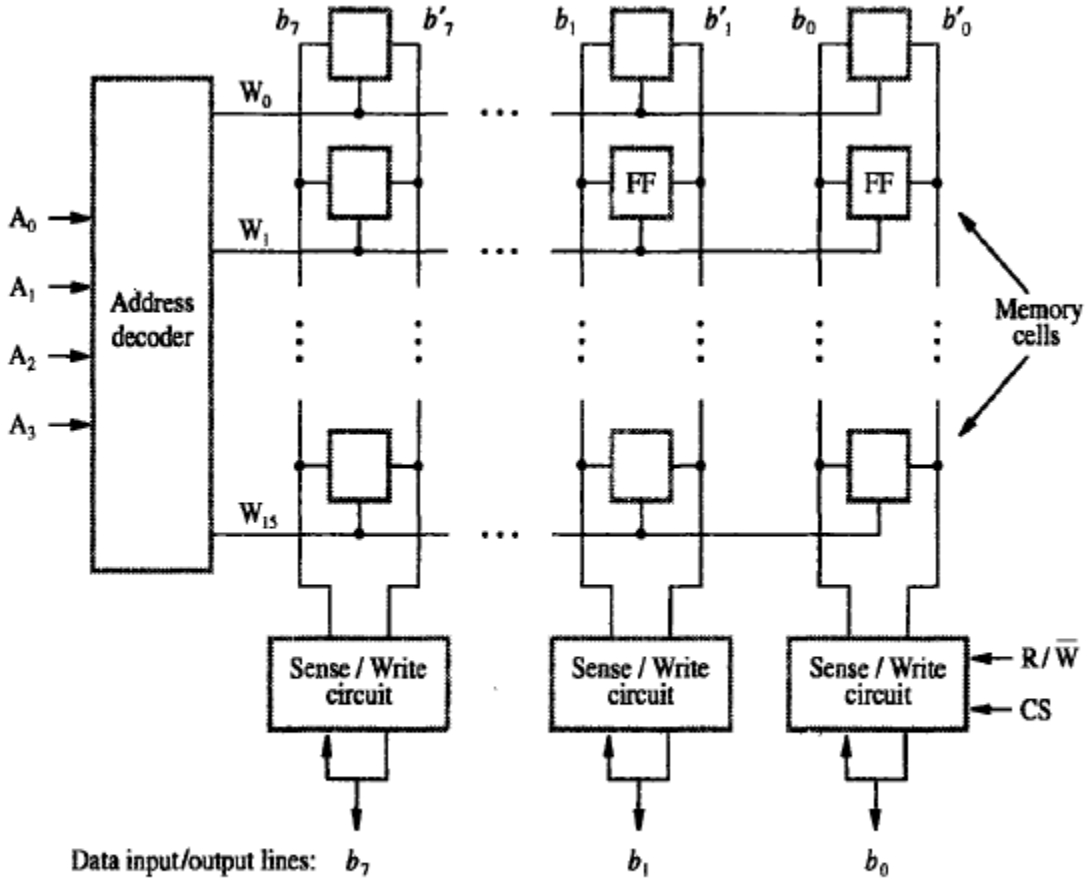
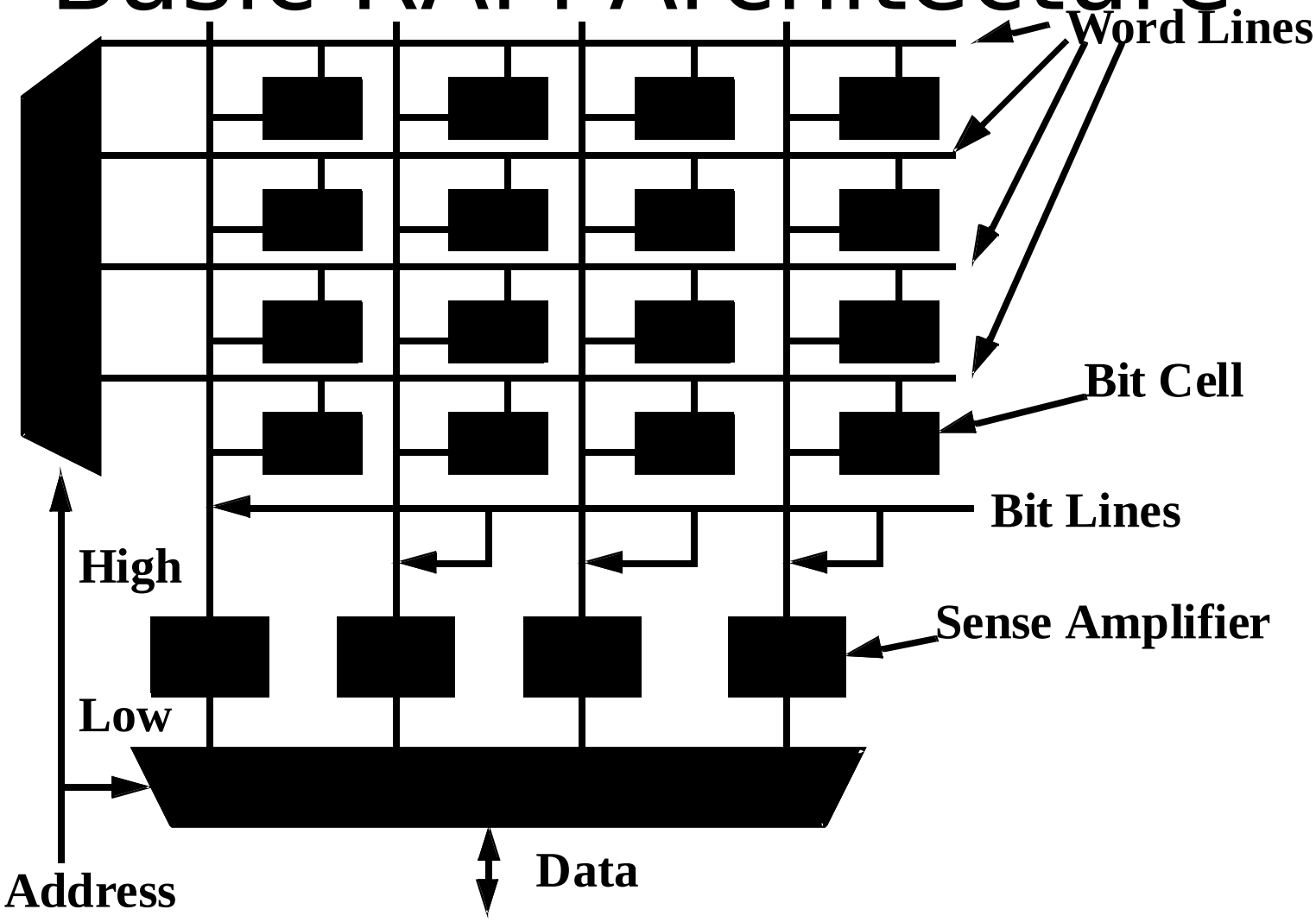


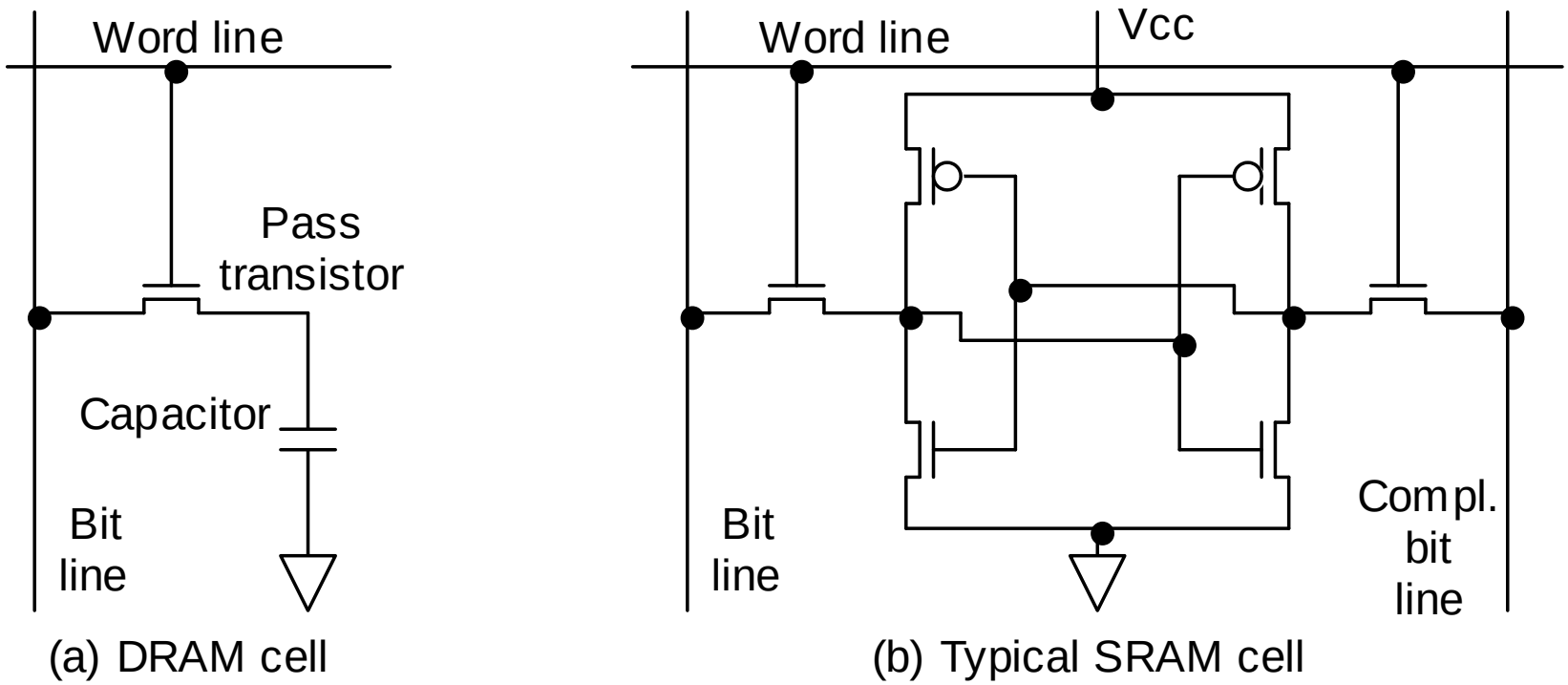
Figure 5.2 Organization of bit cells in a memory chip.

Basic RAM Architecture



Memory Bit Cell
(Inside Pink Boxes of previous slide)

DRAM vs. SRAM Memory Cell Complexity

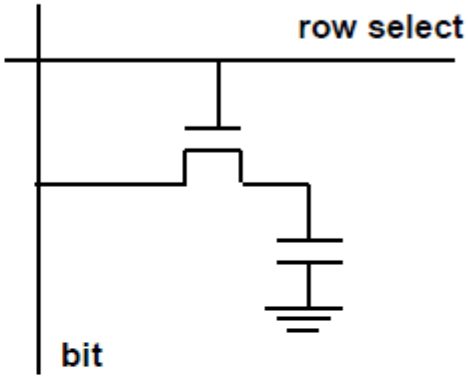


(a) DRAM cell

(b) Typical SRAM cell

Single-transistor DRAM cell, which is considerably simpler than SRAM cell, leads to dense, high-capacity DRAM memory chips.

1-Transistor Memory Cell (DRAM)



- **Write:**
  - 1. Drive bit line
  - 2.. Select row
- **Read:**
  - 1. Precharge bit line to Vdd
  - 2.. Select row
  - 3. Cell and bit line share charges
    - Very small voltage changes on the bit line
  - 4. Sense (fancy sense amp)
    - Can detect changes of ~1 million electrons
  - 5. Write: restore the value
- **Refresh**
  - 1. Just do a dummy read to every cell.

DRAM

- DRAM value is stored as a charge on a capacitor.
  - A single transistor is used to access the stored charge.
  - Capacitors lose charge after several milliseconds
  - To keep a charge, must refresh the capacitor
  - Single-chip memory controllers handle the refresh function independent of the CPU.
- .
- DRAM cells are smaller, thus DRAM are denser

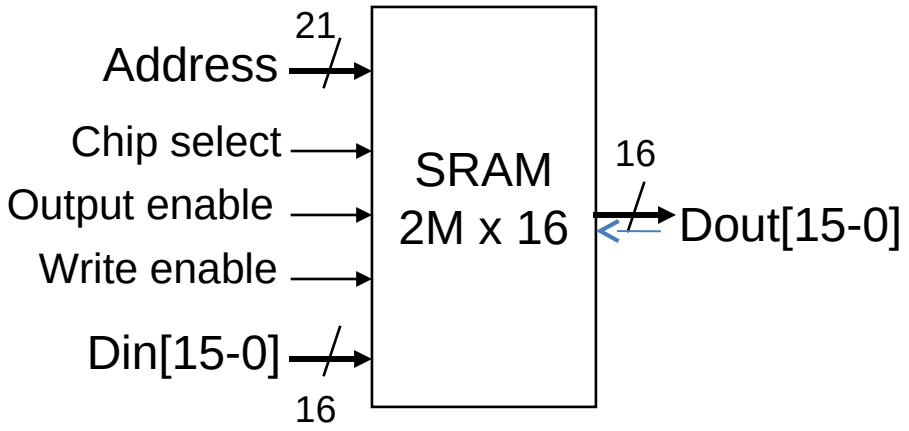
DRAM

- Refreshing
  - Use a two-level decoding structure.
    - Allows us to refresh an entire row at a time
  - Refresh typically consumes 1% to 2% of the active cycles of the DRAM.

RAM contd..

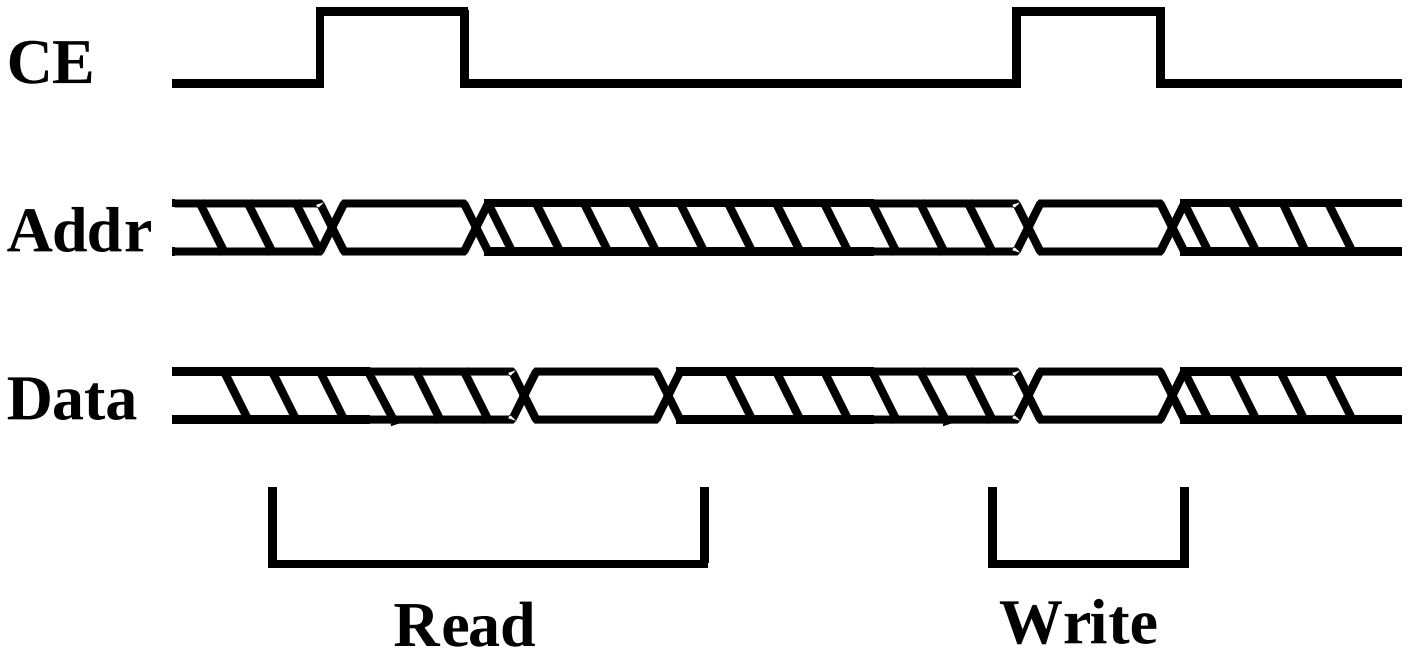
- Main Memory uses *DRAM* for size (density)
  - High density (1 transistor cells), low power, cheap, slow
  - Dynamic: needs to be “refreshed” regularly (~ every 8 ms)
    - 1% to 2% of the active cycles of the DRAM

SRAM



- Caches use *SRAM* for speed and technology compatibility
  - Low density (6 transistor cells), high power, expensive, fast
  - Static: content will last "forever" (until power turned off)

Accessing a Static RAM



Note: CE signal is often active-low as opposed to how shown here. SRAMs also generally have a write enable signal

Memory Subsystem

- 2 Types of Memory:
  - ROM : Read Only Memory
    - Program that is loaded into memory and cannot be changed. Also retains its data even without power.
  - RAM : Random Access Memory
    - Also called read/write memory. This type of memory can have a program loaded and then reloaded. It loses its data with no power.

ROM Chip(Memory)

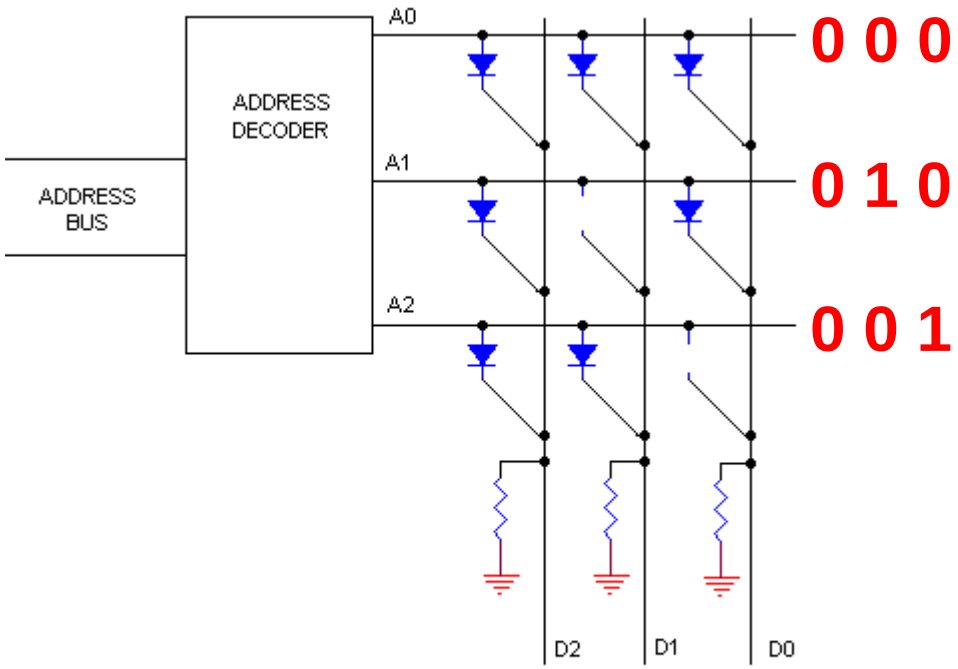
- Read Only Memory (**ROM**)
  - Once programmed, cannot be changed
  - Used as lookup tables to implement functions
  - Used in PCs to store basic input/output systems (BIOS)
  - Nonvolatile: keeps value when power is removed

Different ROM Chips

- Masked ROM :
  - ROM that is programmed with data when fabricated. Data will not change once installed. Hardwired.
- Programmable ROM (PROM) :
  - Capable of being programmed by the user with a ROM programmer. Not hardwired.
- Erasable PROM (EPROM) :
  - Much like the PROM this EPROM can be programmed and then erased by light.
- EEPROM :
  - Another form of EPROM but is reprogammable electrically.(Electrically erasable PROM)

ROM

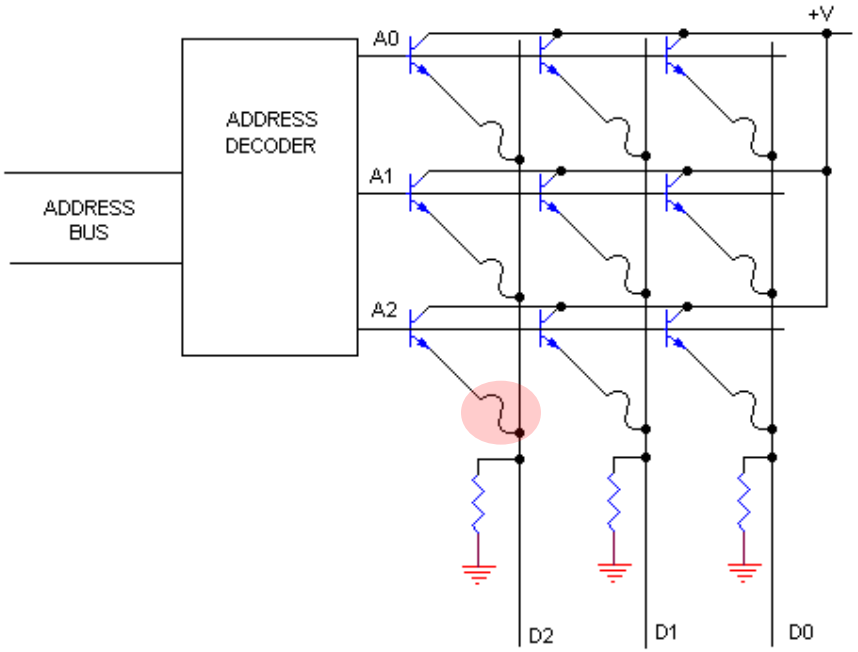
- Data is stored in a ROM by breaking or preserving connections
  - using a diode, transistor or fuses



READ ONLY MEMORY (ROM)

PROM

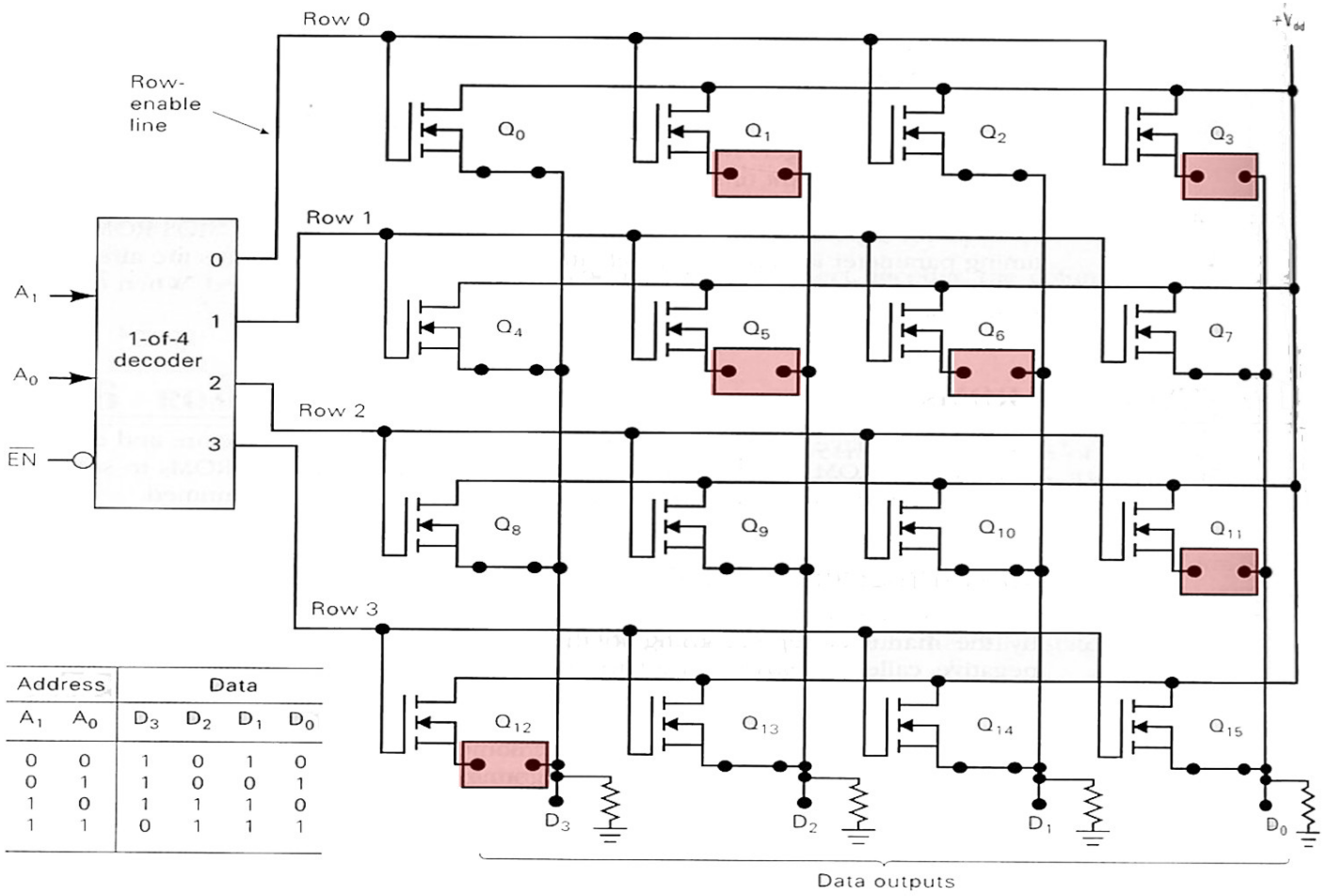
- PROMs can only be programmed once
- They are more fragile than ROMs
  - a jolt of static electricity can cause fuses in the PROM to burn out, changing bits from 1 to 0
- Blank PROMs are inexpensive and are good for prototyping the data for a ROM before committing to the costly ROM fabrication process.



PROGRAMMABLE READ ONLY MEMORY (PROM)

PROM

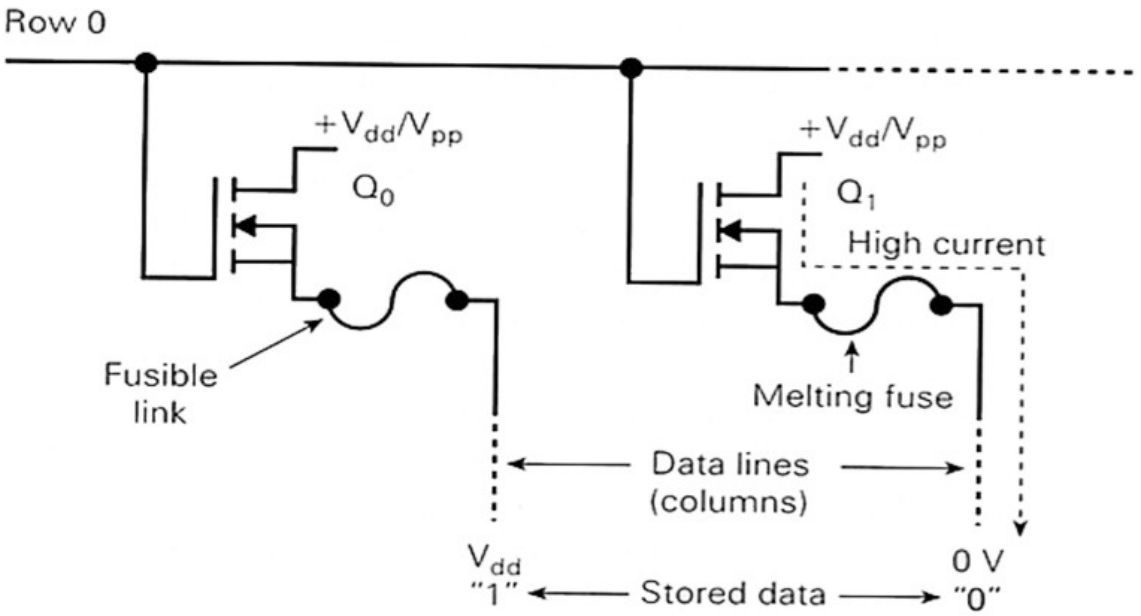
- A closer look



Address		Data			
A_1	A_0	D_3	D_2	D_1	D_0
0	0	1	0	1	0
0	1	1	0	0	1
1	0	1	1	1	0
1	1	0	1	1	1

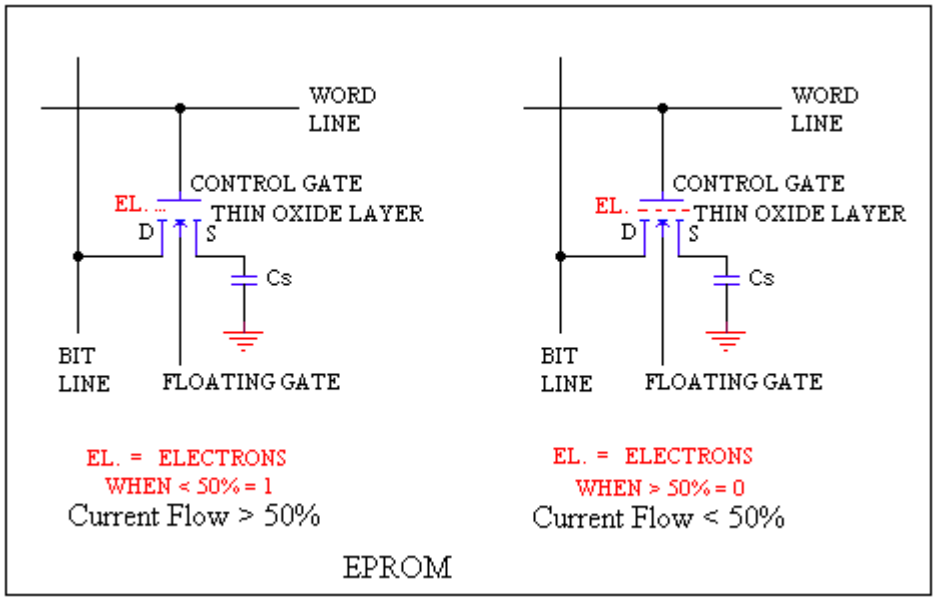
PROM

- Programming the PROM is accomplished by passing a high current through a specific transistor and melting the fuse
  - One-time programmable



EPROM

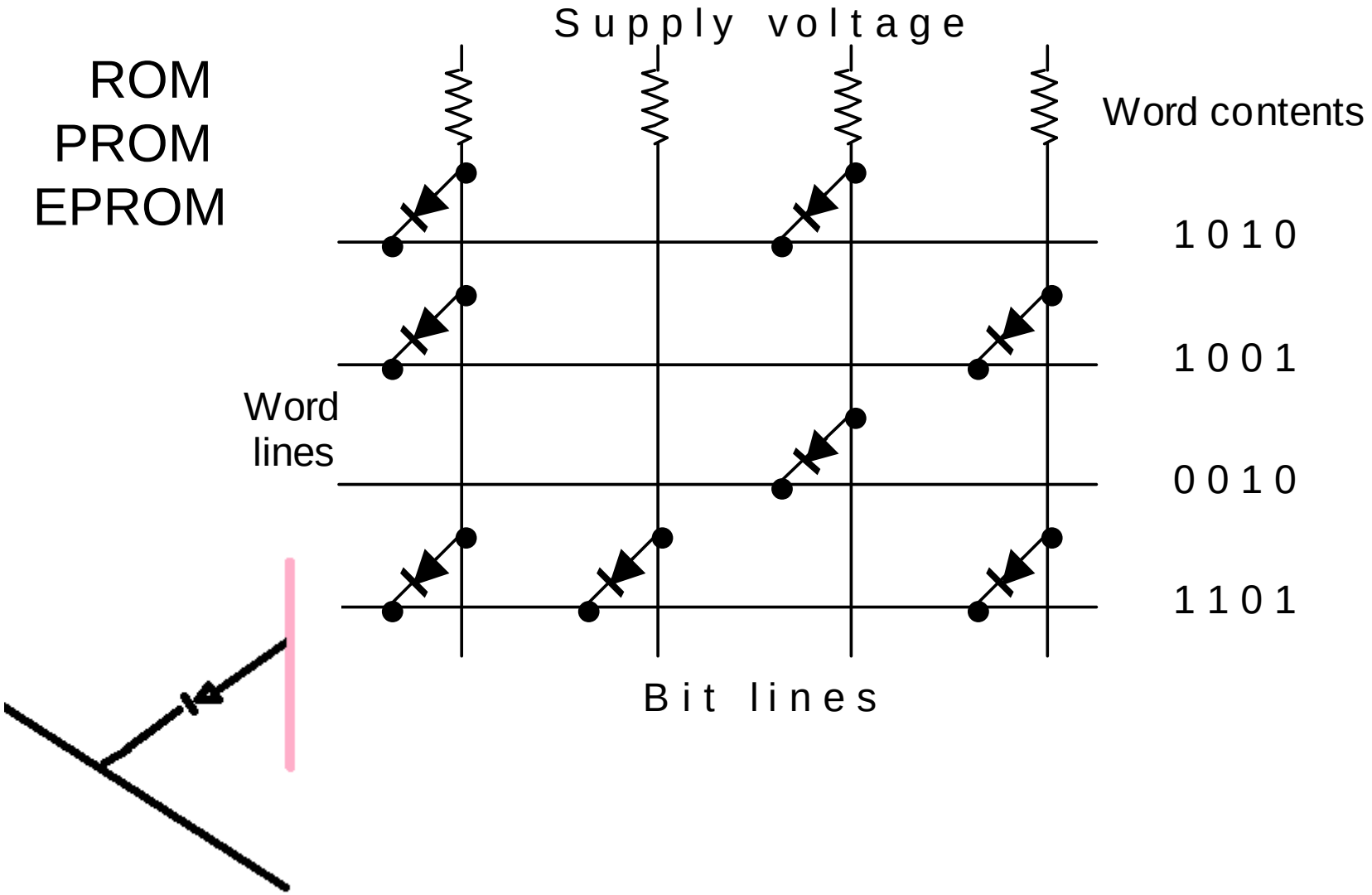
- An EPROM eraser is not selective, it will erase the entire EPROM.
- The EPROM must be removed from the device it is in and placed under the UV light of the EPROM eraser for several minutes.



- An EPROM that is left under UV light too long can become over-erased.
  - In such a case, the EPROM's floating gates are charged to the point that they are unable to hold the electrons at all.

17.5 Nonvolatile Memory

ROM
PROM
EPROM



Increasing Size of Memory Using Chips

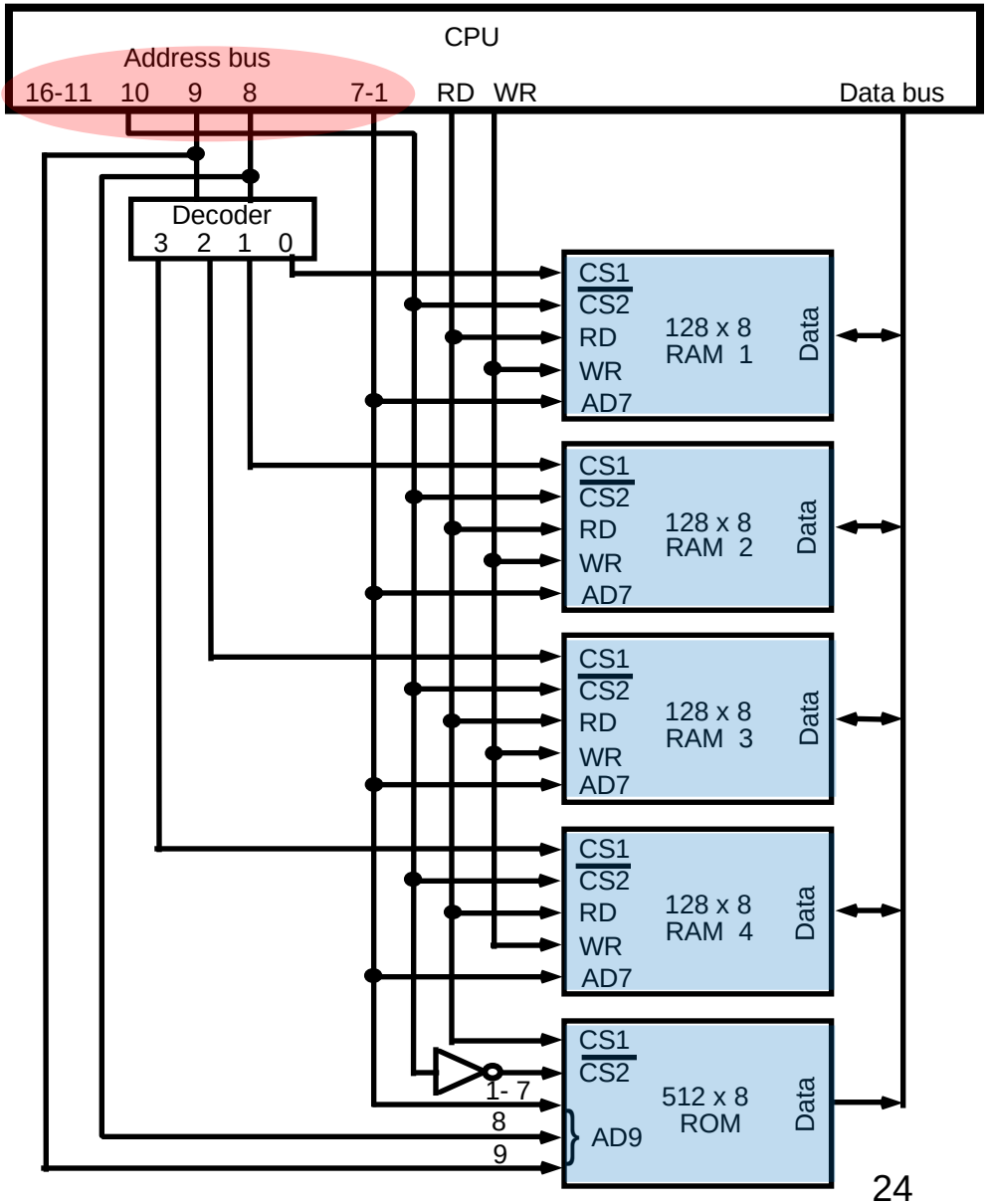
- Memory subsystem is the combination of memory chips
- Example : 8 x 2 chips can be combined to make an 8 x 4 memory.
- Both chips will receive the same 3 address inputs from the bus, as well as the CE and OE signals.
- The data pins of the first chip are connected to bits 3 and 2 and the other to 1 an 0 of the data bus

Memory Subsystem Cont.

- When the CPU reads data it places the address on the address bus.
- Both chips will read in bits A1, A2, and A0 and decode
- Since both chips are using the same CE and OE either both chips are active or not.
- To the CPU it will act just like an 8 x 4 memory chip.

Memory Location Extension: Another Example

- Memory Connection to CPU
- Illustrates the use of both RAM and ROM in the same memory space
- Shows the utility of chip-select inputs
- Shows creative use of address lines



Morris M. Mano :- 12.2
Figure 12.4 on page 455
memory address map and
memory connection to CPU

Memory Address Map for Microcomputer

		Address Bus									
Component	Hexadecimal Addr	10	9	8	7	6	5	4	3	2	1
RAM1	0000-007F	0	0	0	x	x	x	x	x	x	x
RAM2	0080-00FF	0	0	1	x	x	x	x	x	x	x
RAM3	0100-017F	0	1	0	x	x	x	x	x	x	x
RAM4	0180-01FF	0	1	1	x	x	x	x	x	x	x
ROM	0200-03FF	1	x	x	x	x	x	x	x	x	x

Morris M. Mano :- 12.2 Table 12.1memory address map for microcomputer using Hexadecimal address