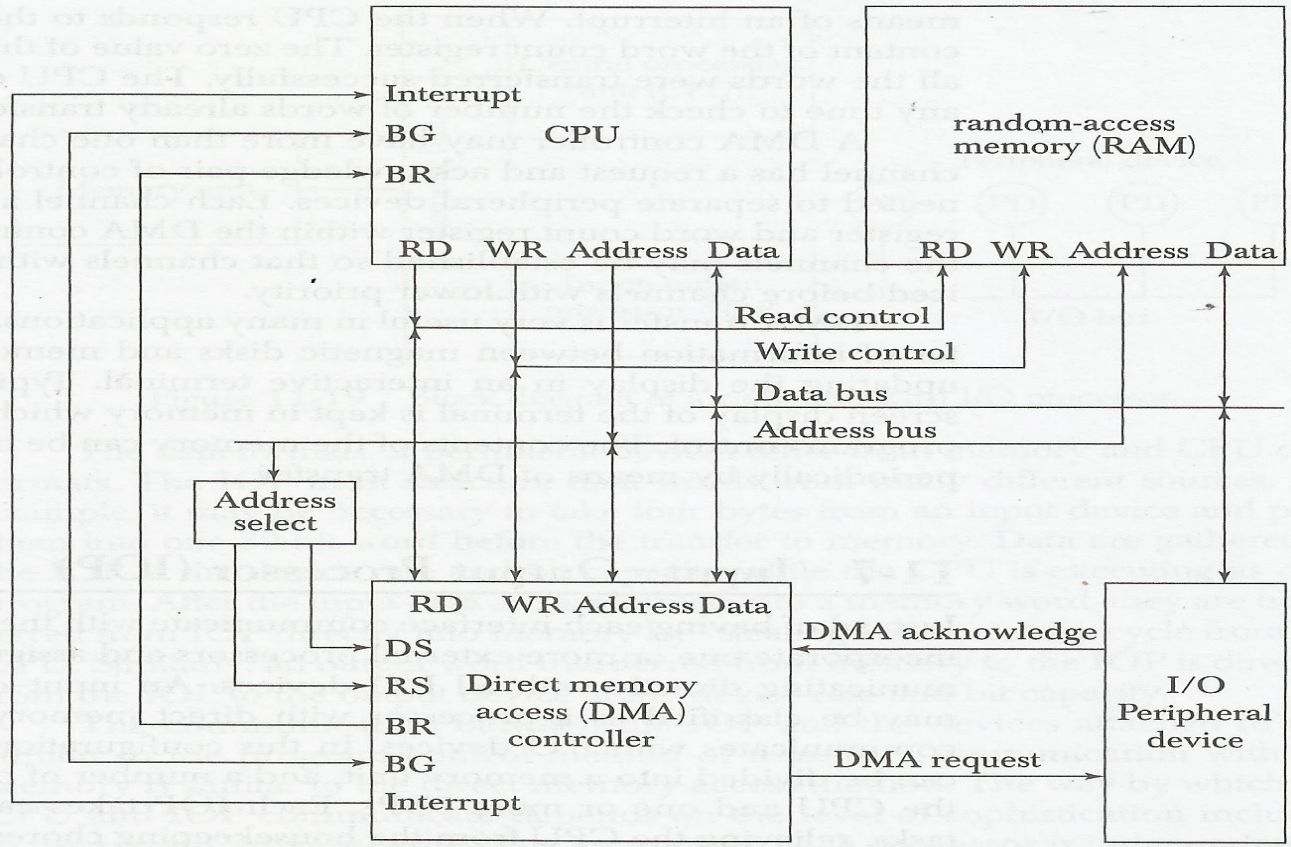

Figure 11-18 DMA transfer in a computer system.

From Mano

Sequence Of DMA Operation

- The DMA request CPU
  - to handle control of buses bus request (BR) signal
- CPU initializes the DMA by sending following information through the data bus.
  - Starting address of memory block for read or write operation.
  - The word count which is the no. of words in the memory block.
  - Control to specify the mode of transfer such as read or write.
  - A control to start the DMA transfer.

Sequence Of DMA Operation contd..

- CPU places the address bus, data bus and read and write lines into high impedance state (which behave like open circuit)
- Then CPU grants the control of buses to DMA using bus grant (BG) signal

Sequence Of DMA Operation contd..

- The DMA takes control over the buses
  - directly interacts with memory and I/O units
  - transfers the data without CPU intervention
- When the transfer completes,
  - DMA disables the BR line.
  - CPU disable BG line and takes control over the buses
  - return to CPU normal operation.