2013

COMPUTER ARCHITECTURE

Time Allotted : 3 Hours | Full Marks : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) The prefetching is a solution for

a) Data Hazard b) Structural Hazard

c) Control Hazard d) None of these.

ii) Performance (P) and execution time (T) of CPU are related by

a) $P \propto T$ b) $P \propto 1/T$

c) $P = T$ d) None of these.

iii) Loop scheduling includes

a) Loop Unrolling b) Software Pipelining

c) Both (i) and (ii) d) None of these.

iv) Pipeline computers perform computations to exploit

a) Temporal Parallelism

b) Spatial Parallelism

c) Sequential behavior of program

d) Modularity of program.

v) The number of machine instructions to be executed in the program is called the

a) Cycle b) Time period

c) Instruction Count d) None of these.

vi) Array Processors are put under which of these categories ?

a) SISD b) SIMD

c) MISD d) MIMD.

vii) A Program segment chosen from parallel processing is known as

a) Grain b) Cluster

c) Work Station d) None of these.

viii) An n-dimensional hypercube has

a) n^n nodes b) n nodes

c) 2^n nodes d) None of these.

ix) The vector stride value is required

a) to deal with the length of vectors

b) to find the parallelism in vectors

c) to access the elements in multi-dimensional vectors

d) none of these.

x) Effective access time (T_{eff}) of memory is given by

a) $T_{eff} = 1/\sum_{i=1}^{n} fi.ti$ b) $T_{eff} = \sum_{i=1}^{n} fi.ti$

c) $T_{eff} = \sum_{i=1}^{n} fi/ti$ d) None of these.

xi) Scatter operation is reverse of

a) Gather b) Masking

c) Chaining d) None of these.

xii) The division of stages of a pipeline into sub-stages is the basis for

a) Pipelining b) Super-pipelining

c) Superscalar d) VLIW.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Explain with an example the requirement of a vector processor.

3. A certain program generates the following sequence of word addresses :

4, 5, 12, 8, 10, 28, 6, 10

A page has four words; the number of page frames in main memory is 3. How many page faults are generated if optimum page replacement policy is used ?

4. a) Define write through and write back schemes and compare them.

b) What is the fundamental difference in interprocesso coordination mechanism between multiprocessor an multicomputer systems ?

5. Define cache coherence. Explain the techniques to avo cache coherence. 2 +

6. a) Discuss briefly MISD architecture.

b) Explain data flow architecture. 2 -

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) What is reservation table ? 2

b) Consider a five-stage pipelined processor specified by following reservation table :

	1	2	3	4	5	6
S_1	×					×
S_2		×			×	
S_3			×			
S_4				×		
S_5		×				×

i) List the set of forbidden latencies and the collision vector. 2

ii) Draw the state transition diagram. 2

iii) List all simple cycles from state diagram. 2

iv) Identify the greedy cycles among the simple cycles. 1

v) Find out minimum Average Latency. 1

vi) Find out maximum throughput of this pipeline. 1

vii) Find out the bounds of MAL. 2

c) Show that the maximum speed-up of a pipeline is equ to its number of stages.

8. a) What do you mean by cache coherence problem Describe one method to remove this problem a indicate the limitations.

b) What do you mean by program flow mechanism Compare between control flow, data flow and dema driven mechanisms. 1

c) Explain in brief with neat diagrams the Flyn classification of computers.

9. a) Derive an expression for effective access time for n-level memory system having hit ratios h_1, h_2, .. h_n a access times t_1, t_2, ..., t_n where $t_1 < t_2 < t_3 < \ldots < t_n$.

b) Consider the performance of a main mem organization, when a cache miss has occurred, as

- 4 clock cycles to send the address.
- 24 clock cycles for the access time per word
- 4 clock cycles to send a word of data.

Estimate —

i) the miss penalty for a cache block of 4 words.

ii) the main memory bandwidth. 3