Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH(IT)(N)/ SEM-5/IT-502/2012-13

2012

COMPUTER ARCHITECTURE

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) A pipeline stage

      a) is sequential circuit

      b) is combinational circuit

      c) consists of both sequential and combinational circuits

      d) none of these.

   ii) How many address bits are required for a 512×8 memory ?

      a) 512 b) 8

      c) 9 d) $A_0 - A_6$.

iii) Consider the cache memory with access time 40 ns has the hit ratio of 80%. The regular memory has an access time of 100 ns. What is the effective access time for CPU to access memory ?

a) 52 ns b) 60 ns

c) 70 ns d) 80 ns.

iv) What will be the speed up for a four stage linear pipeline when the number instructions $n = 64$?

a) 4·5 b) 7·1

c) 6·5 d) none of these.

v) The performance of a pipeline processor suffers if

a) the pipeline stages suffer different delay

b) consecutive instructions are dependent on each other

c) the pipeline stages share same resources

d) all of these.

vi) Array processor is present in

a) SIMD b) MISD

c) MIMD d) none of these.

vii) Dynamic pipeline allows

a) multiple functions to evaluate

b) only steamline connection

c) to perform fixed function

d) none of these.

viii) The number of cycles required to complete n tasks in a k stage pipeline is

a) k b) $n + k - l$

c) $nk + 1$ d) $n - k + 1$.

ix) Which one of the following architecture has no practical usage ?

a) SIMD b) SISD

c) MISD d) MIMD.

x) Superscalar processors have CPI of

a) less than 1 b) grater than 1

c) more than 2 d) greater than 3.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following $3 \times 5 = 15$

2. Explain with an example the requirement of a vector processor.

3. a) Define 'Write Back' and 'Write Through' schemes and compare them.

   b) A hierarchical-MS memory subsystem has the following significances :

      i) Cache access time of 50 sec

      ii) Main storage access time of 550 sec

      iii) 80% of memory requests are for READ

      iv) Hit ratio of 0·9 for READ access

      v) Write through scheme is employed.

      Estimate the average access time of the system considering only memory READ cycle. 2½ + 2½

4. Define Cache Coherence. Explain techniques to avoid Cache Coherence.

5. a) Discuss briefly MISD architecture.

   b) Compare super-scalar, super-pipeline & VLIW techniques. 2½ + 2½

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

6. a) What is pipeline ?

   b) Consider the following reservation table :

	1	2	3	4
S1	X			X
S2		X		
S3			X	

Write down the forbidden latencies and initial collision vector. Draw the state diagram for scheduling the pipeline. Find out the simple, greedy cycle and MAL. If the pipeline clock rate is 25 MHz, then what is the throughput of the pipeline ? What are bounds on MAL ?

2 + 2 + 3 + 3 + 2 + 3

7. a) What is cache memory ? Define global miss and local miss with suitable example.

   b) Describe different technique for reduce Miss Penalty.

   c) Distinguish between write through and write back cache. (2 + 5) + 4 + 4

8. a) What is vector processor ? Write the different types of vector instruction.

   b) Compare between vector processor and array processor.

   c) What are strip mining and vector stride, in respect of vector processor ? (1 + 4) + 5 + 5

9. a) Explain loosely coupled and tightly coupled multiprocessor system.

   b) Compare dynamic connection networks such as multi-stage interconnection networks and crossbar switch networks in terms of bandwidth and hardware complexity such as switching, arbitration, wire etc.

   c) Explain data flow architectures. 5 + 5 + 5

10. Write short notes on any *three* of the following : 3 × 5

a) Array processor

b) Memory interleaving

c) Vector registers architectures

d) SPARC Architecture

e) Cache Coherence.

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