MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

IT-502

COMPUTER ARCHITECTURE

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.
All symbols are of usual significance.

GROUP A
(Multiple Choice Type Questions)

1. Answer *all* questions. $10 \times 1 = 10$

(i) The performance of a pipelined processor suffers if
(A) the pipeline stages have different delays
(B) consecutive instructions are dependent on each other
(C) the pipeline stages share hardware resources
(D) all of these

(ii) What will be the speed up for a 4 segment linear pipeline when the number of instruction $n = 64$?
(A) 4.5 (B) 3.82 (C) 8.16 (D) 2.95

(iii) In which type of memory mapping there will be conflict miss?
(A) direct mapping (B) set associative mapping
(C) associative mapping (D) both (A) and (B)

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(iv) Example of a recirculating network is
(A) 3 cube network (B) ring network
(C) tree network (D) mess connected Illiac network

(v) Array process is present in
(A) MIMD (B) MISD (C) SISD (D) SIMD

(vi) Which type of data hazard is not possible?
(A) WAR (B) RAW (C) RAR (D) WAW

(vii) In general 64 input Omega network requires _____ stages of 2×2 switches
(A) 6 (B) 64 (C) 8 (D) 7

(viii) Virtual address space can be divided into some fixed size
(A) segments (B) blocks (C) pages (D) none of these

(ix) MIPS means
(A) Multiple Instruction Per Second
(B) Millions of Instruction Per Second
(C) Multi-Instruction Performed System
(D) None of these

(x) Which is not the property of a memory module?
(A) inclusion (B) consistency (C) capability (D) locality

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. $3 \times 5 = 15$

2. For the code segment given below, explain how delayed branching can help: 5
11. LOAD R1, A
12. Dec R3,1
13. BrZero R3,15
14. Add R2, R4
15. Sub R5, R6
16. Store R5, B

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3. Explain vector processing. Explain how it is different from array processing. 2+3

4. Draw data flow graph to represent the following computations: 5
   1. $A = P + Q$
   2. $B = A / Q$
   3. $C = P * A$
   4. $D = C - B$
   5. $E = C * A$
   6. $F = D / E$

5. What is the fundamental difference in interprocessor coordination mechanism between multiprocessor and multicomputer systems? Explain with reference to their architectural differences. 5

6. Explain Cache Coherence and Inference. 3+2

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) What do you mean by Cache Coherence problem? Describe one method to remove this problem and indicate its limitations. 5

   (b) What do you mean by Program Flow Mechanism? Compare between Control-Flow, Data-Flow and Demand-Driven mechanism. 1+4

   (c) Explain in brief with neat diagrams the Flynn's classifications of computers. 5

8. (a) What do you mean by loosely coupled and tightly coupled multiprocessors? 5

   (b) Compare and contrast between UMA and NUMA with examples. What is Dumb memory? 4+1

   (c) What are the major differences between Segmentation and Paging? Why the page size is usually a power of 2? 3+2

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9. (a) An address space is specified by 28 bits and corresponding memory space of 26 bits. If a page consists of 4K words 2+3
   (i) How many pages and blocks are there in the system?
   (ii) The associative memory page-table contains the following entries

Page	Block
0	0
1	1
5	2

   Make a list of all virtual addresses (in decimal and in binary), that will cause a page fault.

   (b) Briefly explain the two write policies: write through and write back with advantages and disadvantages. 5

   (c) What are the different types of vector operations? Give different fields in a vector instruction. What is pipeline chaining? 3+1+1

10. (a) A system has 48 bit virtual address, 36 bit physical address and 128 MB main memory address. If the system has 4096 bytes pages, how many virtual and physical pages can have address support? How many page frames of main memory are there? 2+2+1

    (b) Describe the different types of interconnection networks in computer systems. What are multistage switching networks? 4+1

    (c) What do you understand by instruction pipelining and arithmetic pipelining? Why pipeline scheduling is necessary and how it is done? 2+2+1

11. (a) Describe different access methods of the memory system. What will be the maximum capacity of a memory, which uses an address bus of size 8 bit? 1+4

    (b) What is the objective of OPT page replacement algorithm policy of virtual memory? Using LRU, show the pagefault rate for the reference string 1+4
    7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1

    (c) Define pipelining technique. Assume a 4 stage pipeline: 1+4
    Fetch : Read the instruction from the memory
    Decode: Decode the instruction
    Execute: Execute the instruction
    Write: Store the result in destination location
    Draw the space-time diagram for pipelining.