IT-705D

MICROELECTRONICS AND VLSI DESIGN

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP A
(Multiple Choice Type Questions)

1. Answer any *ten* questions. 10×1 = 10

(i) VHDL is acronym of
(A) verilog hardware description language
(B) very high speed insulated chip hardware description language
(C) very high speed integrated circuit hardware description language
(D) none of these.

(ii) For depletion type n-MOS
(A) the threshold voltage is + ve
(B) the threshold voltage is – ve
(C) the threshold voltage is + ve and – ve
(D) all of these

(iii) BiCMOS means
(A) two BJT circuits (B) two CMOS circuits
(C) both BJT and CMOS circuits (D) none of these

(iv) NAND flash memory is constructed with.
(A) 2 parallel cells (B) 16 cells in series
(C) 8 cells in parallel (D) none

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(v) Latch up is defined as the.
(A) low impedance (B) high impedance
(C) medium impedance (D) none

(vi) Designable parameters are.
(A) commonly grouped (B) loosely coupled
(C) tightly coupled (D) none

(vii) Noise parameters are treated as.
(A) static variables. (B) random variables.
(C) constants. (D) none

(viii) A circuit performance major is used to monitor
(A) functionality of circuit (B) durability of circuit
(C) accountability of circuit (D) none

(ix) Designable parameters are
(A) deterministic (B) probabilistic
(C) indeterministic (D) none

(x) Which among the following requires lowest design cycle time?
(A) semi-custom ASIC (B) full-custom ASIC
(C) standard cell-based design (D) FPGA

(xi) Different FPGA programming technologies are based on
(A) SRAM (B) EPROM
(C) Anti-fuse (D) all of these

(xii) The model parameter LAMDA (λ) in a MOS structure stands for
(A) flicker noise coefficient (B) transit time
(C) channel length modulation (D) transconductance

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GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. (a) What is Layout? 1
   (b) Draw the Circuit diagram and Layout of CMOS inverter and explain. 2+2

3. (a) What is Stick Diagram? 1
   (b) Draw the Stick diagram of $F = (A + B + C)\cdot D$ and calculate the area using the λ-rule. 4

4. Explain the *Y*-chart of VLSI design flow. 5

5. What is an FPGA? How is it different from CPLD? What are its advantages? 2+2+1

6. (a) What is ASIC? Give its classification. 2
   (b) Why VLSI design flow is often called as cycle? Explain. 3

7. Write VHDL code in behavioral mode for a full Adder. 5

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

8. (a) Explain the *n*-well CMOS fabrication process with necessary diagram. 10
   (b) Draw the CMOS NAND gate and CMOS NOR gate using Layout technique. 5

9. (a) Explain with example and proper block diagram the Standard Cell based design. 8
   (b) Explain the Moore's Law for both processor and Memory design. 3
   (c) Explain λ-rule. 4

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10. (a) Draw the CMOS full Adder circuit. Hence draw the corresponding mask layout diagram. 3+3
    (b) Explain the static and dynamic power losses in VLSI design. 4
    (c) Why pull up networks are made of *p*-MOS transistor and Pull down networks are made of *n*-MOS transistor.

11. (a) Draw the circuit diagram of CMOS inverter and calculate the followings (Symbols are of usual meaning) 3+3+3
    (i) V_{IL}
    (ii) V_{DI}
    (iii) V_{th}
    (b) Explain the voltage transfer characteristic VTC of the Inverter. 4
    (c) What is uncertain or transition region of the VTC curve, explain. 2

12. (a) Draw the circuit diagram of CMOS NOR based SR Latch and NAND based SR latch. 2.5+2.5
    (b) Draw the circuit diagram of CMOS master slave JK flip flop and explain its timing diagram. 4+3
    (c) Draw the circuit diagram of CMOS clocked D-flip flop 3

13. Write short notes on any *three* of the following: 3×5
    (a) Dynamic logic
    (b) Photo-lithography
    (c) Ion-implantation
    (d) PLA
    (e) Latch up problem in CMOS

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