Open source Power Analysis Tool using TCL

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***Abstract*—Power is major parameter in designing of any circuit and so its analysis. This document shortly discusses power dissipation and need for open source power analysis tools in VLSI industry. It briefly explains power analysis of three mostly used and basic circuits of VLSI industry such as 4-bit adder, S27 benchmark and ALU.**

***Index Terms*—switching power, leakage power, power dissipation, open source tools**

I. Introduction

With increase in technology the demand for high-speed devices is increased. As we know the trade off fact between power and speed, there occurs necessity for low power devices in VLSI industry. For this low power designs, effective calculation or estimation of power is required. Hence, needs the design of an open source tool which analyses the power dissipation and consumption in any circuit.

II. Sources of Power Dissipation

In any circuit there occurs mainly two sources of power dissipation. One is static power dissipation which is also known as leakage power. Other is the dynamic power dissipation. It is sum of switching power, short circuit power.

A. Switching power

The charging and discharging of node capacitance and load capacitance due to signal variations between logic levels causes the power dissipation known as switching power. This makes major portion in the dynamic power dissipation. Fig. 1 shows the power consumption due to charging of load capacitance C_L when the input is changing from low logic to high logic [1]. The equation for switching power is given as

$$P_{\text{switching}} = C_L {V_{DD}}^2 f \tag{1}$$

where f is switching frequency.

B. Short circuit power

The main cause for this power is the path created between supply rail and ground rail i.e short circuit path. During the transition state of CMOS circuits, both PMOS and NMOS are in on state and hence causes a short circuit path between V_{DD} and GND.

C. Leakage power

The static power or leakage power dissipation occurs when there is no signal transitions, i.e., no change in input as well as output. Generally it is low and can be ignored. But with increase in technology or decrease in channel width, the leakage current becomes significant.

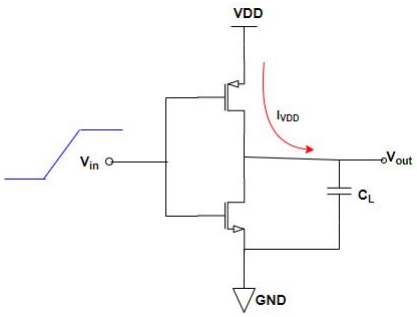

Fig. 1. CMOS inverter circuit during low to high transition

III. Power Analysis

To optimize the system specifications of high speed and low power, estimation of power is necessary. For analysis of any parameter we must have knowledge on calculation of it. The important parameters for estimation of power are switching activity and signal probability. With the help of stochastic processes these parameters are determined and modelled [2] [3].

A. Open source Power Analysis Tools

Open source tools are raging presently in VLSI industry. The boom of these tools also entered into power analysis. There is a need for these open source tools to estimate the power of circuits and optimize them, as commercial tools cannot be afforded by everyone. There are many open source power tools presently such as Pandapower [4].

IV. Application Circuits in VLSI

VlSI industry is an ocean of circuit implementations and their applications. Here is the brief power analysis about the three mostly used and very fundamental circuits.

A. 4-bit Fast adder

An adder is a combinational circuit that help in performing addition of two numbers as name suggests. Fast adder is the circuit which has computational efficiency higher than normal adder. The 4-bit adder as shown in fig. 2 is ISCAS 74X series benchmark circuit 74283 [5] which contains propagate/generate(P/G) circuit and CLA(carry look ahead) circuit which reduces propagation delay [6].

The delay in propagation of signals leads to static power consumption and switching activity of signals, presence of wire capacitance causes switching power.

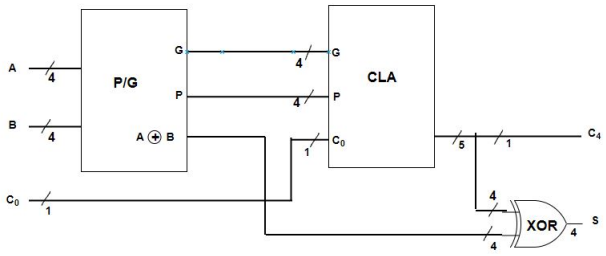

Fig. 2. 4-bit fast adder block diagram

B. S27 benchmark

Fig. 3 is a standard ISCAS'89 benchmark sequential circuit S27 [5] that has ability to scan 4 inputs using 3 scan flip flops(FF) and gives output based on it. The circuit is mainly used for testing patterns and fault coverage [7].

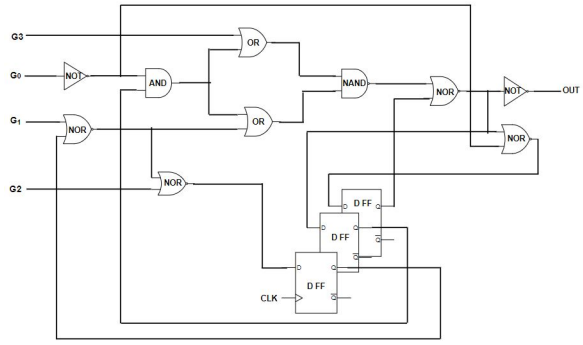

Fig. 3. S27 logic diagram

The power dissipation in this circuit is mainly due to clock given to FF and hence dynamic power dissipation is very much significant in this circuit.

C. 4-bit ALU

Arithmetic and Logic unit(ALU) is heart of every processor and performs all arithmetic and logical operations. 74181 is a 4-bit ALU which is 7400 series circuit that implemented in TTL (Transistor-Transistor Logic) technology [8].

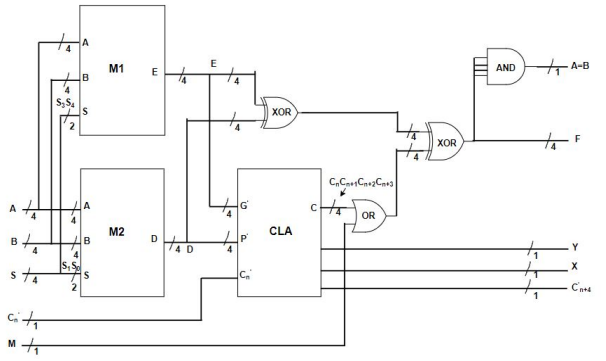

Fig. 4. 4-bit ALU block diagram

The block diagram of 74181 is shown in fig. 4 [5] and has mainly 3 blocks M1, M2 as shown in fig. 5 and CLA. If signal M=1 then only functional select(S) signal in ALU block can produce one among 16 possible logic expressions.

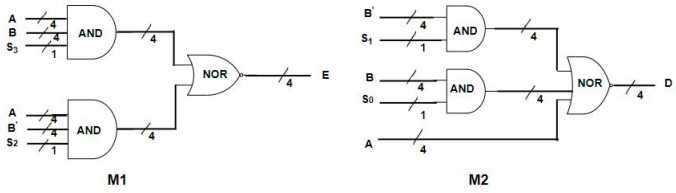

Fig. 5. M1 and M2 logic diagrams

ALU has power dissipation as waiting for some loop instructions may take much time to execute and the blocks that are not operating for some operations or instructions can lead to static power.

V. POWER ANALYSIS USING TCL

Using Tool Command Language(TCL) and NI Multisim 14.1 the power analysis is done. The idea of power calculation is given in steps as follows:

[1] Draw the schematic and run in "NI Multisim" software.
[2] Generate the SPICE netlist file.
[3] Read the SPICE file and extract the components required for power estimation.
[4] Calculate the switching power and leakage power using TCL code.
[5] Run the TCL code for results.

A. CMOS inverter

Here is the circuit diagram of CMOS Inverter drawn in multisim.

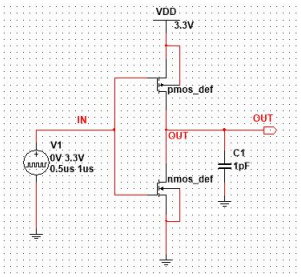

Fig. 6. CMOS inverter simulation circuit

B. 4-bit Fast Adder

The implementation of 4-bit fast adder is done. The gate level schematic and test circuit are given in fig. 7 and fig. 8 respectively.

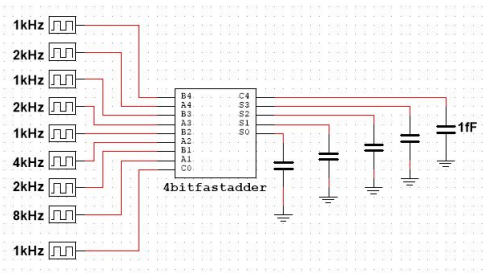

Fig. 7. 4-bit fast adder test circuit

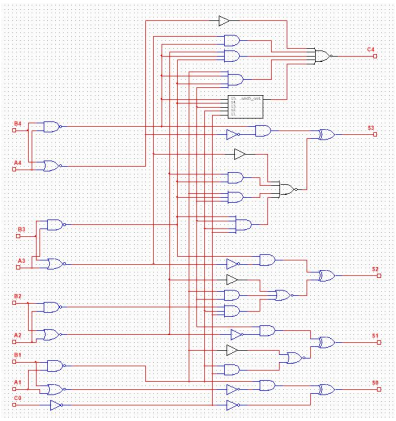

Fig. 8. Gate level schematic of 4-bit fast adder

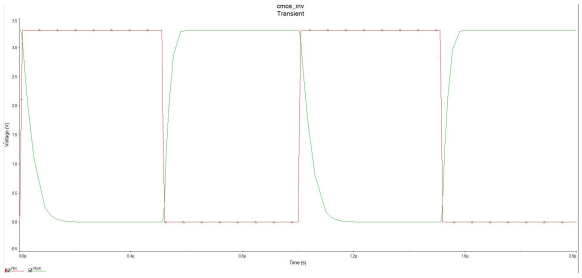

Fig. 9. CMOS inverter transient output

```
xC1 OUT 0 virtual_capC1
.subckt virtual_capC1 1 2
r1 1 2 1e30
c1 1 2 1e-012  IC=0
.ends

*## Multisim Component Q2 ##*
mQ2 OUT IN VDD VDD PMOS__TRANSISTORS_VIRTUAL__1__1  L=1.8e-007  W=2e-007

*## Multisim Component Q1 ##*
mQ1 OUT IN 0 0 NMOS__TRANSISTORS_VIRTUAL__1__1  L=1.8e-007  W=1e-007

*## Multisim Component V1 ##*
vV1 IN 0 ac 0 0
+   distof1 0 0
+   distof2 0 0
+   pulse(0 3.3 0 1e-008 1e-008 5e-007 1e-006)

*## Multisim Component VDD ##*
VDDVDD  VDD 0 dc 3.3


.model PMOS__TRANSISTORS_VIRTUAL__1__1 pmos
+ (
+  Level=3 VTO=0 KP=2e-005 GAMMA=0 PHI=0.6 CBD=0 CBS=0 IS=1e-014
+  PB=0.8 CGSO=0 CGDO=0 CGBO=0 CJ=0 MJ=0.5 CJSW=0 MJSW=0.33 JS=0
+  TOX=4e-009 LD=0 U0=600 FC=0.5 XJ=0 XD=0 KAPPA=0.2 L=1.8e-007
+  W=2e-007
+ )


.model NMOS__TRANSISTORS_VIRTUAL__1__1  nmos
+ (
+  Level=3 VTO=0 KP=2e-005 GAMMA=0 PHI=0.6 CBD=0 CBS=0 IS=1e-014
+  PB=0.8 CGSO=0 CGDO=0 CGBO=0 CJ=0 MJ=0.5 CJSW=0 MJSW=0.33 JS=0
+  TOX=4e-009 LD=0 U0=600 FC=0.5 XJ=0 XD=0 KAPPA=0.2 L=1.8e-007
+  W=1e-007
+ )
```

Fig. 10. CMOS inverter Netlist

Fig. 11. 4-bit fast adder simulation output

VI. Results and Discussion

Cmos inverter simulation and SPICE netlist generated by Multisim are shown in fig. 9 and fig. 10.

Fig. 11 show the simulation output of 4-bit fast adder circuit.

The average switching power and leakage power calculated for cmos inverter circuit by TCL code are 13.612 uW and 0.148 uW respectively. The command promt result after running Tcl code is given in fig.12. Rough estimation of switching power for 4-bit adder circuit gives 27.04 nW(C_L is 1fF).

```
Expected switching power in watt of cmos_inv is 1.3612499999999997e-5
Expected Leakage power in watt of cmos_inv is 1.4828904286808079e-7

C:\Users\VAHINI\Documents\National Instruments\Circuit Design Suite 14.1>tclsh powercaladder.tcl
Expected switching power in watt of 4-bit adder is 2.703857421875e-8
```

Fig. 12. CMOS inverter and 4-bit adder Power result

VII. Conclusion

Simulations and Netlist for cmos inverter and 4-bit fast adder are generated using Multisim. Switching power and leakage power are calculated for inverter using TCL code. For 4-bit adder switching power is roughly calculated.

VIII. Future Work

The actual idea is to read variables from netlist and calculate the power using TCL code but these results came for manual input. So automating the code and improvising it for calculating power for all types of circuits.

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