FPGA BASED ADAPTIVE FILTER FOR DYNAMIC AUDIO NOISE REMOVAL

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1 PROBLEM:

In human cochlea, the quality factor of audio filters centered at various frequencies changes based on the intensity of audio in that frequency band Kates (1993). This allows us to focus on the speaker in a noisy environment and it is the same mechanism by which we focus our eyes on the subject in front of us.

We wish to explore this adaptive filtering mechanism of changing quality factors based on a hardware implementation in FPGAs. This project is intended to be a small part of bigger hardware audio processing project that would be a low power consuming silicon cochlea.

2 DATA:

We will be using Microsoft Scalable Noisy Speech Dataset (MS-SNSD). This dataset contains clean spoken audio and various environmental noise files in .wav format. The dataset also contains a recipe file to create a noisy audio dataset at desired SNR ratio. We will be generating the noisy audio dataset from the files provided. In addition we will try to synthesize noisy audio from noise that is non-gaussian distributed to test how the filter performs.

3 Proposed solution: Rosado-Muñoz et al. (2009)

As mentioned in the paper cited, we intend to use a finite state machine machine based adaptive filter that adapts the filter weights based on the error function given by: $J(n) = \frac{\log(\cosh(\beta*e(n)))}{\beta}$. As mentioned in the paper, we are using this error to optimize the removal of impulsive noise, rather than gaussian noise since practical noisy audio doesn't have a gaussian distributed noise. We will follow the following steps in our project:

- Implement the FPGA based finite state machine filter and try to run it on a FPGA board to verify the functionality of the system.
- We will then move to modify the system to adapt based on frequency input.

Our goal will be to extract filtered audio from the board.

4 EXPERIMENTS WE WILL RUN:

We will run experiments that will span various HDL methodologies. We will try to optimize the system based on finite state machine, combinational logic and any other architecture that consumes least amount of power and infrastructure. If the system works well, we will try to process real time audio as well.

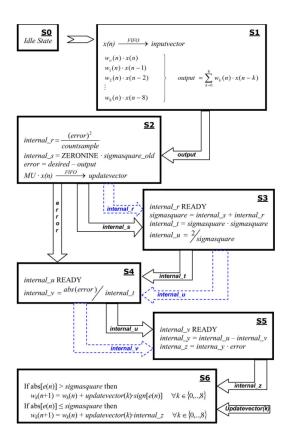


Figure 1: FSM based FPGA filter design

REFERENCES

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Alfredo Rosado-Muñoz, Manuel Bataller-Mompeán, Emilio Soria-Olivas, Claudio Scarante, and Juan F Guerrero-Martínez. Fpga implementation of an adaptive filter robust to impulsive noise: Two approaches. *IEEE Transactions on Industrial Electronics*, 58(3):860–870, 2009.