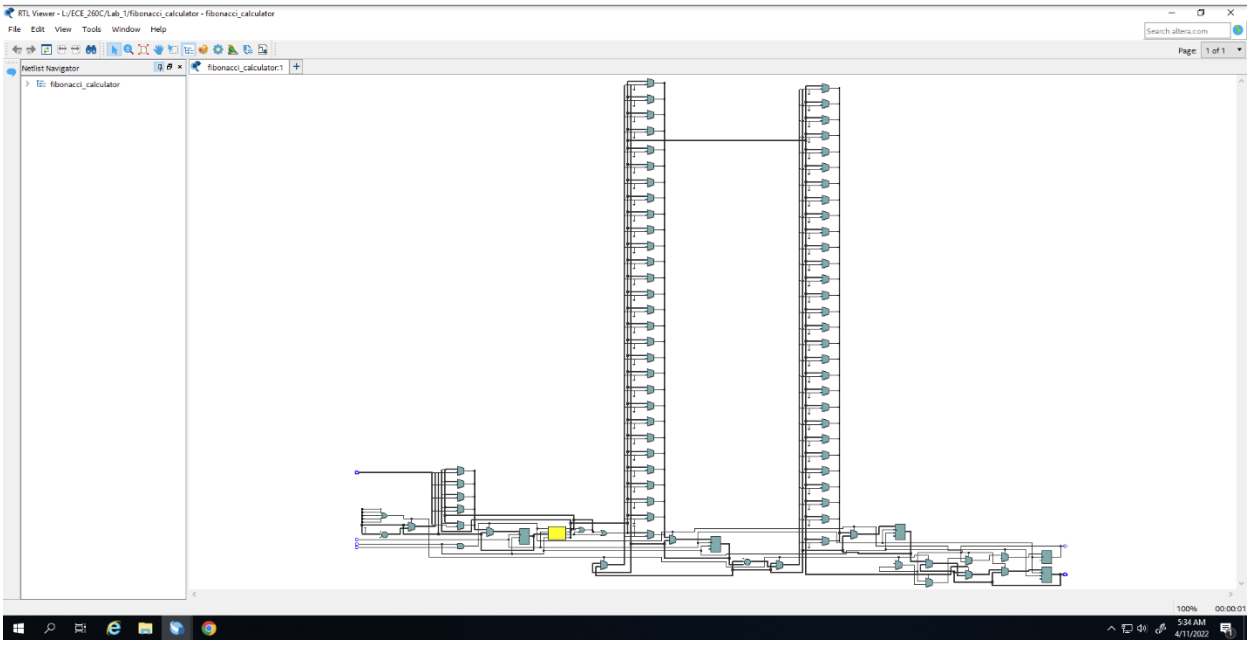
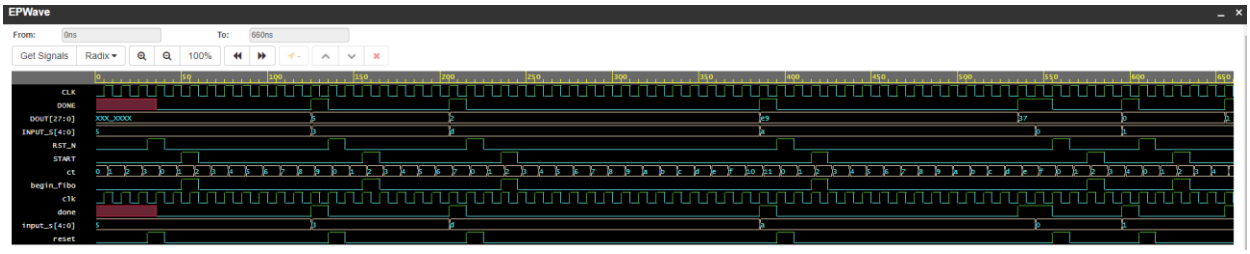
ECE 260C Assignment 1 submission Ankur Sharma (A59005284)

1. RTL View



2. Waveforms



3. Area

Fitter Summary	
Fitter Status	Successful - Mon Apr 18 05:14:23 2022
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	fibonacci_calculator
Top-level Entity Name	fibonacci_calculator
Family	Arria II GX
Device	EP2AGX45DF29I5
Timing Models	Final
Logic utilization	< 1 %
Combinational ALUTs	103 / 36,100 (< 1 %)
Memory ALUTs	0 / 18,050 (0 %)
Dedicated logic registers	97 / 36,100 (< 1 %)
Total registers	97
Total pins	38 / 404 (9 %)
Total virtual pins	0
Total block memory bits	0 / 2,939,904 (0 %)
DSP block 18-bit elements	0 / 232 (0 %)
Total GXB Receiver Channel PCS	0 / 8 (0 %)
Total GXB Receiver Channel PMA	0 / 8 (0 %)
Total GXB Transmitter Channel PCS	0 / 8 (0 %)
Total GXB Transmitter Channel PMA	0 / 8 (0 %)
Total PLLs	0 / 4 (0 %)
Total DLLs	0 / 2 (0 %)

4. Transcript

```
# Loading sv_std.std
# Loading work.fibo_testbench2(fast)
# Loading work.fibonacci_calculator(fast)
# ** Warning: (vsim-3015) [PCDPC] - Port size (29) does not match conn
#    Time: 0 ns  Iteration: 0  Instance: /fibo_testbench2/U_Fibonacci_
#
# vsim -voptargs=+acc=npr
# run -all
# fib_ct= 5, ct=          8, fib_out=        5, correct=        5
# fib_ct= 3, ct=          6, fib_out=        2, correct=        2
# fib_ct=13, ct=         16, fib_out=      233, correct=      233
# fib_ct=10, ct=         14, fib_out=       55, correct=       55
# fib_ct= 0, ct=          3, fib_out=        0, correct=        0
# fib_ct= 1, ct=          4, fib_out=        1, correct=        1
# ** Note: $stop    : testbench.sv(86)
#    Time: 665 ns  Iteration: 0  Instance: /fibo_testbench2
# Break at testbench.sv line 86
# exit
# End time: 01:40:40 on Apr 18,2022, Elapsed time: 0:00:01
# Errors: 0, Warnings: 1
Done
```

5. Timing

Slow 900mV 100C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name	Note
1	361.93 MHz	260.01 MHz	clk	limit due to minimum period restriction (max I/O toggle rate)

6. Resource Utilization

Analysis & Synthesis Resource Usage Summary	
Resource	Usage
Estimated ALUTs Used	103
-- Combinational ALUTs	103
-- Memory ALUTs	0
-- LUT_REGs	0
Dedicated logic registers	97
Estimated ALUTs Unavailable	1
-- Due to unpartnered combinational logic	1
-- Due to Memory ALUTs	0
Total combinational functions	103
Combinational ALUT usage by number of inputs	
-- 7 input functions	1
-- 6 input functions	4
-- 5 input functions	4
-- 4 input functions	61
-- <=3 input functions	33
Combinational ALUTs by mode	
-- normal mode	73
-- extended LUT mode	1
-- arithmetic mode	29
-- shared arithmetic mode	0
Estimated ALUT/register pairs used	117
Total registers	97
-- Dedicated logic registers	97
-- I/O registers	0
-- LUT_REGs	0
I/O pins	38
DSP block 18-bit elements	0
Maximum fan-out node	clk~input
Maximum fan-out	97
Total fan-out	739
Average fan-out	2.68