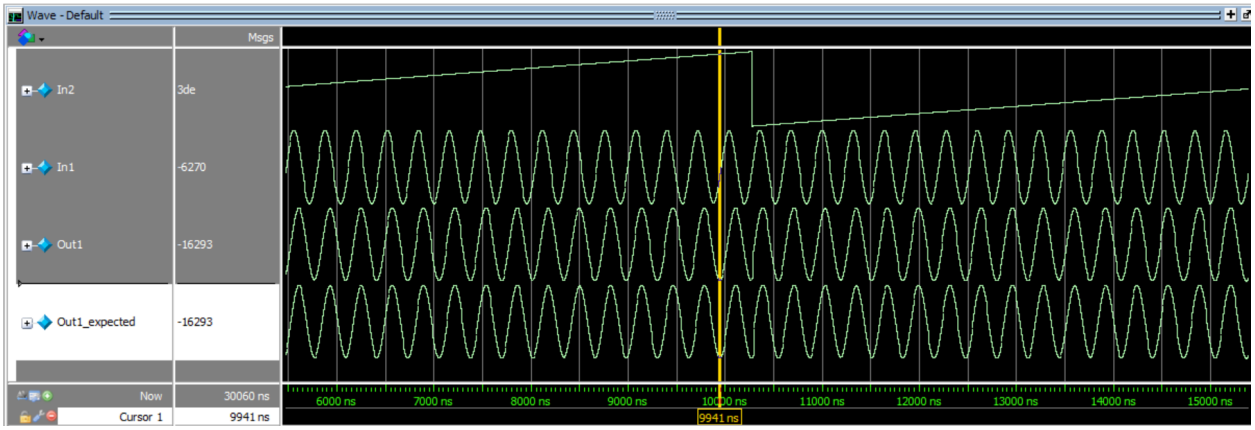
ECE 260C SP22 | LAB 3 Farrow Filter

Apurva A59005541, Ankur A59005284, Ishan A59012998, Chinmay A59011094

1) Baseline Design:

To gain an understanding of how well the system performs in terms of timing and resource utilization, we first synthesized the baseline architecture HDL output from Simulink, in Quartus and Vivado for Intel Arria and Xilinx Ultrascale FPGAs respectively, and simulated with the generated testbench in ModelSim.

a) ModelSim Simulation Output Waveforms:



b) Quartus Resource Usage and Timing Report:

Resource	Usage
Estimated ALUTs Used	723
-- Combinational ALUTs	723
-- Memory ALUTs	0
-- LUT_REGs	0
Dedicated logic registers	92
Estimated ALUTs Unavailable	0
-- Due to unpartnered combinational logic	0
-- Due to Memory ALUTs	0
Total combinational functions	723
Combinational ALUT usage by number of inputs	
-- 7 input functions	0
-- 6 input functions	1
-- 5 input functions	7
-- 4 input functions	80
-- <=3 input functions	635
Combinational ALUTs by mode	
-- normal mode	102
-- extended LUT mode	0
-- arithmetic mode	561
-- shared arithmetic mode	60
Estimated ALUT/register pairs used	749
Total registers	92
-- Dedicated logic registers	92
-- I/O registers	0
-- LUT_REGs	0
I/O pins	48
DSP block 18-bit elements	12
Maximum fan-out node	clk_enable~input
Maximum fan-out	93
Total fan-out	2667
Average fan-out	2.88

Slow 900mV 100C Model Fmax Summary			
Fmax	Restricted Fmax	Clock Name	Note
24.91 MHz	24.91 MHz	clk	

c) Vivado Timing Summary at 1GHz clock constraint. Achieved Fmax = 93.2 MHz.

Design Timing Summary

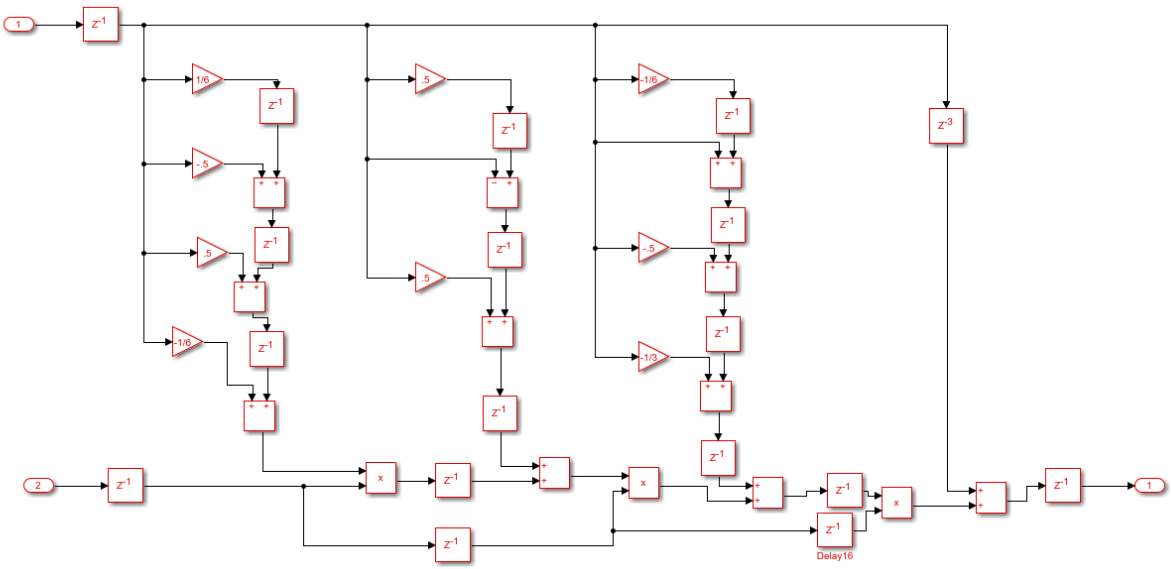
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-9.730 ns	Worst Hold Slack (WHS):	-0.072 ns	Worst Pulse Width Slack (WPWS):	-0.122 ns
Total Negative Slack (TNS):	-154.372 ns	Total Hold Slack (THS):	-2.859 ns	Total Pulse Width Negative Slack (TPWS):	-0.122 ns
Number of Failing Endpoints:	16	Number of Failing Endpoints:	48	Number of Failing Endpoints:	1
Total Number of Endpoints:	64	Total Number of Endpoints:	64	Total Number of Endpoints:	93

Timing constraints are not met.

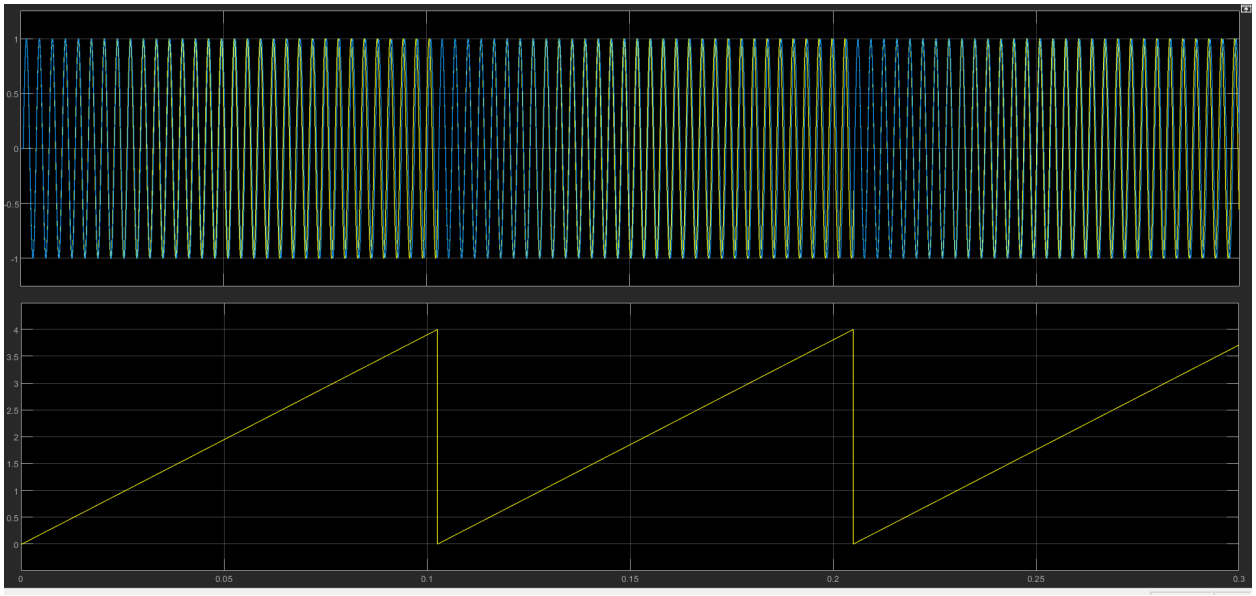
2) Pipelining+Transposed FIR Architecture to improve performance:

To improve the performance, we used transposed FIR architecture along with pipelining.

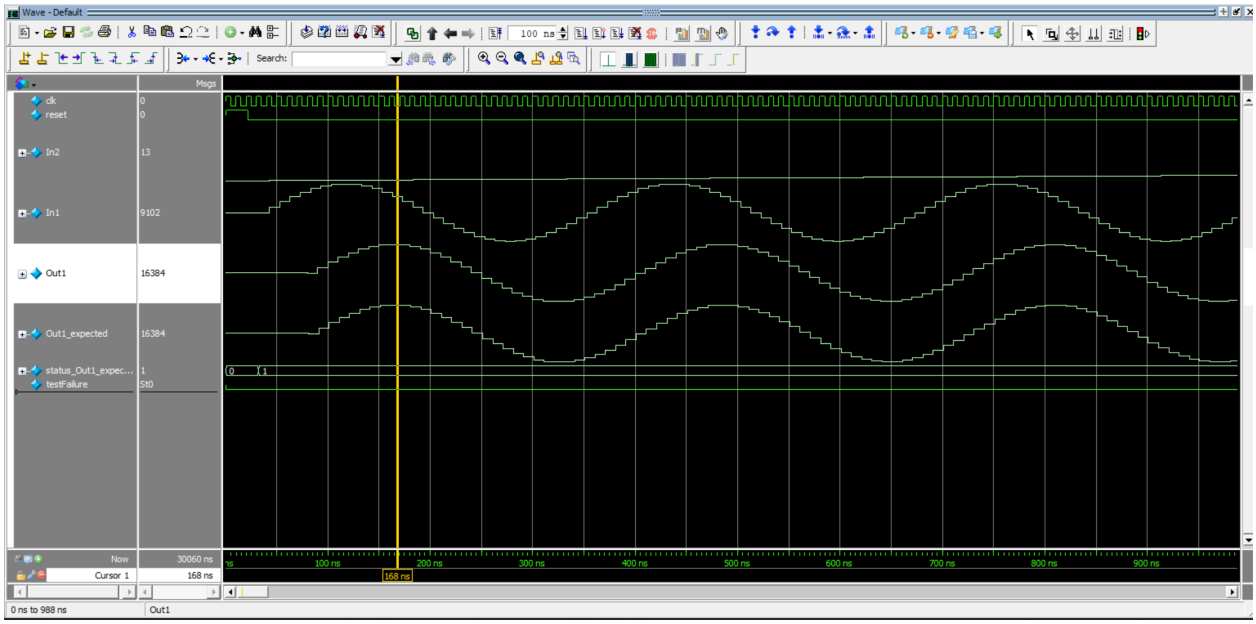
Pipelined+Transposed FIR Architecture (Simulink Model)



a) Simulink Waveforms:



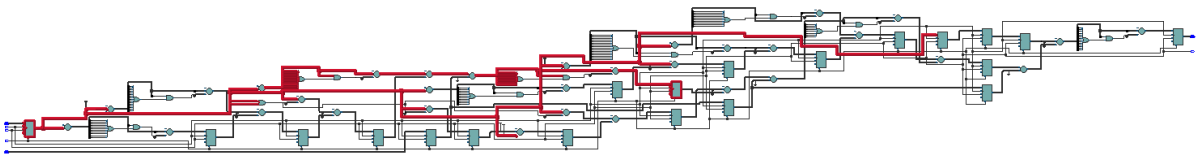
b) Pipelined Modelsim simulation output waveforms: (Verification for arithmetic accuracy)



c) Quartus: Timing Report, RTL view, Floorplan and techmap:

```
+-----------------------------------------------------+
; Slow 900mV 85C Model Fmax Summary                   ;
+------------+-----------------+------------+------+
; Fmax       ; Restricted Fmax ; Clock Name ; Note ;
+------------+-----------------+------------+------+
; 60.34 MHz ; 60.34 MHz       ; clk        ;      ;
+------------+-----------------+------------+------+
```

Longest delay path exist between the highlighted blocks.



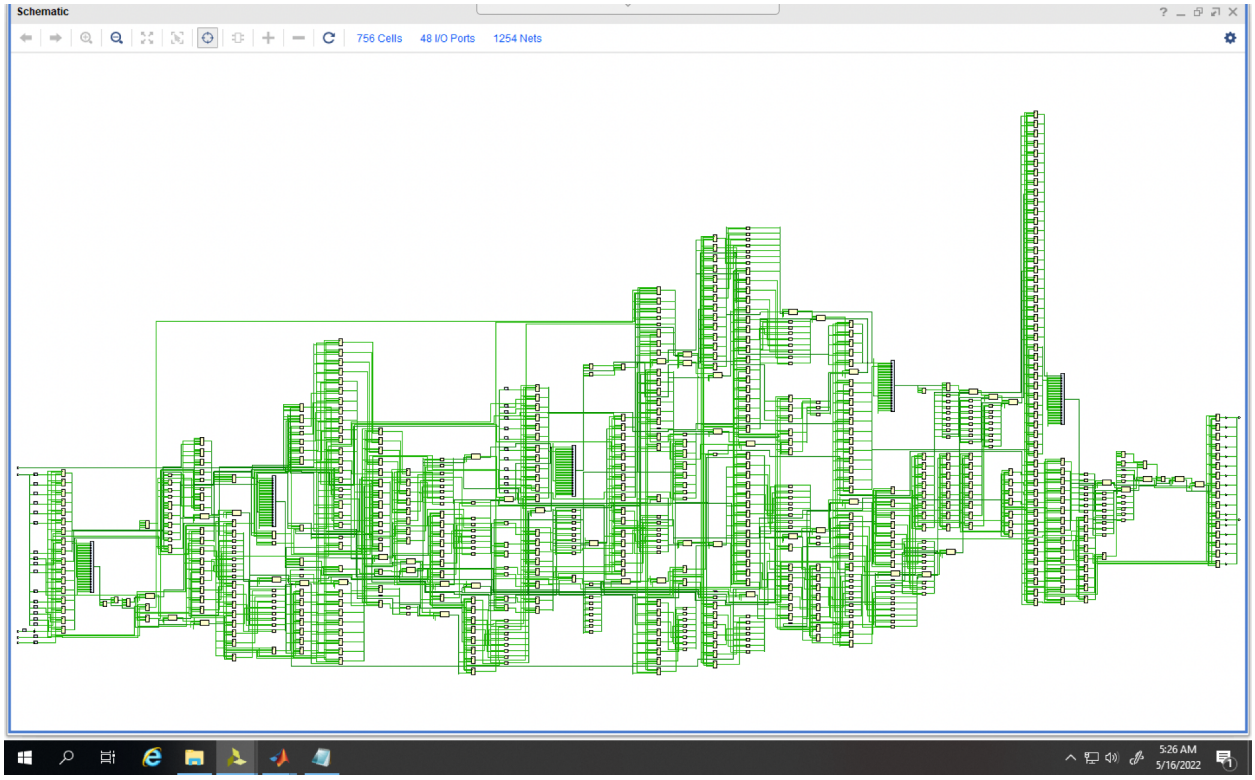
d) Vivado Timing Report, RTL schematic view and Resource Usage

Timing report at 1GHz. Achieved Fmax 191MHz.

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-4.225 ns	Worst Hold Slack (WHS):	0.039 ns	Worst Pulse Width Slack (WPWS):	-0.122 ns
Total Negative Slack (TNS):	-346.321 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	-0.122 ns
Number of Failing Endpoints:	213	Number of Failing Endpoints:	0	Number of Failing Endpoints:	1
Total Number of Endpoints:	348	Total Number of Endpoints:	348	Total Number of Endpoints:	385

Timing constraints are not met.

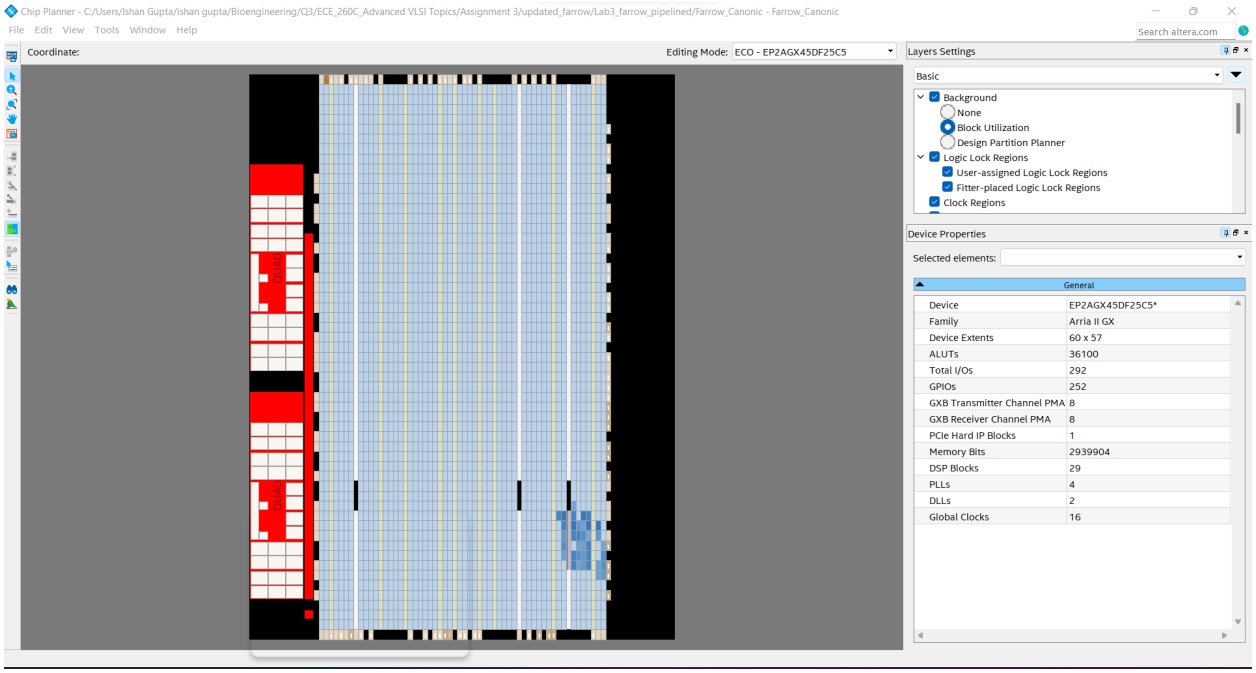


Resources used

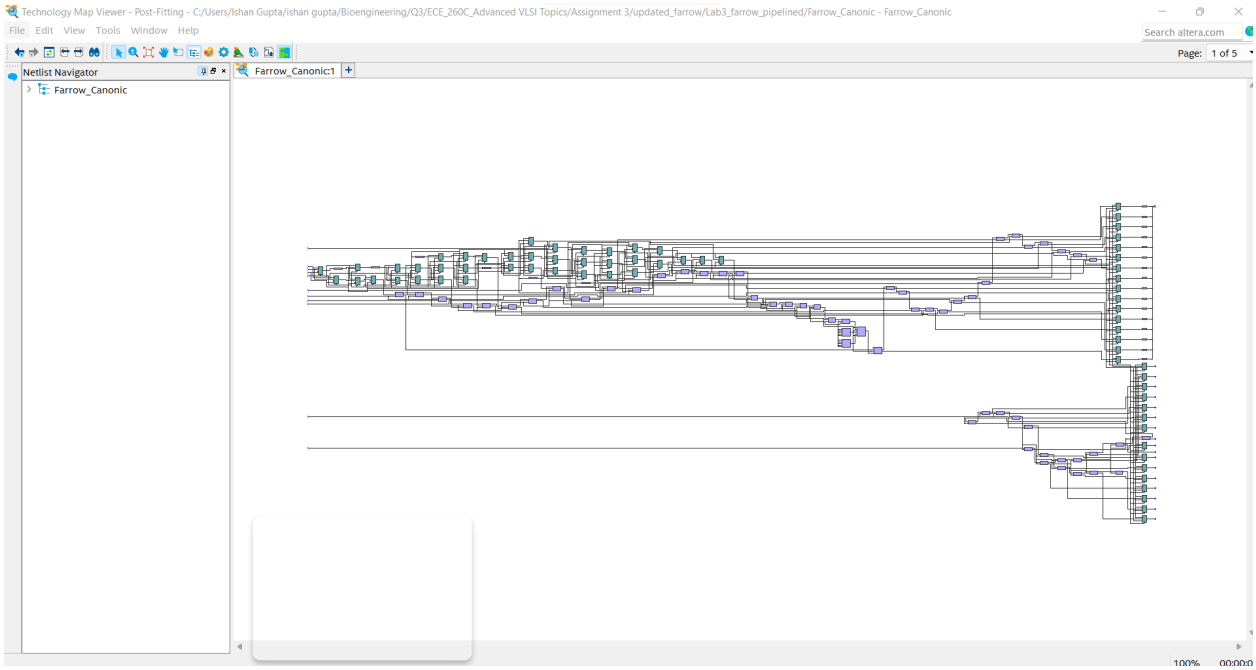
Hierarchy

Name	CLB LUTs (230400)	CLB Registers (460800)	CARRY8 (28800)	CLB (28800)	LUT as Logic (230400)	DSPs (1728)	Bonded IOB (464)	HPIOB_M (192)	HPIOB_S (192)	HDIOB_M (24)	HDIOB_S (24)	GLOBAL CLOCK BUFFERs (544)
N Farrow_Canonic	258	384	46	72	258	5	48	6	6	18	18	1

Floorplan



Technology map

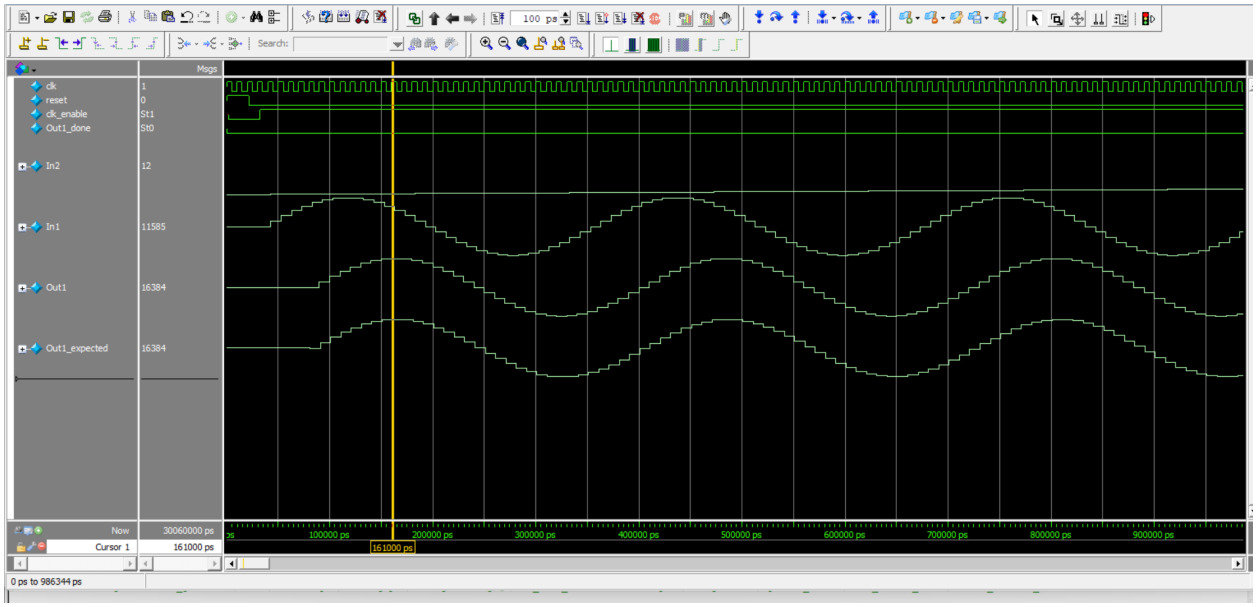


<u>Issues/Conclusions:</u>

After pipelining, the longest path consists of a multiplier and an adder. So for further performance improvement, we need to make changes in the multiplier itself. Hence we implemented a better version of multiplier that used less number of adders using the booth algorithm.

3) Pipelining + Transposed FIR Architecture + Booth Multiplier to improve performance:

a) Modelsim simulation output waveforms: (Verification for arithmetic accuracy)



b) Quartus Timing Report, RTL view, Floorplan, Techmap

```
+-----------------------------------------------------+
; Slow 900mV 100C Model Fmax Summary                  ;
+------------+-----------------+------------+------+
; Fmax       ; Restricted Fmax ; Clock Name ; Note ;
+------------+-----------------+------------+------+
; 166.03 MHz ; 166.03 MHz      ; clk        ;      ;
+------------+-----------------+------------+------+
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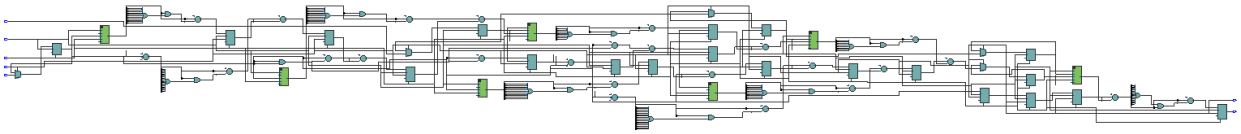
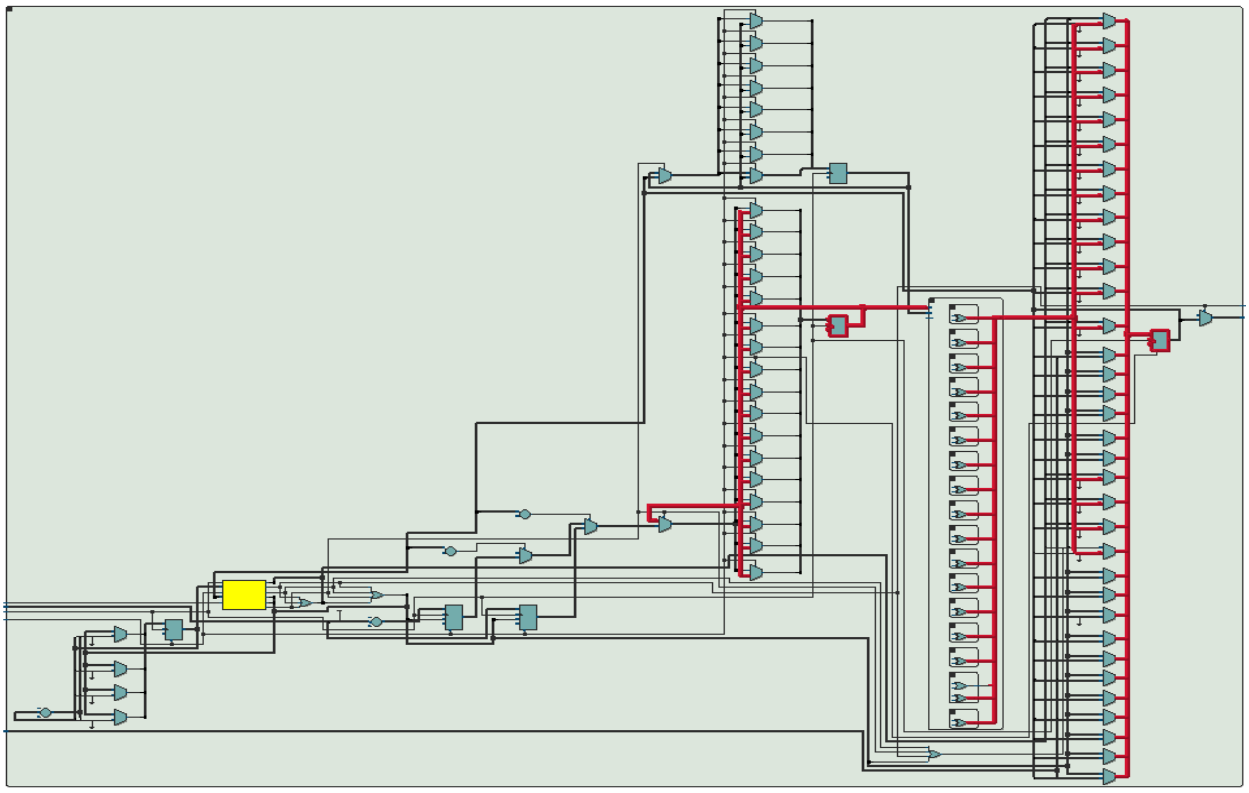
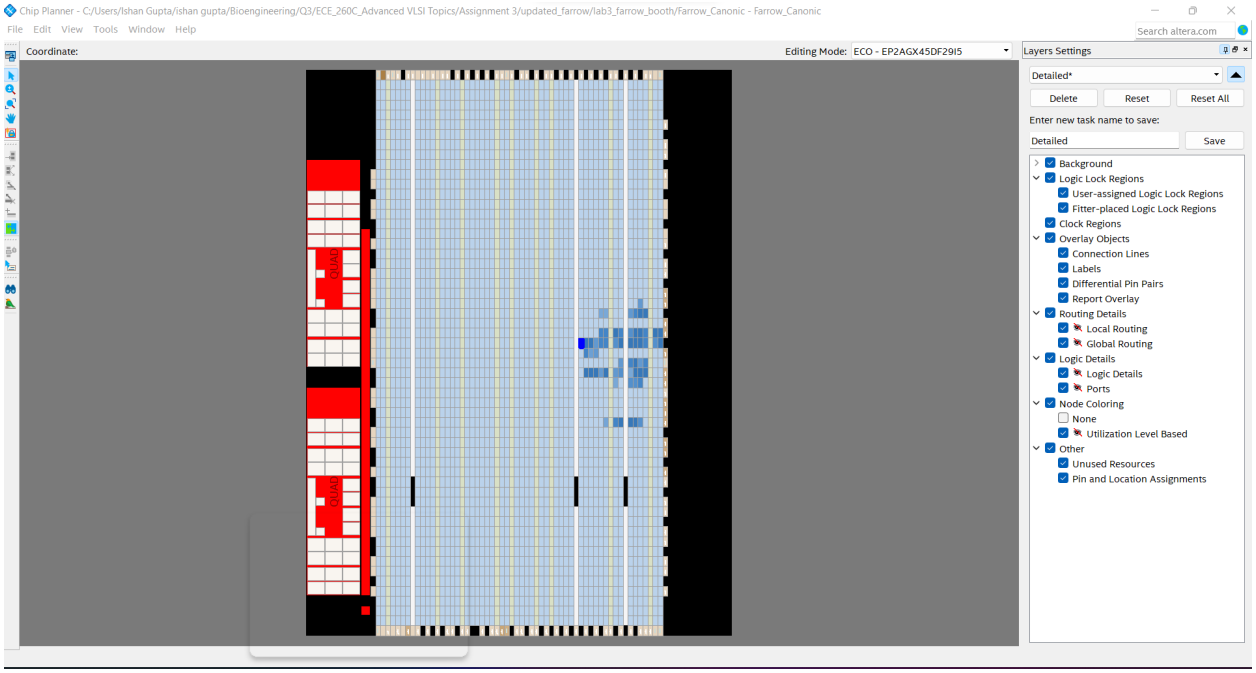


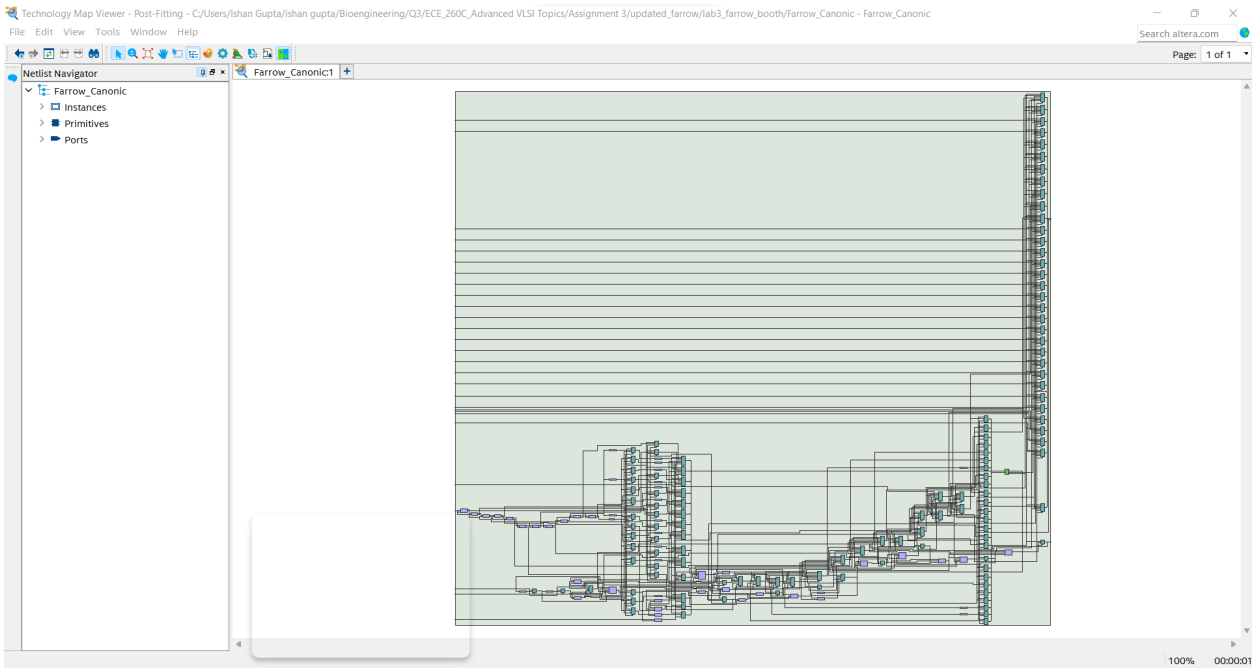
The green blocks are Booth multiplier blocks. Longest delay path exists within the multiplier. The highlighted blocks represent the longest delay path. An RTL view of the Booth Multiplier Block is pasted below



Floorplan



Techmap



c) Vivado Timing Report, RTL view and Resource Usage

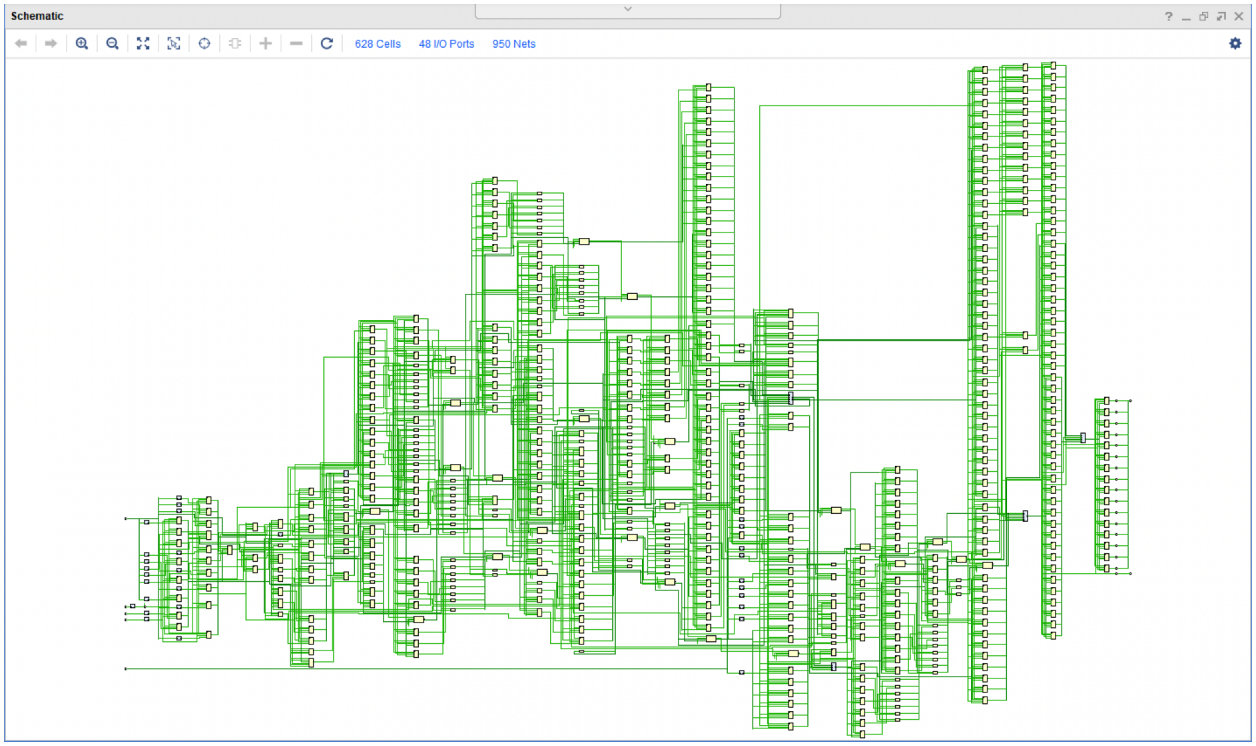
Timing report at 1GHZ. Achiever Fmax = 670 MHz.

Design Timing Summary

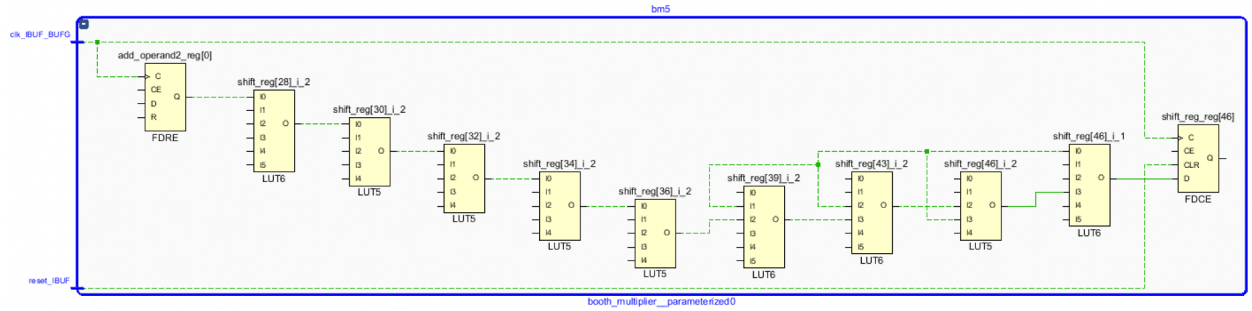
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-0.492 ns	Worst Hold Slack (WHS):	0.029 ns	Worst Pulse Width Slack (WPWS):	-0.122 ns
Total Negative Slack (TNS):	-63.176 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	-0.122 ns
Number of Failing Endpoints:	342	Number of Failing Endpoints:	0	Number of Failing Endpoints:	1
Total Number of Endpoints:	1320	Total Number of Endpoints:	1320	Total Number of Endpoints:	873

Timing constraints are not met.

RTL schematic view



Longest delay path in booth multiplier



Resource Usage

Hierarchy

Name	CLB LUTs (230400)	CLB Registers (460800)	CARRY8 (28800)	Bonded IOB (464)	GLOBAL CLOCK BUFFERs (544)
Farrow_Canonic	806	863	52	48	1
bm1 (booth_multiplier)	134	62	9	0	0
bm4 (booth_multiplier_0)	90	62	3	0	0
bm5 (booth_multiplier__parameterized0)	142	121	5	0	0
bm6 (booth_multiplier__parameterized0_1)	142	121	5	0	0
bm7 (booth_multiplier__parameterized0_2)	142	121	7	0	0

7. Summary:

- We began with the vanilla design given as part of the assignment. That design was a canonical representation of the Farrow filter and hence had a long path with several adders and multipliers. That path had a significant delay and as a result we could only reach as far as ~24MHz in Quartus and 93 MHz in Vivado.
- To further improve it, we changed from canonical to transpose representation of the filter. This change reduced the longest path to a couple of adders and multipliers which gave us ~27MHz in Quartus (Please note that this result hasn't been added in the detailed results above)
- We then added pipelines in the longest path to ensure that we had only a single multiplier adder pair in between two flops. This design ran at a frequency of ~60MHz (Quartus) and 191MHz (Vivado) . In this design, the main violator was the multiplier which was inferred by the tool and had a string of back to back adders. Since this was inferred by the tool, we couldn't modify the multiplier to improve its performance.
- Finally to get around this we modified the multipliers to Booth Multipliers.These multipliers were coded and instantiated in verilog. They consist of Carry Lookahead Adders. The key advantage of Booth Multiplier is that it reduces the number of partial products, which results in faster operation. This turned out to be an effective modification, as we were able to significantly increase our maximum frequency ending up with 166MHz in Quartus and 670MHz in Vivado.