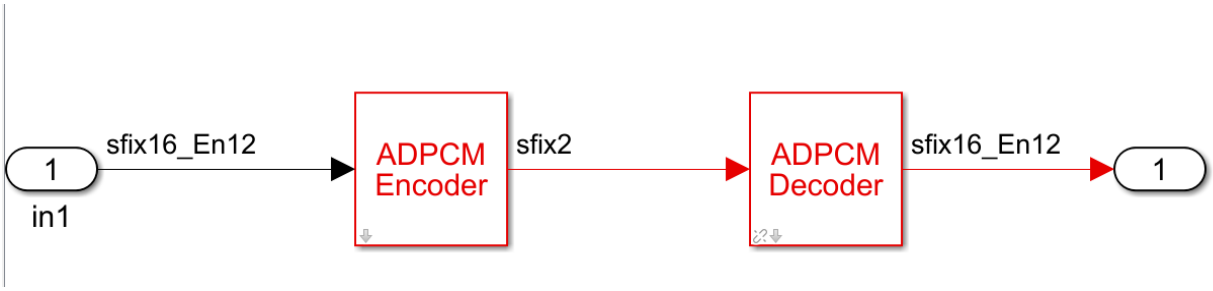
Adaptive Differential Pulse-Code Modulation

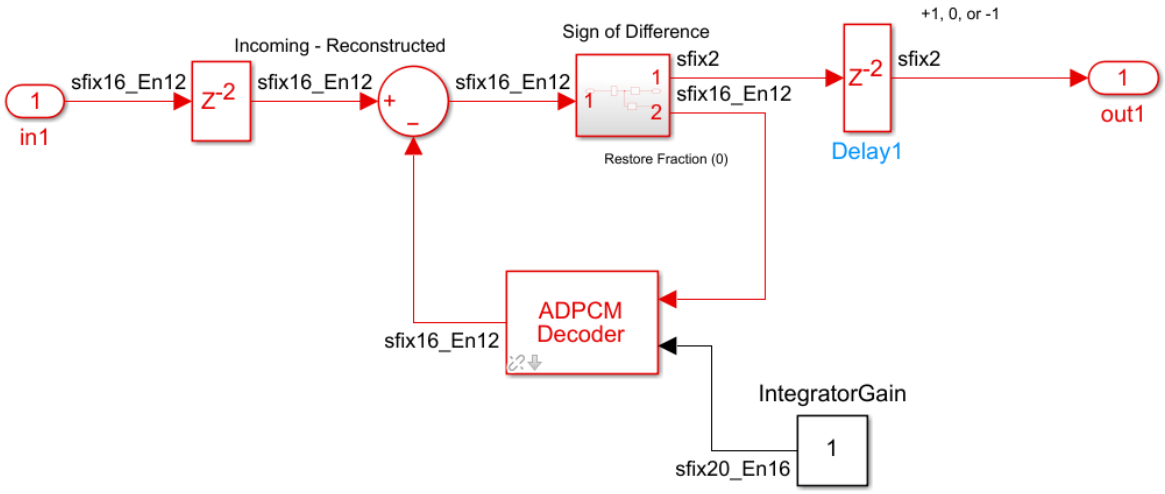
Abstract

We started with the default simulink models of ADPCM discussed in class. Below are the block diagrams showing its functioning.



1) **Top module**: This contains an encoder that encodes the incoming quantized message signal into signed binary pulses representing +1,0,-1 in decimal representation. Essentially, it converts the incoming signal into a differential pulse which only passes the difference between the amplitude of adjacent data samples across the communication channel. This helps in reducing the number of bits to be transferred across the channel.

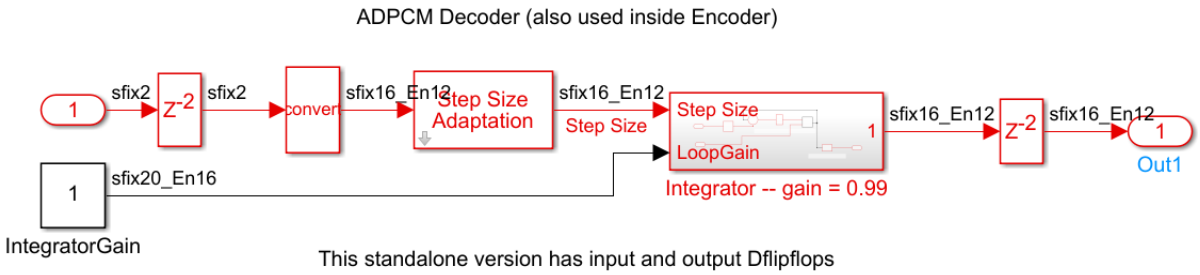
   The decoder receives the encoded signal and reconstructs the transmitted signal using step size adaptation to reduce the errors in the reconstructed signal.



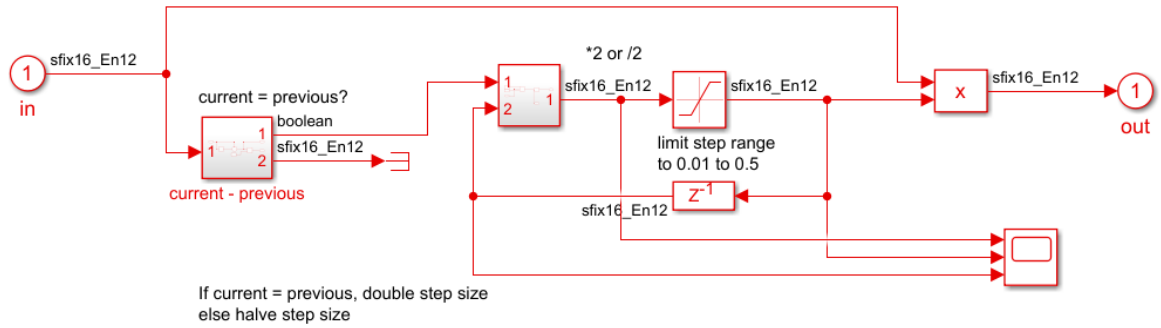
2) **Encoder:** The encoder block takes the difference between the incoming signal and the reconstructed signal and quantises the difference into +1,0 or -1 with the help of the sign

of difference block shown in the above diagram. The quantized data is further converted into signed binary bit data and transmitted across the channel.

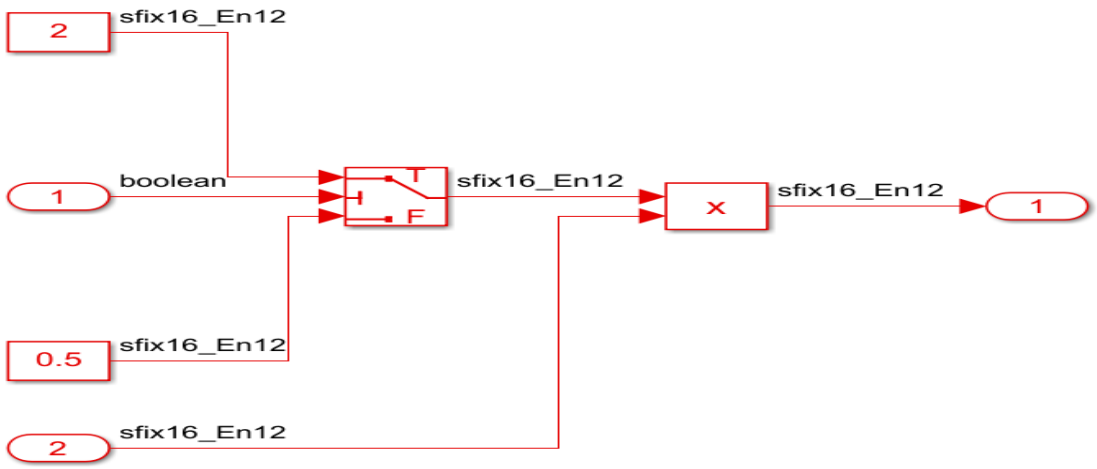
Note: The decoder in the feedback loop reconstructs the data and helps to improve the encoding through negative feedback.



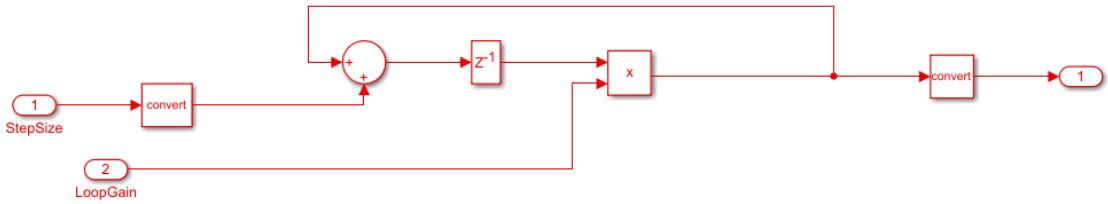
3) **ADPCM Decoder:** This decoder is sitting at the receiving terminal and takes DPCM data as input, does step size adaptation and keeps adding the steps on the previous value and thus reconstructs the message signal.



4) **Step Size Adapter:** The above block represents the internal structure of the Step size adaptation block. The input encoded data bifurcates into two parts. One part goes directly to the multiplier where it gets multiplied with the adapted value to form the adapted step size as the output.
The other part goes into the **current-previous block** which outputs logic 1 if both current and previous values are the same and logic 0 if both are different. Logically, both current and previous value being equal can happen only if the slope of the data is not changing its sign (i.e. monotonically increasing or decreasing or zero), which points towards increase in the step size.



5) ***2 or /2 block:** Here the input gets multiplied by 2 if it is logic 1 or by 0.5, if it is logic 0. This is the part, where the step size is enhanced if data keeps on either increasing or decreasing. Next, input 2 (i.e. the previous limited step) gets multiplied to the current factor of 2 or 0.5. This helps in exponential increment or decrement of step size. So, there is a step limit block next to it that limits the step size within 0.01 to 0.5. Now, after getting multiplied with the incoming bit stream, the step gets its sign (because incoming data can be +1, -1 or 0). Thus the output of the step size adaptation block is the adapted step size which is now fed to the integrator block.



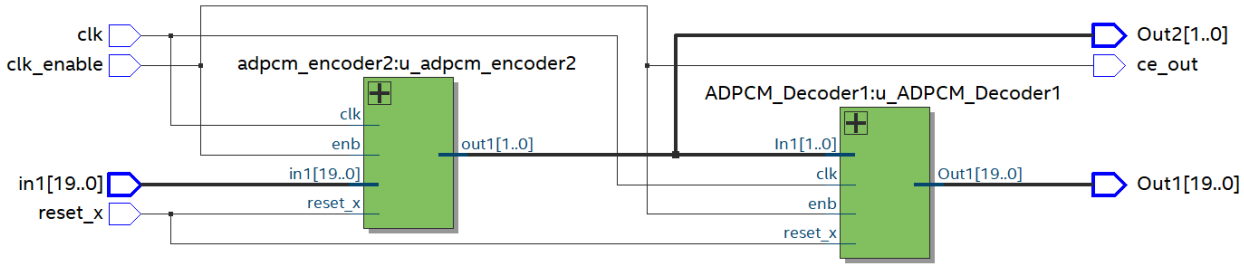
6) **Integrator:** The above block represents the inside of the integrator block. Here the adapted step value is added to the previous stored sample value thus reconstructing the message signal (encoded difference is added to the previous sample to generate a new sample). The loop gain is multiplied to the reconstructed value to make the whole control system stable.

We have done multiple implementations in FPGA (Xilinx Vivado and Quartus Altera) and Synopsys DC.
For our baseline ADPCM, we have an FPGA implementation using Quartus and an ASIC implementation using Synopsys DC and Cadence Innovus.
For our optimized ADPCM, we have FPGA implementations for Xilinx as well as Altera FPGAs using Vivado and Quartus.

Baseline Implementation using Raw provided code:

To get an idea of how the system is performing in terms of area usage as well as frequency, we first synthesized the system from the code generated by the functional but unoptimized ADPCM Simulink model. We got the following results:

Schematic:
The RTL schematic is as seen below.



We have also included in our submission the generated RTL schematic file with the expanded encoder and decoder blocks.

Area Summary:

; Analysis & Synthesis Resource Usage Summary	
; Resource	; Usage
; Estimated ALUTs Used	; 357
; -- Combinational ALUTs	; 357
; -- Memory ALUTs	; 0
; -- LUT_REGs	; 0
; Dedicated logic registers	; 128
;	;
; Estimated ALUTs Unavailable	; 5
; -- Due to unpartnered combinational logic	; 5
; -- Due to Memory ALUTs	; 0
;	;
; Total combinational functions	; 357
; Combinational ALUT usage by number of inputs	;
; -- 7 input functions	; 0
; -- 6 input functions	; 21
; -- 5 input functions	; 57
; -- 4 input functions	; 73
; -- <=3 input functions	; 206
;	;
; Combinational ALUTs by mode	;
; -- normal mode	; 146
; -- extended LUT mode	; 0
; -- arithmetic mode	; 190
; -- shared arithmetic mode	; 21
;	;
; Estimated ALUT/register pairs used	; 381
;	;
; Total registers	; 128
; -- Dedicated logic registers	; 128
; -- I/O registers	; 0
; -- LUT_REGs	; 0
;	;
;	;
; I/O pins	; 46
;	;
; DSP block 18-bit elements	; 20
;	;
; Maximum fan-out node	; clk_enable~input
; Maximum fan-out	; 129
; Total fan-out	; 1879
; Average fan-out	; 3.13

Clock Summary:

Fmax	Restricted Fmax	Clock Name
29.47 MHz	29.47 MHz	clk

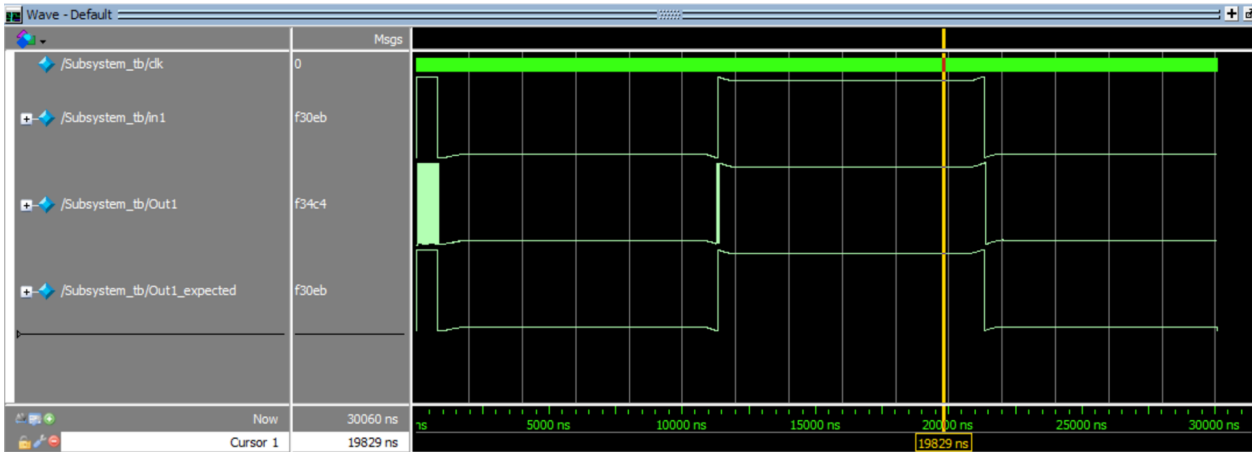
Setup Slack:

Clock	Slack	End Point TNS
clk	-32.928	-3353.914

Hold Slack:

Clock	Slack	End Point TNS
clk	0.546	0.000

Simulation:

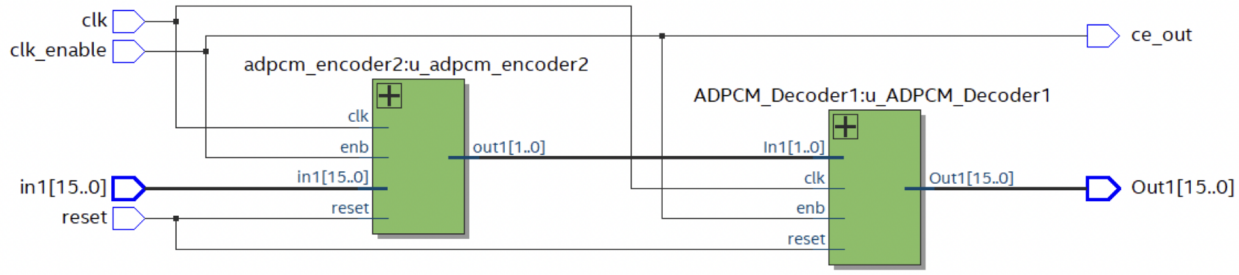


Thus, we got a maximum frequency of 29.47 MHz with a setup slack of -32 ns. From this, we started optimizing the system to increase frequency and reduce slack.

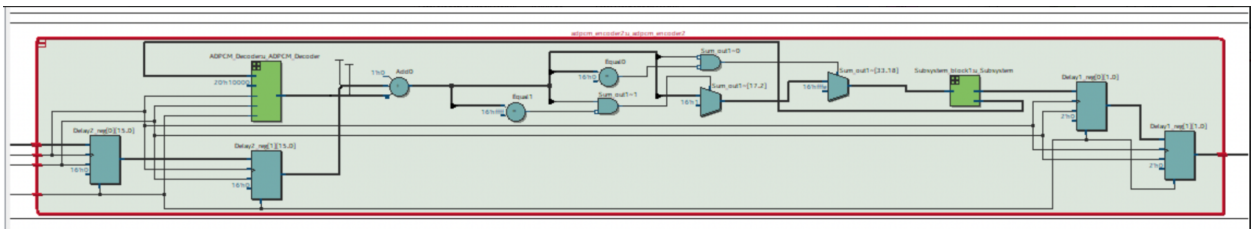
Optimized System:

Quartus:

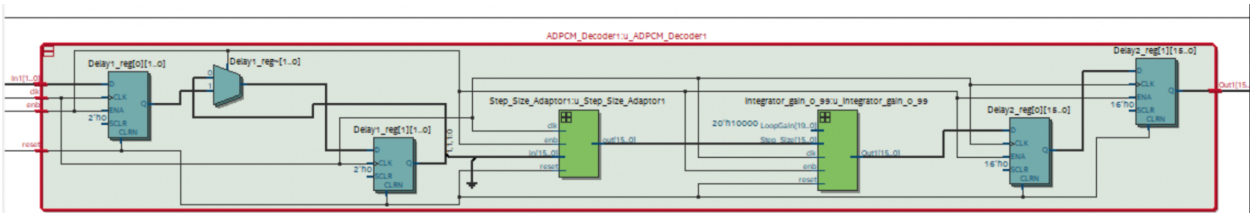
Post implementation circuit:



Encoder:



Decoder:



Area summary:

Analysis & Synthesis Summary	
Analysis & Synthesis Status	Successful - Mon May 02 01:22:03 2022
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	adpcm
Top-level Entity Name	adpcm
Family	Arria II GX
Logic utilization	N/A
Combinational ALUTs	263
Memory ALUTs	0
Dedicated logic registers	140
Total registers	140
Total pins	36
Total virtual pins	0
Total block memory bits	0
DSP block 18-bit elements	16
Total GXB Receiver Channel PCS	0
Total GXB Receiver Channel PMA	0
Total GXB Transmitter Channel PCS	0
Total GXB Transmitter Channel PMA	0
Total PLLs	0
Total DLLs	0

Clock summary:

	Fmax	Restricted Fmax	Clock Name	Note
1	40.83 MHz	40.83 MHz	clk	

Setup slack:

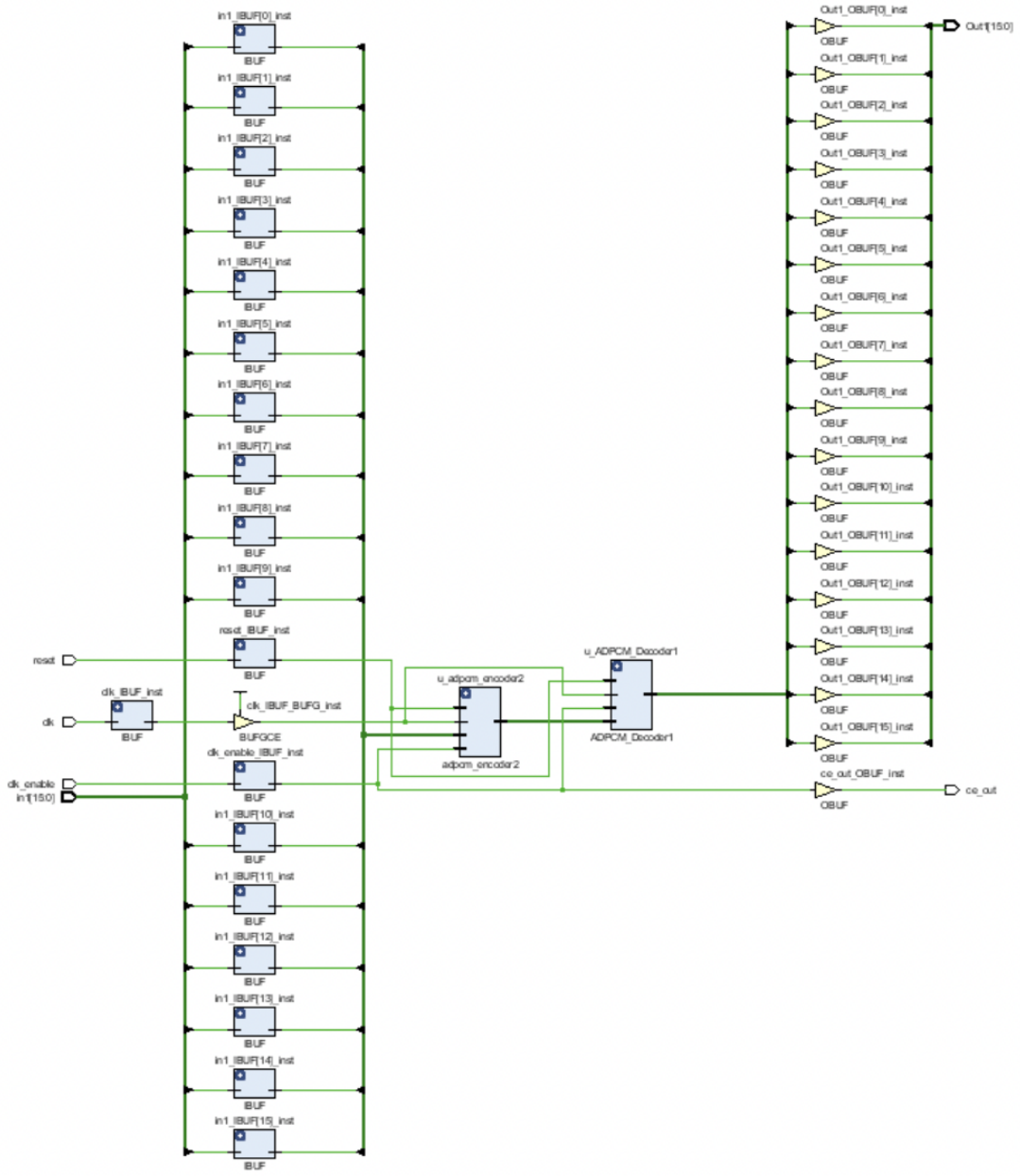
	Clock	Slack	End Point TNS
1	clk	-23.493	-1204.904

Hold Slack:

	Clock	Slack	End Point TNS
1	clk	0.217	0.000

Vivado:

Post synthesis block diagram:



Power usage summary:

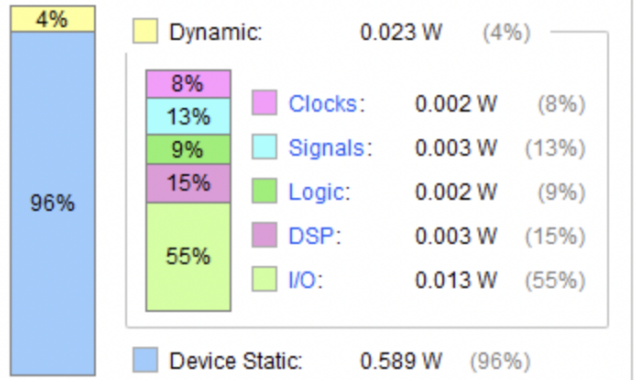
Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**0.612 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**25.5°C**
Thermal Margin:	74.5°C (85.0 W)
Effective ϑJA:	0.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

On-Chip Power



Clock summary:

We got a Fmax of ~110MHz on Zynq Ultrascale+ FPGA.:

Name	Waveform	Period (ns)	Frequency (MHz)
clk	{0.000 4.550}	9.100	109.890

Design Timing Summary

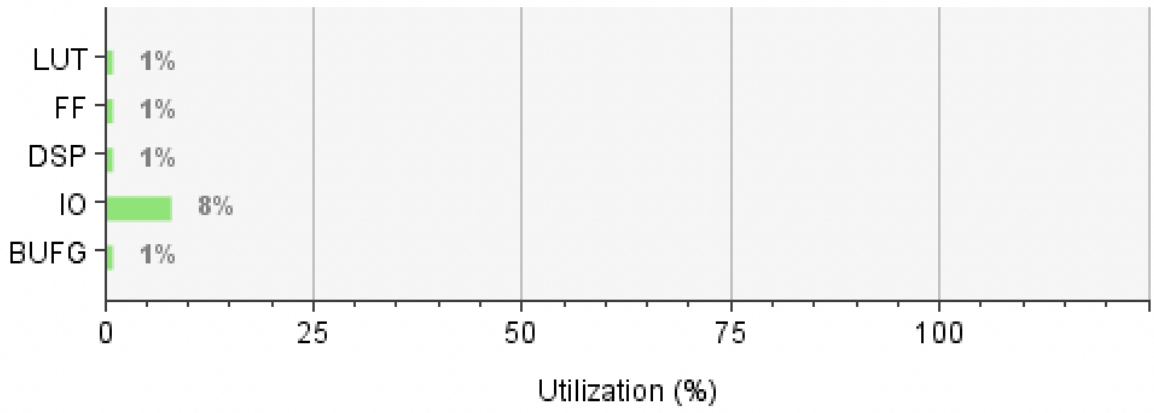
Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.070 ns	Worst Hold Slack (WHS):	0.015 ns	Worst Pulse Width Slack (WPWS):	4.275 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	127	Total Number of Endpoints:	127	Total Number of Endpoints:	144

All user specified timing constraints are met.

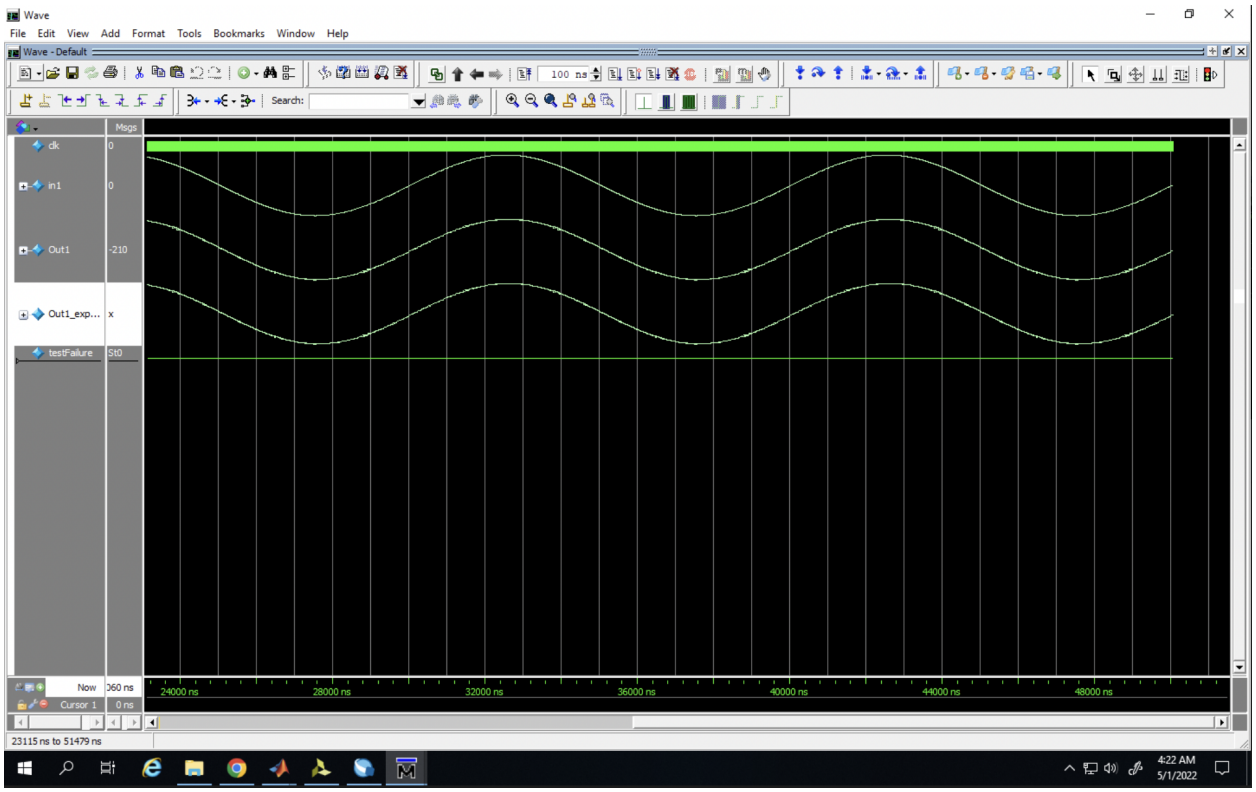
Resource utilization:

Name	CLB LUTs (230400)	CLB Registers (460800)	CARRY8 (28800)	CLB (28800)	LUT as Logic (230400)	DSPs (1728)	Bonded IOB (464)	HDIOB_M (24)	HDIOB_S (24)	GLOBAL CLOCK BUFFERs (544)
N adpcm	204	143	28	68	204	4	36	18	18	1
u_ADPCM_Decoder1 (ADPCM_Decoder1)	87	71	12	35	87	2	0	0	0	0
u_adpcm_encoder2 (adpcm_encoder2)	117	72	16	34	117	2	0	0	0	0

Resource	Utilization	Available	Utilization %
LUT	204	230400	0.09
FF	143	460800	0.03
DSP	4	1728	0.23
IO	36	464	7.76
BUFG	1	544	0.18



Circuit Simulation from TB:



Conclusions:

To ensure that the timing meets the specifications, we performed the following optimizations:

1. Added delays in the beginning and end of encoder and decoder modules
2. Reduced the precision from 20 fixed, 16 floating bits to 16 fixed and 12 floating bits.

This increased the fmax on Intel Arria II FPGA from 30MHz to ~45MHz. However, further reduction of precision led to high error. Which is why we decided to test our changes on Xilinx's FPGAs. On Zynq Ultrascale+ we were able to achieve ~110MHz fmax. Which fit the required constraints.

Upon investigation of why this happened, we can see a clear disparity in the mapping of the FPGA resources. While Xilinx FPGA used only 4 DSP blocks, 143 FFs and 204 LUTs, Intel FPGAs mapped the logic to 16 DSP blocks and 263 LUTs and 140 logic registers (similar to FFs). The higher number of resources mapped to by the Intel FPGAs can be a reason for the slower clock speed. Another reason can be that the inherent blocks are faster on the Xilinx FPGAs.

Baseline ADPCM Post PNR implementations (Synopsys DC and Innovus):

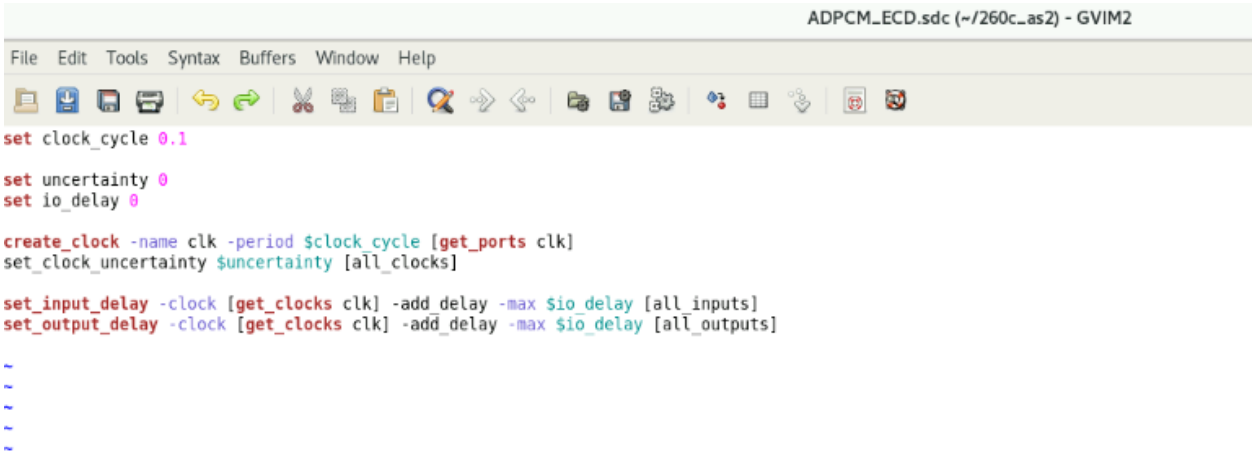
1) **Power Report:**

```
Total Power
-----------------------------------------------------------------------------------------
Total Internal Power:      114.31195684        49.3919%
Total Switching Power:     116.99839570        50.5527%
Total Leakage Power:         0.12831625         0.0554%
Total Power:               231.43866904
-----------------------------------------------------------------------------------------


Group                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
Sequential                         19.65       1.338    0.008712          21       9.074
Macro                                 0           0           0           0           0
IO                                    0           0    1.53e-06    1.53e-06   6.611e-07
Combinational                     90.54       111.7      0.1183       202.3       87.43
Clock (Combinational)             4.114       3.981    0.001336       8.096       3.498
Clock (Sequential)                    0           0           0           0           0
-----------------------------------------------------------------------------------------
Total                             114.3         117      0.1283       231.4         100
-----------------------------------------------------------------------------------------


Rail                  Voltage   Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
Default                     1      114.3         117      0.1283       231.4         100


Clock                           Internal   Switching     Leakage       Total  Percentage
                                Power      Power         Power         Power  (%)
-----------------------------------------------------------------------------------------
clk                               4.114       3.981    0.001336       8.096       3.498
-----------------------------------------------------------------------------------------
Total (excluding duplicates)      4.114       3.981    0.001336       8.096       3.498
-----------------------------------------------------------------------------------------


-----------------------------------------------------------------------------------------
*   Power Distribution Summary:
*       Highest Average Power:   CTS_ccl_BUF_clk_G0_L1_2 (CKBD16):       1.975
*       Highest Leakage Power:               FE_RC_229_0 (ND3D8):    0.0001468
*       Total Cap:  3.63e-11 F
*       Total instances in design:  5586
*       Total instances in design with no power:     0
*          Total instances in design with no activity:     0
*       Total Fillers and Decap:     0
-----------------------------------------------------------------------------------------
```

2) Timing Report:

```
#####################################################################
#  Generated by:      Cadence Innovus 15.23-s045_1
#  OS:                Linux x86_64(Host ID ieng6-ece-14.ucsd.edu)
#  Generated on:      Fri Apr 29 22:11:23 2022
#  Design:            Subsystem
#  Command:           report_timing > timing.rpt
#####################################################################
Path 1: VIOLATED Setup Check with Pin u_adpcm_encoder2_u_ADPCM_Decoder_u_
Integrator_gain_0_99_Delay_out1_reg_0_/CP
Endpoint:   u_adpcm_encoder2_u_ADPCM_Decoder_u_Integrator_gain_0_99_Delay_out1_
reg_0_/D (v) checked with  leading edge of 'clk'
Beginpoint: u_adpcm_encoder2_u_ADPCM_Decoder_u_Integrator_gain_0_99_Delay_out1_
reg_6_/Q (^) triggered by  leading edge of 'clk'
Path Groups: {clk}
Analysis View: WC_VIEW
Other End Arrival Time          0.052
- Setup                         0.046
+ Phase Shift                   0.100
+ CPPR Adjustment               0.000
= Required Time                 0.107
- Arrival Time                  1.641
= Slack Time                   -1.534
     Clock Rise Edge                     0.000
     + Clock Network Latency (Prop)      0.053
     = Beginpoint Arrival Time           0.053
     +-----------------------------------------------------------------------------------------------------------+
     |                    Instance                    |     Arc      |   Cell   | Delay | Arrival | Required |
     |                                                |              |          |       |  Time   |   Time   |
     |------------------------------------------------+--------------+----------+-------+---------+----------|
     | u_adpcm_encoder2_u_ADPCM_Decoder_u_Integrator_gain | CP ^         |          |       |   0.052 |   -1.482 |
     | _0_99_Delay_out1_reg_6_                        |              |          |       |         |          |
     | u_adpcm_encoder2_u_ADPCM_Decoder_u_Integrator_gain | CP ^ -> Q ^  | EDFCNQD4 | 0.132 |   0.184 |   -1.350 |
     | _0_99_Delay_out1_reg_6_                        |              |          |       |         |          |
     | FE_OCPC265_u_adpcm_encoder2_u_ADPCM_Decoder_u_Inte | I ^ -> ZN v  | INVD2    | 0.017 |   0.201 |   -1.333 |
     | grator_gain_0_99_Delay_out1_6_                 |              |          |       |         |          |
     | U4084                                          | B v -> S ^   | FA1D4    | 0.089 |   0.290 |   -1.244 |
     | U1368                                          | A1 ^ -> ZN v | ND2D2    | 0.016 |   0.306 |   -1.228 |
     | U1367                                          | A1 v -> ZN ^ | ND2D2    | 0.015 |   0.321 |   -1.213 |
     | U3366                                          | B ^ -> S v   | FA1D4    | 0.093 |   0.414 |   -1.120 |
     | U532                                           | I v -> ZN ^  | CKND4    | 0.015 |   0.429 |   -1.105 |
     | U531                                           | A1 ^ -> ZN v | ND2D4    | 0.020 |   0.449 |   -1.085 |
     | U2902                                          | A1 v -> ZN ^ | ND2D4    | 0.019 |   0.469 |   -1.066 |
     | U2900                                          | A1 ^ -> ZN v | NR3D3    | 0.016 |   0.485 |   -1.050 |
     | U2898                                          | A1 v -> ZN ^ | NR2D4    | 0.023 |   0.508 |   -1.026 |
     | U2609                                          | A2 ^ -> ZN v | ND2D4    | 0.025 |   0.533 |   -1.001 |
     | U2585                                          | A1 v -> ZN ^ | ND2D4    | 0.020 |   0.553 |   -0.981 |
     | U3050                                          | A1 ^ -> ZN v | ND3D8    | 0.023 |   0.576 |   -0.959 |
     | U3026                                          | A1 v -> ZN ^ | NR2XD8   | 0.022 |   0.598 |   -0.936 |
     | FE_RC_9_0_dup                                  | B1 ^ -> ZN v | INR2D4   | 0.017 |   0.615 |   -0.919 |
     | FE_OCPC398_FE_RN_23                            | I v -> Z v   | CKBD4    | 0.026 |   0.641 |   -0.893 |
     | FE_RC_261_0_dup                                | A1 v -> ZN ^ | OAI21D4  | 0.034 |   0.675 |   -0.859 |
     | U2891_dup                                      | A2 ^ -> ZN v | CKND2D4  | 0.023 |   0.698 |   -0.836 |
     | FE_RC_26_0                                     | A1 v -> ZN ^ | OAI21D4  | 0.025 |   0.723 |   -0.811 |
     | FE_RC_189_0_dup                                | I ^ -> Z ^   | BUFFD16  | 0.044 |   0.767 |   -0.767 |
```

3) .sdc file:



Here, the input clock was set with time-period = 0.1ns
This gave us a negative setup slack of -1.534ns. Thus if the clock period is set to 1.634 ns, our violation will be resolved, i.e. our system is able to run at 1/1.634 Hz ~ **600+MHz.**

4) Area Report:

```
============================
Floorplan/Placement Information
============================
Total area of Standard cells: 18546.840 um^2
Total area of Standard cells(Subtracting Physical Cells): 18546.840 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 19768.320 um^2
Total area of Chip: 19768.320 um^2
Effective Utilization: 9.3821e-01
Number of Cell Rows: 78
% Pure Gate Density #1 (Subtracting BLOCKAGES): 93.821%
% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 93.821%
% Pure Gate Density #3 (Subtracting MACROS): 93.821%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 93.821%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 93.821%
% Pure Gate Density #6 ((Unpreplaced Standard Inst + Unpreplaced Block Inst + Unpreplaced Black Blob Inst + Fixed Clock Inst Area) / (Free Site Area + Fixed Clock Inst Area) for insts are placed): 93.821%
% Core Density (Counting Std Cells and MACROs): 93.821%
% Core Density #2(Subtracting Physical Cells): 93.821%
% Chip Density (Counting Std Cells and MACROs and IOs): 93.821%
% Chip Density #2(Subtracting Physical Cells): 93.821%
# Macros within 5 sites of IO pad: No
Macro halo defined?: No

============================
Wire Length Distribution
============================
Total M1 wire length: 465.4600 um
Total M2 wire length: 19805.1100 um
Total M3 wire length: 22629.0000 um
Total M4 wire length: 6890.2000 um
Total M5 wire length: 403.4000 um
Total M6 wire length: 24.2000 um
Total M7 wire length: 263.4000 um
Total M8 wire length: 178.4000 um
Total wire length: 50659.1700 um
Average wire length/net: 8.7509 um
Area of Power Net Distribution:
    ------------------------------
    Area of Power Net Distribution
    ------------------------------
    Layer Name  Area of Power Net  Routable Area  Percentage
    M1  0.0000  19768.3200  0.0000%
    M2  0.0000  19768.3200  0.0000%
    M3  0.0000  19768.3200  0.0000%
    M4  0.0000  19768.3200  0.0000%
    M5  0.0000  19768.3200  0.0000%
    M6  0.0000  19768.3200  0.0000%
    M7  0.0000  19768.3200  0.0000%
    M8  0.0000  19768.3200  0.0000%  For more information click here
```

Note: Reports are also separately attached for reference.