A Low-Offset Dynamic Comparator with Area-Efficient and Low-Power Offset Cancellation

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***Abstract*—A low-offset two-stage dynamic comparator has been proposed for parallel multi-channel processing. Low offset is achieved from two aspects: 1st-stage offset cancellation and 2nd-stage offset suppression. A fully dynamic offset cancellation scheme based on current auto-zeroing is adopted to effectively cancel out the 1st-stage offset. It features small area overhead and low energy consumption. For the 2nd-stage offset suppression, a high gain is designed for the 1st-stage dynamic amplifier by optimizing the overdrive voltage of input transistors. To maintain low offset performance across a wide range of input common-mode voltages, the overdrive voltage of the input pair is required to stay low. Therefore, a tail current source is employed for the 1st stage to ensure constant common-mode discharging current. As a result, the overdrive voltage can be stably kept low under various operation conditions. The proposed comparator has been designed in a standard CMOS 0.18 μm process. It operates under a supply voltage of 1.2 V at 10 MHz. Simulation results have verified the low-offset property of the comparator. The input-referred offset (1 σ) is reduced from 19.25 mV to 1.296 mV after cancellation and it remains constant with the input common-mode voltage changing from 0 V to 0.8 V. The offset is further reduced to 771 μV when the 2nd-stage input pair are enlarged by 4 times. At the same time, the energy consumption is increased from 147 fJ/Conv to 168 fJ/Conv.**

I. Introduction

Comparators have been widely used for converting analog signals to digital signals. A high-quality comparator is essential to the performance of mixed-signal systems such as analog-to-digital converters (ADC) [1] [2] and image signal processors [3][4]. Compared to conventional comparators with static power, fully dynamic comparators [1][2][3] only consume dynamic power during evaluation. They have been proven to be suitable for low-supply, low-power and high-speed applications.

Offset is an important factor limiting the overall accuracy of a comparator. For single-comparator systems, offset can be easily calibrated and corrected in either the digital domain or the analog domain. On the other side, the problem of offset is more severe for parallel multi-channel processing such as time-interleaved ADCs [2] or column-parallel image processing [3][4]. The mismatch among different comparators will degrade the system's performance very much.

Simply enlarge transistors is not a good solution as it brings limited improvement. Employ a preamplifier to enable auto-zeroing [4] will remove a large portion of the offset. However it is neither energy-efficient nor suitable for low-supply processing because of the design requirements of the static amplifier. In recent years, various digital offset cancellation techniques have been implemented. The fundamental idea is to calibrate the offset of a comparator and then insert imbalances to compensate it. Such techniques include current compensation [5], load compensation [6], charge compensation [7] and threshold compensation [8]. These approaches can suppress the offset to a very low level. However, the major drawbacks of these techniques are the large area overhead and power-hungry calibration process, which impede their application to area-limited and power-limited parallel multi-channel systems.

On the other hand, dynamic offset cancellation has the advantages of both low power and small area [9][10][11]. In [9], a CMOS charge-transfer based preamplifier is employed to perform auto-zeroing in the reset phase and amplify input signal without static power consumption. The idea is further extended in [10], which enables two-sided amplification by using a differential architecture instead of a single-ended CMOS design. In contrast to this charge-transfer based output-offset-storage method, a dynamic input-offset-storage scheme is proposed in [11]. It demonstrates better offset cancellation performance, but there are some drawbacks of such comparator architecture. Firstly, the low dependency of offset on the input common-mode (CM) voltage is achieved by adjusting the reset CM voltage. Therefore prior knowledge of the input CM voltage is required. When these two CM voltages don't match, the offset will vary a lot. The same problem also exists in [9] and [10]. It hinders their use for applications with varying input CM voltage [2][3][4]. Secondly, the stacking structure typically has disadvantages in terms of speed, kickback noise and supply voltage, compared with a two-stage structure [12].

In this paper, a low-offset dynamic comparator is proposed to overcome the above issues. It is designed based on the two-stage comparator structure to maintain the advantages of high flexibility, low kickback noise, high speed and low supply voltage. The offset is minimized from two aspects. The 1st-stage offset is cancelled out by an input-offset-storage scheme developed from [11] with major drawbacks resolved. The 2nd-stage offset is suppressed by the high gain of the 1st-stage dynamic amplifier. Finally, the overall offset can be effectively reduced with low dependency on the input CM voltage.

The remainder of the paper is organized as follows. Section

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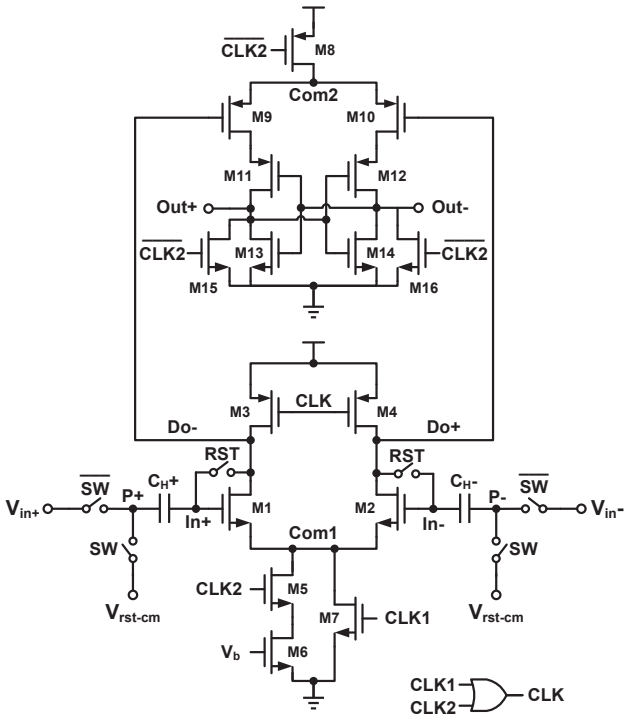

Fig. 1. Circuit structure of the proposed two-stage dynamic comparator.

II will describe the circuit structure and operation principle of the proposed comparator. After that, detailed offset analysis will be presented. Simulation results in Section III will verify the comparator performance with comparison to prior designs. Conclusion comes in Section IV.

II. Comparator Design

A. Circuit Structure

The circuit structure of the proposed comparator is illustrated in Fig.1. It is developed based on the two-stage comparator proposed in [1] which features high energy efficiency. The 1st stage is a dynamic amplifier composed of M1-M7. It amplifies the input signal difference between two nodes ($In+$, $In-$) by differentially discharging output nodes ($Do+$, $Do-$). The 2nd stage contains another dynamic amplifier (M8-M10) stacked on a latch (M11-M14). $Do+$ and $Do-$ are directly fed to the 2nd dynamic amplifier which drives the latch to generate full-swing digital outputs ($Out+, Out-$) by positive feedback. Compared to the conventional design, a few differences can be observed. Firstly, the input-storage offset cancellation scheme introduces a few reset devices, including reset switches controlled by RST/SW and sampling capacitors $C_H\pm$. Secondly, there are two paths from the common node $Com1$ to ground. They operate at different operation phases to optimize comparator performance which will be illustrated detailedly in the following sections. Thirdly, another tail (M8) is added in the 2nd stage and sources of M9 and M10 are connected as another common node ($Com2$). M8 acts both as an enabling switch and a current source to enhance the 2nd-stage gain.

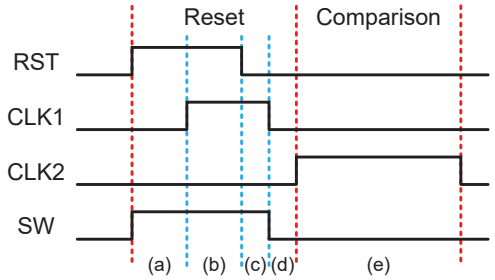

Fig. 2. Comparator control timing diagram.

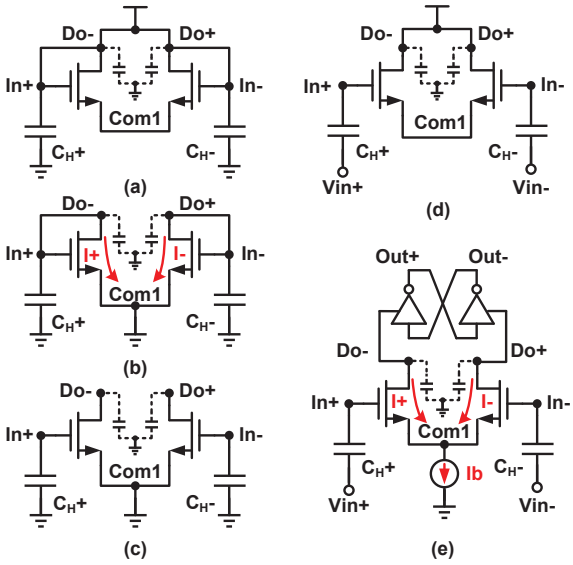

Fig. 3. Comparator operation flow: (a) Reset storage capacitors $C_H\pm$; (b) Discharge $C_H\pm$ through M1 and M2 respectively; (c) Store reset voltages including offset in $C_H\pm$; (d) Reset output nodes $Do+$ and $Do-$ to VDD and sample input signals V_{in+} and V_{in-}; (e) Compare $In+$ and $In-$ by discharging $Do+$ and $Do-$ through a common current source I_b and drive the 2nd stage to generate latch outputs $Out+$ and $Out-$.

B. Operation Principle

The operation of the comparator has been divided into two phases: Reset and Comparison. Offset cancellation is conducted in the reset phase followed by evaluation in the comparison phase. There are 4 control signals (RST, $CLK1$, $CLK2$ and SW) for proper comparator operation. Reset signal CLK is the OR result of $CLK1$ and $CLK2$. The control timing diagram is depicted in Fig.2. $CLK2$ controls the comparison while the other three work for offset cancellation.

Based on the control timing in Fig.2, a detailed operation flow of 5 steps is elaborated in Fig.3. (a) A complete operation starts by turning on the reset switches using RST. $In+$ is connected to $Do-$ and then reset to VDD, so do $In-$ and $Do+$. (b) $CLK1$ rises up after voltage reset is completed. It disables M3 and M4 and enables M7. $C_H\pm$ start to discharge through M1 and M2 respectively to ground. (c) After some time, M1 and M2 enter the subthreshold region and $I\pm$ are drastically reduced. RST falls down to sample reset voltages in C_H+ and C_H- respectively. Offset is contained between

the reset voltages and stored. (d) $Do+$ and $Do-$ are reset to VDD again for comparison. At the same time, SW goes down to input V_{in+} and V_{in-}. (e) Evaluation starts. $In+$ and $In-$ are compared by discharging $Do+$ and $Do-$ through a common current source I_b. Then $Do+$ and $Do-$ drive the 2nd stage to generate latch outputs $Out+$ and $Out-$.

C. Offset Analysis

In a two-stage comparator design, offset comes from both the 1st stage and the 2nd stage. The 2nd-stage offset is suppressed by the 1st-stage gain. In the case of high gain, the 1st-stage offset becomes dominant, most of which is contributed by input transistors (M1, M2). So the design strategy here is to cancel out the mismatch between M1 and M2, and maintain a high gain to suppress the 2nd-stage offset.

The offset caused by the mismatch between M1 and M2 is cancelled by dynamic input offset storage in the reset phase.

During the discharging process in the reset phase, the gate and the drain of M1 and M2 are connected. Consequently, larger channel current I_{ds} will reduce the gate drive voltage V_{gs} more, which will in turn reduce I_{ds}. Due to such negative feedback, $I_{ds}+$ and $I_{ds}-$ will get closer and closer. After M1 and M2 enter the subthreshold region, the current difference ΔI_{ds} can be smaller than 1 nA and thus $I_{ds}\pm$ are auto-zeroed. The process is verified by the operation waveforms of V_{gs} and I_{ds} in Fig.4.

When RST falls down after M1 and M2 enter the subthreshold region in Step (c), the relation between I_{ds} and V_{gs} for M1 and M2 is expressed as

$$I_{ds} = 2n \cdot \beta \cdot {U_T}^2 \cdot e^{\frac{V_{gs}-V_{th}}{nU_T}} \tag{1}$$

where $\beta = \mu_n C_{ox}\frac{W}{L}$ represents the current factor, $U_T = \frac{kT}{q}$ is the thermal voltage. Therefore, the voltage stored in C_H after reset is

$$V_g = V_{th} + nU_T \cdot ln(\frac{I_{ds}}{2n \cdot \beta \cdot {U_T}^2}) + V_{Com1} \tag{2}$$

where V_{Com1} is the common-node voltage at $Com1$. It can be seen that both the threshold voltage V_{th} and the current factor β have been included in the reset voltage. As a result, offset caused by V_{th} and β mismatch is stored and cancelled out for comparison. Essentially, offset is cancelled by auto-zeroing $I_{ds}\pm$ using input offset storage.

Before comparison, $V_{in}\pm$ are connected to $C_H\pm$ so that $In\pm$ become $V_g - V_{rst-cm} + V_{in}\pm$. Assume $V_{in}\pm = V_{in-cm}\pm \Delta V$, where V_{in-cm} is the input CM voltage. The CM discharging currents for comparison are

$$I_{ds}^{'}\pm = (I_{ds}\pm) \cdot e^{\frac{V_{in-cm}-V_{rst-cm}-V_{Com1}^{'}+V_{Com1}}{nU_T}} \tag{3}$$

The current difference $\Delta I_{ds}^{'}$ can be calculated as

$$\Delta I_{ds}^{'} = \Delta I_{ds} \cdot e^{\frac{V_{in-cm}-V_{rst-cm}-V_{Com1}^{'}+V_{Com1}}{nU_T}} \tag{4}$$

In order to minimize offset residue, ΔI_{ds} and $V_{in-cm} - V_{rst-cm} - V_{Com1}^{'} + V_{Com1}$ have to be kept small. As stated above, ΔI_{ds} is minimized by the negative feedback in the reset phase. In our design, V_{Com1} is nearly 0 V during discharging, therefore efforts should be spent on reducing $V_{in-cm} - V_{rst-cm} - V_{Com1}^{'}$. It equals keeping the overdrive voltage $(V_{gs} - V_{th})$ of M1 and M2 low. If $V_{Com1}^{'}$ is set to ground as prior designs do, the offset will increase exponentially with $V_{in-cm} - V_{rst-cm}$.

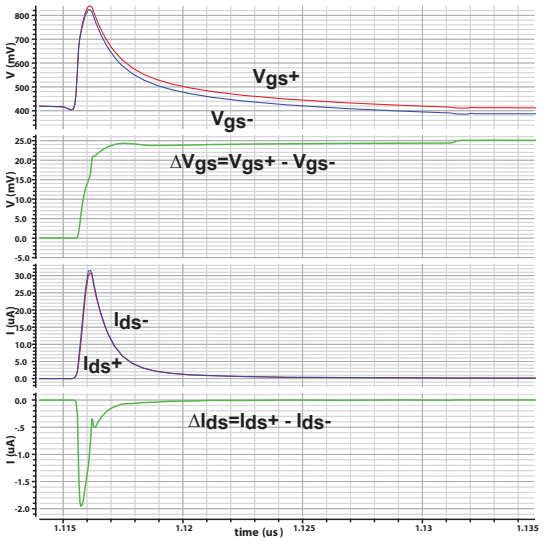

Fig. 4. Discharging process under mismatch in the reset phase.

On the other side, for 2nd-stage offset reduction, a high gain is required. The gain of the 1st stage amplifier can be derived as [8]:

$$A_v = -\frac{g_m}{I_{ds}} \cdot |V_{thp}| \tag{5}$$

where $\frac{g_m}{I_{ds}}$ belongs to M1 and M2, V_{thp} is the threshold voltage of M9 and M10. As $\frac{g_m}{I_{ds}}$ is inversely proportional to $V_{gs} - V_{th}$, it is necessary to reduce the overdrive voltage of M1 and M2, i.e., to reduce $V_{in-cm} - V_{rst-cm} - V_{Com1}^{'}$. It shares the same target with the 1st-stage offset cancellation.

In order to maintain low $V_{in-cm} - V_{rst-cm} - V_{Com1}^{'}$ for offset reduction, a simple and reliable way is to employ a tail current source I_b to make I_{ds} constantly small during the evaluation [13]. That is the reason for the current bias in our design. Using smaller current bias can bring lower $V_{in-cm} - V_{rst-cm} - V_{Com1}^{'}$ and thus better offset cancellation, but at the cost of larger delay and thus lower operation frequency.

III. Simulation Results

The proposed comparator has been designed and simulated using a 0.18 μm mixed-signal CMOS technology. Small-size transistors are used for implementation. They are all sized to be 460nm/180nm. The supply voltage is 1.2 V and the operation frequency is 10 MHz, targeting moderate-speed sensing applications. In our design, V_{rst-cm} is set to 0 V so as to maximize the input range. The input common-mode voltage range is from 0 V to 0.8 V.

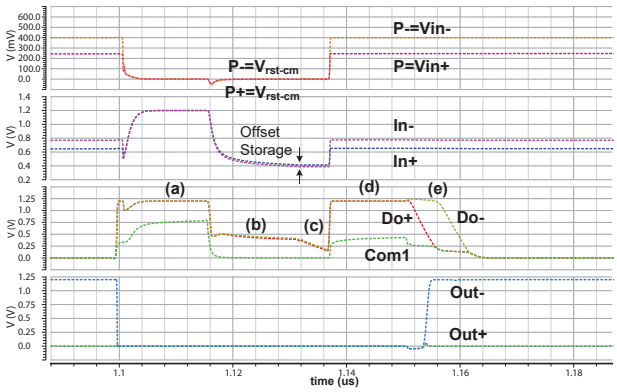

Fig. 5. Transient waveforms for one operation period.

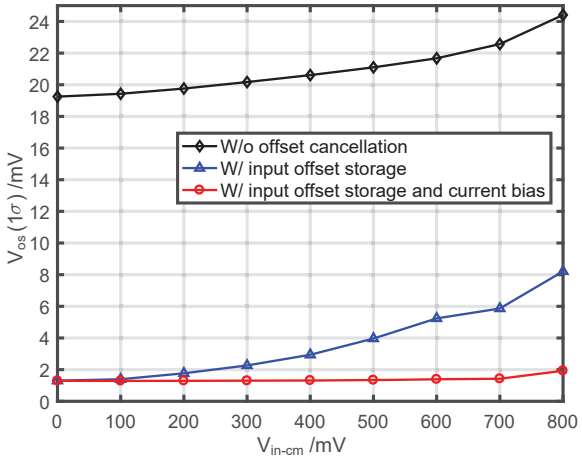

Fig. 6. Overall offset cancellation performance of the proposed comparator.

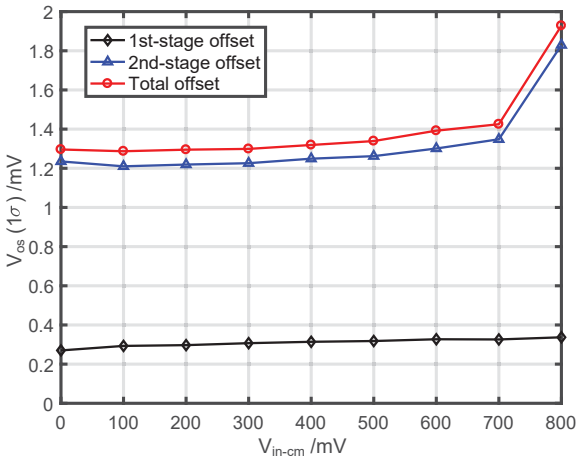

Fig. 7. Offset contribution from the 1st stage and the 2nd stage.

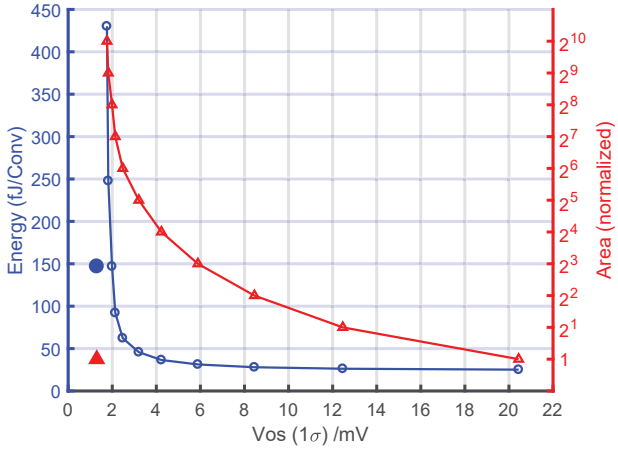

Fig. 8. Comparison with transistor sizing in terms of energy and area.

A. Circuit Transient Behaviour

According to the control timing in Fig.2, main node voltages in one operation period are shown in Fig.5. During capacitor discharging in the reset phase, offset appears between $In+$ and $In-$, and remains stable after M1 and M2 enter the subthreshold region. After sampling, the offset is stored between $In+$ and $In-$. It is cancelled when $V_{in}\pm$ are capacitively input. In the comparison phase, instead of dropping to ground, $Com1$ follows V_{in-cm} during the amplification process because of the constant bias current. Therefore, the overdrive voltage of the input pair is kept low to achieve low offset. The proposed dynamic comparator operates properly as expected.

B. Offset Cancellation Performance

Offset is the major concern in our design and the offset cancellation performance is illustrated in Fig.6. Without the offset cancellation, the input-referred offset V_{os} (1σ) is about 19.25 mV when V_{in-cm} is 0 V. As V_{in-cm} increases, V_{os} will exponentially increase to be more than 24 mV. With the dynamic input offset storage, V_{os} can be reduced to 1.296 mV, but it still has strong dependency on V_{in-cm}. V_{os} becomes larger than 8 mV with V_{in-cm} at 800 mV. It verifies the offset analysis in Section II. When the tail current source is introduced for the comparison phase, such situation is improved a lot. V_{os} remains at a low level in spite of varying V_{in-cm}. V_{os} is a bit larger when V_{in-cm} is 800 mV because the input voltages at $In\pm$ exceed VDD.

Further investigation is conducted for the offset contribution from the 1st stage and the 2nd stage individually. As seen in Fig.7, most of the input-referred offset comes from the 2nd stage. The 1st-stage offset has been reduced from about 19 mV to about 300 μV. On the other hand, the 2nd-stage offset is more than 1.2 mV because of small transistor size, mainly contributed by M9 and M10. The offset can be further reduced by enlarging M9 and M10. Simulation shows that overall offset of 771 μV can be achieved when M9 and M10 are enlarged by 4 times. At the same time, energy consumption will increase from 147 fJ/Conv to 168 fJ/Conv. Most of the energy consumption is caused by the input offset storage.

C. Comparison with Transistor Sizing

As both threshold variation $\sigma_{V_{th}}$ and current factor variation σ_β are inversely proportional to $\sqrt{W \cdot L}$, enlarge input transistor size will help to reduce offset. But it is difficult to achieve low offset due to the square root relation. To show the

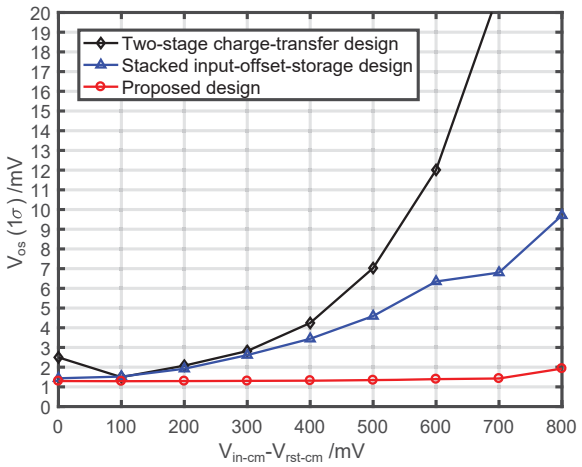

Fig. 9. Offset cancellation performance comparison among three designs with dynamic offset cancellation.

TABLE I
PERFORMANCE SUMMARY OF THREE DESIGNS

Design	Proposed design	Stacked input-offset-storage design	Two-stage charge-transfer design
Technology	CMOS 0.18 um	CMOS 0.18 um	CMOS 0.18 um
Supply (V)	1.2	1.2	1.2
Operation frequency (Hz)	10 M	10 M	10 M
Input-referred 1σ Offset (mV)	1.296	1.435	1.493
Input-referred 1σ Noise (μV)	1021	878	978
Worst delay (ns)	14.97	30.35	1.60
Energy (fJ/Conv.)	147	150	64

area efficiency and energy efficiency of the proposed design, we compare our method with transistor sizing by simulation in Fig.8. The transistor sizing is only performed on M1 and M2. $\frac{g_m}{I_{ds}}$ is kept unchanged to maintain the same 2nd-stage offset. The area is of M1 and M2, and normalized by the proposed design. Observed from Fig.8, V_{os} is reduced while area and energy consumption are increased. To obtain the same offset level as the proposed comparator, simple sizing will cause 3 times larger energy and 1000 times larger area, which is not practical for parallel multi-channel processing.

D. Comparison with Prior Designs

To further verify the comparator performance, low-offset comparators with area-efficient dynamic offset cancellation schemes from [10] and [11] are taken for comparison. For the sake of fairness, the two designs are reimplemented using the same process and with the same transistor sizing. The simulated results are depicted in Fig.9. For the stacked input-offset-storage design in [11], it uses the same setting of V_{in-cm} and V_{rst-cm}. For the two-stage charge-transfer design from [10], $V_b = 0.2\ V$ and $V_{rst-cm} = 0.6\ V$ are set. Its results are shifted right for 200 mV to fit into the unified axis.

All of the three designs can effectively reduce offset when $V_{in-cm} = V_{rst-cm}$. The stacked input-offset-storage design and the proposed design show better cancellation performance. However, the two reference designs exhibit great sensitivity to CM voltage variation, which degrades the performance a lot. As $V_{in-cm} - V_{rst-cm}$ increases, V_{os} is worsened drastically. When $V_{in-cm} - V_{rst-cm} = 800\ mV$, the offset of the charge-transfer design is larger than 25 mV and the offset of the input-offset-storage design can reach beyond 9 mV. On the contrary, the proposed design shows strong invariability to CM voltage change. It maintains the low-offset level across the whole input CM range from 0 to 800 mV.

The major metrics of the three designs are summarized in Table I. The proposed design shows the best offset cancellation with moderate speed and moderate energy consumption. The noise level is slightly higher due to smaller g_m, which can be improved by input pair sizing. The worst delay is smaller than 15 ns, which is suitable for applications under 30 MHz operation frequency. It can be optimized for high-speed applications by using larger transistors and current source. The charge-transfer design has the best energy efficiency because of small signal swing but at the cost of smaller gain and thus offset. The energy efficiency of the proposed design can be improved by reducing the sampling capacitors and the reset voltage since most of the energy is consumed by charging the sampling capacitors to the reset voltage.

E. Post-Layout Simulation

The layout of the proposed comparator has been drawn with RC extraction. The dimension of the comparator is $16.5 \times 5.5\ \mu m^2$. Post-layout simulation shows static offset of 305 μV, mainly due to imbalanced parasitic capacitance at $Do+$ and $Do-$. Different from offset caused by transistor fabrication, the offset caused by imbalanced parasitics is static for all the channels as the layout is usually repeated every channel. It will be much easier to suppress such systematic offset by optimizing the layout or using global offset compensation in the digital or analog domain.

IV. CONCLUSION

A low-offset two-stage comparator for parallel multi-channel processing has been presented in this work. An area-efficient and low-power input-offset-storage scheme is used to suppress the offset to a low level. The low offset is maintained across a wide range of input CM voltages thanks to the introduction of a current source for the comparison phase. The current source ensures low 1st-stage offset and improves the 1st-stage gain to suppress the 2nd-stage offset. Simulation results have verified the performance of the proposed design. Comparison with prior designs proves the advantages of the proposed design. The dynamic comparator is suitable for parallel-processing applications because of its low offset, small area and high energy efficiency. Further improvement will be performed on optimization of the design for lower energy consumption and lower noise.

ACKNOWLEDGMENT

The authors would like to acknowledge the support from Hong Kong Innovation and Technology Fund (ITF) under Grant ITS/195/14FP.

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