

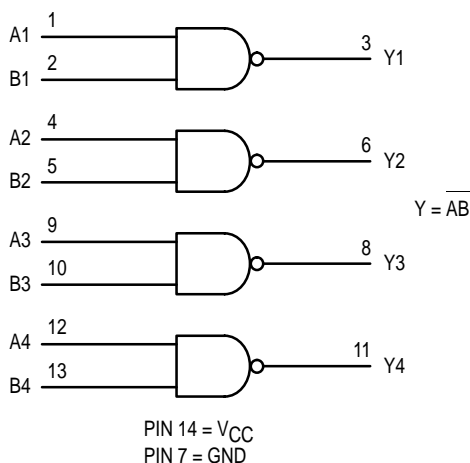
## Quad 2-Input NAND Gate with LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC54/74HCT00A may be used as a level converter for interfacing TTL or NMOS outputs to high-speed CMOS inputs.

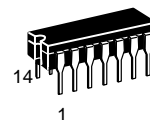
The HCT00A is identical in pinout to the LS00.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 48 FETs or 12 Equivalent Gates

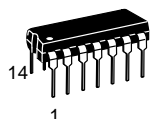
### LOGIC DIAGRAM



## MC54/74HCT00A



**J SUFFIX**  
CERAMIC PACKAGE  
CASE 632-08



**N SUFFIX**  
PLASTIC PACKAGE  
CASE 646-06



**D SUFFIX**  
SOIC PACKAGE  
CASE 751A-03

### ORDERING INFORMATION

MC54HCTXXAJ	Ceramic
MC74HCTXXAN	Plastic
MC74HCTXXAD	SOIC

### PIN ASSIGNMENT

A1	1	14	$V_{CC}$
B1	2	13	B4
Y1	3	12	A4
A2	4	11	Y4
B2	5	10	B3
Y2	6	9	A3
GND	7	8	Y3

### FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

3



## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	– 0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package†	750 500	mW
$T_{stg}$	Storage Temperature	– 65 to + 150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds SOIC or Plastic Package Ceramic Dip	260 300	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

† Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C

Ceramic DIP: – 10 mW/°C from 100° to 125°C

SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	– 55	+ 125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	0	500	ns

## DC CHARACTERISTICS FOR THE MC54/74HCT00A (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limits						Unit
				– 55 to 25°C		≤ 85°C		≤ 125°C		
				Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	Minimum High–Level Input Voltage	V <sub>out</sub> = 0.1 or V <sub>CC</sub> – 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	2.00 2.00		2.00 2.00		2.00 2.00		V
V <sub>IL</sub>	Maximum Low–Level Input Voltage	V <sub>out</sub> = 0.1 or V <sub>CC</sub> – 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5		0.80 0.80		0.80 0.80		0.80 0.80	V
V <sub>OH</sub>	Minimum High–Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	4.40 5.40		4.40 5.40		4.40 5.40		V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA	4.5	3.98		3.84		3.70		
V <sub>OL</sub>	Maximum Low–Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5 5.5		0.10 0.10		0.10 0.10		0.10 0.10	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   = 4.0 mA	4.5		0.26		0.33		0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5		±0.10		±1.00		±1.00	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 0 μA	5.5		1		10		40	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ – 55°C		25 to 125°C				mA
				2.9		2.4				

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS FOR THE MC54/74HCT00A (V<sub>CC</sub> = 5.0 V ± 10%, CL = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

Symbol	Parameter	Fig.	Guaranteed Limits						Unit
			– 55 to 25° C		≤ 85° C		≤ 125° C		
			Min	Max	Min	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Output Y	1, 2		19		24		28	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output	1, 2		15		19		22	ns
C <sub>in</sub>	Maximum Input Capacitance	—		10		10		10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

C <sub>PD</sub>	Power Dissipation Capacitance (Per Gate)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		15	

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>. For load considerations, see Chapter 2 of the Motorola High-Speed CMOS Data Book (DL129/D).

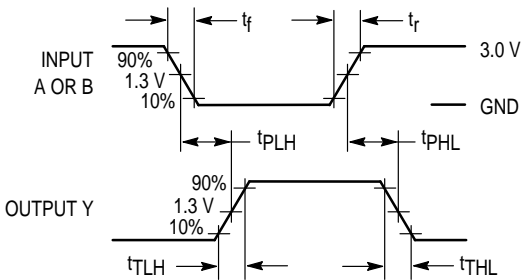
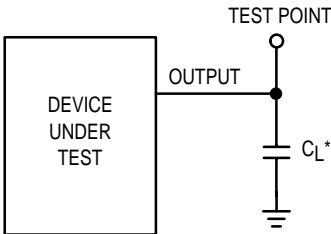
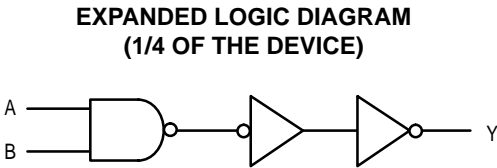


Figure 1. Switching Waveforms

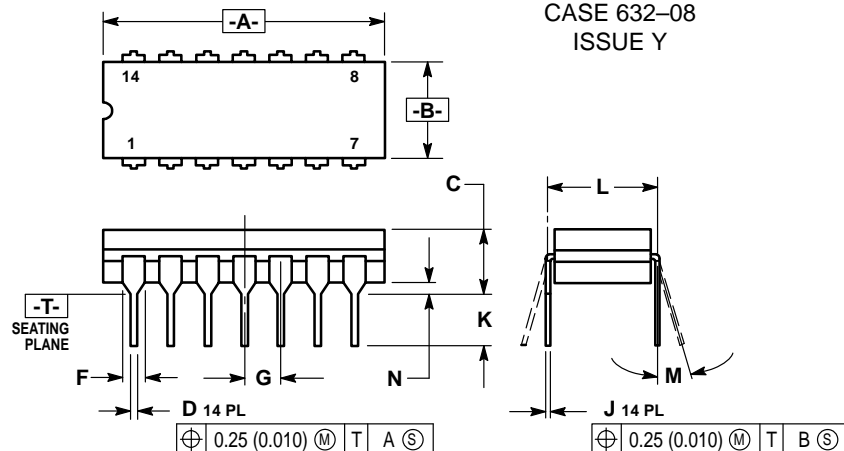


\* Includes all probe and jig capacitance

Figure 2. Test Circuit



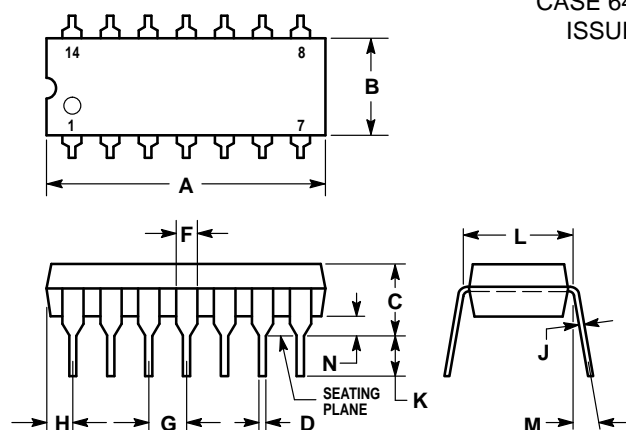
## OUTLINE DIMENSIONS

**J SUFFIX**  
 CERAMIC DIP PACKAGE  
 CASE 632-08  
 ISSUE Y


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

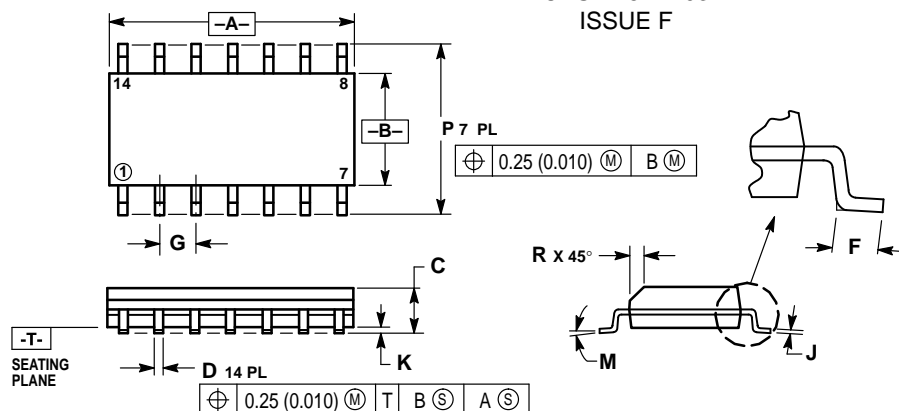
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

**N SUFFIX**  
 PLASTIC DIP PACKAGE  
 CASE 646-06  
 ISSUE L


## NOTES:

1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

**D SUFFIX**  
 PLASTIC SOIC PACKAGE  
 CASE 751A-03  
 ISSUE F


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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