HoangNguyen

Full name: Nguyen Thai Hoang

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I enjoy learning and doing research. My main interest is representation learning, especially in graph-structured data and natural language processing.

EDUCATION

2015-2017 **Tokyo Institute of Technology** - *M.Eng., Research/Teaching Assistant* — Tokyo, Japan

Computer Science major in School of Computing, specializing in Complex Networks. (funded by the Japanese Government)

`[Machine Learning, Complex Networks] - GPA: 3.94/4.00 (JP system: 3.0/3.0)`

2009-2014 **Hanoi University of Science and Technology** - *B.E., Research Assistant* — Hanoi, Vietnam

Majored in Computer Engineering and Telecommunication (5 years program).

`[Embedded Systems, FPGA] - GPA: 3.21/4.00 (major GPA: 3.45/4.00)`

WORK EXPERIENCE

2014-2015 **WebSoSanh, JSC** - *Machine Learning Engineer* — Hanoi, Vietnam

Design machine learning-based solutions for handling consumer products data. By engineering several state-of-the-art embedding techniques and 1D convolutional neural networks, my solutions achieve up to 20% (absolute) improvements over the existing system. Our team also develop an API to provide our service to the users and other departments.

2016-2017 **Tokyo Institute of Technology** - *Teaching Assistant* — Tokyo, Japan

- Winter 2016: Machine Learning. Instructor for Weka 3.6 Toolkit.
- Spring 2017: Information Literacy I & II.

RESEARCH EXPERIENCE

2015-2017 **Murata Laboratory** - *Research Assistant* — Tokyo, Japan

- Network Science: Motifs Analysis and Network Representation Research.
- Deep Learning: Deep Neural Network Compression Research.
- Implemented a novel graph embedding algorithm that utilizes motif structures. The motif injection leads up to 5 percentage point advantage (accuracy and F1 score) in various benchmark network datasets.
- ReLiG @ IJCAI-17: Workshop paper & oral presentation.
- NetSci 2016: BrainNet project oral presentation.

2012-2015 **ESRC Laboratory** - *Research Assistant, Laboratory Manager* — Hanoi, Vietnam

- Embedded Systems Design and FPGA Technology Research.
- Implemented a network on chip architecture and improved its performance by 40% using pipelining and parallel read-write buffers.

LANGUAGES

Vietnamese *native*
English *fluent (iBT: 102)*
Japanese *basic*

PROGRAMMING

Python, C++
Java, Javascript, HTML/CSS
Haskell, Scala, Coq

FRAMEWORKS

NetworkX, Tensorflow
graph-tool, Theano, Sklearn
Cocos2dx, Cocoa

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AWARDS

2015-2017 **Japanese Government Scholarships (MEXT)** - *Master Studies* — Tokyo, Japan

The Monbukagakusho (Ministry of Education, Culture, Sports, Science & Technology) Scholarship is awarded to excellent students to pursue a higher degree in Japan.

2009-2015 **Study-aid Scholarships** - *Undergraduate Studies* — Hanoi, Vietnam

Study-aid scholarships are awarded every semester to outstanding undergraduate students of Hanoi University of Science and Technology.

COURSEWORK

2015-2017 **Tokyo Institute of Technology** - *Master Studies* — Tokyo, Japan

Complex Networks; Machine Learning; Advanced Artificial Intelligence; High Performance Scientific Computing; Discrete Algebraic and Geometric Structures I.

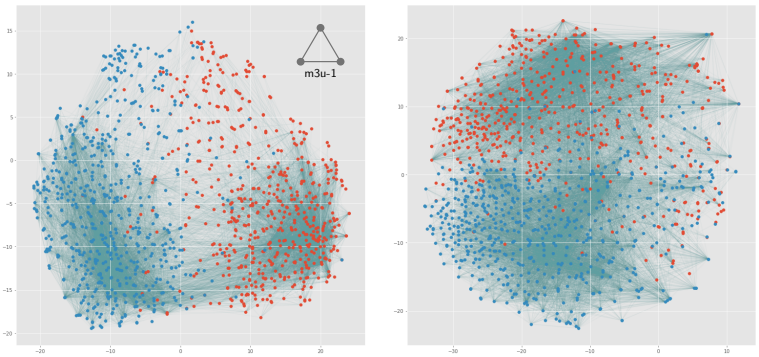
2009-2015 **Hanoi University of Science and Technology** - *Undergraduate Studies* — Hanoi, Vietnam

VLSI Design; Embedded Systems Design; Algebra; Analysis; Applied Software Engineering; Probability and Statistic; Networking.

PROJECTS

Deep-CREST: Deep Neural Network Compression (JST funded project).
In this project, we study the methods for deep neural network compression and the impact of these methods to the robustness of the feature mapping functionality.

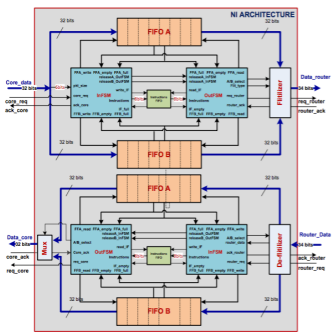
MAGE: Motifs Aware Graph Embedding (ReLiG @ IJCAI-17).



Polblog network.

Left: Motifwalk algorithm;
Right: Deepwalk algorithm.

Torus2x2PNI: A 2x2 Network on Chip Architecture with Pipelined Network Interface.



Pipelined Network Interface Architecture.

Top module: Interface between processor and router;
Bottom module: Interface between router and processor.

This proposed architecture has two buffers for each module enabling parallel read/write operations.