# Hoang T. Nguyen

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## Education

- **Tokyo Institute of Technology** — Tokyo, Japan
  *M.Sc. in Computer Science* — *2015-2017*
  - Academic rating: 3.0 / 3.0 (Japanese system for government scholars)
  - Computer Science Department GPA: 4.0 / 4.0
  - Mathematics and Computing Department GPA: 4.5 / 4.0
- **Hanoi University of Science and Technology** — Hanoi, Vietnam
  *B.S.Eng in Electronics Engineering and Telecommunications* — *Class of 2014 - K54*
  - Magna Cum Laude.
  - Major GPA: 3.4 / 4.0
  - Cummulative GPA: 3.21 / 4.0
- **HNUE High School for Gifted Students** — Hanoi, Vietnam
  *Physics Class* — *Class of 2009 - K40*
  - Selected for National Physics Olympiad training.

## Coursework

**Electrical Engineering and Computer Science:** Machine Learning, Advanced Artificial Intelligence, Distributed Algorithms, Advanced Databases, Complex Network, High Performance Scientific Computing, Advanced Inverse Problem, Programming Language Design, Computer Architecture

**Mathematics:** Discrete Geometry, Linear Algebra, Analysis

## Awards and Honors

**2014** Best undergraduate thesis defense. Raw score: 10.0 / 10.0

**2015** Japanese Government Scholarship for Master study at Tokyo Institute of Technology.

## Experience

- **Murata Laboratory** — Tokyo, Japan
  *Research Assistant* — *September 2015 - Present*
  - Research on brain network constructions.
  - Network embedding research.
  - Fuji Xerox database research.
  - Teaching Assistant for Machine Learning and Complex Network courses.
- **Donuts Hanoi Co, Ltd.** — Hanoi, Vietnam
  *Software Engineer Internship* — *September 2014 - January 2015*
  - Develop game named bla bla bla.
  - Detail of implementation.

**ESRC Laboratory, SET** — Hanoi, Vietnam
*Undergraduate Researcher* — *March 2012 - August 2014*

- Worked in the Embedded System and Reconfigurable Computing Laboratory (Room 618, Ta Quang Buu Library) in School of Electroncis and Telecommunications, with PhD candidate Nguyen Van Cuong and Associate Prof. Pham Ngoc Nam.
- Design and implemented a traffic rating software using OpenCV platform. My software was able to rate current traffic video input and give out results as A to F levels of conjunction.
- Received training in VLSI design based on Xilinx and Quartus FPGA platform.
- Worked and practiced theory of Network on Chip. Designed a fully functional 2x3 Mesh network with Network Interface and Reconfiguration. My group's design is an optimized version of seniors in ESRC Lab's previous work. By applying pipeline technique, we are able to increase throughput of the Network Interface by 40% compare to our seniors' version. Further more, the network itself can handle much more data due to new structure of our Mesh-Router.

## Technical Skills

- **Programming Languages ($\tilde{4}$000 lines):** Python.
- **Programming Languages ($\tilde{2}$000 lines):** Java SE, C++ (Cocos2d-x).
- **Programming Languages ('Hello, World!'):** C, MATLAB, Coq, Julia, Haskell, Scala.
- **Machine Learning Framworks:** Tensorflow (2 projects), Sklearn (1 project).
- **Others:** Complex network analysis (2 projects), Arduino (1 project).
- **Hardware Description Languages:** Verilog HDL ( 2000 lines), VHDL ( 1000 lines).

## Other Skills

- **Documents:** LaTeX, Adobe InDesign / Photoshop / Illustrator
- **Languages:** English (TOEFL iBT: 103 - Test date: Feb 22nd, 2014), Japanese (Beginner)

## Leadership and Service

- **2012-2014** Senior member and manager of ESRC Laboratory. Hanoi, Vietnam.
- **2009-2010** Class president and member of standing HUST student committee. Hanoi, Vietnam.

## Interests and Hobbies

- **Sports:** Kendo, weight lifting, swimming.
- **Creative Activities:** LEGO, books, hiking, data visualization.