Solutions to Lab 1

UCF file:

```
Net "SW0" LOC="J11" | IOSTANDARD = LVCMOS33;

Net "LED0" LOC="C11"| IOSTANDARD = LVCMOS33;
```

VHDL code:

```
----------------------------------------------------------------------------------
-- Company:
-- Engineer:
--
-- Create Date:    11:33:34 12/03/2015
-- Design Name:
-- Module Name:    ToggleLed - Behavioral
-- Project Name:
-- Target Devices:
-- Tool versions:
-- Description:
--
-- Dependencies:
--
-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
--
----------------------------------------------------------------------------------
library IEEE;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity ToggleLed is Port (SW0: in STD_LOGIC:='1';

          LED0 : out STD_LOGIC:='0');
end ToggleLed;
```

```
architecture Behavioral of ToggleLed is

begin

LED0 <= SW0;

end Behavioral;
```