```
1   ----------------------------------------------------------------------------------
2   -- Company: HSRW
3   -- Engineer: Andy Stamm
4   --
5   -- Create Date:    08:49:12 12/17/2015
6   -- Design Name:
7   -- Module Name:    D-latch
8   -- Project Name:  Lab 3.2
9   -- Target Devices:
10  -- Tool versions:
11  -- Description:
12  --
13  -- Dependencies:
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.STD_LOGIC_ARITH.ALL;
23  use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx primitives in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  library IEEE;
35  use IEEE.STD_LOGIC_1164.ALL;
36  use IEEE.STD_LOGIC_ARITH.ALL;
37  use IEEE.STD_LOGIC_UNSIGNED.ALL;
38
39  entity d_latch is
40     Port( BTN0, BTN1: in std_logic;
41           LED1: out std_logic);
42
43  end d_latch;
44
45  architecture Behavioral of d_latch is
46  signal data: std_logic;
47
48  begin
49  -- logic design of the D-Latch
50  data <= BTN0 when (BTN1 = '1') else data;
51  LED1 <= data;
52
53  end architecture Behavioral;
54
55
56
```