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1   ----------------------------------------------------------------------------------
2   -- Company: HSRW
3   -- Engineer: Andy Stamm
4   --
5   -- Create Date:    08:49:12 12/17/2015
6   -- Design Name:
7   -- Module Name:    7 segment 4bit to hex - Behavioral
8   -- Project Name:     Lab 2.2
9   -- Target Devices:
10  -- Tool versions:
11  -- Description:
12  --
13  -- Dependencies:
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.STD_LOGIC_ARITH.ALL;
23  use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx primitives in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  library IEEE;
35  use IEEE.STD_LOGIC_1164.ALL;
36  use IEEE.STD_LOGIC_ARITH.ALL;
37  use IEEE.STD_LOGIC_UNSIGNED.ALL;
38
39  entity seven_segment is
40         Port (  clk, SW0, SW1, SW2, SW3  : in     STD_LOGIC;                      --
    inputs to the entity
41                 COM0 : out  STD_LOGIC;
    --ouput anode of the seven segment display
42                 SEGA0, SEGB0, SEGC0, SEGD0, SEGE0, SEGF0, SEGG0 : out  STD_LOGIC  --
    ouputs of the first seven segment dislay
43               );
44  end entity seven_segment;
45
46  architecture Behavioral of seven_segment is
47  signal temp: std_logic_vector(6 downto 0);   -- vector to drive the 7-segment display
48  signal btn: std_logic_vector(3 downto 0);    -- vector to save the switch state
49
50      begin
51         process(clk)
52             begin
53              if clk'event and clk='1' then -- wait for the rising edge of the clock
    then assign SW state to vector
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54                 btn(0)<=SW0;
55                 btn(1)<=SW1;
56                 btn(2)<=SW2;
57                 btn(3)<=SW3;
58              end if;
59          end process;
60
61      process
62         begin
63            -- assign the decoded output to the first seven segment display outputs
64            SEGA0 <= temp(0);
65            SEGB0 <= temp(1);
66            SEGC0 <= temp(2);
67            SEGD0 <= temp(3);
68            SEGE0 <= temp(4);
69            SEGF0 <= temp(5);
70            SEGG0 <= temp(6);
71            COM0<='0';        -- enable the first seven segment display
72      end process;
73
74            -- decoding the four bit vector to the first seven segment display
75            with btn Select
76               temp<="0111111" when "0000",
77                     "0000110" when "0001",
78                     "1011011" when "0010",
79                     "1001111" when "0011",
80                     "1100110" when "0100",
81                     "1101101" when "0101",
82                     "1111101" when "0110",
83                     "0000111" when "0111",
84                     "1111111" when "1000",
85                     "1101111" when "1001",
86                     "1110111" when "1010",
87                     "1111100" when "1011",
88                     "0111001" when "1100",
89                     "1011110" when "1101",
90                     "1111001" when "1110",
91                     "1110001" when "1111",
92                     "1000000" when others;
93
94
95   end Behavioral;
96
```