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LABORATORY 3:
Seven Segment Display

Model-based Hardware Design

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Contents

1. Safety instructions

ESD Warning

Caution Although this product has been designed to be as robust as possible, ESD (Electrostatic Discharge) can damage or upset this product. This product must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

The NI Digital Electronics FPGA Board is designed and intended for use as a development platform for hardware or software in an educational/professional laboratory environment. To facilitate usage, the board is manufactured with its components and connecting traces openly exposed to the operator and the environment. As a result, ESD sensitive (ESDS) components on the board, such as the semiconductor integrated circuits, can be damaged when exposed to an ESD event. To indicate the ESD sensitivity of the NI Digital Electronics FPGA Board, it carries the symbol shown below.

Handling the NI Digital Electronics FPGA Board can damage the board components if ESD prevention measures are not applied. **Before handling or setup, equalize your potential with the board by touching one of the integrated ESD discharge pads.** During all handling and setup, ESD prevention measures must be applied. In addition, the NI Digital Electronics FPGA Board should be handled by the edges. Touching exposed circuits, components or connectors could result in an ESD event.

2. Introduction to Seven-Segment Display

The NI Digital Electronics FPGA Board has two seven segment displays, DISP1, in **a common cathode configuration**. Try locating the seven-segment display on your FPGA board, otherwise refer to the first laboratory. The two digit seven-segment display circuitry is shown in Figure 1.

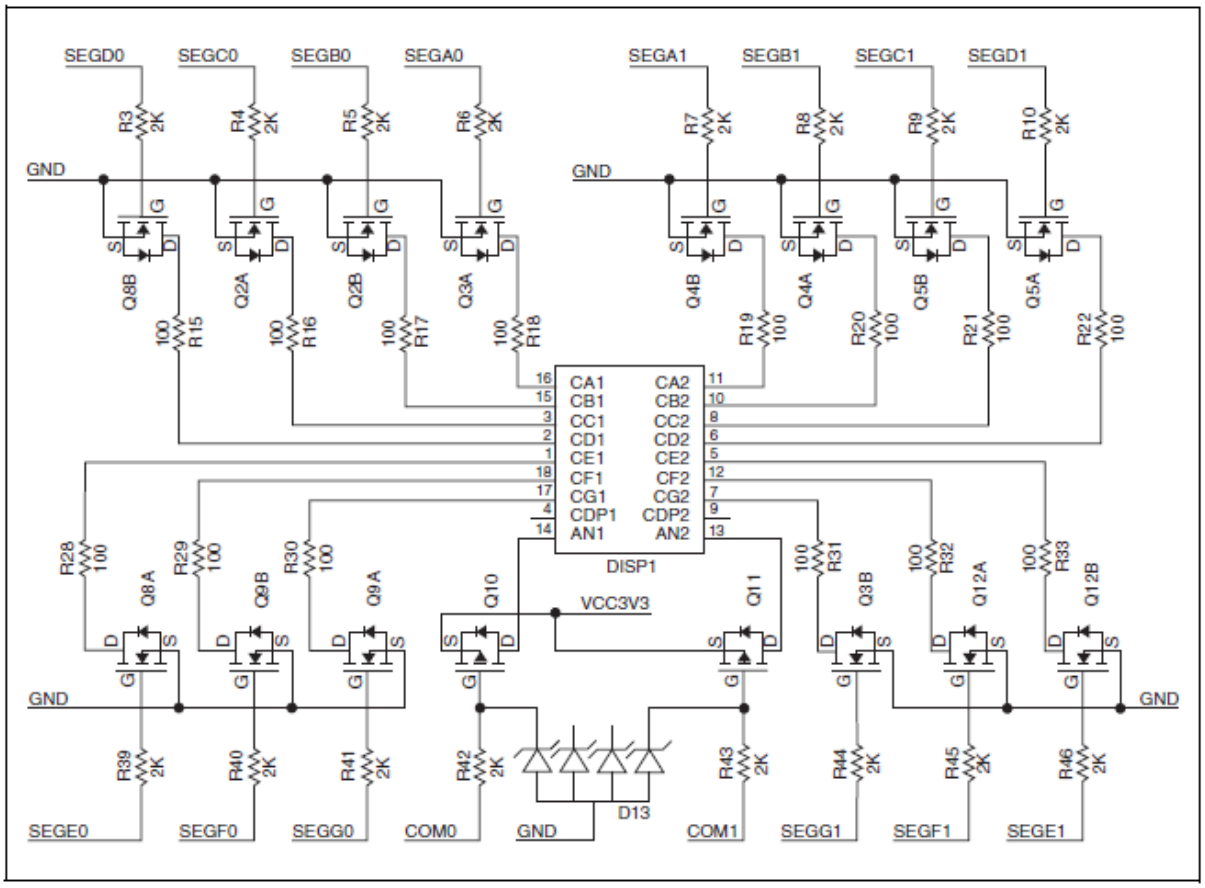

Figure 1: Two Digit Seven-Segment Display Circuit Diagram

Each digit is composed of seven segments arranged in a figure 8 pattern, with an LED embedded in each segment. Segment LEDs are SEG*x*0 for digit 0, and SEG*x*1 for digit 1, as shown in Figure 2.

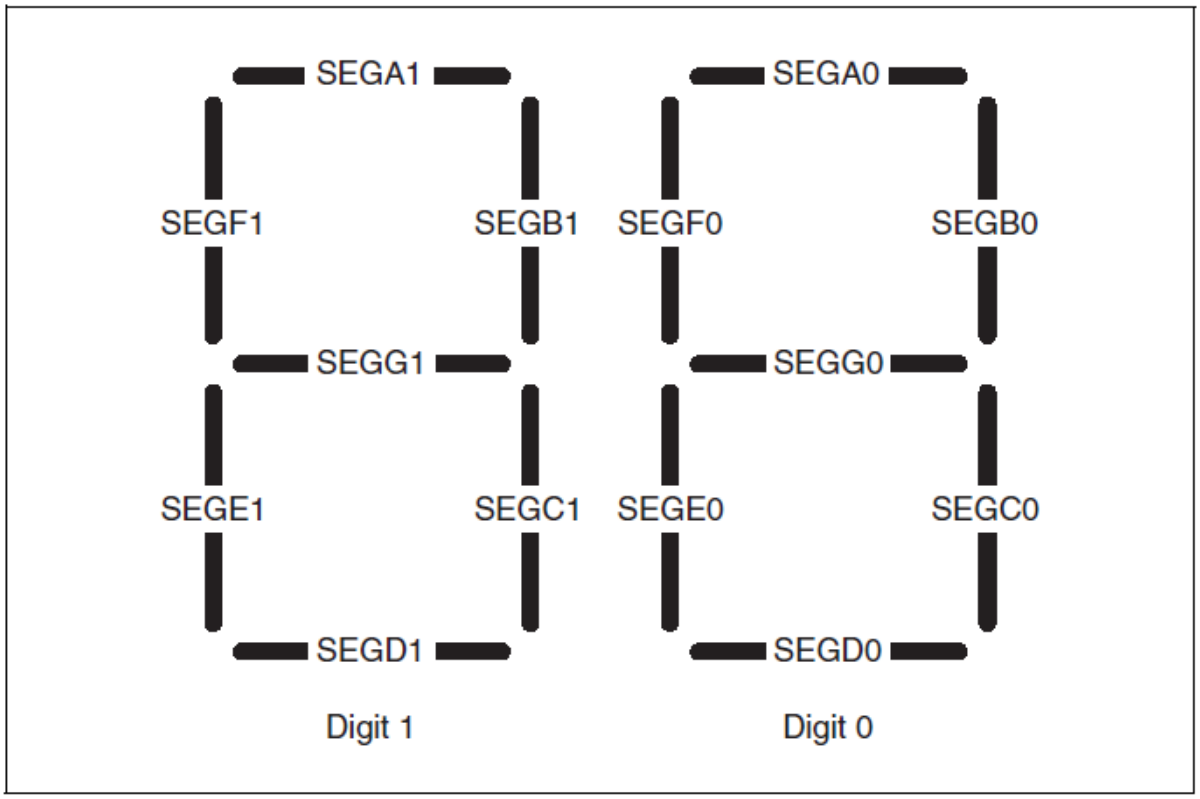

Figure 2: Seven-Segment Display

Segment LEDs can be individually illuminated, so different patterns can be displayed on a digit by lighting certain LED segments. To light an individual LED segment, drive the associated line High (using 3.3 V or 5 V).

Lines COM0 and COM1 can be used to enable/disable each digit of the display to allow using the display in multiplexed mode. (**low = enable**). Both lines are connected to the FPGA.

3. UCF File Constraints

Slide Switches

The UCF file constraints for the eight slide switches, SW0 to SW7, are listed as follows. SWx refers to the slide switch line, LOC indicates the FPGA line location, and IOSTANDARD is the I/O standard used.

```
Net "SW0" LOC="J11" | IOSTANDARD = LVCMOS33;
Net "SW1" LOC="J12" | IOSTANDARD = LVCMOS33;
Net "SW2" LOC="H16" | IOSTANDARD = LVCMOS33;
Net "SW3" LOC="H13" | IOSTANDARD = LVCMOS33;
Net "SW4" LOC="G12" | IOSTANDARD = LVCMOS33;
Net "SW5" LOC="E14" | IOSTANDARD = LVCMOS33;
Net "SW6" LOC="D16" | IOSTANDARD = LVCMOS33;
```

Seven-Segment Displays

The UCF file constraints for the seven-segment displays are listed as follows: SEGxx refers to the display segment line, COMx refers to the display anode line, LOC indicates the FPGA line location, IOSTANDARD is the I/O standard used, SLEW refers to the slew rate, the maximum rate of change of a signal, and DRIVE indicates the current drive strength on the FPGA in milliamps.

```
Net "SEGA0" LOC="E3" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGB0" LOC="E1" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGC0" LOC="G5" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGD0" LOC="D1" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGE0" LOC="E4" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGF0" LOC="C1" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGG0" LOC="C2" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "COM0" LOC="B2" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGA1" LOC="H6" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGB1" LOC="K2" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGC1" LOC="H3" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGD1" LOC="K1" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGE1" LOC="G4" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGF1" LOC="J2" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGG1" LOC="G3" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "COM1" LOC="G2" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
```

4. Task 1: Four-bit binary number converted into two-digit decimal

In order to successfully complete this task you need to generate your programing file, download and test it on your FPGA board using the methods provided in the previous laboratory.

You are to design a circuit with VHDL that converts a four-bit binary number $V = v_3v_2v_1v_0$ into its two-digit decimal equivalent $D = d_1d_0$. A partial design of this circuit is given in Figure 3. It includes a comparator that checks when the value of V is greater than 9, and uses the output of this comparator in the control of the 7-segment displays. Use the switches for inputting the binary number and the display for the decimal number.

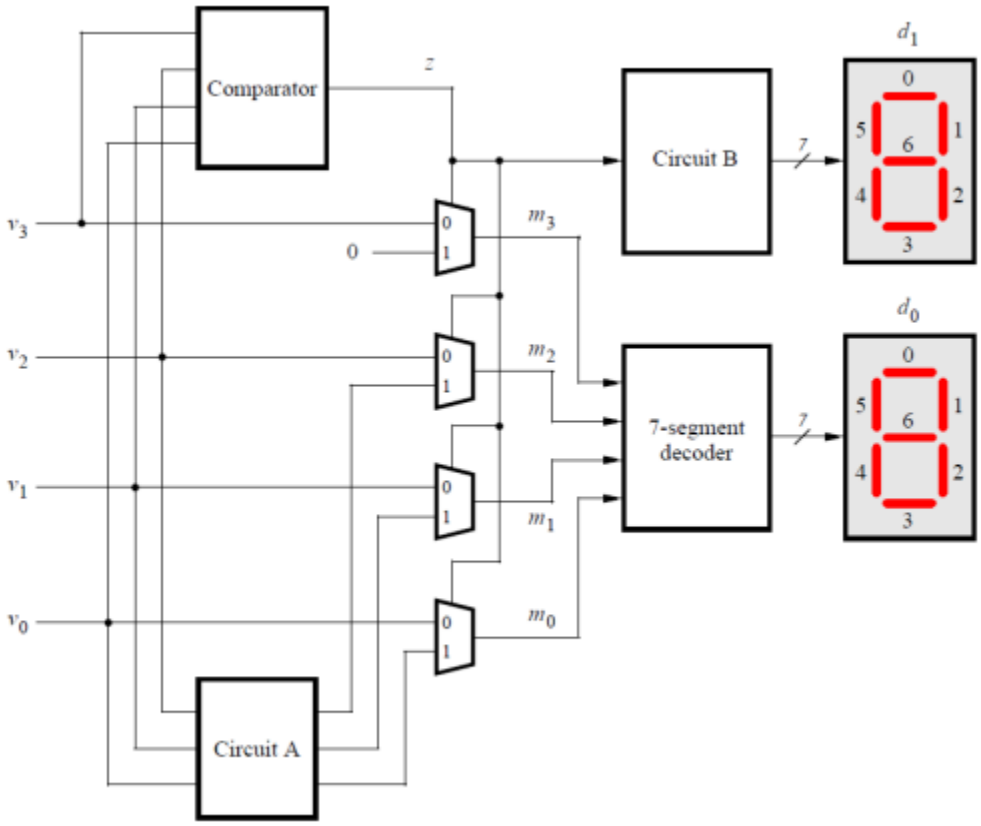

Figure 3: Partial design of the binary-to-decimal conversion circuit.

Decimal	Binary
0	0
1	1
2	10
3	11
4	100
5	101
6	110
7	111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

Figure 4: Decimal to binary table

*Using Karnaugh map to visualize the way the digits on the display are created might be useful.

5. Task 2: Four-bit binary number converted into hex number

Please expand your task one to a four-bit binary number displaying one hex number on one seven segment display.

6. Bonus Task: Six-bit binary number converted into a decimal number

Please expand your task one to a six-bit binary number displaying a two digit decimal number on both seven segment displays.